

P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
- 20	0.0033 at $V_{GS} = - 10$ V	- 60	85 nC
	0.0055 at $V_{GS} = - 4.5$ V	- 60	

FEATURES

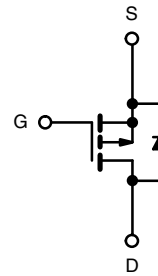
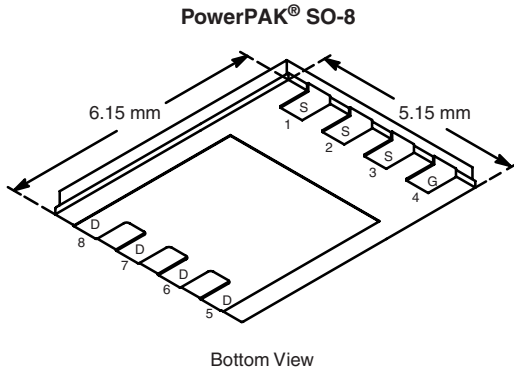
- Halogen-free
- TrenchFET[®] Power MOSFET
- 100 % UIS Tested



RoHS
COMPLIANT

APPLICATIONS

- Adaptor Switch



P-Channel MOSFET

Ordering Information: Si7633DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 20	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	- 60 ^a
		$T_C = 70$ °C	- 60 ^a
		$T_A = 25$ °C	- 34 ^{b, c}
		$T_A = 70$ °C	- 27 ^{b, c}
Pulsed Drain Current	I_{DM}	- 100	A
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C	
		$T_A = 25$ °C	- 5.6 ^{b, c}
Single Pulse Avalanche Current	I_{AS}	- 25	mJ
Single Pulse Avalanche Energy	E_{AS}	31	
Maximum Power Dissipation	P_D	$T_C = 25$ °C	104
		$T_C = 70$ °C	66.6
		$T_A = 25$ °C	6.25 ^{b, c}
		$T_A = 70$ °C	4.0 ^{b, c}
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	$t \leq 10$ s	R_{thJA}	15	20	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	0.9	1.2	

Notes:

- Package limited.
- Surface Mounted on 1" x 1" FR4 board.
- $t = 10$ s.
- See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 54 °C/W.



SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	- 20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		- 19		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			6.4		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	- 1.0		- 3.0	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$			- 1	μA
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			- 10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5\text{ V}, V_{GS} = -10\text{ V}$	- 30			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -20\text{ A}$		0.0027	0.0033	Ω
		$V_{GS} = -4.5\text{ V}, I_D = -15\text{ A}$		0.0044	0.0055	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\text{ V}, I_D = -20\text{ A}$		80		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		9500		pF
Output Capacitance	C_{oss}			1830		
Reverse Transfer Capacitance	C_{rss}			1740		
Total Gate Charge	Q_g	$V_{DS} = -10\text{ V}, V_{GS} = -10\text{ V}, I_D = -20\text{ A}$		173	260	nC
				85	130	
Gate-Source Charge	Q_{gs}	$V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -20\text{ A}$		24		
Gate-Drain Charge	Q_{gd}			37		
Gate Resistance	R_g	$f = 1\text{ MHz}$		1.5		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 10\text{ }\Omega$ $I_D \cong -1.0\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$		21	40	ns
Rise Time	t_r			12	30	
Turn-Off Delay Time	$t_{d(off)}$			100	150	
Fall Time	t_f			25	40	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 10\text{ }\Omega$ $I_D \cong -1.0\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		100	150	
Rise Time	t_r			90	140	
Turn-Off Delay Time	$t_{d(off)}$			85	130	
Fall Time	t_f			50	75	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			60	A
Pulse Diode Forward Current ^a	I_{SM}				100	
Body Diode Voltage	V_{SD}	$I_S = -5\text{ A}$		- 0.74	- 1.1	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 3.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		65	130	ns
Body Diode Reverse Recovery Charge	Q_{rr}			85	170	nC
Reverse Recovery Fall Time	t_a			34		ns
Reverse Recovery Rise Time	t_b			31		

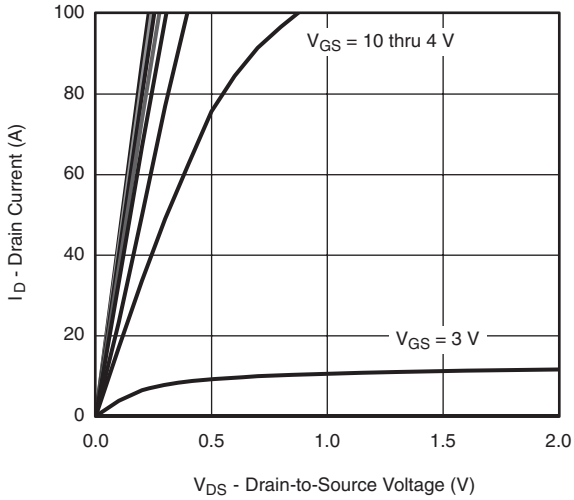
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

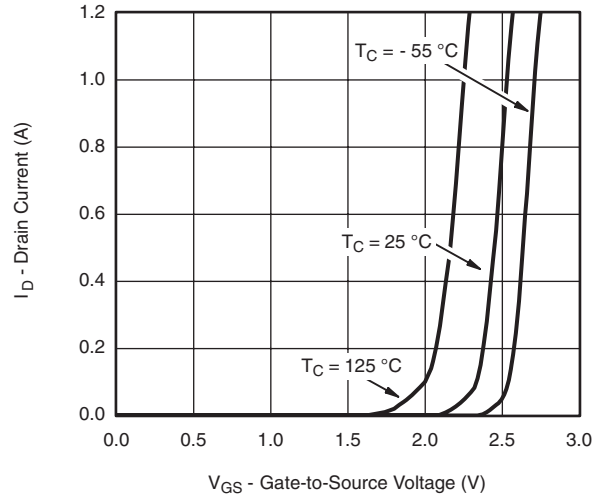
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



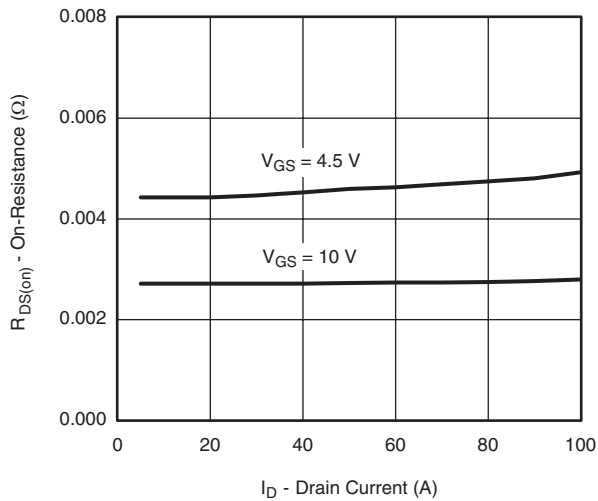
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



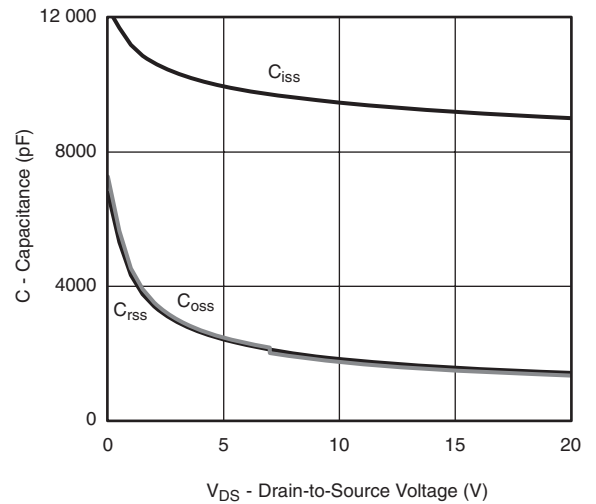
Output Characteristics



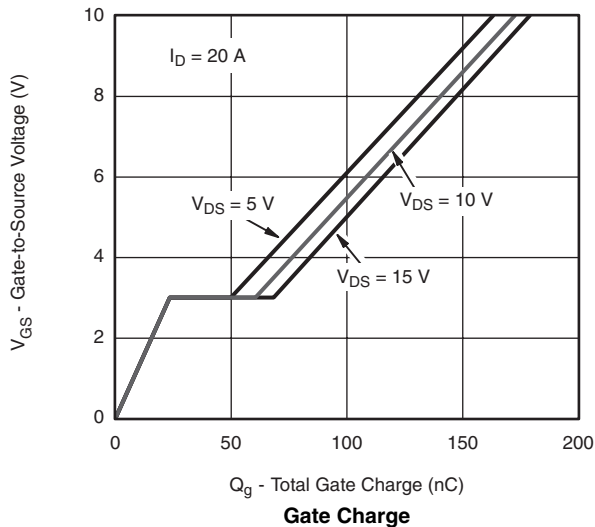
Transfer Characteristics



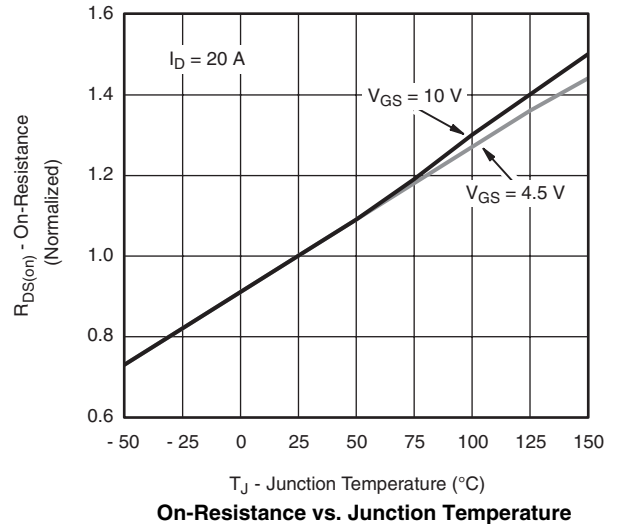
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



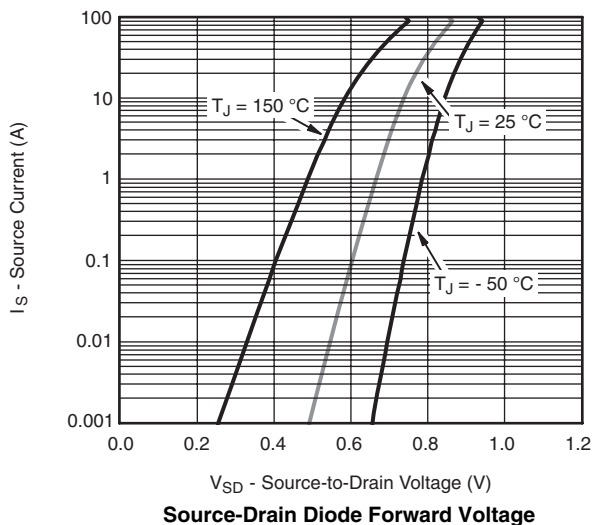
Gate Charge



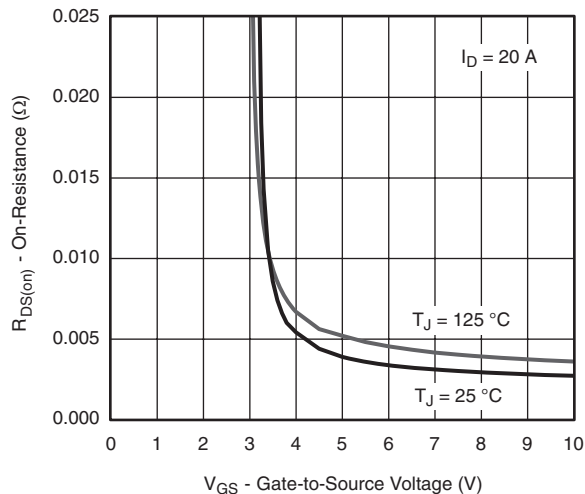
On-Resistance vs. Junction Temperature



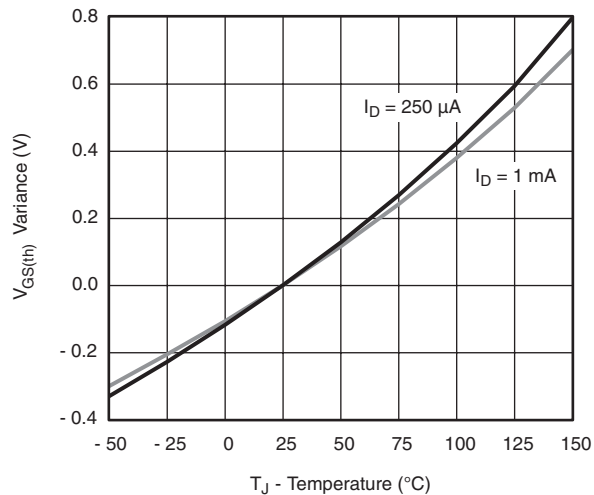
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



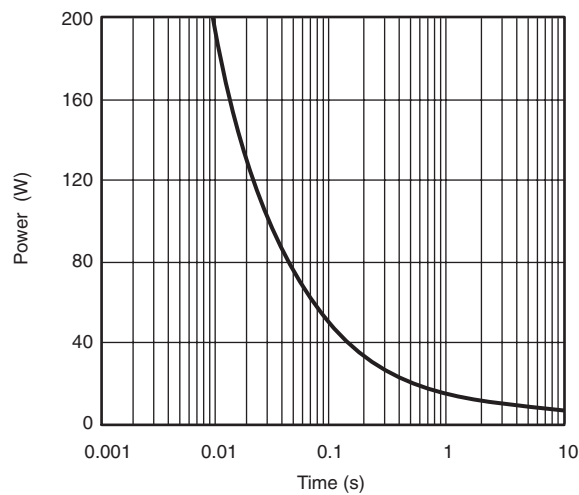
Source-Drain Diode Forward Voltage



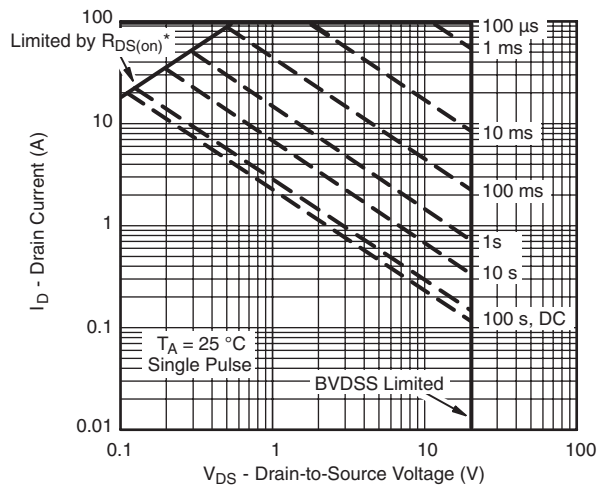
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



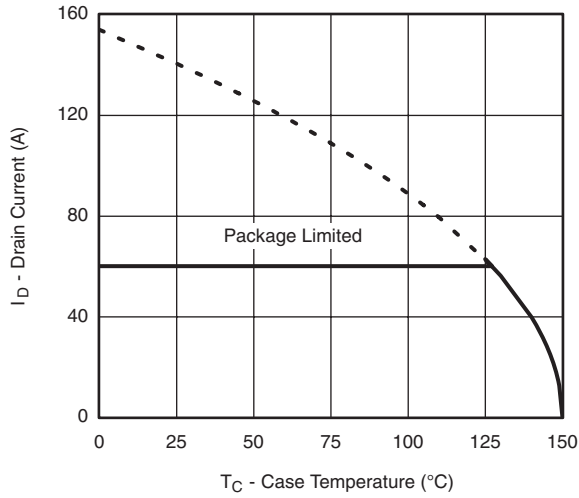
Single Pulse Power, Junction-to-Ambient



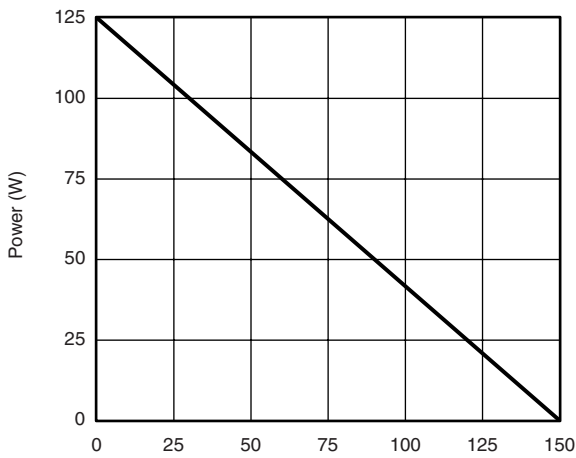
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

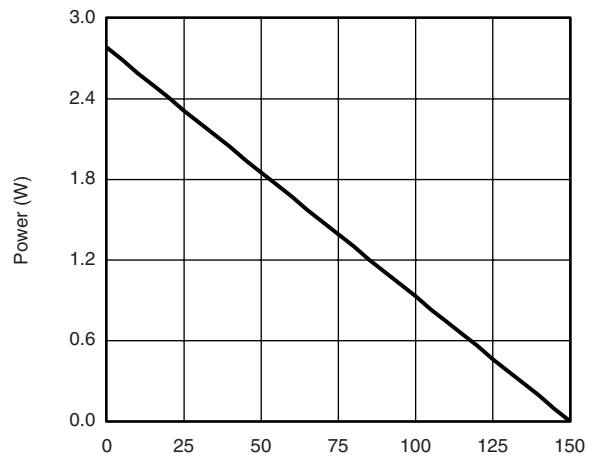
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*



Power, Junction-to-Case

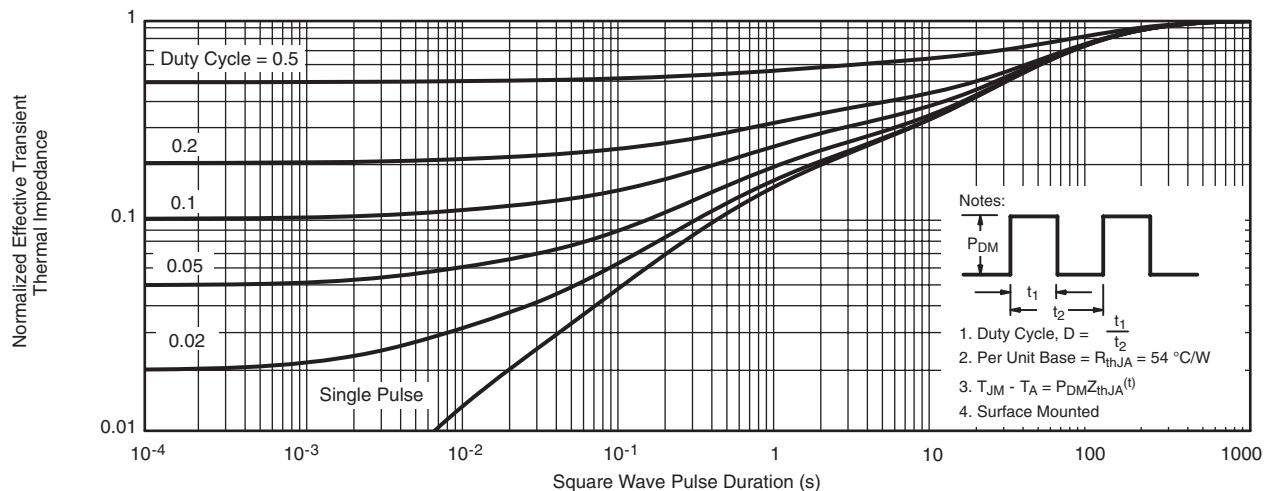


Power, Junction-to-Ambient

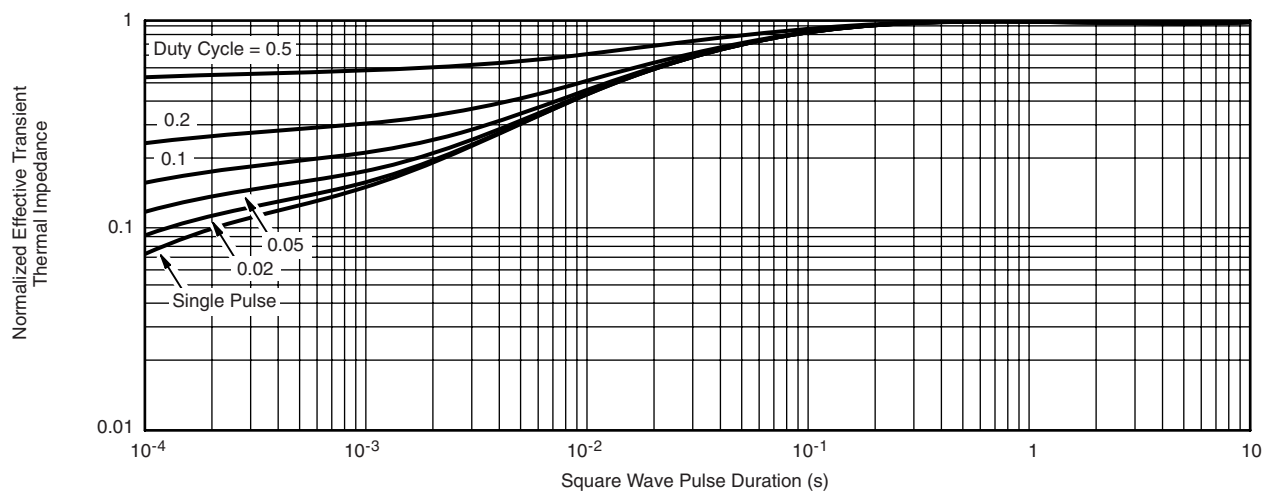
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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