TOSHIBA Multichip Discrete Device

# HN7G01FE

Power Management Switch Applications
Driver Circuit Applications
Interface Circuit Applications

Q1 (transistor): 2SA1955 equivalent

• Q2 (MOSFET): SSM3K03FE equivalent

#### Q1 (Transistor) Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Collector-base voltage	V <sub>CBO</sub>	-15	V
Collector-emitter voltage	V <sub>CEO</sub>	-12	V
Emitter-base voltage	V <sub>EBO</sub>	-5	V
Collector current	IC	-400	mA
Base current	ΙΒ	-50	mA

#### Q2 (MOSFET) Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Drain-source voltage	$V_{DS}$	20	V
Gate-source voltage	V <sub>GSS</sub>	10	V
Drain current	ID	50	mA

# Unit: mm 1.6±0.05 1.2±0.05 **EMITTER** 2. 3. 4. **BASE DRAIN** SOURCE 5. GATE COLLECTOR ES6 **JEDEC JEITA TOSHIBA** 2-2N1F

Weight: 0.003 g (typ.)

## Q1, Q2 Common Ratings (Ta = 25°C)

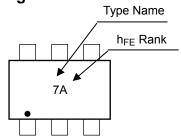
Characteristic	Symbol	Rating	Unit
Power dissipation	P (Note 1)	100	mW
Junction temperature	Тj	125	°C
Storage temperature range	T <sub>stg</sub>	-55~125	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

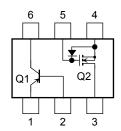
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Total rating

#### Marking



#### Pin Assignment (top view)



# Q1 (Transistor) Electrical Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Condition	Min	Тур.	Max	Unit
Collector cutoff current	I <sub>CBO</sub>	$V_{CB} = -15 \text{ V}, I_E = 0$	_	_	-0.1	μΑ
Emitter cutoff current	I <sub>EBO</sub>	$V_{EB} = -5 \text{ V}, I_C = 0$	_	_	-0.1	μΑ
DC current gain	h <sub>FE</sub> (Note 2)	$V_{CE} = -2 \text{ V}, I_{C} = -10 \text{ mA}$	300	_	1000	
Collector-emitter saturation voltage	V <sub>CE</sub> (sat) (1)	$I_C = -10$ mA, $I_B = -0.5$ mA		-15	-30	mV
	V <sub>CE</sub> (sat) (2)	$I_C = -200 \text{ mA}, I_B = -10 \text{ mA}$		-110	-250	1117
Base-emitter saturation voltage	V <sub>BE (sat)</sub>	$I_C = -200 \text{ mA}, I_B = -10 \text{ mA}$	_	-0.87	-1.2	٧

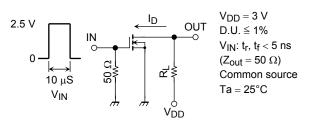
Note 2: hFE classification A: 300~600, B: 500~1000

## Q2 (MOSFET) Electrical Characteristics (Ta = 25°C)

Chara	Characteristic Symbol Test Condition		Min	Тур.	Max	Unit	
Gate leakage curr	ent	I <sub>GSS</sub>	$V_{GS} = 10 \text{ V}, V_{DS} = 0$	_	_	1	μΑ
Drain-source brea	kdown voltage	V (BR) DSS	$I_D = 100 \ \mu A, \ V_{GS} = 0$	20	_	_	V
Drain cutoff currer	nt	I <sub>DSS</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0	_	_	1	μΑ
Gate threshold vo	Itage	V <sub>th</sub>	$V_{DS} = 3 \text{ V}, I_{D} = 0.1 \text{ mA}$	0.7	_	1.3	V
Forward transfer a	admittance	Y <sub>fs</sub>	$V_{DS} = 3 \text{ V}, I_{D} = 10 \text{ mA}$	25	50	_	mS
Drain-source ON-	resistance	R <sub>DS</sub> (ON)	$I_D = 10 \text{ mA}, V_{GS} = 2.5 \text{ V}$	_	4	12	Ω
Input capacitance		C <sub>iss</sub>	$V_{DS} = 3 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	_	11.0	_	pF
Reverse transfer of	capacitance	C <sub>rss</sub>	$V_{DS} = 3 V$ , $V_{GS} = 0$ , $f = 1 MHz$	_	3.3	_	pF
Output capacitance		Coss	$V_{DS} = 3 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	_	9.3	_	pF
Switching time	Turn-on time	t <sub>on</sub>	$V_{DD} = 3 \text{ V}, I_D = 10 \text{ mA}, V_{GS} = 0~2.5 \text{ V}$	_	0.16	_	6
	Turn-off time	t <sub>off</sub>	$V_{DD} = 3 \text{ V}, I_D = 10 \text{ mA}, V_{GS} = 0~2.5 \text{ V}$	_	0.19	_	μS

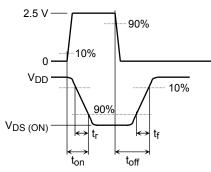
# **Switching Time Test Circuit**

(a) Switching time test circuit

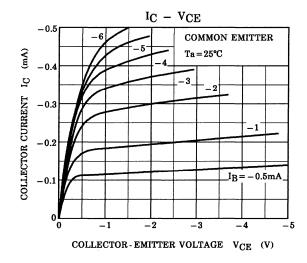


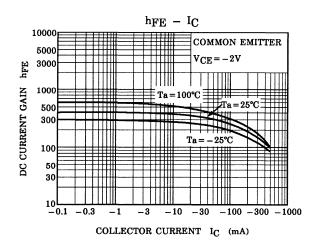


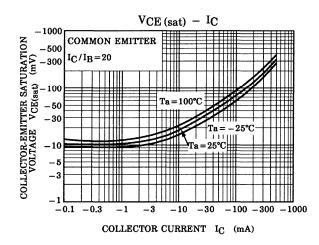


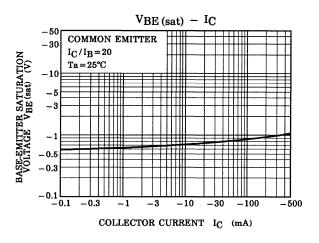


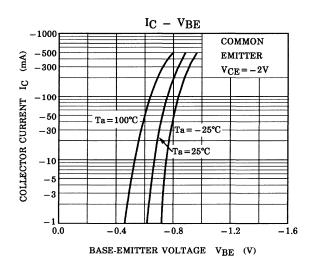
#### Q1 (Transistor)





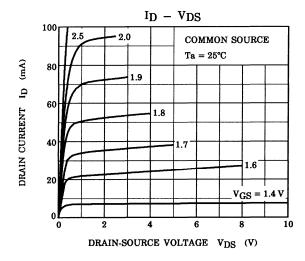


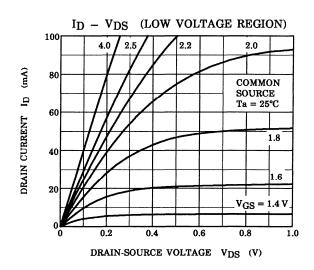


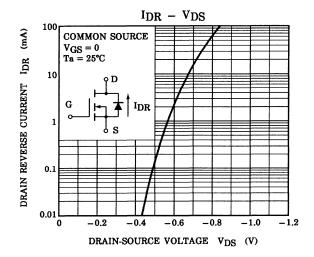


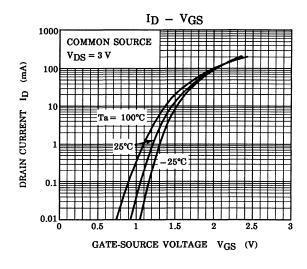
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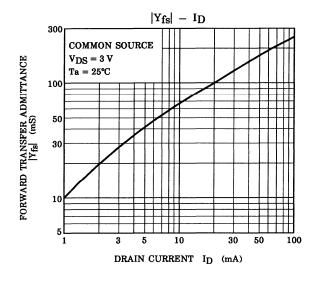
#### Q2 (S-MOS)

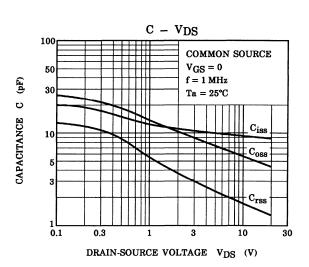




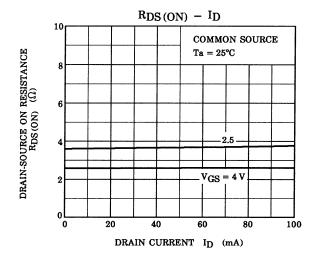


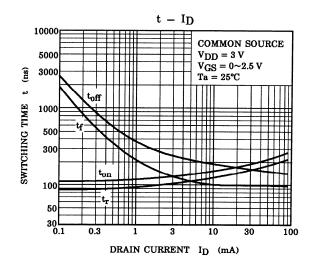


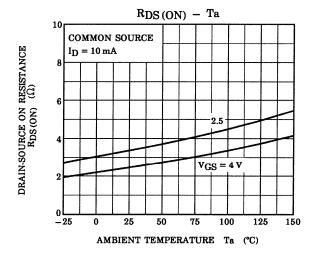




# Q2 (S-MOS)

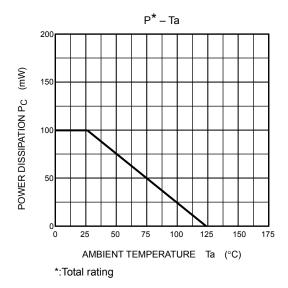






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# Q1, Q2 Common



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