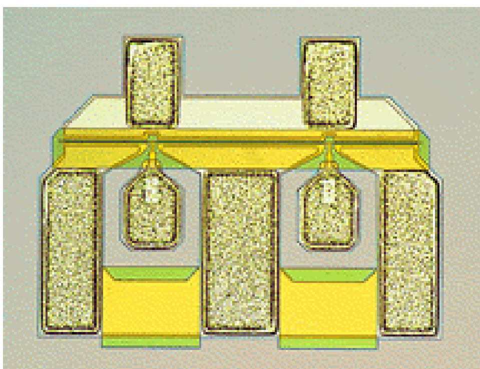
TriQuint SEMICONDUCTOR®

Product Data Sheet

February 1, 2002

Discrete MESFET

TGF1350-SCC



Key Features and Performance

- 0.5 um x 300 um FET
- 1.5 dB Noise Figure with 11dB Associated Gain at 10 GHz
- 2.5 dB Noise Figure with 7 dB Associated Gain at 18 GHz
- All-Gold Metallization for High Reliability
- Recessed Gate Structure
- 0.620 x 0.514 x 0.102 mm (0.024 x 0.020 x 0.004 in.)

Description

The TriQuint TGF1350-SCC is a single-gate GaAs field-effect transistor (FET) used for low-noise applications DC to 18 GHz. Bond pad is gold plated for compatibility with thermocompression and thermosonic compatibility wire-bonding processes. The TGF1350-SCC is readily assembled using automated equipment. Die attach should be accomplished with conductive epoxy only. Eutectic attach is not recommended .

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TABLE I
MAXIMUM RATINGS

Symbol	Parameter 4/	Value	Notes
V^+	Positive Supply Voltage	8 V	
V^-	Negative Supply Voltage Range	-6V TO 0V	
P_D	Power Dissipation	0.7 W	3/
T_{CH}	Operating Channel Temperature	150 ^{0}C	1/ 2/
T_M	Mounting Temperature (30 Seconds)	320 ^{0}C	
T_{STG}	Storage Temperature	-65 to 150 ^{0}C	

1/ These ratings apply to each individual FET.

2/ Junction operating temperature will directly affect the device median time to failure (T_M). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

3/ Power dissipation, P_D is at (or below) 25°C base-plate temperature. For operation above 25°C base-plated temperature, derate linearly at the rate of 1.4 mW/ °C

4/ These ratings represent the maximum operable values for this device.

TYPICAL MAXIMUM STABLE GAIN

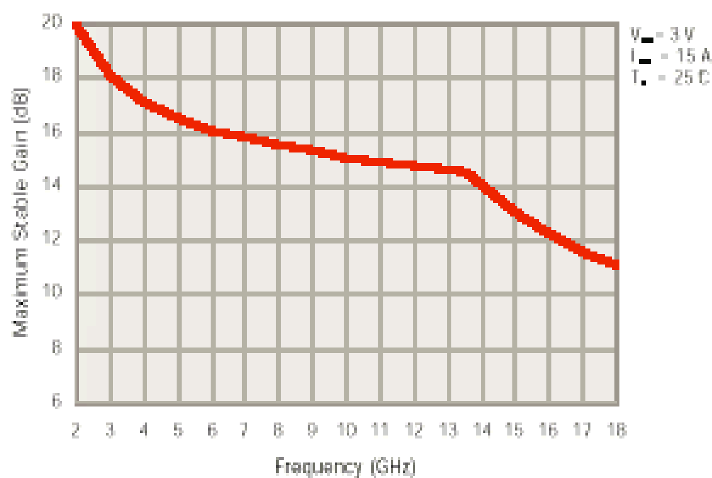

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TABLE II
DC PROBE TEST
(TA = 25 °C ± 5 °C)

Symbol	Parameter	Minimum	Maximum	Unit
Idss	Saturated Drain Current	30	84	mA
V_P	Pinch-off Voltage	-1.8	-0.5	V
BVGS	Breakdown Voltage Gate-Source	-30	-6	V
BVGD	Breakdown Voltage Gate-Drain	-30	-6	V

TABLE III
AUTOPROBE FET PARAMETER MEASUREMENT CONDITONS

FET Parameters	Test Conditions
I_{DSS} : Maximum drain current (I_{DS}) with gate voltage (V_{GS}) at zero volts.	V_{GS} = 0.0 V, drain voltage (V_{DS}) is swept from 0.5 V up to a maximum of 3.5 V in search of the maximum value of I_{DS}; voltage for I_{DSS} is recorded as VDSP.
V_P : Pinch-Off Voltage; V_{GS} for I_{DS} = 0.5 mA/mm of gate width.	V_{DS} fixed at 2.0 V, V_{GS} is swept to bring I_{DS} to 0.5 mA/mm.
V_{BVGD} : Breakdown Voltage, Gate-to-Drain; gate-to-drain breakdown current (I_{BD}) = 1.0 mA/mm of gate width.	Drain fixed at ground, source not connected (floating), 1.0 mA/mm forced into gate, gate-to-drain voltage (V_{GD}) measured is V_{BVGD} and recorded as BVGD; this cannot be measured if there are other DC connections between gate-drain, gate-source or drain-source.
V_{BVGS} : Breakdown Voltage, Gate-to-Source; gate-to-source breakdown current (I_{BS}) = 1.0 mA/mm of gate width.	Source fixed at ground, drain not connected (floating), 1.0 mA/mm forced into gate, gate-to-source voltage (V_{GS}) measured is V_{BVGS} and recorded as BVGS; this cannot be measured if there are other DC connections between gate-drain, gate-source or drain-source.

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TYPICAL S-PARAMETERS

Frequency	S_{11}		S_{21}		S_{12}		S_{22}	
(GHz)	MAG	ANG (°)	MAG	ANG (°)	MAG	ANG (°)	MAG	ANG (°)
2.0	0.98	-28	3.22	157	0.03	75	0.71	-12
2.5	0.96	-36	3.17	151	0.04	71	0.71	-14
3.0	0.93	-44	3.07	146	0.04	68	0.71	-14
3.5	0.93	-51	2.99	141	0.05	65	0.69	-16
4.0	0.90	-56	2.88	137	0.05	62	0.68	-17
4.5	0.89	-60	2.78	133	0.05	61	0.68	-19
5.0	0.88	-64	2.73	129	0.06	60	0.67	-24
5.5	0.87	-67	2.65	125	0.06	58	0.66	-28
6.0	0.85	-70	2.55	121	0.06	56	0.66	-30
6.5	0.83	-74	2.46	118	0.06	55	0.66	-31
7.0	0.82	-77	2.36	116	0.06	54	0.66	-32
7.5	0.82	-80	2.28	113	0.06	54	0.66	-32
8.0	0.81	-82	2.22	110	0.06	53	0.66	-33
8.5	0.81	-85	2.15	107	0.06	52	0.65	-34
9.0	0.80	-88	2.12	104	0.06	51	0.65	-38
9.5	0.79	-92	2.08	101	0.06	51	0.65	-40
10.0	0.78	-96	2.05	98	0.06	51	0.65	-43
10.5	0.78	-99	2.02	95	0.06	50	0.65	-45
11.0	0.77	-103	2.00	92	0.06	48	0.65	-48
11.5	0.78	-106	1.96	88	0.06	46	0.65	-51
12.0	0.77	-110	1.90	84	0.06	44	0.65	-54
12.5	0.77	-114	1.84	81	0.06	42	0.64	-56
13.0	0.76	-117	1.79	79	0.06	39	0.64	-58
13.5	0.75	-120	1.74	76	0.06	37	0.64	-60
14.0	0.75	-123	1.69	73	0.07	35	0.64	-64
14.5	0.74	-125	1.64	69	0.07	32	0.64	-69
15.0	0.74	-128	1.56	65	0.07	29	0.65	-74
15.5	0.74	-131	1.49	61	0.07	25	0.66	-78
16.0	0.73	-133	1.43	59	0.08	23	0.65	-81
16.5	0.72	-136	1.38	57	0.08	21	0.65	-81
17.0	0.73	-139	1.36	54	0.08	21	0.66	-81
17.5	0.73	-140	1.31	52	0.09	22	0.66	-82
18.0	0.74	-142	1.26	50	0.09	22	0.66	-83

T_A = 25°C, V_{DS} = 3 V, I_{DS} = 15mA

Reference planes for S-parameter data are located at center of gate and drain bond pads. Three 0.7 mil diameter wires, approximately 13 mils long, are bonded from the center of each of the source pads to ground. The S-parameters are also available on floppy disk and the world wide web.

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RF CHARACTERISTICS

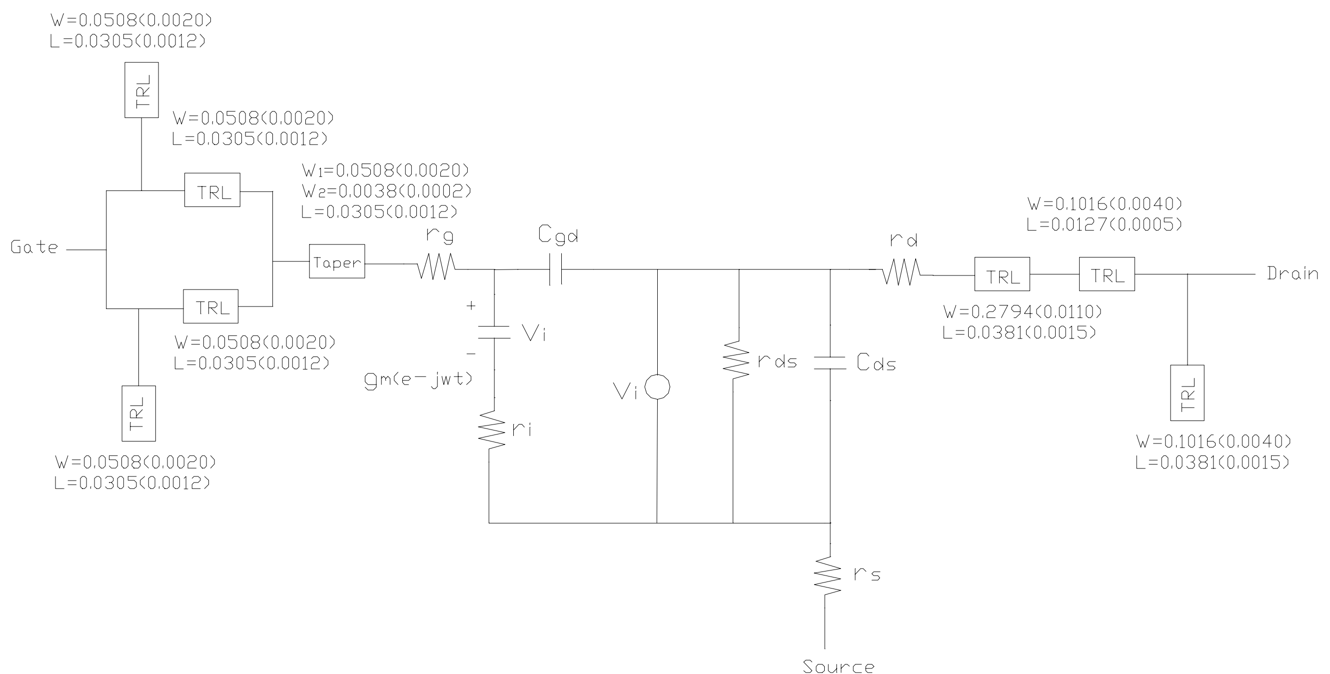
PARAMETER		TEST CONDITIONS	TYP	UNIT
NF_{MIN}	Minimum noise figure	10 GHz	1.5	dB
		18 GHz	2.5	
G_A	Associated gain	10 GHz	11	
		18 GHz	7	

V_{DS} = 3 V, I_{DS} = 15mA, T_A = 25°C

TYPICAL MODEL PARAMETERS

PARAMETER		VALUE	STANDARD DEVIATION	UNIT
r_s	Source resistance	5.62	0.6	Ω
r_d	Drain resistance	4.48	0.4	Ω
r_g	Gate resistance	4.68	0.5	Ω
g_m	Transconductance	52.32	6	mS
r_{ds}	Drain–to–source resistance	224	40	Ω
r_i	Input resistance	1.30	1	Ω
C_{gs}	Gate–to–source capacitance	0.351	0.027	pF
C_{gd}	Gate–to–drain capacitance	0.0159	0.0037	pF
C_{ds}	Drain–to–source capacitance	0.0877	0.0095	pF
τ	Time constant	2.33	0.1	ps

EQUIVALENT SCHEMATIC



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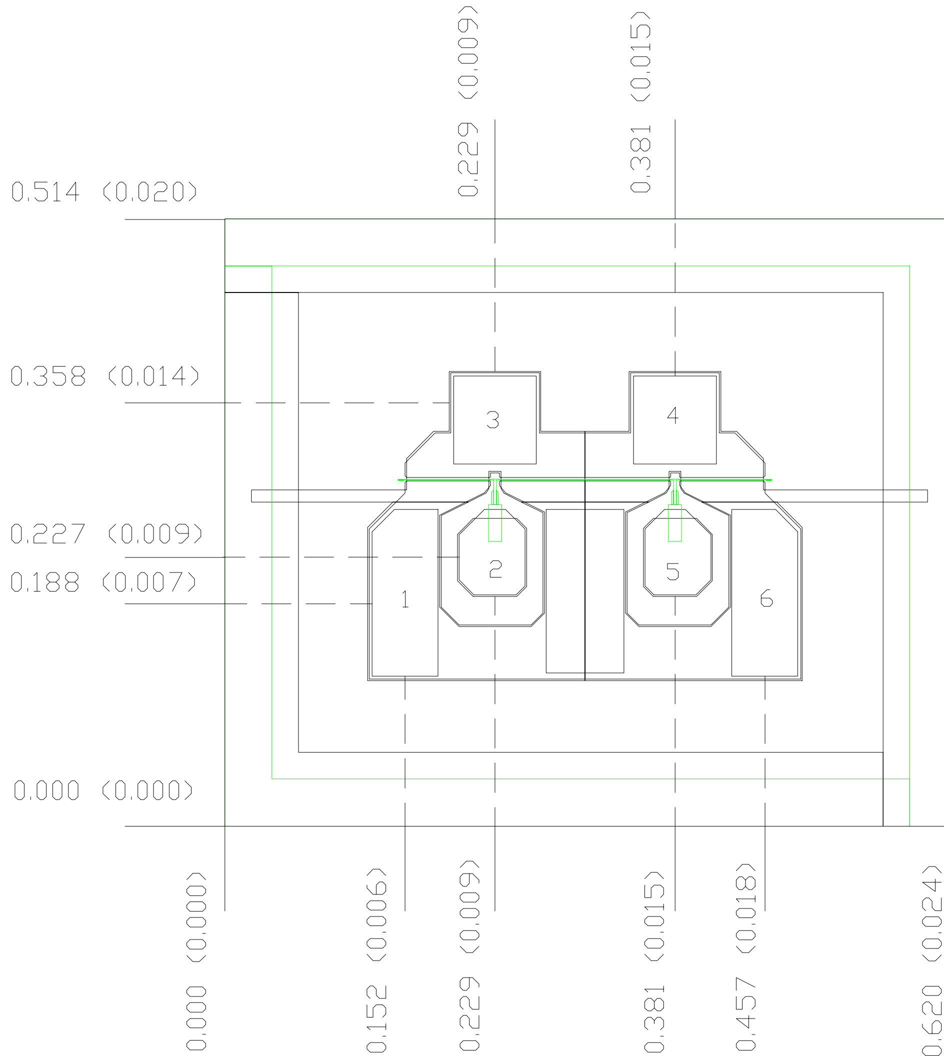
Mechanical Drawing



Units: millimeters (inches)
Thickness: 0.1016 (0.004)
Chip edge to bond pad dimensions are shown to center of bond pad
Chip size tolerance: +/- 0.051 (0.002)

Bond pads #1,6	(Source)	0.056 x 0.141 (0.002 x 0.006)
Bond pads #2,5	(Gate)	0.056 x 0.066 (0.002 x 0.003)
Bond pads #3,4	(Drain)	0.070 x 0.074 (0.003 x 0.003)

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handing, assembly and test.

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Assembly Process Notes

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300°C.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire.
- Maximum stage temperature is 200°C.

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