AP561

0.7-2.9 GHz 8W Power Amplifier

Product Features

- 0.7 – 2.9 GHz
- +39 dBm P1dB
- 13 dB Gain @ 2.6 GHz
- 1.5% EVM @ 30 dBm Pout
- +12 V Supply Voltage
- Lead-free/green/RoHS-compliant 5x6 mm power DFN package

Applications

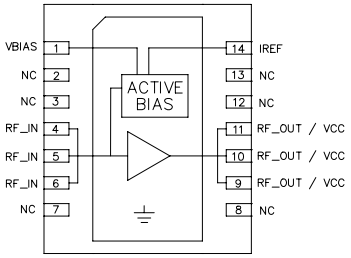
- Final stage amplifiers for repeaters
- High Power Amplifiers
- Mobile Infrastructure
- LTE/WCDMA/EDGE/CDMA

Product Description

The AP561 is a high dynamic range broadband power amplifier in a surface mount package. The single-stage amplifier has 13 dB Gain, while being able to achieve high performance for 0.7–2.9 GHz applications with up to +39 dBm of compressed 1dB power.

The AP561 uses a high reliability +12V InGaP/GaAs HBT process technology. The device incorporates proprietary bias circuitry to compensate for variations in linearity and current draw over temperature. The device does not require any negative bias voltage; an internal active bias allows the AP561 to operate directly off a commonly used +12V supply and has the added feature of a +5V power down control pin. RoHS-compliant 5x6mm DFN package is surface mountable to allow for low manufacturing costs to the end user.

Functional Diagram



Function	Pin No.
RF_{IN}	4,5,6
RF_{OUT}	9,10,11
I_{REF}	14
V_{BIAS}	1
NC	2,3,7,8,12,13

Specifications

Parameter	Units	Min	Typ	Max
Operational Bandwidth	GHz	0.7		2.9
Test Frequency	MHz		2600	
Output Channel Power	dBm		+30	
Power Gain	dB		13.1	
Input Return Loss	dB		13	
Output Return Loss	dB		6.2	
Error Vector Magnitude	%		1.5	
Operating Current, Icc	mA		480	
Collector Efficiency	%		17.6	
RF Switching Speed	ns		50	
Output P1dB	dBm		39.0	
Quiescent Current, Icq	mA		300	
Reference Current, Iref	mA		10	
Vpd[4]	V		+5	
Vcc	V		+12	

Notes:
1. Test conditions unless otherwise noted: T = 25ºC, Vpd = +5V, Vcc = +12, Icq = 300mA at Pout = +30 dBm and f = 2.6 GHz.
2. Using an 802.16-2004 OFDMA, 64QAM-1/2,1024-FFT, 20 symbols, 30 subchannels signal, 9.5 dB PAR @ 0.01%.
3. Switching speed: 50% TTL to 100/0% RF.Vpd used for device power down (low=RF off).
4. Vpd relates to Iref as shown in Table 1 on Page 13.
5. Capable of handling 10:1 VSWR @ 12 V_{DC}, WiMax signal, $Pout_{AVG}$ = 30dBm.

Typical Performance

Parameter	Units	Typical		
Test Frequency	MHz	880	2140	2600
Channel Power	dBm	+28	+28	+30
Power Gain	dB	15.8	13.8	13.1
Input Return Loss	dB	15	12	13
Output Return Loss	dB	10	8.0	6.2
Error Vector Magnitude	%			1.5
ACLR	dBc	-52	-50	
Operating Current, Icc	mA	470	430	480
Collector Efficiency	%	11.2	12	17.6
Output P1dB	dBm	39	37.1	39.0
Quiescent Current, Icq	mA		300	
Reference Current, Iref	mA		10	
Vpd	V		+5	
Vcc	V		+12	

Absolute Maximum Rating

Parameter	Rating
Pin max (CW into 50Ω load)	+33 dBm
BVcbo	35 V
Pdiss max	14 W
Supply Voltage	15 V
Storage Temperature	-55 to +150 ºC
Max Junction Temperature, T_J For 10^6 hours MTTF	158 ºC
Thermal Resistance, Θ_{JC}	8.4 °C / W

Operation of this device above any of these parameters may cause permanent damage.

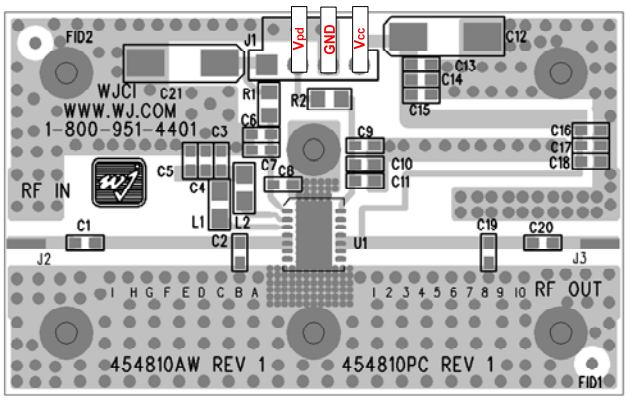
Ordering Information

Part No.	Description
AP561-F	0.7-2.9 GHz 12V 8W Power Amplifier
AP561-PCB900	869-894 MHz Evaluation Board
AP561-PCB2140	2110-2170 MHz Evaluation Board
AP561-PCB2500	2.5-2.7 GHz Evaluation Board

Standard T/R size = 500 pieces on a 7" reel.

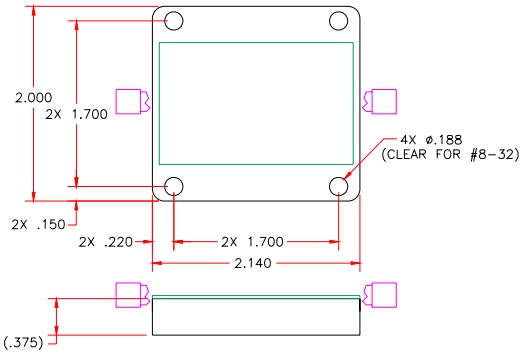
Specifications and information are subject to change without notice

Application Circuit PC Board Layout



Circuit Board Material: 0.0147" Rogers Ultralam 2000, single layer, 1 oz copper, ε_r = 2.45, Microstrip line details: width = .043", spacing = .050"

Baseplate Configuration



Notes:
1. Please note that for reliable operation, the evaluation board will have to be mounted to a much larger heat sink during operation and in laboratory environments to dissipate the power consumed by the device. The use of a convection fan is also recommended in laboratory environments.
2. The area around the module underneath the PCB should not contain any soldermask in order to maintain good RF grounding.
3. For proper and safe operation in the laboratory, the power-on sequencing is recommended.

Evaluation Board Bias Procedure

Following bias procedure is recommended to ensure proper functionality of AP561 in a laboratory environment. The sequencing is not required in the final system application.

Bias.	Voltage (V)
Vcc	+12
Vpd	+5

Turn-on Sequence:

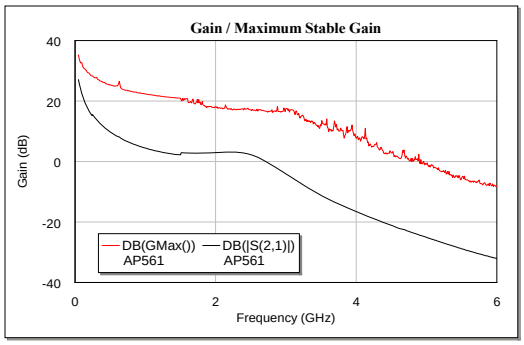
1. Attach input and output loads onto the evaluation board.
2. Turn on power supply Vcc = +12V.
3. Turn on power supply Vpd = +5V.
4. Turn on RF power.

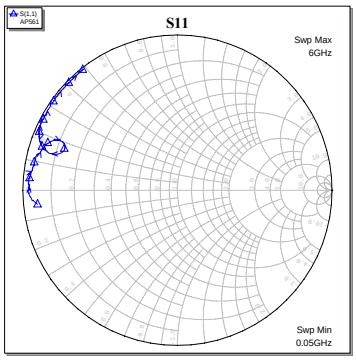
Turn-off Sequence:

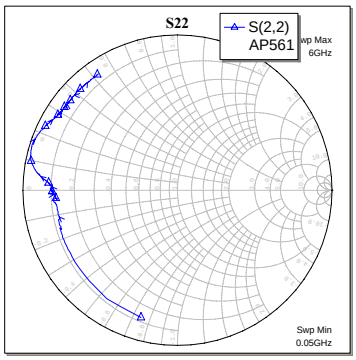
1. Turn off RF power.
2. Turn off power supply Vpd = +5V.
3. Turn off power supply Vcc = +12V.

Typical Device Data

S-Parameters (V_{CC}= +12 V, I_{CC} = 300 mA, 25 °C, unmatched 50 ohm system)







Notes:
The gain for the unmatched device in 50 ohm system is shown as the trace in black color. For a tuned circuit for a particular frequency, it is expected that actual gain will be higher, up to the maximum stable gain. The maximum stable gain is shown in the red line.

S-Parameters (V_{CC} = +12 V, I_{CQ} = 300 mA, 25 °C, unmatched 50 ohm system, calibrated to device leads)

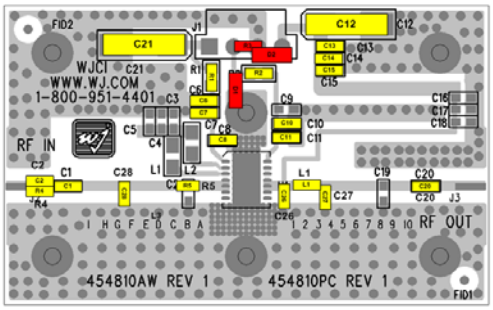
Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	-0.83	-174.19	27.09	122.75	-43.35	29.12	-1.38	-106.01
100	-0.43	-177.42	22.26	106.35	-43.10	8.71	-1.82	-138.64
300	-0.35	179.26	14.06	89.18	-41.21	1.08	-2.02	-164.78
500	-0.32	177.35	9.81	79.93	-40.63	0.69	-2.10	-172.01
700	-0.34	175.28	7.08	71.64	-40.35	3.54	-2.09	-176.13
900	-0.40	173.11	5.19	63.88	-40.26	-3.79	-1.99	-177.89
1100	-0.47	170.97	3.82	55.72	-40.09	-9.55	-1.86	-178.93
1300	-0.53	168.26	2.80	47.12	-39.83	-16.44	-1.78	-179.77
1500	-0.59	165.56	2.18	37.92	-39.58	-23.59	-1.68	179.34
1700	-0.87	161.87	2.75	25.71	-38.56	-35.47	-1.67	177.40
1900	-1.14	158.99	2.84	12.58	-37.79	-49.59	-1.45	176.17
2100	-1.58	157.33	3.04	-4.10	-37.20	-69.96	-1.07	174.50
2300	-2.07	158.08	3.08	-26.45	-36.71	-98.60	-0.57	171.36
2500	-2.11	161.67	2.27	-53.16	-36.83	-134.34	-0.20	166.20
2700	-1.52	163.86	0.21	-79.14	-37.65	-170.26	-0.18	160.52
2900	-0.93	162.94	-2.57	-100.12	-38.71	157.51	-0.38	155.92
3100	-0.60	161.26	-5.57	-115.90	-39.66	133.27	-0.55	152.79
3300	-0.44	159.75	-8.55	-127.57	-40.18	115.97	-0.68	150.56
3500	-0.30	157.96	-11.15	-136.15	-40.26	102.36	-0.77	148.63
3700	-0.20	156.27	-13.44	-143.55	-40.26	94.11	-0.84	147.06
3900	-0.16	154.67	-15.57	-150.57	-39.83	85.11	-0.87	145.70
4100	-0.14	152.82	-17.53	-157.27	-39.91	78.44	-0.87	144.40
4300	-0.15	150.80	-19.35	-163.61	-39.49	72.37	-0.86	143.38
4500	-0.13	148.32	-21.11	-170.25	-39.09	66.71	-0.89	142.13

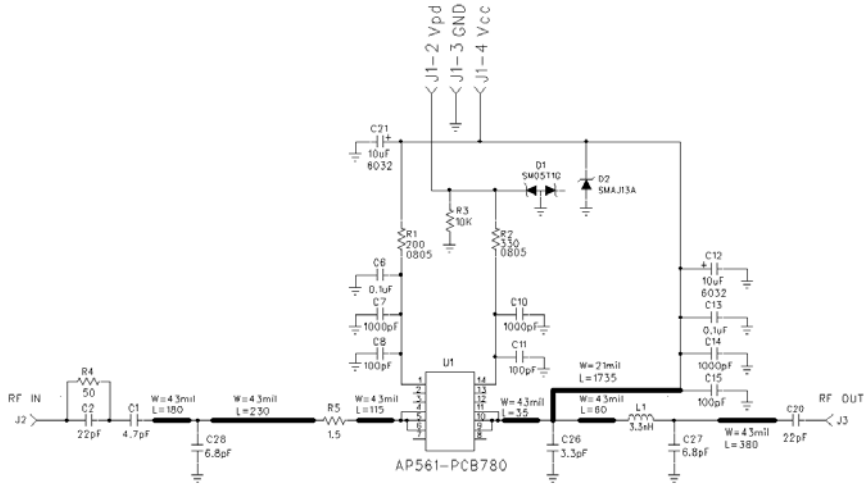
Device S-parameters are available for download off of the website at: http://www.tqs.com

776-787 MHz Reference Design

Typical O-FDMA Performance at 25°C

Frequency (MHz)	776	780	787	Units
Channel Power	+28	+28	+28	dBm
Power Gain	16.1	16.2	16.2	dB
Input Return Loss	11	12	13	dB
Output Return Loss	11	11	11	dB
EVM	0.68	0.64	0.57	%
ACLR	-51	-51	-52	dBc
Operating Current, Icc	405	404	402	mA
Collector Efficiency	13	13	12.9	%
Output P1dB	37.8	37.9	38	dBm
Quiescent Current Icq	300			mA
Reference Current Iref	10			mA
Vpd	+5			V
Vcc	+12			V

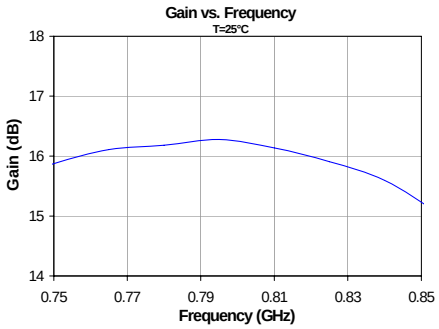


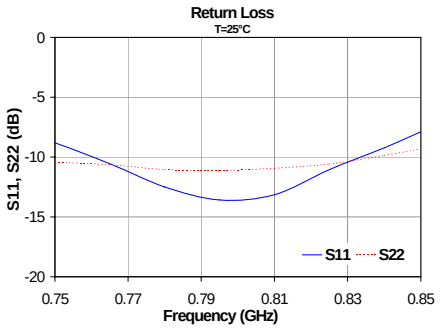


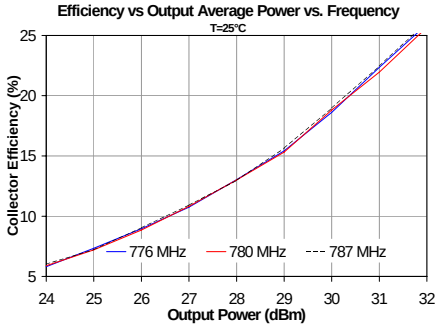
Notes:
1. The primary RF microstrip line is 50 Ω.
2. Do not exceed 5.5V on Vpd or damage to D1 will occur.
3. Do not exceed 13V on Vcc or damage to D2 will occur.
4. Components shown on the silkscreen but not on the schematic are not used.
5. The edge of C26 is placed at 35mil from edge of AP561. (1.2 ° @ 780 MHz)
6. The edge of L1 is placed 60mil from the edge of C26. (2 ° @ 780 MHz)
7. The edge of C27 is placed next to the edge of L1.
8. The edge of C20 is placed 380mil from the edge of C27. (12.9 ° @ 780 MHz)
9. The edge of R5 is placed at 115mil from edge of AP561. (3.9 ° @ 780 MHz)
10. The edge of C28 is placed 230mil from the edge of R5. (7.8 ° @ 780 MHz)
11. The edge of C1 is placed 180mil from the edge of C28. (6.1 ° @ 780 MHz)
12. 0 Ω jumpers can be replaced with copper trace in target application.

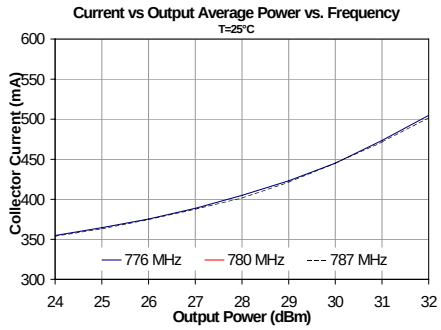
776-787 MHz Application Circuit Performance Plots

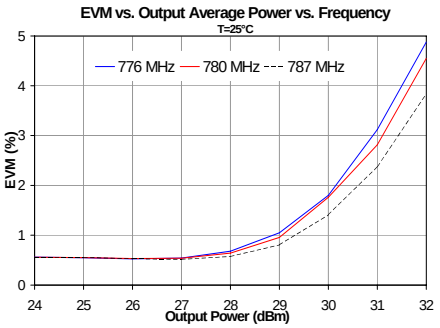
802.16-2004 O-FDMA, 64QAM-1/2, 1024-FFT, 20 symbols and 30 subchannels. 9.5 dB PAR @ 0.01%, 5 MHz Carrier BW

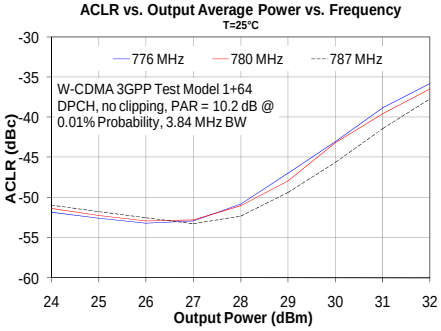








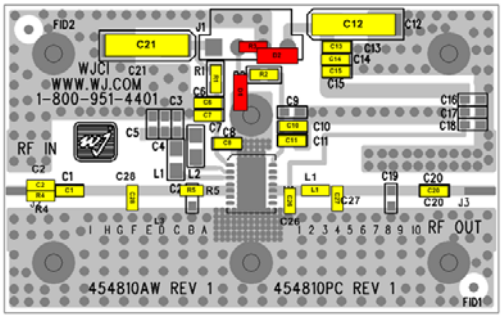


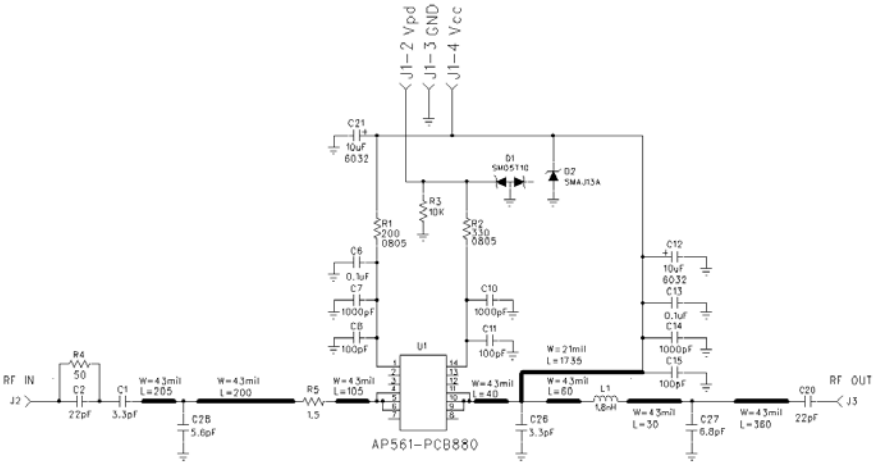


869-894 MHz Reference Design (AP561-PCB900)

Typical W-CDMA Performance at 25°C

Frequency (MHz)	869	880	894	Units
Channel Power	+28	+28	+28	dBm
Power Gain	15.7	15.8	15.7	dB
Input Return Loss	14	15	15	dB
Output Return Loss	9.8	10	11	dB
ACLR	-53	-52	-52	dBc
Operating Current, Icc	475	470	460	mA
Collector Efficiency	11	11.2	11.4	%
Output P1dB	39.1	39	38.8	dBm
Quiescent Current Icq	300			mA
Reference Current Iref	10			mA
Vpd	+5			V
Vcc	+12			V



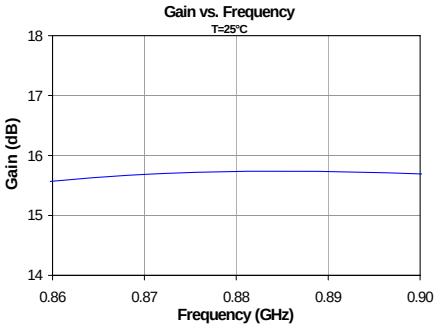


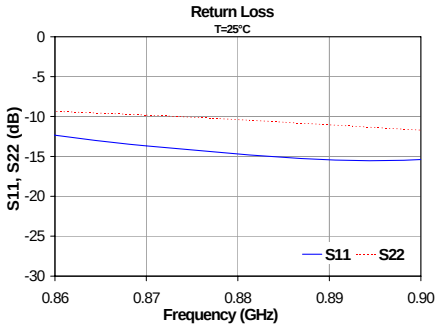
Notes:

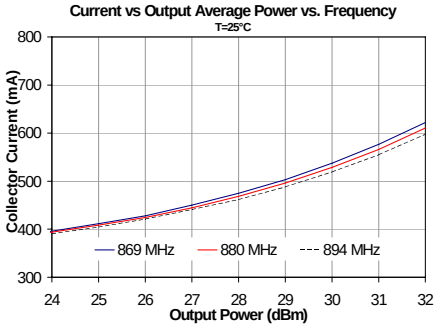
1. The primary RF microstrip line is 50 Ω.
2. Do not exceed 5.5V on Vpd or damage to D1 will occur.
3. Do not exceed 13V on Vcc or damage to D2 will occur.
4. Components shown on the silkscreen but not on the schematic are not used.
5. The edge of C26 is placed at 40mil from edge of AP561. (1.5 ° @ 880 MHz)
6. The edge of L1 is placed 60mil from the edge of C26. (2.3 ° @ 880 MHz)
7. The edge of C27 is placed 43 mil from the edge of L1. (1.6 ° @ 880 MHz)
8. The edge of C20 is placed 380mil from the edge of C27. (14.6 ° @ 880 MHz)
9. The edge of R5 is placed at 105mil from edge of AP561. (4 ° @ 880 MHz)
10. The edge of C28 is placed 200mil from the edge of R5. (7.7 ° @ 880 MHz)
11. 0 Ω jumpers can be replaced with copper trace in target application.

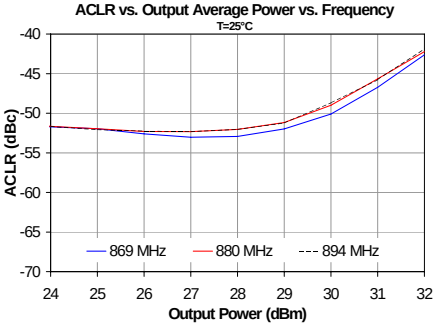
869-894 MHz Application Circuit Performance Plots

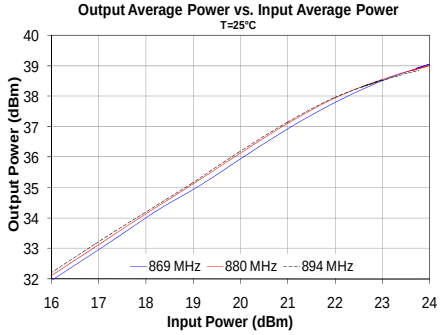
W-CDMA 3GPP Test Model 1+64 DPCH, no clipping, PAR = 10.2 dB @ 0.01% Probability, 3.84 MHz BW

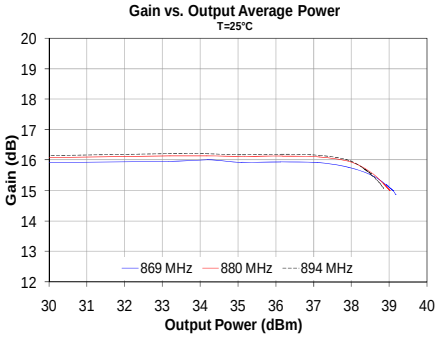








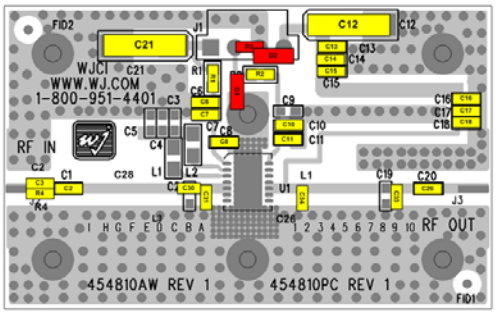


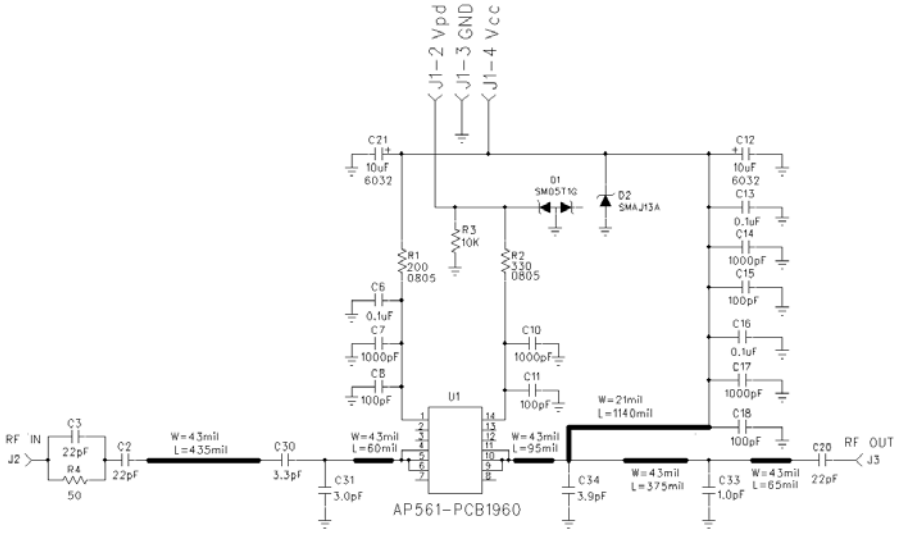


1930-1990 MHz Reference Design

Typical W-CDMA Performance at 25°C

Frequency (MHz)	1930	1960	1990	Units
Channel Power	+28	+28	+28	dBm
Power Gain	15.3	15.4	15.3	dB
Input Return Loss	12	16	18	dB
Output Return Loss	7.7	7.6	7.5	dB
ACLR	-49	-49	-51	dBc
Operating Current, Icc	440	430	425	mA
Collector Efficiency	11.7	12	12.3	%
Output P1dB	39.1	38.7	38.2	dBm
Quiescent Current Icq	300			mA
Reference Current Iref	10			mA
Vpd	+5			V
Vcc	+12			V



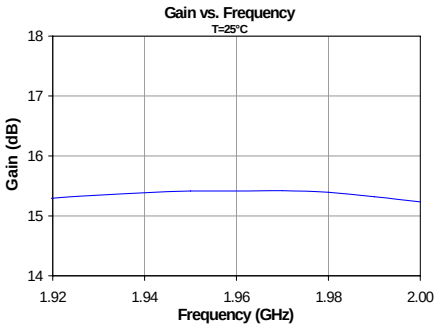


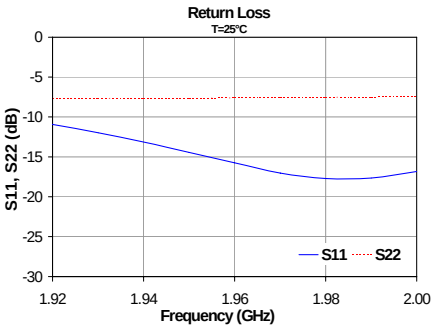
Notes:

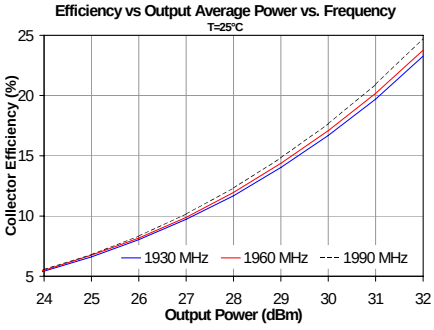
1. The primary RF microstrip line is 50 Ω.
2. Do not exceed 5.5V on Vpd or damage to D1 will occur.
3. Do not exceed 13V on Vcc or damage to D2 will occur.
4. Components shown on the silkscreen but not on the schematic are not used.
5. The edge of C34 is placed at 95mil from edge of AP561. (8.1° @ 1960 MHz)
6. The edge of C33 is placed 375mil from the edge of C34. (32° @ 1960 MHz)
7. The edge of C20 is placed 65mil from the edge of C33. (5.6° @ 1960 MHz)
8. The edge of C31 is placed 60mil from edge of AP561. (5.1° @ 1960 MHz)
9. The edge of C30 is placed next to the edge of C31
10. The edge of C2 is placed 435mil from the edge of C30. (37.2° @ 1960 MHz)
11. 0 Ω jumpers can be replaced with copper trace in target application.

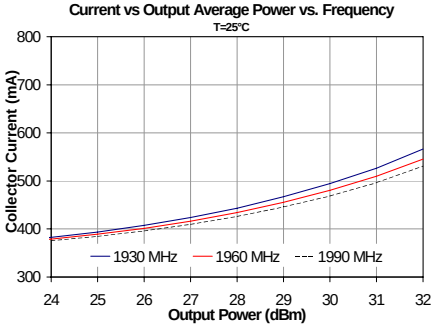
1930-1990 MHz Application Circuit Performance Plots

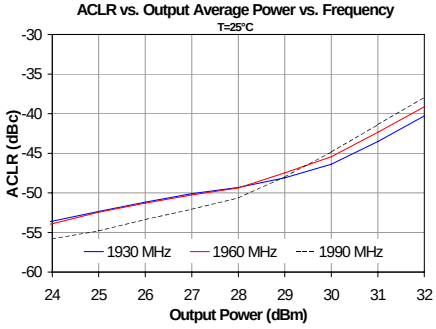
W-CDMA 3GPP Test Model 1+64 DPCH, no clipping, PAR = 10.2 dB @ 0.01% Probability, 3.84 MHz BW







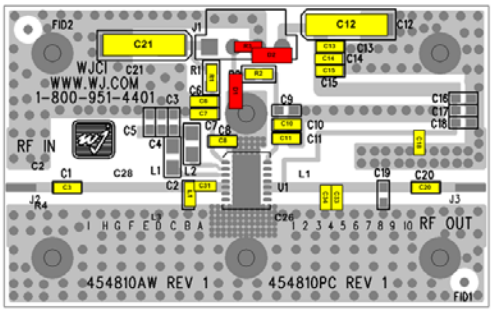


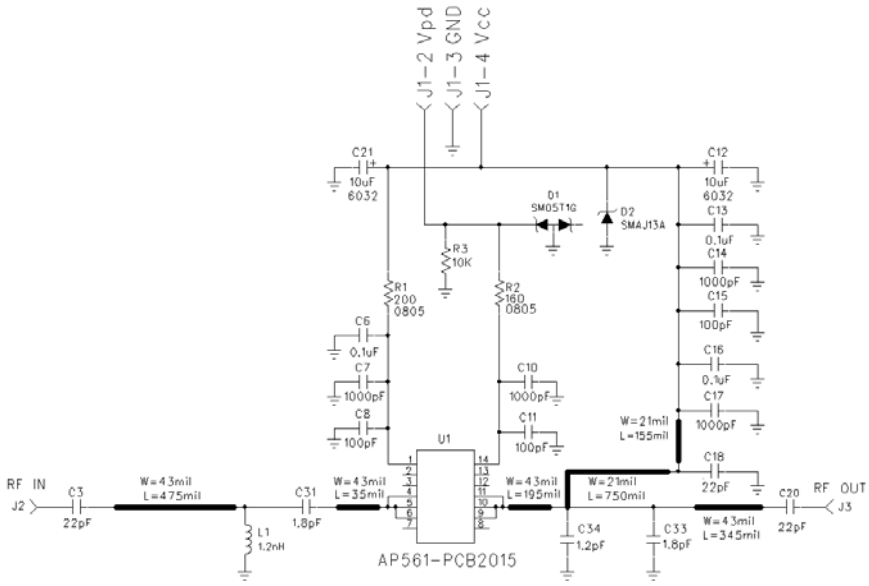


2010-2025 MHz Reference Design

Typical TD-SCDMA Performance at 25°C

Frequency (MHz)	2010	2015	2025	Units
Channel Power	+27	+27	+27	dBm
Power Gain	13	13	13	dB
Input Return Loss	8.4	8.6	8.7	dB
Output Return Loss	6.7	6.6	6.4	dB
ACLR	-49	-49	-49	dBc
Operating Current, Icc	673	675	679	mA
Collector Efficiency	6.2	6.2	6.1	%
Output P1dB	37.4	37.3	37.1	dBm
Quiescent Current Icq	600			mA
Reference Current Iref	20			mA
Vpd	+5			V
Vcc	+12			V

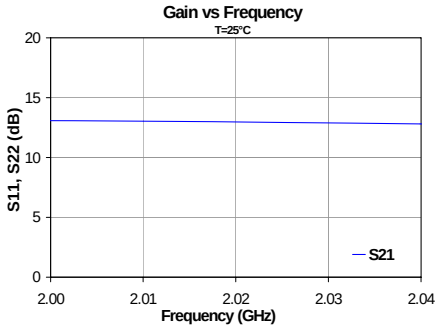


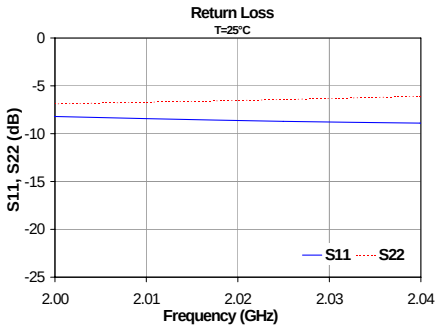


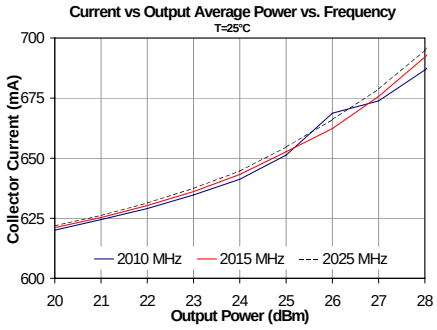
Notes:
1. The primary RF microstrip line is 50 Ω.
2. Do not exceed 5.5V on Vpd or damage to D1 will occur.
3. Do not exceed 13V on Vcc or damage to D2 will occur.
4. Components shown on the silkscreen but not on the schematic are not used.
5. The edge of C31 is placed at 35mil from edge of AP561. (3.1° @ 2015 MHz)
6. The edge of L1 next to the edge of C31.
7. The edge of C34 is placed at 195mil from edge of AP561. (17.1° @ 2015 MHz)
8. The edge of C33 is placed next to the edge of C34.
9. 0 Ω jumpers can be replaced with copper trace in target application.

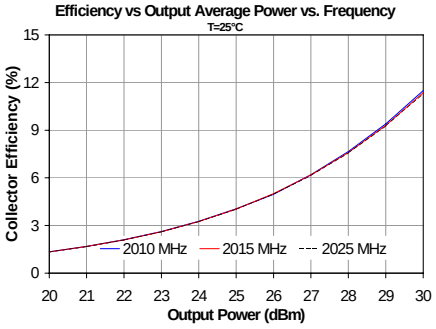
2010-2025 MHz Application Circuit Performance Plots

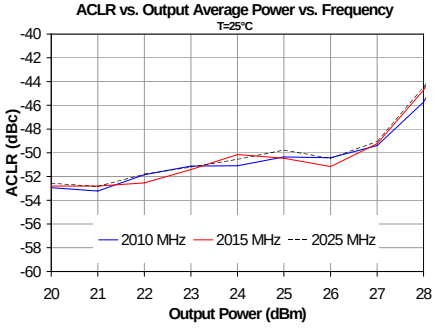
TD-SCDMA 3 Carrier, PAR = 10 dB @ 0.01% Probability, 1.28 MHz BW







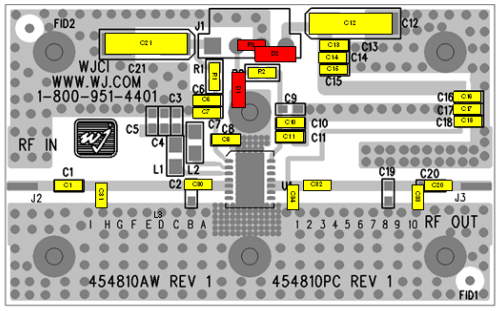


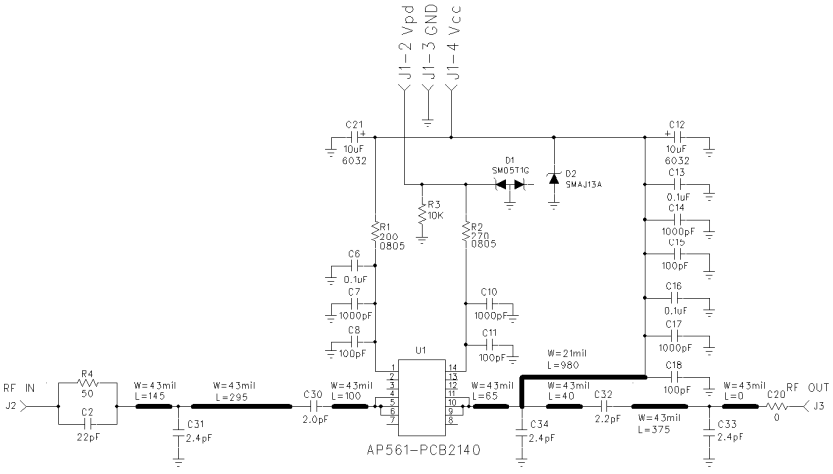


2110-2170 MHz Application Circuit (AP561-PCB2140)

Typical W-CDMA Performance at 25°C

Frequency (MHz)	2110	2140	2170	Units
Channel Power	+28	+28	+28	dBm
Power Gain	13.5	13.8	13.1	dB
Input Return Loss	7.0	12	21	dB
Output Return Loss	12	8.0	6.1	dB
ACLR	-50	-50	-48	dBc
Operating Current, Icc	420	430	450	mA
Collector Efficiency	12	12	11.5	%
Output P1dB	37.7	37.1	36.5	dBm
Quiescent Current Icq	400			mA
Reference Current Iref	15			mA
Vpd	+5			V
Vcc	+12			V

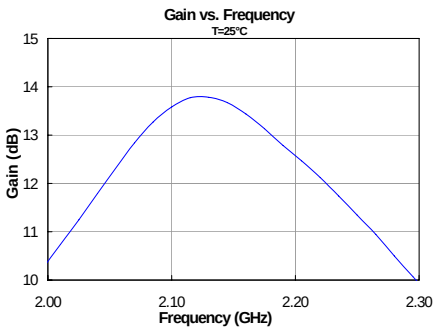


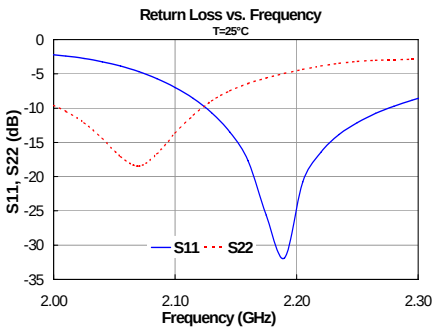


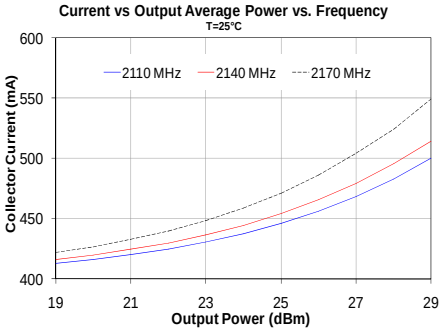
Notes:
1. The primary RF microstrip line is 50 Ω.
2. Do not exceed 5.5V on Vpd or damage to D1 will occur.
3. Do not exceed 13V on Vcc or damage to D2 will occur.
4. Components shown on the silkscreen but not on the schematic are not used.
5. The edge of C34 is placed at 65mil from AP561 RFout pin. (6 º @ 2140 MHz)
6. The edge of C32 is placed 40mil from the edge of C34. (3.7 º @ 2140 MHz)
7. The edge of C33 is placed 375mil from the edge of C32. (35 º @ 2140 MHz)
8. The edge of C30 is placed at 100mil from AP561 RFin pin. (9.3 º @ 2140 MHz)
9. The edge of C31 is placed 295mil from the edge of C30. (25.6 º @ 2140 MHz)
10. 0 Ω jumpers can be replaced with copper trace in target application.

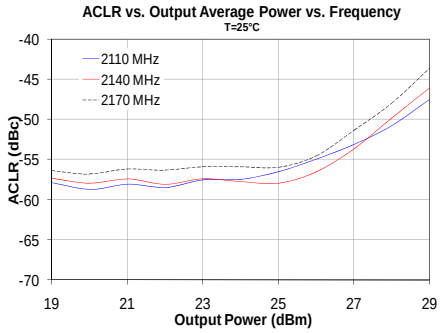
2110-2170 MHz Application Circuit Performance Plots

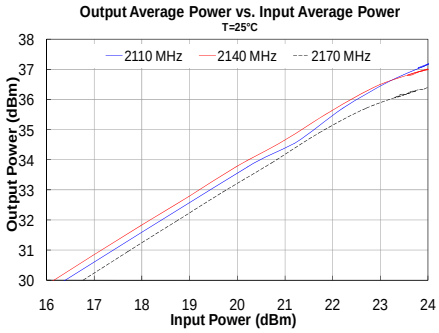
W-CDMA 3GPP Test Model 1+64 DPCH, no clipping, PAR = 10.2 dB @ 0.01% Probability, 3.84 MHz BW

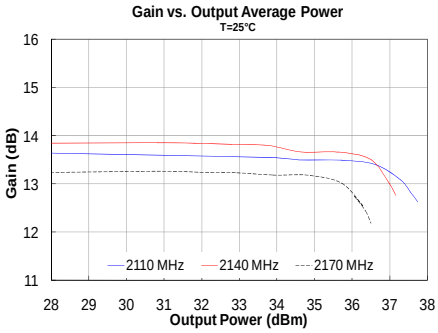








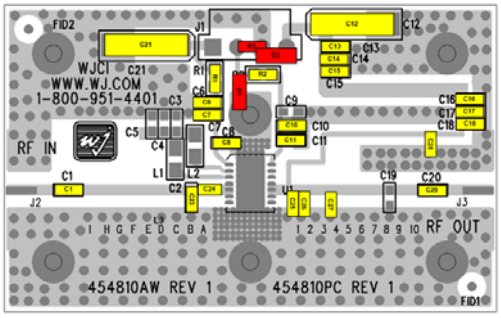


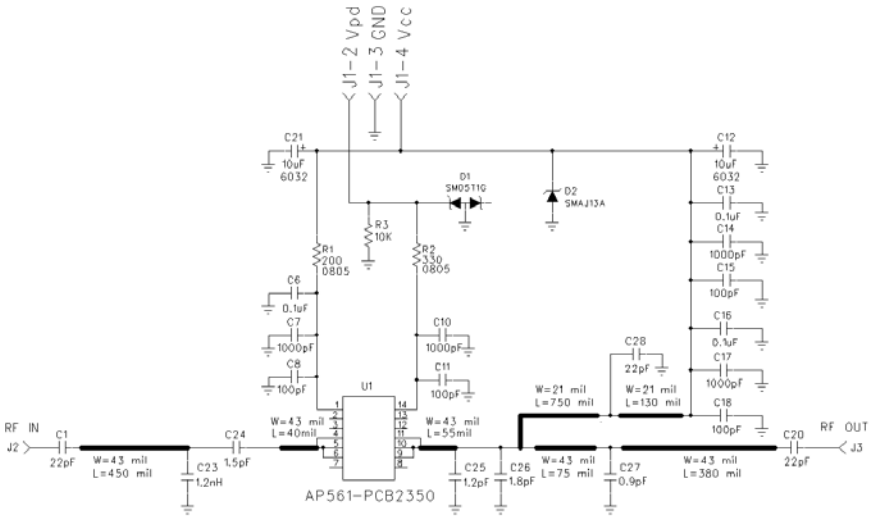


2.3-2.4 GHz Reference Design

Typical O-FDMA Performance at 25°C

Frequency (GHz)	2.3	2.35	2.4	Units
Channel Power	+30	+30	+30	dBm
Power Gain	13.8	13.9	13.7	dB
Input Return Loss	12	16	20	dB
Output Return Loss	7.3	7.6	6.8	dB
EVM	1.9	1.6	1.6	%
Operating Current, Icc	515	490	475	mA
Collector Efficiency	16	16.8	17.8	%
Output P1dB	39.7	39	38	dBm
Quiescent Current Icq	300			mA
Reference Current Iref	10			mA
Vpd	+5			V
Vcc	+12			V

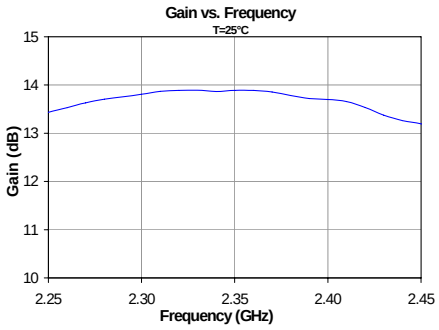


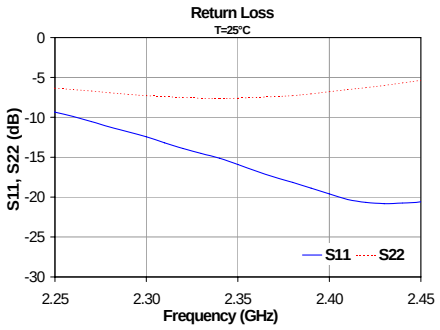


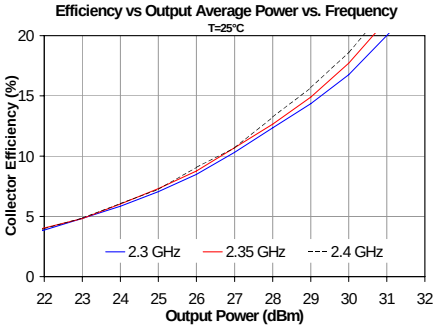
Notes:
1. The primary RF microstrip line is 50 Ω.
2. Do not exceed 5.5V on Vpd or damage to D1 will occur.
3. Do not exceed 13V on Vcc or damage to D2 will occur.
4. Components shown on the silkscreen but not on the schematic are not used.
5. The edge of C25 is placed at 55mil from AP561 RFout pin. (5.6 º @ 2350 MHz)
6. The edge of C26 is placed next to the edge of C25.
7. The edge of C27 is placed 75mil from the edge of C26. (7.7 º @ 2350 MHz)
8. The edge of C24 is placed at 40mil from AP561 RFin pin. (4.1 º @ 2350 MHz)
9. The edge of C23 is placed next to the edge of C24.
10. 0 Ω jumpers can be replaced with copper trace in target application.

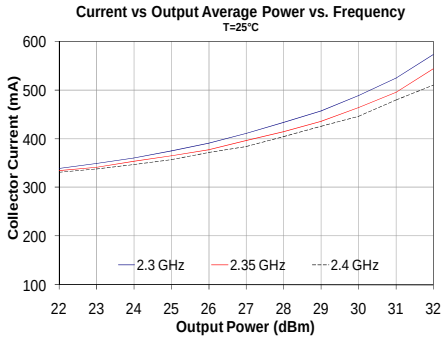
2.3-2.4 GHz Application Circuit Performance Plots

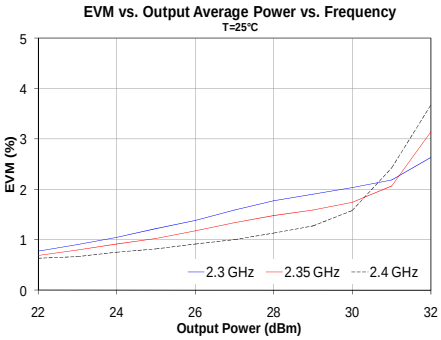
802.16-2004 O-FDMA, 64QAM-1/2, 1024-FFT, 20 symbols and 30 subchannels. 9.5 dB PAR @ 0.01%, 5 MHz Carrier BW







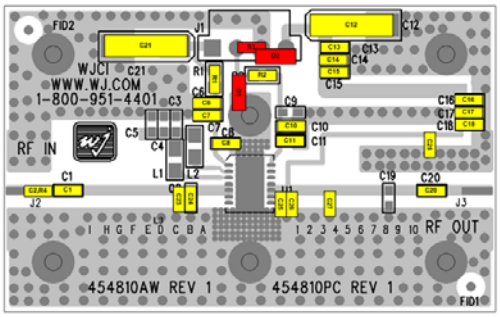


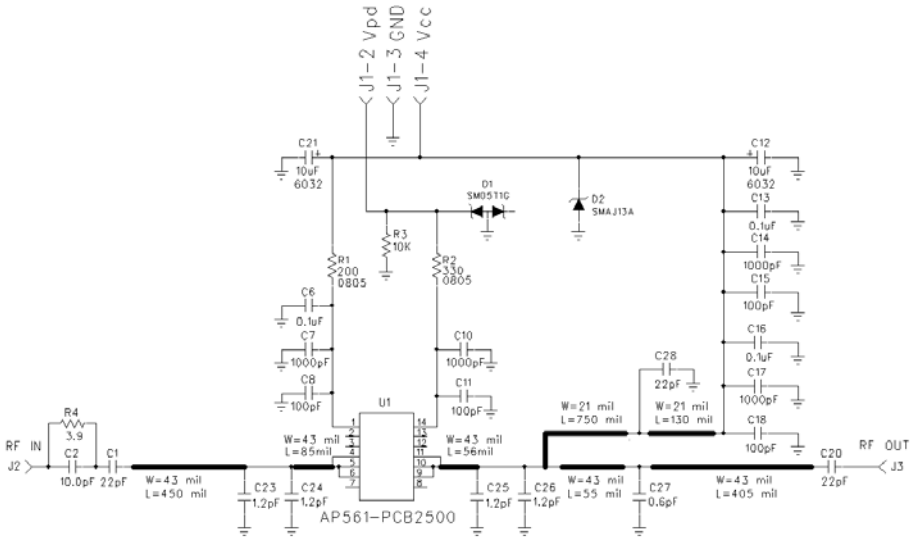


2.5-2.7 GHz Application Circuit (AP561-PCB2500)

Typical O-FDMA Performance at 25°C

Frequency (GHz)	2.5	2.6	2.7	Units
Channel Power	+30	+30	+30	dBm
Power Gain	13.4	13.1	12.2	dB
Input Return Loss	12	13	16	dB
Output Return Loss	6.4	6.2	4.3	dB
EVM	2.2	1.5	2.1	%
Operating Current, Icc	510	480	490	mA
Collector Efficiency	15.8	17.6	16	%
Output P1dB	39.7	39.0	37.6	dBm
Quiescent Current Icq	300			mA
Reference Current Iref	10			mA
Vpd	+5			V
Vcc	+12			V

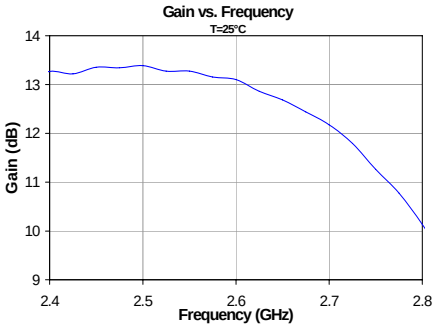


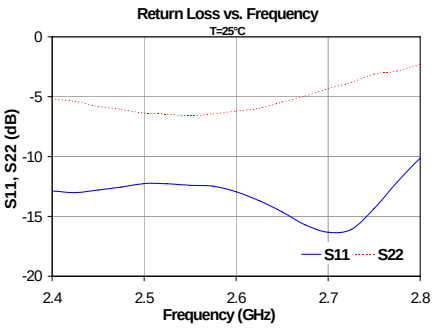


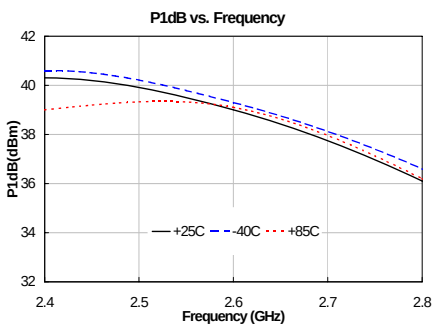
Notes:
1. The primary RF microstrip line is 50 Ω.
2. Do not exceed 5.5V on Vpd or damage to D1 will occur.
3. Do not exceed 13V on Vcc or damage to D2 will occur.
4. Components shown on the silkscreen but not on the schematic are not used.
5. The edge of C23 is placed right next to C24.
6. The edge of C24 is placed at 85mil from AP561 RFout pin. (9.6° @ 2.6 GHz)
7. The edge of C25 is placed at 56mil from AP561 RFin pin. (6.3° @ 2.6 GHz)
8. The edge of C26 is placed right next to C25.
9. The edge of C27 is placed 55mil from the edge of C26. (6.2° @ 2.6 GHz)
10. 0 Ω jumpers can be replaced with copper trace in target application.

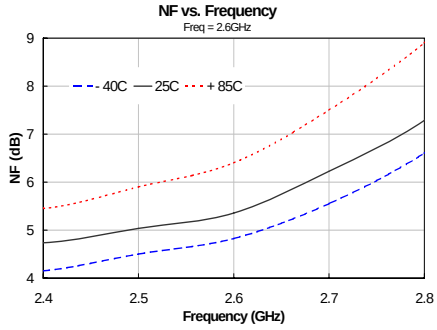
2.5-2.7 GHz Application Circuit Performance Plots

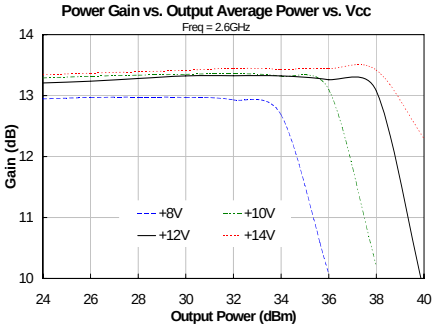
802.16-2004 O-FDMA, 64QAM-1/2, 1024-FFT, 20 symbols and 30 subchannels. 9.5 dB PAR @ 0.01%, 5 MHz Carrier BW

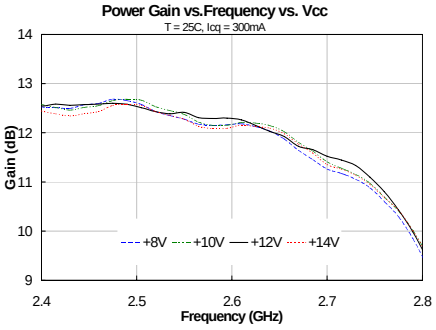




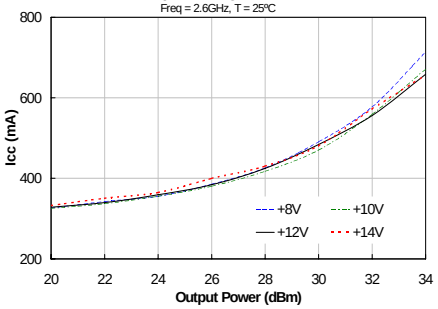




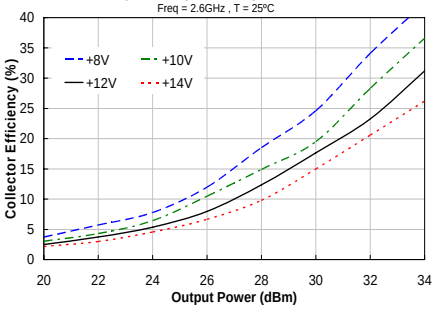




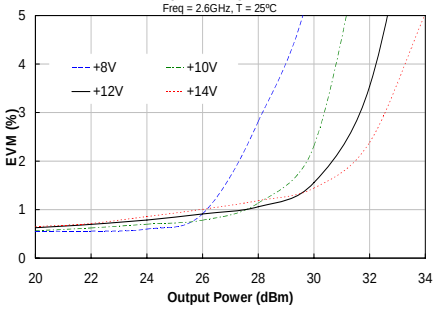
Icc vs. Output Average Power vs. Vcc



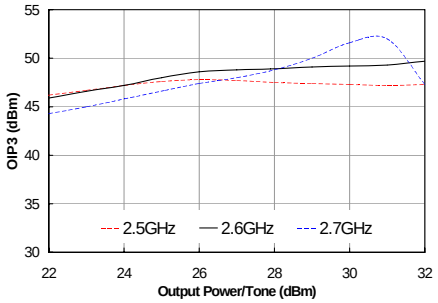
Efficiency vs. Output Average Power vs. Vcc



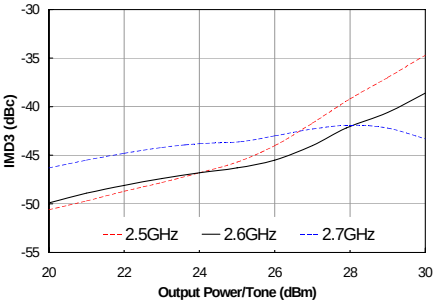
EVM vs. Output Average Power vs. Vcc



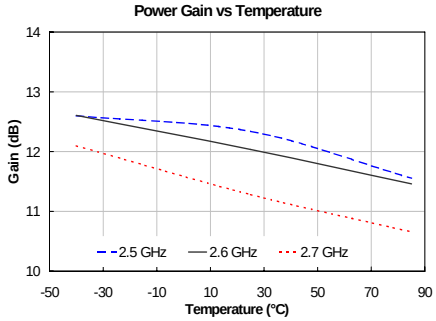
OIP3 vs. Output Power / Tone



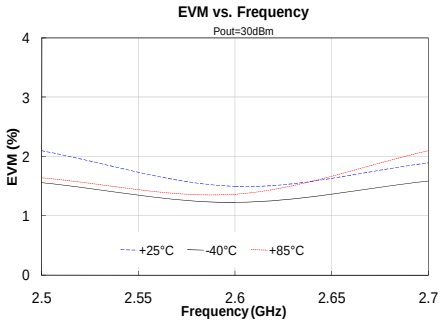
IMD3 vs. Output Power / Tone



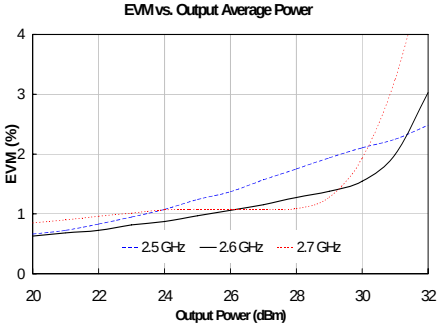
Power Gain vs Temperature



EVM vs. Frequency



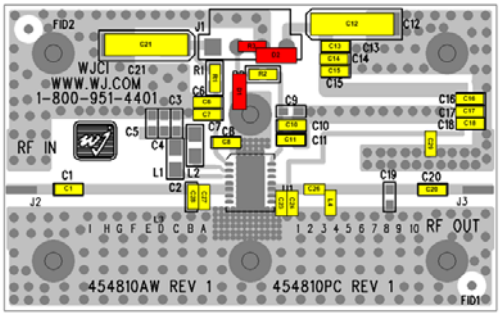
EVM vs. Output Average Power

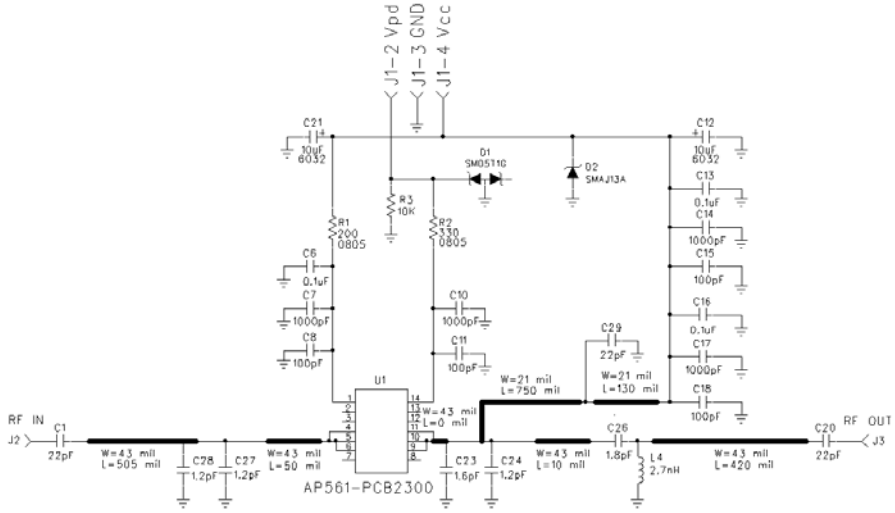


2.3-2.9 GHz Application Circuit

Typical O-FDMA Performance at 25°C

Frequency (GHz)	2.3	2.6	2.9	Units
Channel Power	+30	+30	+30	dBm
Power Gain	11.8	11.5	12.1	dB
Input Return Loss	17	14	16	dB
Output Return Loss	3.3	4.0	5.9	dB
EVM	1.9	2.5	2.4	%
Operating Current, Icc	630	640	570	mA
Collector Efficiency	13	12.7	14.3	%
Output P1dB	40	39	39	dBm
Quiescent Current Icq	300			mA
Reference Current Iref	10			mA
Vpd	+5			V
Vcc	+12			V

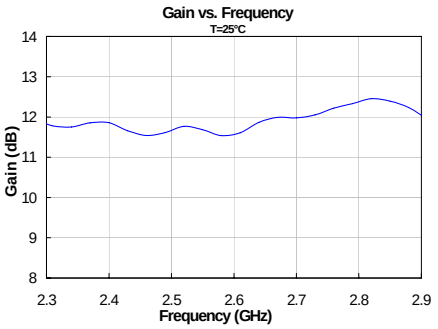


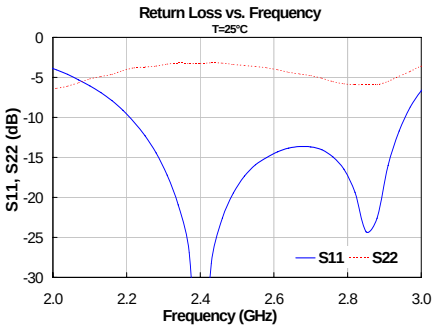


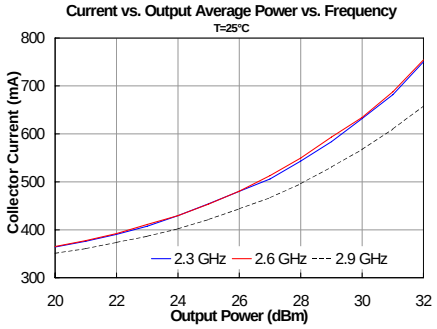
Notes:
1. The primary RF microstrip line is 50 Ω.
2. Do not exceed 5.5V on Vpd or damage to D1 will occur.
3. Do not exceed 13V on Vcc or damage to D2 will occur.
4. Components shown on the silkscreen but not on the schematic are not used.
5. The edge of C26 is placed 10mil from C24. (1.1 ° @ 2.6 GHz)
6. The edge of L4 is placed right next to C26.
7. The edge of C23 is placed next to AP561 RFout pin.
8. The edge of C24 is placed right next to C23.
9. The edge of C27 is placed at 50mil from AP561 RFin pin. (5.6 ° @ 2.6 GHz)
10. The edge of C28 is placed right next to C27.
11. 0 Ω jumpers can be replaced with copper trace in target application.

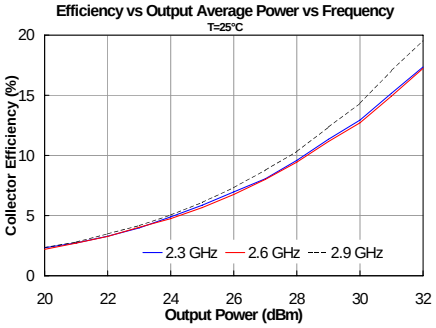
2.3-2.9 GHz Application Circuit Performance Plots

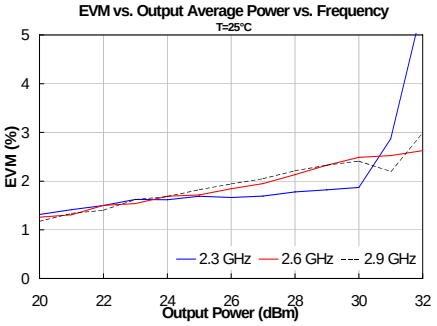
802.16-2004 O-FDMA, 64QAM-1/2, 1024-FFT, 20 symbols and 30 subchannels. 9.5 dB PAR @ 0.01%, 5 MHz Carrier BW









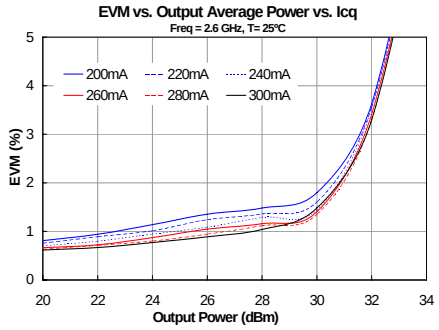


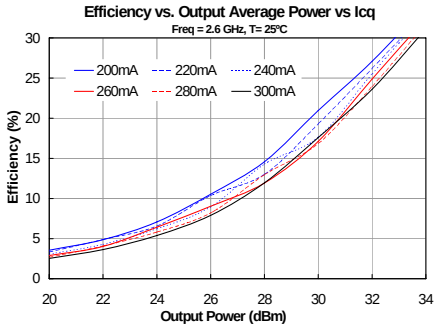
2.5 – 2.7 GHz Application Note: Changing Icq Biasing Configurations

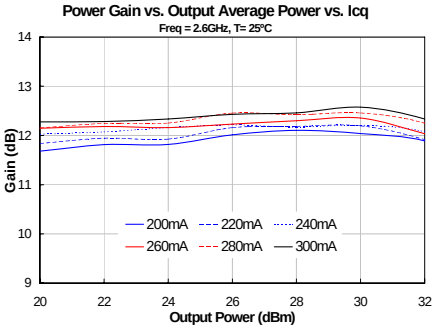
The AP561 can be configured to operate with lower bias current by varying the bias-adjust resistor R2. (Table 1) The recommended circuit configurations shown previously in this datasheet have the device operating with a 300 mA as the quiescent current (I_{CQ}). This biasing level represents a tradeoff in terms of EVM and efficiency. Lowering I_{CQ} will improve upon the efficiency of the device, but degrade the EVM performance. Measured data shown in the plots below represents the AP561-PCB2500 measured and configured for 2.6GHz applications. It is expected that variation of the bias current for other frequency applications will produce similar performance results.

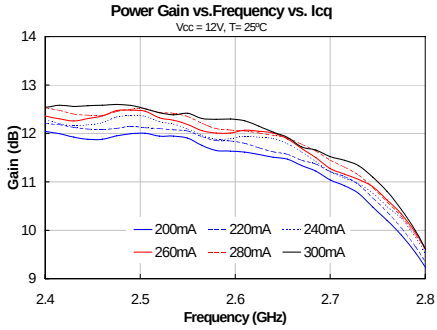
Table 1 : Reduced Current Operation

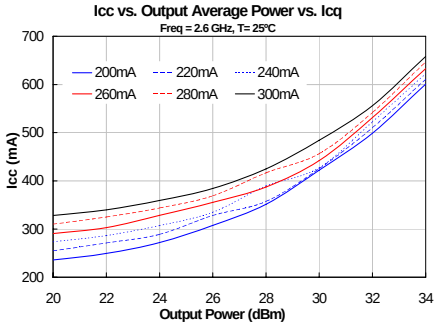
Icq (mA)	R2 (Ω)	V_{PD} (V)	I_{REF} (V)
300	**330**	**5**	**2.85**
280	336	5	2.81
260	240	5	2.78
240	343	5	2.76
220	348	5	2.73
200	351	5	2.71

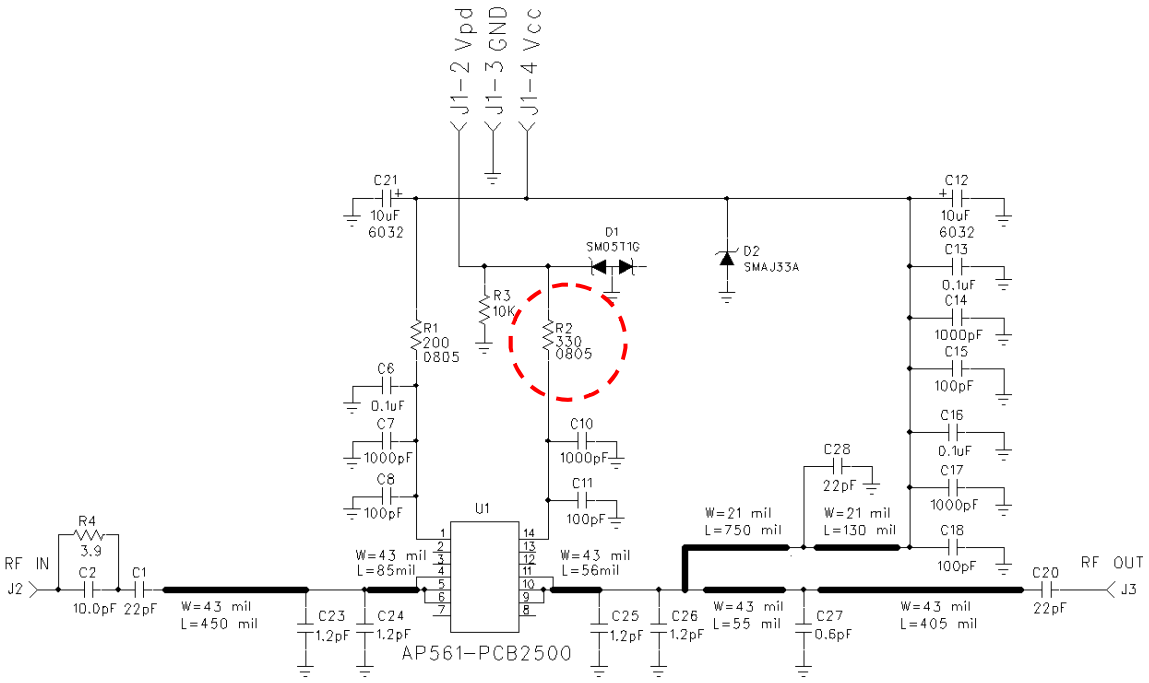










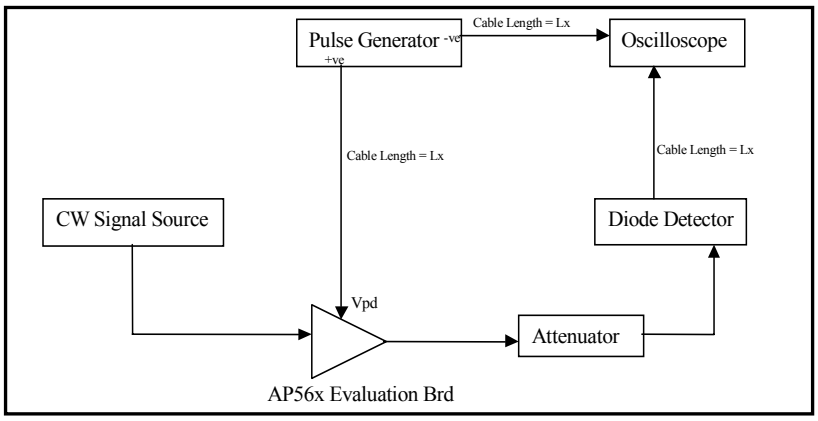


Parameter Measurement Information

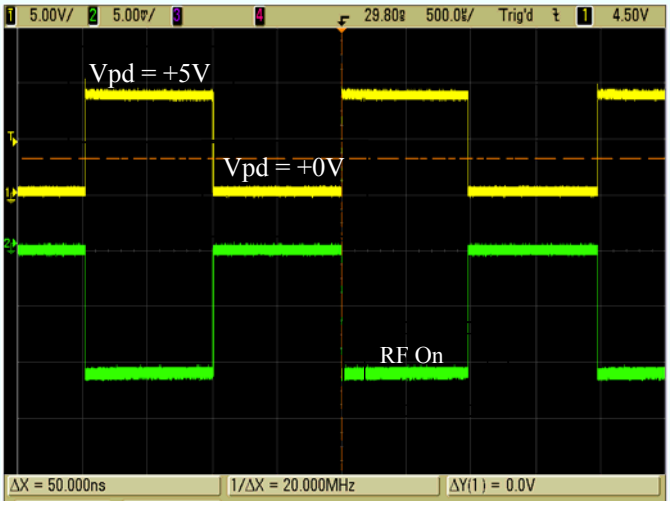
Switching Speed Test

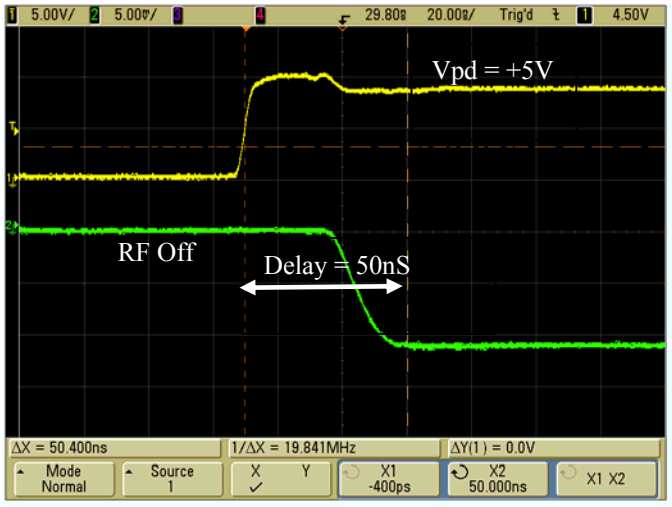
Test Conditions:

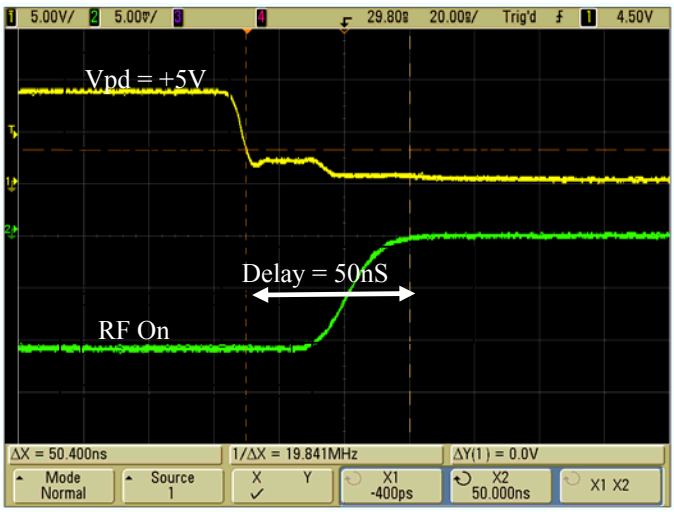
Vcc = +12V at 25°C
Output Power = +30dBm @ 2.5 GHz
Rep Rate = 1 KHz, 50% duty cycle
Vpd amplitude = +5V
R2=200 ohms, C9=12pF
(C10, C11 removed for best switching performance)
Xtal Detector Voltage =15mV (square law)



Test Result Waveforms:



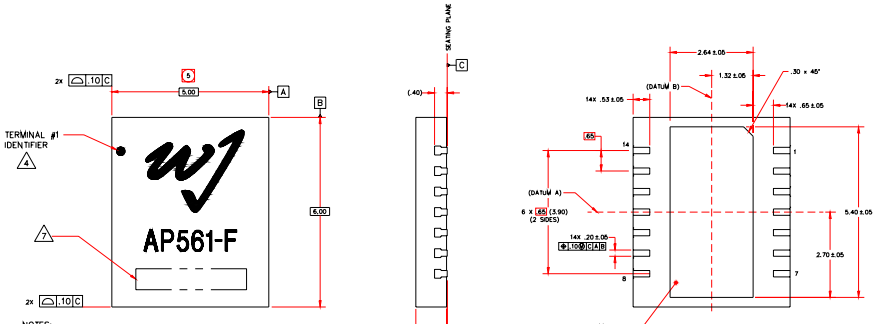




Mechanical Information

This package is lead-free/Green/RoHS-compliant. The plating material on the pins is annealed matte tin over copper. It is compatible with both lead-free (maximum 260 °C reflow temperature) and leaded (maximum 245 °C reflow temperature) soldering processes.

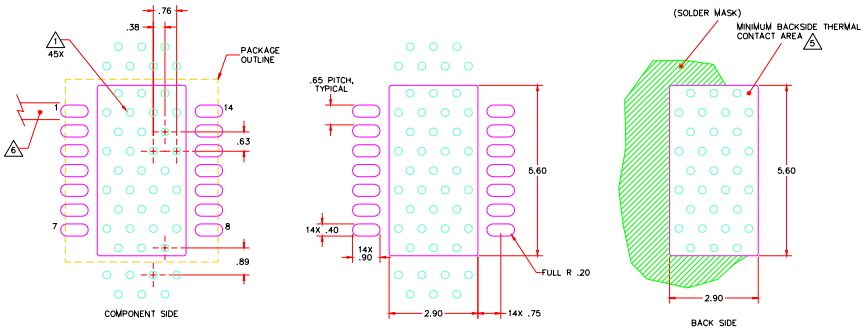
Outline Drawing



NOTES:

1. EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MO-229, ISSUE C (VARIATION VJGC) FOR THERMALLY ENHANCED PLASTIC VERY THIN FINE PITCH QUAD FLAT NO LEAD PACKAGE (QFN).
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.4M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION CONFORM TO JESD 95-1 SPP-012.
5. COPLANARITY APPLIES TO THE EXPOSED GROUND/THERMAL PAD AS WELL AS THE TERMINALS.
6. ALPHA-NUMERIC LOT CODE.

Mounting Configuration / Land Pattern



NOTES:

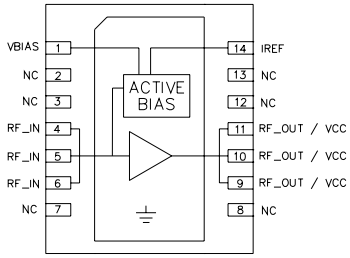
1. GROUND/THERMAL VIAS ARE CRITICAL FOR THE PROPER PERFORMANCEOF THIS DEVICE. VIAS SHOULD USE A .35mm (ø80/.0135") DIAMETER DRILL AND HAVE A FINAL, PLATED THRU DIAMETER OF .25mm (.010").
2. ADD AS MUCH COPPER AS POSSIBLE TO INNER AND OUTER LAYERS NEAR THE PART TO ENSURE OPTIMAL THERMAL PERFORMANCE.
3. TO ENSURE RELIABLE OPERATION, DEVICE GROUND PADDLE-TO-GROUND PAD SOLDER JOINT IS CRITICAL.
4. ADD MOUNTING SCREWS NEAR THE PART TO FASTEN THE BOARD TO A HEATSINK. ENSURE THAT THE GROUND/THERMAL VIA REGION CONTACTS THE HEATSINK.
5. DO NOT PUT SOLDER MASK ON THE BACK SIDE OF THE PC BOARD IN THE REGION WHERE THE BOARD CONTACTS THE HEATSINK.
6. RF TRACE WIDTH DEPENDS UPON THE PC BOARD MATERIAL AND CONSTRUCTION.
7. USE 1 OZ. COPPER MINIMUM.
8. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
9. A HEATSINK UNDERNEATH THE AREA OF THE PCB FOR THE MOUNTED DEVICE IS STRICTLY REQUIRED FOR PROPER THERMAL OPERATION. DAMAGE TO THE DEVICE CAN OCCUR WITHOUT THE USE OF ONE.

Product Marking

The component will be laser marked with a "AP561-F" product label with an alphanumeric lot code on the top surface of the package.

Tape and reel specifications for this part will be located on the website in the "Application Notes" section.

Functional Pin Layout



Pin	Function
1	VBIAS
2, 3, 7, 8, 12, 13	N/C
4, 5, 6	RF IN
9, 10, 11	RF Output / Vcc
14	IREF
Backside paddle	GND

MSL / ESD Rating

Caution! ESD sensitive device.

ESD Rating: Class 1A
Value: Passes ≥250V to <500V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class IV
Value: Passes ≥1000V to <2000V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating: Level 3 at +260 °C convection reflow
Standard: JEDEC Standard J-STD-020