SG901-1071 Miniature Wi-Fi Radio

Overview

The SG901-1071 WiFi module is optimized to simplify successful integration into systems requiring the latest performance with small size. This module is a highly integrated single chip based 802.11b/g/n WLAN radio for embedded, low-power and extremely small form factor mobile applications. The product conforms to the IEEE 802.11B, G, and N protocols operating in the 2.45GHz ISM frequency band supporting 802.11n modulations up to 72.2Mbps, all 802.11g OFDM modulations, and all mandatory 802.11b modulations.

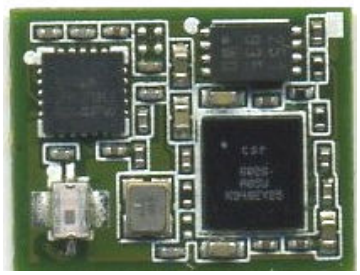
The SG901-1071 is a fully integrated wireless radio including RF Synthesizer/VCO, high-speed data converters, digital baseband processor, onboard MAC and PHY processors, Power Management, Power Amplifier, and LNA.

An on-board EEPROM stores calibration data for alignment-free integration. No customer calibration required.

Bluetooth integration features of the radio are made available.

An on-board crystal and filter simplify system integration. The addition of 1.8V, 3.3V, and VHIO supplies, Antenna, and host communication, provides a complete WiFi solution. For maximum flexibility, the SG901-1071 can be optionally supplied without internal oscillator and accept a wide range of external reference clock frequencies.

Host control is provided by either an SDIO or SPI interface.



Features

- Very Small Footprint (12.0 x 9.5 x1.7mm)
- Factory Calibrated
- RoHs Compliant
- Fully Integrated 802.11 System Solution
- Ultra Low Current Consumption, 2.5 m A DITM = 1
- Fully Compliant with the IEEE 802.11B,G, and N WLAN Standards
- Support for 802.11n Modulations up to 72.2Mbps, and all 802.11g and Mandatory 802.11b Modulations
- Intelligent Power Control, Including 802.11 Power Save Mode
- Supports SPI Interface and SDIO Interface
- Factory Support for Linux 2.6/Android, Windows CE
- Source Code Available for porting to RTOS or Custom OS
- Hardware driver is provided under GPL
- Flexible I/O Voltage
- Contact Factory for FCC compliant applications

Applications

• Hand-held Devices
• Embedded Systems
• Portable Systems
• Point of Sale terminals
• Personal Digital Assistants (PDA)
• Cameras
• Cable Replacement

Ordering Information

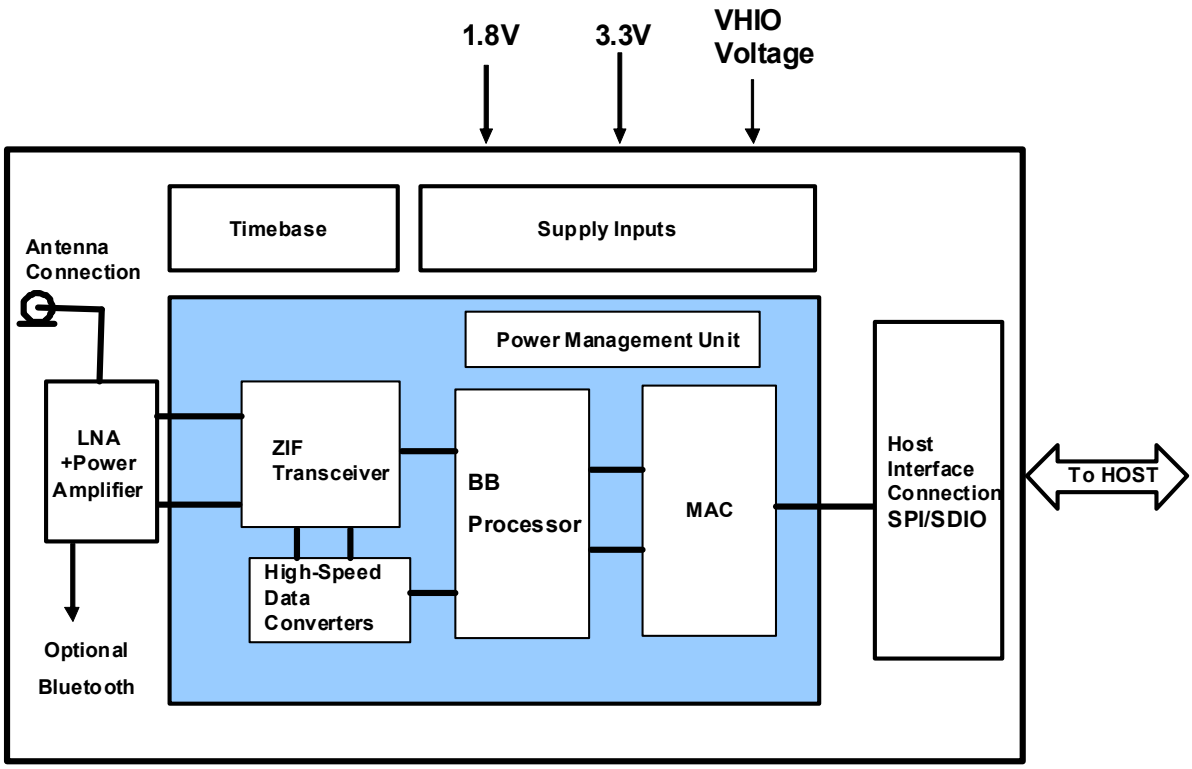
Packaging	Temp Range	Part Number
Tape and Reel	Extended	SG901-1071-ET-TR
Bulk	Extended	SG901-1071-ET-BLK
Tape and Reel	Commercial	SG901-1071-CT-TR
Bulk	Commercial	SG901-1071-CT-BLK

Evaluation Kit Available

This EVK supports embedded software development.

EVK for 1071	SG923-0007

Block Diagram



General Electrical Specifications

Parameter		Test Condition / Comment	Min.	Typ.	Max.	Units
Absolute Maximum Ratings						
3.3V , VHIO Supplies			-0.3		3.6	V
VLDO Supply, POWERUP pin			-0.3		2.5	V
Operating Conditions and Input Power Specifications						
Operating Temperature Range		ET Version (Extended Temperature)	-30		85	°C
		CT Version (Commercial Temperature)	0		70	°C
3.3V Supply	Input Supply Voltage	3.3V Supply input	2.7	3.3	3.6	V
	Standby Mode Current	32.768kHz Mode		270		uA
	Power Save Mode Current	DTIM = 1		2.5		mA
	Peak TX Current	POUT 18dBm, 54Mbps		190	250	mA
	Peak RX Current	Processing Beacons		10	15	mA
Power Save Mode Settling Times	Wake up Time	From 32.768KHz Mode		5		mS
	Ramp up	To Processing Beacons		360		uS
	Ramp Down	To Stand By 32.768KHz mode		760		uS
VHIO Supply	Input Supply Voltage	VHIO input supply determines Host CMOS logic levels	1.7		3.6	V
	Input Supply Current	VHIO = 1.8V		1		mA
	Standby Mode Current	VHIO = 1.8V		100		uA
VLDO Supply	Input Supply Voltage	Required Internal regulator supply input	1.45		2.0	V
	Continuous Receive	2.4GHz OFDM		135		mA
	Continuous Transmit	2.4GHz OFDM		160		mA
	POWERUP	LDOs enabled	1.0		2.0	V
Input Voltage Levels	VIL	all but POWERUP	-0.3		0.25VHIO	V
	VIH	all but POWERUP	0.625VHIO		VHIO+0.3	V
Output Voltage Levels	VOL	IOL = 8.0mA			0.4	V
	VOH	IOH = -8.0mA	0.75VHIO		VHIO	V
Host Interface	SDCLK	SDIO and SPI max clock rate			50	MHz
Input Capacitance			1.0		5.0	pF

RF Characteristics (Max and Min based on temperature range)

Parameter		Test Condition / Comment	Min.	Typ.	Max.	Units
Antenna Port Impedance				50		Ohms
Antenna Input Return Loss		CH1 to CH14	-9.5		-14	dB
RX Sensitivity	11b, 1Mbps		-97	-96.3	-95	dBm
	11b, 2 Mbps		-94	-93.5	-91	dBm
	11b, 5.5 Mbps		-93	-91	-88	dBm
	11b, 11 Mbps		-89	-86.7	-85	dBm
	11g, 9Mbps		-92	-89.6	-88	dBm
	11g, 18Mbps		-87	-85.9	-84	dBm
	11g, 36Mbps		-80	-78.6	-77	dBm
	11g, 54Mbps		-74	-72.4	-70	dBm
	11n, MCS1			-86		dBm
	11n, MCS3			-80		dBm
	11n, MCS5			-72		dBm
	11n, MCS7			-69		dBm
Channel to Channel De-sensitivity	CH1 to 14	11g, 54Mbps 10% PER	-0.7		0.7	dB
Maximum Input Signal	CH7	11g, 54Mbps	-19		-16	dBm
Adjacent Channel Rejection	1Mbps			50		
	11Mbps			47		
	9Mbps			25		dB
	54Mbps			13		dB
	MCS1			24		dB
	MCS7			5		dB
TX Output Power	11b, 1Mbps	@802.11b spectral mask	15	16.5	19.1	dBm
	11b, 11Mbps		15.5	16.2	19.4	dBm
	11g, 9Mbps	@802.11g spectral mask	17	18.2	19.5	dBm
	11g, 54Mbps	EVM = -27dB, 4.5%	11.7	13.4	15.1	dBm
	802.11n MCS1	@802.11n spectral mask		17		dBm
	802.11n MCS7	EVM = -27dB		13		dBm

Pinout List

SIGNAL NAME	PIN NUMBER	DESCRIPTION		NOTES
Reference Clock Pins				
OSC_EN	4	Oscillator Enable Output		not normally used – Contact Sagrad for options
REF_CLK	19	Reference Oscillator Input		normally not connected - Contact Sagrad for options
RF Pins				
BTH	13	Bluetooth RF Switched RF Connection		RF Connection for Input - Output
2G4_RF	16	Wi-Fi / Bluetooth Antenna Port, 50 ohms		Careful RF design is needed for this and nearby ground
Serial Interface Pins (VHIO Domain, logic levels compatible with the VHIO (Pin 32) input voltage)				
SDCMD	25	SPI MOSI (input)	SDIO CMD	VHIO Domain
SDCLK	26	SPI Clock Input	SDIO CLK	VHIO Domain
SDD0	24	SPI MISO (output)	SDIO Data 0	VHIO Domain
SDD1	23	SPI: Interrupt Output	SDIO Data 1	VHIO Domain
SDD2	22		SDIO Data 2	VHIO Domain
SDD3	21	SPI Chip Select Input	SDIO Data 3	VHIO Domain
Control Pins				
POWERUP	5	Power Up Enable (from Host)		VLDO Domain with internal pull up High = operating, Low = off
RSTn	31	Reset Input		VHIO Domain – Active Low reset
SLEEPCLK	33	32.768 kHz Sleep Clock Input		VHIO Domain
DBG_SPI_CSn	27	Debug SPI Chip Select Input		VHIO Domain
DBG_SPI_CLK	30	Debug SPI Clock Input		VHIO Domain
DBG_SPI_MISO	28	Debug SPI Data Output		VHIO Domain
DBG_SPI_MOSI	29	Debug SPI Data Input		VHIO Domain
Bluetooth Coexistence Pins (VHIO Domain)				
WLAN_DENY	1	Bluetooth Coexistence		VHIO Domain
BT_ACTIVE	3	Bluetooth Coexistence		VHIO Domain
BT_PERIODIC	2	Bluetooth Coexistence		VHIO Domain
BT_STATUS	34	Bluetooth Coexistence		VHIO Domain
Power and Ground Pins				
VHIO	32	Supply Voltage for I/O's		1.7 to 3.6V, Internally decoupled with a 0.1uF capacitor
VLDO	6	External regulator supply input		1.45 to 2.0V, Internally decoupled with a 2.4uF capacitor
3.3V	8	RF supply		2.7 to 3.6V, Internally decoupled with a 0.2uF capacitor
GND	7, 9, 10, 11, 12, 14, 15, 17, 18, 20, 35	Ground Connections		

Software Support

The 1071 and 1078 modules are supported through highly portable software. The hardware drivers and Wi-Fi stack as provided is compatible with Linux kernel 2.6. The source code for the hardware abstraction is available under a GPL license and is available from Sagrad. The licensed Wi-Fi licensed stack available from Sagrad is provided in binary form without a license. Source code for the Wi-Fi stack is available to the customer. To obtain source code for the stack contact Sagrad sales at www.sagrad.com. Software and source code are available free of charge but require a software license agreement for the Wi-Fi stack source.

In almost all cases the GPL driver will need to be modified for the customer's specific hardware. The Wi-Fi stack will only need to be modified for compatibility to the customers OS and compiler. In many cases such as Linux near zero modification of the Wi-Fi stack will be required.

The Wi-Fi module/stack currently is only tested in client mode and is compatible with any access point that meets 802.11 standards. An access point mode code base is planned in the future.

The complete 802.11 stack requires about 350KB of space for the implementation of the entire specification. Extremely small versions can be created by knowledgeable customers but is a considerable task and requires detailed understanding of 802.11.

As a service to customers, Sagrad offers extended technical support on a fee basis.

Software Details:

MAC

■ Comprehensive MAC functionality according to IEEE 802.11-2007, including QoS traffic scheduling

■ Supports the following optional IEEE 802.11n features:
- MPDU aggregation
- MSDU aggregation
- Immediate Block Acknowledgement
- PSMP
- MTBA
- RIFS
- L-SIG TXOP protection

Link adaptation using MCS feedback

Encryption

■ Hardware encryption according to IEEE 802.11-2007 and IEEE 802.11w/D10.0:
- WEP40/64
- WEP104/128
- CCMP (AES)
- TKIP
- BIP

■ Hardware encryption support for SMS4 to supportWAPI
■ Hardware encryption support for Cisco® CKIP

OS Support:

Windows Mobile 7 and 6.x, Windows CE 6.1 and 5, Linux v2.6, Android

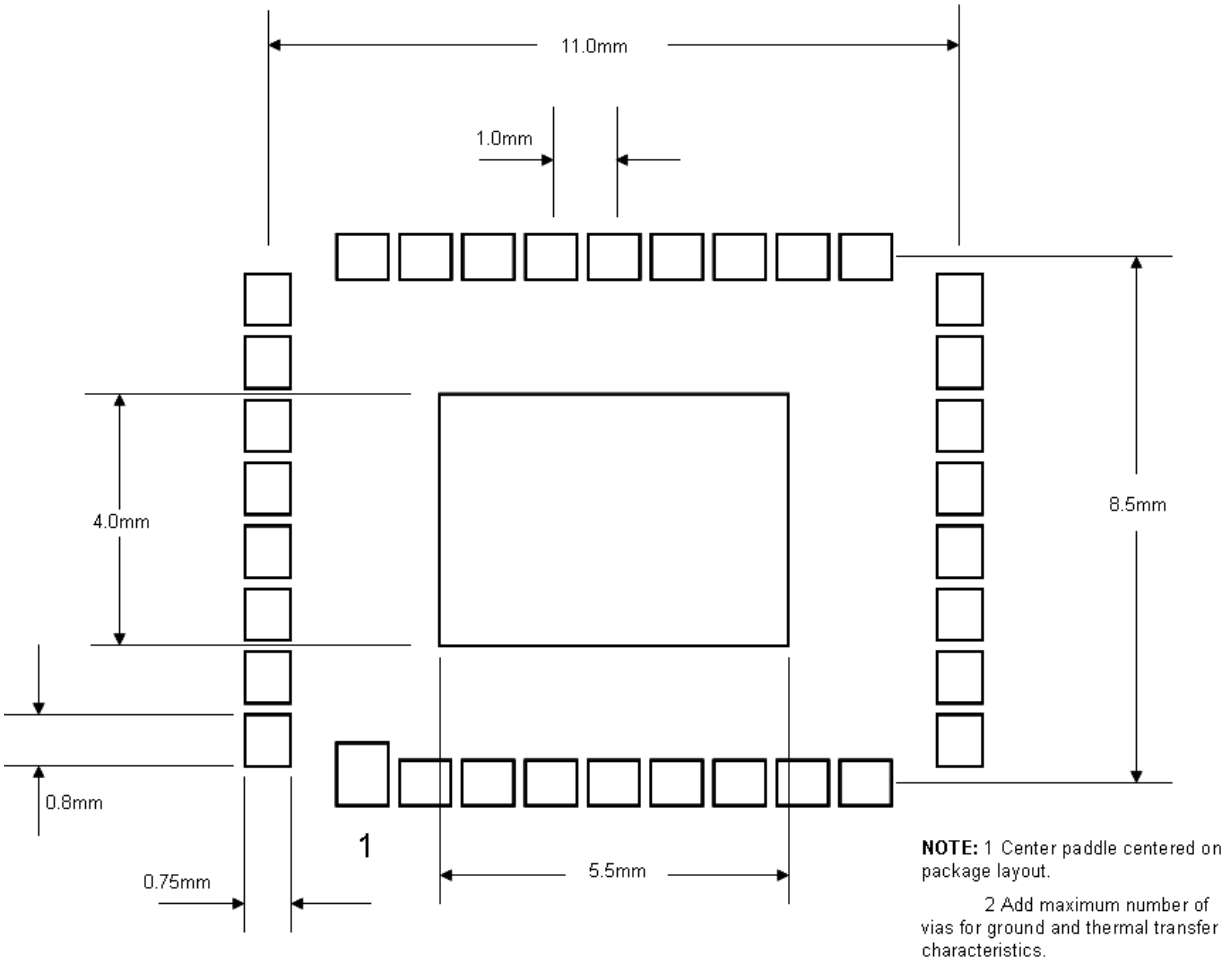
Module has been tested with the following SDIO/PCI bridges:

Arasan Reference SD Host Controller" - (PCI\VEN_1095&DEV_0670)
Ricoh R5C822 SD Host Controller" - (PCI\VEN_1180&DEV_0822)
JMicron JMB38x family SD Host Controller" - (PCI\VEN_197B&DEV_2381)
JMicron JMB387 SD Host Controller" - (PCI\VEN_197B&DEV_2386)

Bluetooth Coexistence

Feature	Linux
Bluetooth Coexistence	
PTA (802.15.2)	Yes
802.11/BT on same Antenna	Yes
Data and Voice Simultaneously	Yes
Data and Data Simultaneously	Yes
Voice and Voice Simultaneously	Yes

Recommended Layout

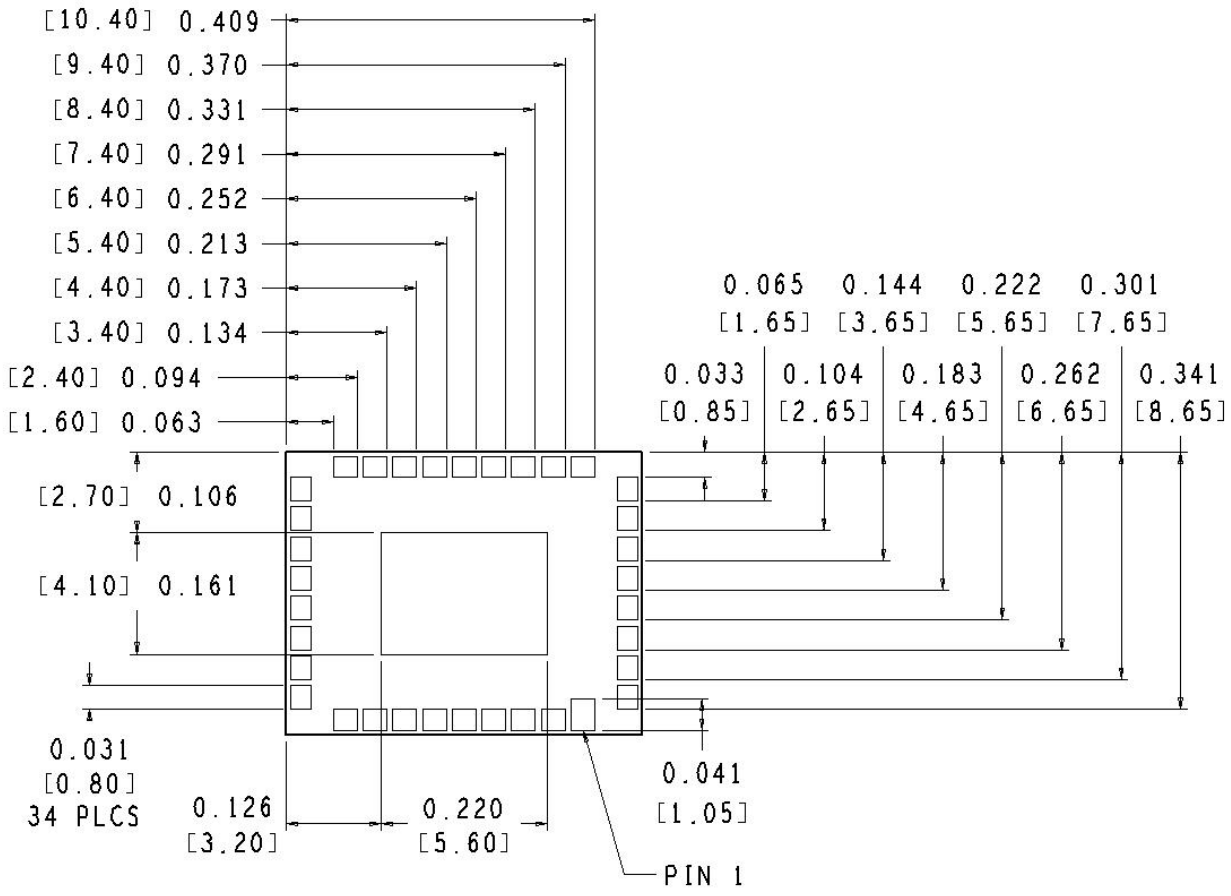


PCB design requires detailed review of the center exposed pad. This pad requires good thermal conductivity. Soldering coverage should be maximized and checked via x-ray for proper design. There is a trade off in providing enough solder for conductivity, and too much which allows the module to "float" on the paddle creating reliability issues. Sagrad recommends two approaches, a large center via that allows excess soldering to flow down into the host PCB with smaller vias around it. Or many smaller vias with just enough space for the viscosity of the chosen solder/flux to allow some solder to flow into the smaller vias. Each of these approaches need to result in 60% or more full contact solder coverage on the paddle after reflow. Sagrad strongly encourages PCB layout teams to work with their EMS providers to insure vias and solder paste designs will result in satisfactory performance.

Note Pin one is on the bottom left of this diagram and is enlarged.

This view is viewed from the top.

Mechanical



The nominal size of the part is 12x9.5mm with a height of 1.7mm

Packaging

The part comes packaged in Tape and Reel or Bulk.