

AH3

High Dynamic Range Gain Block

Applications

- 3G / 4G Mobile Infrastructure
- CDMA, WCDMA, LTE
- IF Applications

Product Features

- 50 – 870 MHz
- +41 dBm OIP3
- 3 dB Noise Figure
- 13 dB Gain
- +20 dBm P1dB
- Internally matched
- Single +5 V Supply
- MTTF > 100 Years
- Lead-free/Green/RoHS-compliant SOT-89 Package

General Description

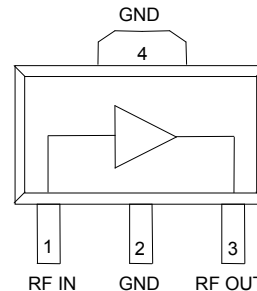
The AH3 is a high dynamic range amplifier in a low-cost surface-mount package. The combination of low noise figure and high output IP3 at the same bias point makes it ideal for receiver and transmitter applications. The device combines dependable performance with superb quality to maintain MTTF values exceeding 100 years at mounting temperatures of +85 °C. The AH3 is available in the environmentally-friendly lead-free/green/RoHS-compliant SOT-89 package.

The broadband amplifier uses a high reliability GaAs MESFET technology and is targeted for applications where high linearity is required. In addition, the AH3 is internally matched for 50 ohms.



SOT-89 Package

Functional Block Diagram



Pin Configuration

Pin #	Symbol
1	RF Input
2	GND
3	RF Output
4	GND Paddle

Ordering Information

Part No.	Description
AH3-G	High Dynamic Range Amplifier
AH3WB-PCB	50 – 870 MHz Evaluation Board

Standard T/R size = 1000 pieces on a 7" reel.

Specifications

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-55 to +125 °C
RF Input Power, CW, 50Ω, T = 25°C	+10 dBm
Supply Voltage, V _{dd}	+6 V
Thermal Resistance (jnc. to case) θ _{jc}	59 °C/W

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V _{dd}	+3	+5	+5.25	V
T _J (for >10 ⁶ hours MTTF)			160	°C
Operating Temp. Range	-40		+85	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{dd} = +5 V, T_{LEAD} = 25 °C, 800 MHz.

Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range		50		870	MHz
Test Frequency			800		MHz
Gain		12	12.9	14	dB
Input Return Loss			10		dB
Output Return Loss			20		dB
Output P1dB			+20		dBm
Output IP3	See Note 1.	+37	+41		dBm
Noise Figure			2.9		dB
Supply Voltage, V _{dd}			+5		V
Supply Current, I _{dd}		120	150	180	mA

Notes:

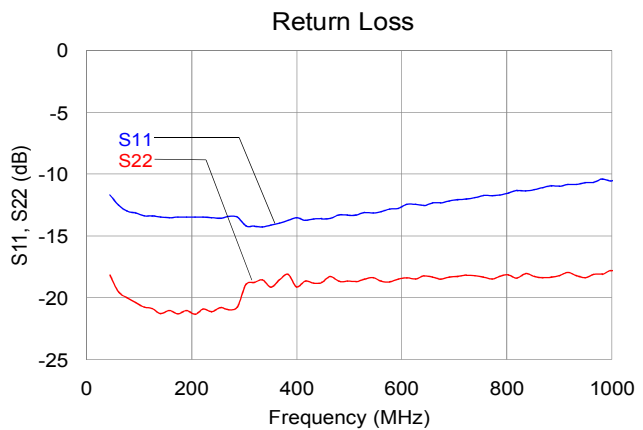
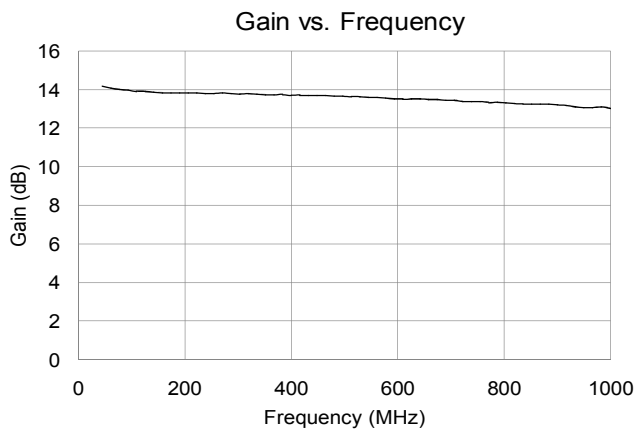
- 3OIP measured with two tones at an output power of +5 dBm/tone separated by 10 MHz. The suppression on the largest IM3 product is used to calculate the 3OIP using a 2:1 rule.

Device Characterization Data

S-Parameter Data

Test conditions unless otherwise noted: $V_{dd} = +5\text{ V}$, $T_{LEAD} = 25\text{ }^{\circ}\text{C}$, calibrated to device leads

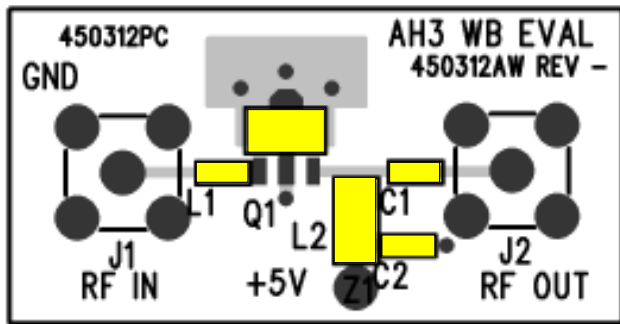
Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (angle)	S22 (dB)	S22 (ang)
50	-11.93	-33.34	14.15	169.58	-19.95	7.77	-18.60	-126.62
100	-13.21	-28.09	13.95	170.57	-19.98	2.69	-20.54	-149.57
150	-13.51	-28.85	13.85	169.10	-19.86	0.25	-21.16	-160.72
200	-13.48	-32.18	13.83	167.34	-19.85	-1.46	-21.23	-167.36
250	-13.55	-36.10	13.81	164.90	-19.87	-3.41	-20.91	-170.48
300	-14.05	-44.73	13.78	162.57	-19.86	-4.62	-19.26	-177.22
350	-14.12	-48.60	13.75	160.01	-19.91	-5.48	-19.07	-175.89
400	-13.53	-55.70	13.70	157.51	-19.92	-7.31	-19.12	-178.33
450	-13.60	-61.16	13.69	155.04	-19.95	-7.85	-18.71	-179.04
500	-13.32	-65.93	13.65	152.52	-19.90	-10.12	-18.67	178.55
550	-13.11	-70.97	13.60	150.15	-19.85	-10.20	-18.46	178.78
600	-12.65	-75.78	13.52	147.48	-19.91	-11.07	-18.43	177.91
650	-12.43	-80.45	13.51	145.06	-19.89	-12.83	-18.29	177.33
700	-12.10	-84.62	13.46	142.56	-19.87	-12.67	-18.31	175.94
750	-11.79	-88.75	13.39	140.08	-19.82	-14.15	-18.29	176.28
800	-11.54	-93.43	13.33	137.61	-19.92	-14.94	-18.18	174.92
850	-11.28	-96.17	13.26	135.38	-19.84	-15.94	-18.26	173.97
900	-10.97	-100.66	13.21	132.61	-20.09	-16.96	-18.20	174.37
950	-10.69	-104.85	13.08	129.83	-20.09	-19.21	-18.35	175.02
1000	-10.53	-107.99	13.04	127.70	-19.92	-19.33	-17.83	174.09



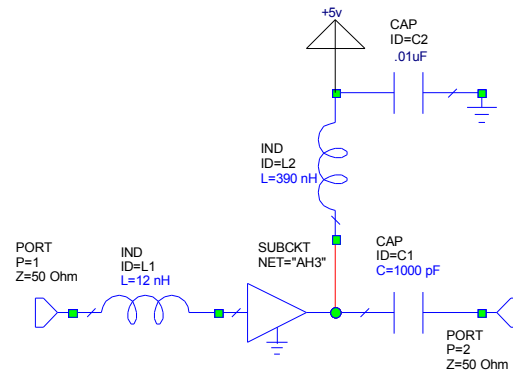
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High Dynamic Range Gain Block

Reference Design 50 - 870 MHz (AH3WB-PCB)



See PC Board Layout, page 6 for more information



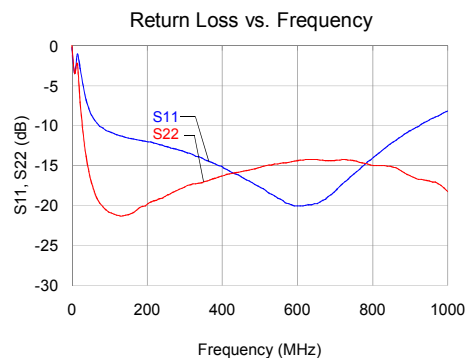
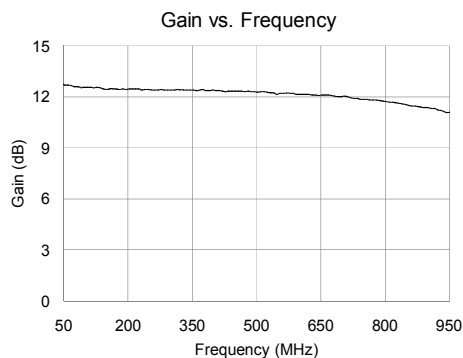
Bill of Material

Ref Des	Value	Description	Manufacturer	Part Number
Q1		High Dynamic Range Block	TriQuint	AH3
C1	1000 pF	Cap, Chip, 0603, 5%, 50V, X7R	various	
C2	.01 uF	Cap, Chip, 0603, 5%, 50V, X7R	various	
L1	12 nH	Ind, Chip, 0603, 5%	various	
L2	390 nH	Coil Wire-wound, 1008, 5%	Coilcraft	1008CS-391XJLC

Typical Performance 50-800 MHz (AH3WB-PCB)

Test conditions unless otherwise noted: $V_{dd} = +5V$, $T_{LEAD} = 25^\circ C$

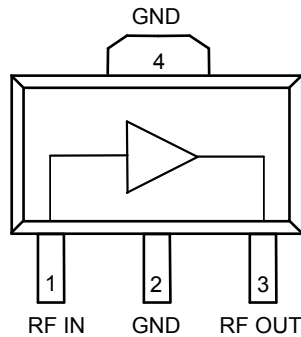
Frequency	MHz	50	450	800
Gain	dB	13.2	13	12.5
Input Return Loss	dB	8.4	16	15
Output Return Loss	dB	18.7	16	15
Output P1dB	dBm	+20	+20	+20
OIP3 @ +5 dBm/tone $\Delta f = 10$ MHz	dBm	+36	+40	+41
Noise Figure	dB	6	3.5	3.4
I_{dd}	mA		150	
V_{dd}	V		+5	



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Pin Description



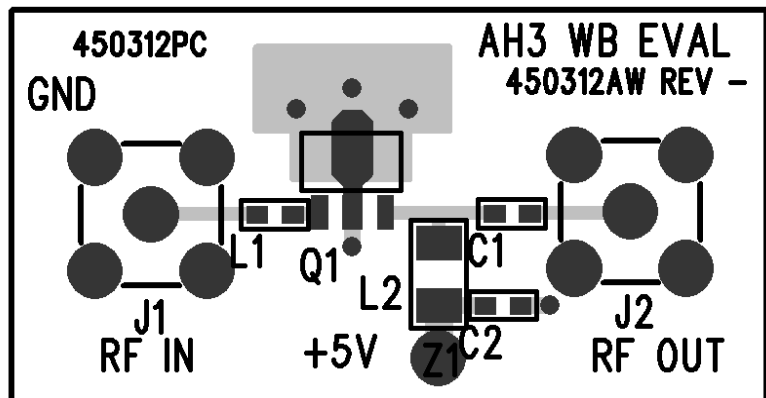
Pin	Symbol	Description
1	RF IN	RF Input. Internally DC grounded. No DC blocking capacitor required.
2, 4	GND	RF/DC Ground. Ensure good solder attach for optimal RF and thermal performance.
3	RF OUT	RF Output. DC supply input.

Applications Information

PC Board Layout

Circuit Board Material: .062" total thickness with a .014" FR-4 top RF layer, 4 layers (other layers added for rigidity), 1 oz copper, 50Ω Microstrip line details: width = .025".

The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.



For further technical information, Refer to http://www.triquint.com/prodserv/more_info/default.aspx?prod_id=AH3

AH3

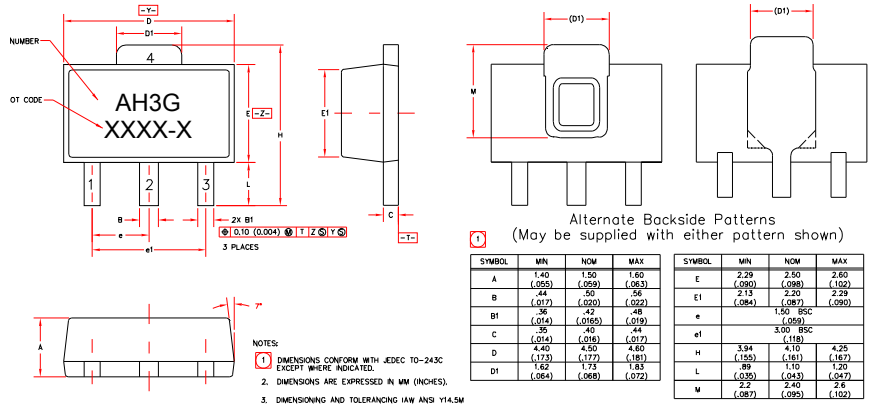
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Mechanical Information

Package Information and Dimensions

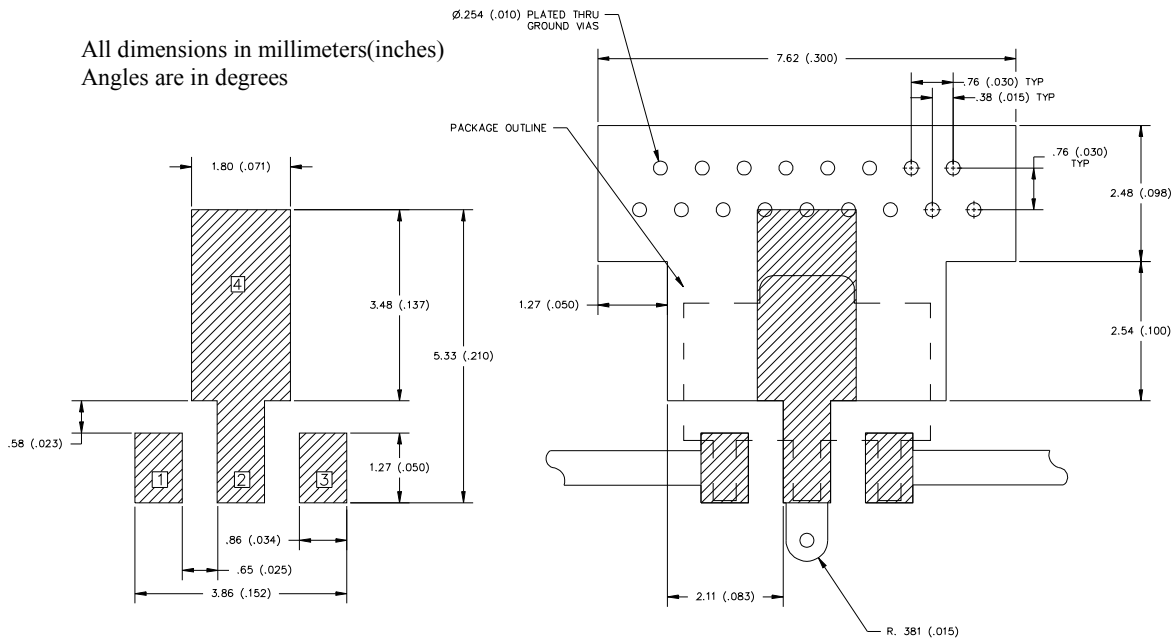
Lead-free/Green/RoHS-compliant.
 Package pin plating - NiPdAu.
 Compatible with lead-free (Tmax=260°C)
 and lead (Tmax=245 °C) soldering
 processes.

The AH3-G will be marked with an
 "AH3G" designator. An alphanumeric lot
 code ("XXXX-X") is also marked below
 the part designator on the top surface of
 the package



Mounting Configuration

All dimensions in millimeters(inches)
 Angles are in degrees



Notes:

1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink.
4. Do not put solder mask on the backside of the PC board in the region where the board contacts the heatsink.
5. RF trace width depends upon the PC board material and construction.
6. Use 1 oz. Copper minimum.

Product Compliance Information

ESD Information



Caution! ESD-Sensitive Device

ESD Rating: Class1B
Value: Passes ≥ 500 to < 1000 V.
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class IV
Value: Passes ≥ 1000 to < 2000 V.
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating

The part is rated Moisture Sensitivity Level 3 at 260°C per JEDEC standard J-STD-020.

Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260°

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free

Contact Information

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