AH118

¼ Watt, High Linearity InGaP HBT Amplifier

Applications

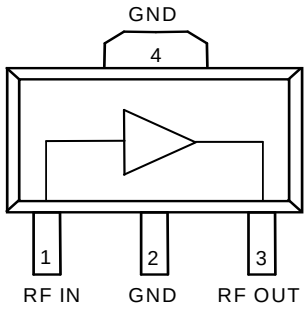
- Final stage amplifiers for Repeaters
- Mobile Infrastructure

SOT-89 Package

Product Features

- 60 – 3500 MHz
- +24.7 dBm PIdB
- +40.5 dBm Output IP3
- 20.4 dB Gain @ 900 MHz
- 16.5 dB Gain @ 1900 MHz
- +5V Single Positive Supply
- Lead-free/Green/RoHS-compliant SOT-89 Package

Functional Block Diagram



General Description

The AH118 is a high dynamic range driver amplifier in a low-cost surface mount package. The InGaP/GaAs HBT is able to achieve high performance across a broad range with +40.5 dBm OIP3 and +24.7 dBm of compressed 1dB power. The AH118 is available in a lead-free/green/RoHS-compliant SOT-89 package. All devices are 100% RF and DC tested.

The AH118 is targeted for use as a driver amplifier in wireless infrastructure where high linearity and medium power is required. Internal biasing allows the AH118 to maintain high linearity over temperature and operate directly off a single +5V supply. This combination makes the device an excellent candidate for transceiver line cards in current and next generation multi-carrier 3G base stations.

Pin Configuration

Pin #	Function
1	Input / Base
2	Ground
3	Output / Collector
4	Ground

Ordering Information

Part No.	Description
AH118-89G	High IP3 InGaP HBT Amp
AH118-89PCB900	900 MHz Evaluation Board
AH118-89PCB2140	2140 MHz Evaluation Board

Standard T/R size = 1000 pieces on a 7” reel.

Specifications

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to +150 °C
RF Input Power, T = 25ºC	+15 dBm
Device Voltage	+6 V
Device Current	220 mA

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{cc}	+4.75	+5	+5.25	V
I_{cc}		160		mA
T_J (for >10^6 hours MTTF)			200	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

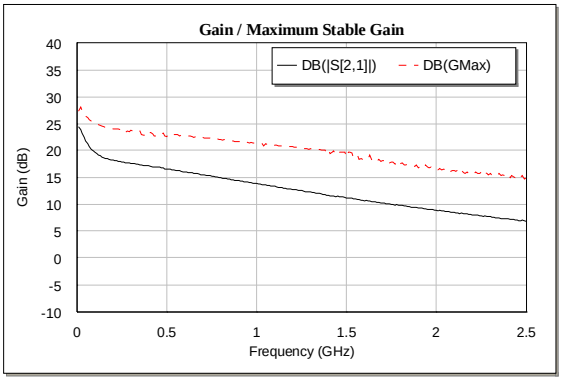
Electrical Specifications

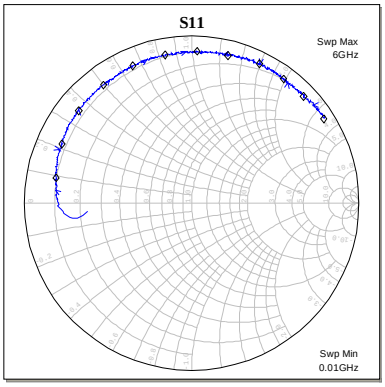
Test conditions unless otherwise noted: +25ºC on a tuned test fixture

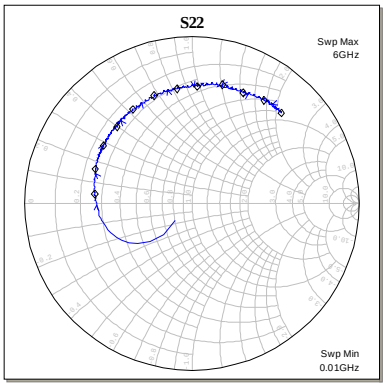
Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range		60		3500	MHz
Test Frequency			1900		MHz
Gain		13.5	16.0		dB
Input Return Loss			12		dB
Output Return Loss			20		dB
Output P1dB		+23	+24.7		dBm
Output IP3	See Note 1	+39.5	+40.5		dBm
WCDMA Channel Power @ -45 dBc ACLR, 2140 MHz	See Note 2		+16.7		dBm
Noise Figure			4.3		dB
Vcc			+5		V
Operational Current Range		140	160	175	mA
Thermal Resistance (junction to case)				92	°C/W

Notes:
1. OIP3 is measured with two tones separated by 1 MHz at 11dBm output power/tone. The suppression on the largest IM3 product is used to calculate the OIP3 using a 2:1 rule.
2. Signal: W-CDMA 3GPP Test Model 1+64 DPCH, PAR = 10 dB @ 0.01% Probability, 3.84 MHz BW

Device Characterization Data







Note:

1. S-Parameters (V_{Device} = +5 V, I_{CC} = 160 mA, 25 °C, unmatched 50 ohm system).
2. The gain for the unmatched device in 50 ohm system is shown as the trace in black color. For a tuned circuit for a particular frequency, it is expected that actual gain will be higher, up to the maximum stable gain. The maximum stable gain is shown in the dashed red line.
3. The impedance plots are shown from 0.5 – 6 GHz, with markers placed at 0.5 – 6.0 GHz in 0.5 GHz increments.

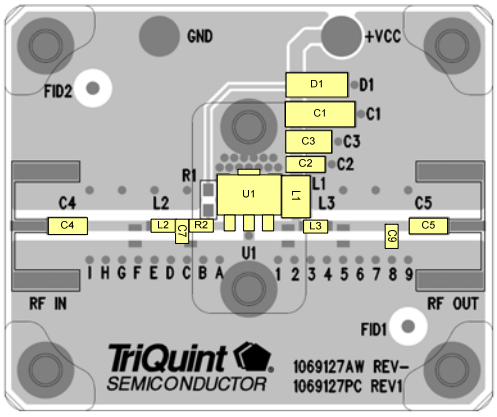
S-Parameter Data

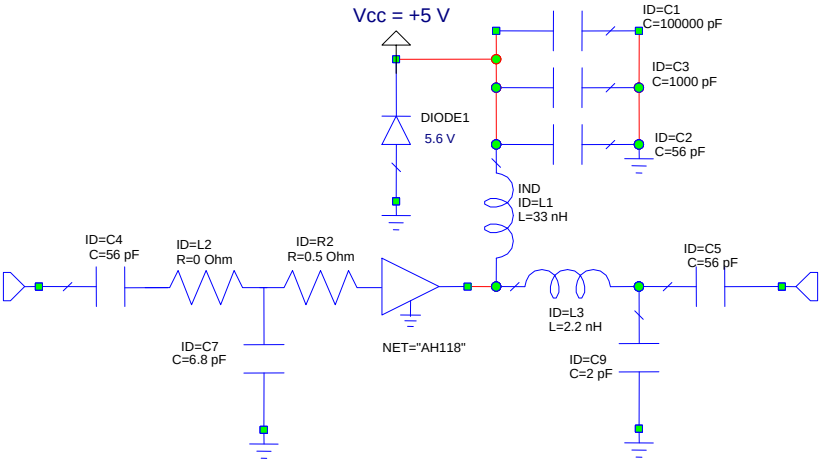
V_{cc} = +5 V, I_{cq} = 160 mA, T = 25 °C, unmatched 50 Ohm system, calibrated to device leads

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (angle)	S22 (dB)	S22 (ang)
50	-2.69	-173.38	21.74	153.70	-31.02	11.24	-7.02	-148.17
100	-2.16	-177.19	19.63	150.82	-30.31	7.90	-5.57	-162.45
200	-1.91	178.30	18.22	148.19	-29.87	5.01	-5.06	-173.51
400	-1.77	172.47	17.13	135.41	-29.83	4.07	-4.77	177.87
600	-1.60	166.83	15.99	121.91	-29.49	2.79	-4.60	171.65
800	-1.45	161.09	14.97	109.02	-29.18	2.11	-4.44	166.08
1000	-1.40	155.39	13.84	97.28	-28.70	1.64	-4.26	160.40
1200	-1.25	149.59	12.76	86.83	-28.63	-0.09	-4.14	155.01
1400	-1.20	143.79	11.71	76.95	-28.30	-1.34	-3.97	149.63
1600	-1.17	137.57	10.63	68.15	-27.94	-4.47	-4.00	144.03
1800	-1.13	132.05	9.75	59.55	-27.63	-7.00	-3.86	139.02
2000	-1.11	126.72	8.88	52.22	-27.51	-8.43	-3.84	134.24
2200	-1.05	121.50	8.00	45.09	-27.06	-11.00	-3.62	129.30
2400	-0.99	115.58	7.31	37.40	-27.02	-14.19	-3.55	124.42
2600	-0.93	110.41	6.52	30.66	-26.78	-18.24	-3.46	119.42
2800	-0.95	105.30	5.73	23.51	-26.66	-20.10	-3.34	114.26
3000	-0.92	100.11	5.05	17.07	-26.61	-23.28	-3.30	109.29

Device S-parameters are available for download off of the website at: http://www.triquint.com

Reference Design 920-960 MHz (AH118-89PCB900)





Notes:

1. The diode D1 is used as over-voltage protection on the evaluation boards. It is not specifically required in the final circuit layout in a system using a DC regulator.
2. L2 - the 0 Ω resistor - can be removed (with a thru line) in the final circuit layout.
3. The distance from U1 pin1 pad to the edge of C7 is 120 mil.
4. The distance from U1 pin3 pad to the edge of C9 is 350 mil.

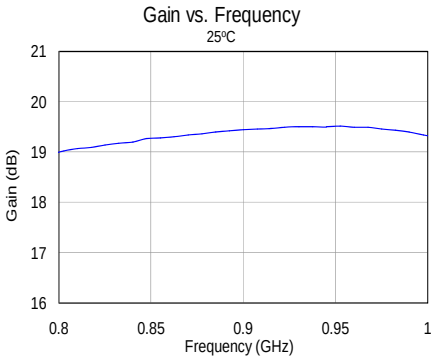
Bill of Material

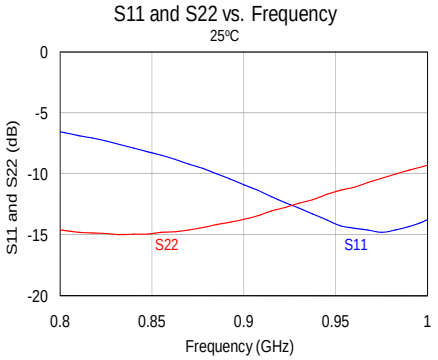
Ref Des	Value	Description	Manufacturer	Part Number
U1		High Linearity Amplifier	TriQuint	AH118-89G
C1	0.1 µF	Cap, Chip, 1206, 50 V, 10%, X7R	various	
C2, C4, C5	56 pF	Cap, Chip, 0603, 50 V, 5%, NPO/COG	various	
C3	1000 pF	Cap, Chip, 0805, 50 V, 5%, NPO	various	
C7	6.8 pF	Cap, Chip, 0603, 200 V, NPO/COG	various	
C9	2.0 pF	Cap, Chip, 0603, 200 V, NPO/COG	various	
L1	33 nH	Ind, Chip, 0603, 5%, Ceramic Core	various	
L2	0 Ω	Res, Chip, 0603, 5%, 1/16 W	various	
L3	2.2 nH	Ind, Chip, 0603, ±0.3 nH, Multilayer	various	
R2	0.51 Ω	Res, Chip, 0603, 5%, 1/10 W	various	
R1		No Load Part		
D1		Zener Diode, SOD-123		

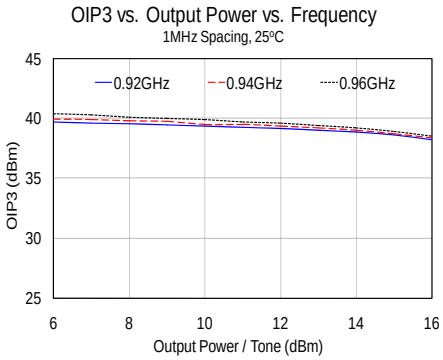
Typical Performance 920-960 MHz (AH118-89PCB900)

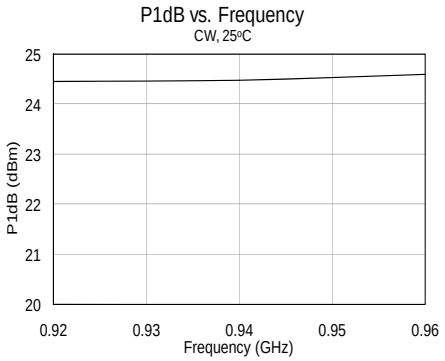
Frequency	MHz	920	940	960
Gain [1]	dB	19.5	19.5	19.5
Input Return Loss	dB	12.5	13.2	14.2
Output Return Loss	dB	12.5	11.7	11.0
Output P1dB	dBm	24.4	24.5	24.6
Output IP3 [2]	dBm	39.3	39.5	39.7
Channel Power @ -45 dBc ACLR [3]	dBm	16.7	16.7	16.7
Noise Figure	dB	4.3	4.4	4.5
Quiescent Current , Icq	mA		160	
Device / Supply Voltage , Vcc	V		+5	

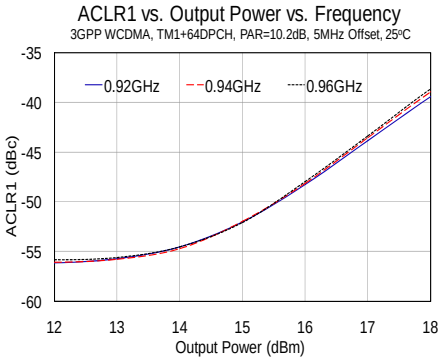
Notes
1. Test conditions unless otherwise noted: 25 ºC, +5V, in tuned application circuit.
2. OIP3 is measured at 11 dBm Pout / tone with 1 MHz spacing.
3. ACLR test set-up: 3GPP WCDMA, TM1+64DPCH, +5MHz Offset, PAR = 10.2 dB @ 0.01% Probability.



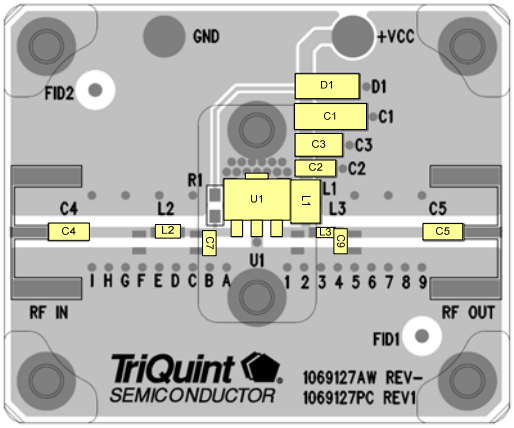


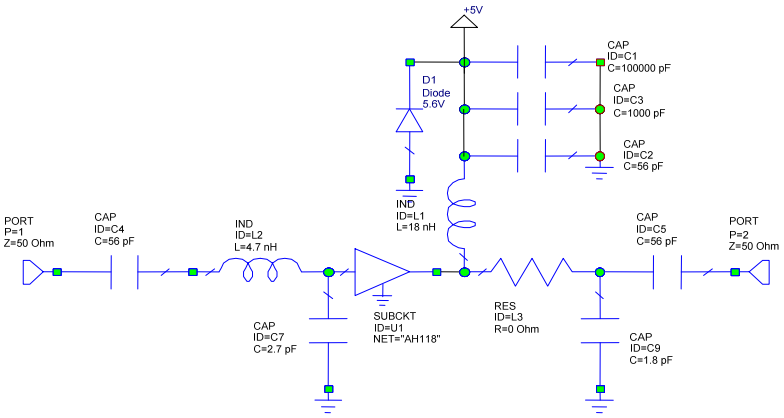






Reference Design 1900 MHz





Note:
1. The diode D1 is used as over-voltage protection on the evaluation boards. It is not specifically required in the final circuit layout in a system using a DC regulator.
2. L2 - the 0 Ω resistor - can be removed (with a thru line) in the final circuit layout.
3. C7 should be placed at the silk screen marker 'B' on the TriQuint evaluation board.
4. C7 should be placed at the silk screen marker '4' on the TriQuint evaluation board.

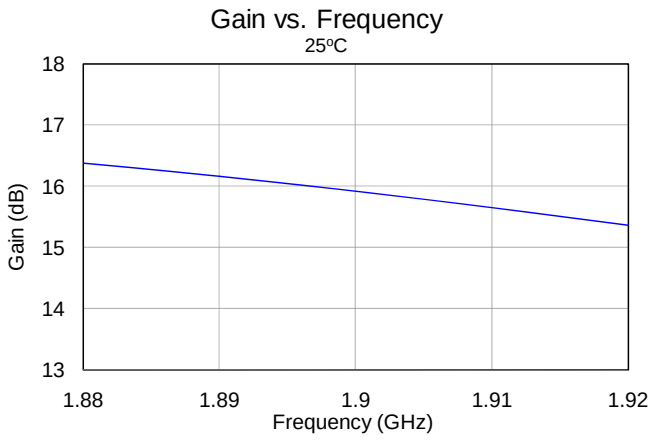
Bill of Material

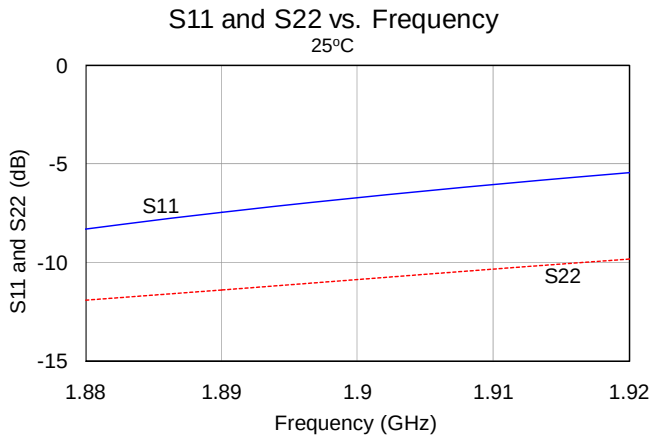
Ref Des	Value	Description	Manufacturer	Part Number
U1		High Linearity Amplifier	TriQuint	AH118-89G
C1	0.1 µF	Cap, Chip, 1206, 50 V, 10%, X7R	various	
C2, C4, C5	56 pF	Cap, Chip, 0603, 50 V, 5%, NPO/COG	various	
C3	1000 pF	Cap, Chip, 0805, 50 V, 5%, NPO	various	
C7	2.7 pF	Cap, Chip, 0603, 50 V, ±0.05 pF, NPO/COG	various	
C9	1.8 pF	Cap, Chip, 0603, 50 V, ±0.05 pF, NPO/COG	various	
L1	18 nH	Ind, Chip, 0603, 5%, Ceramic Core	various	
L2	4.7 nH	Ind, Chip, 0603, ±0.3 nH, Multilayer	various	
L3	0 Ω	Res, 0402, Chip, 5%, 1/16 W	various	
R1		No Load Part		
D1		Zener Diode, SOD-123		

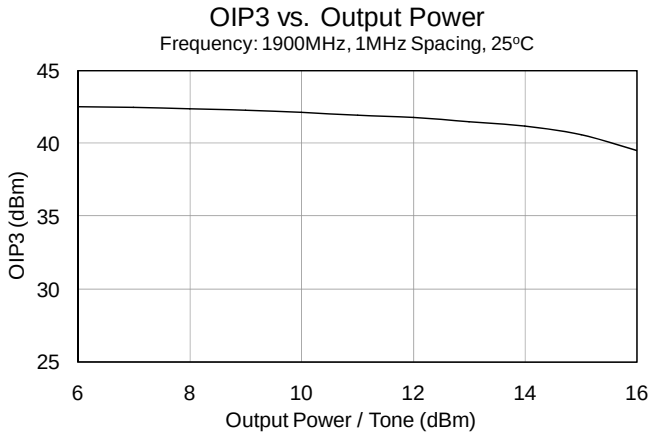
Typical Performance 1900 MHz

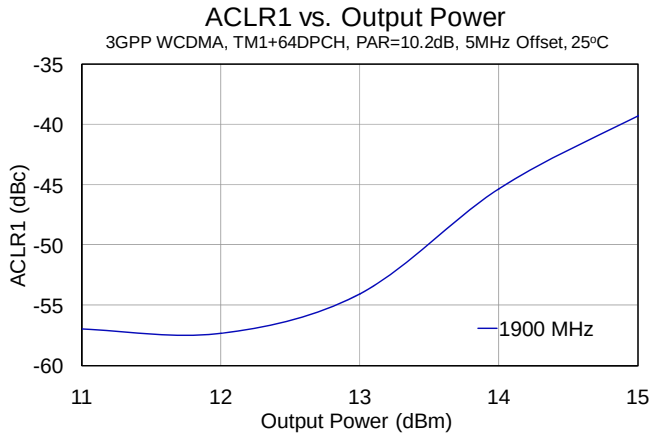
Frequency	MHz	1900
Gain [1]	dB	16.0
Input Return Loss	dB	7.5
Output Return Loss	dB	11.4
Output P1dB	dBm	25.4
Output IP3 [2]	dBm	41.5
Channel Power @ -45 dBc ACLR [3]	dBm	14
Quiescent Current , Icq	mA	160
Device / Supply Voltage , Vcc	V	+5

Notes
1. Test conditions unless otherwise noted: 25 ºC, +5V, in tuned application circuit.
2. OIP3 is measured at 11 dBm Pout / tone with 1 MHz spacing.
3. ACLR test set-up: 3GPP WCDMA, TM1+64DPCH, +5MHz Offset, PAR = 10.2 dB @ 0.01% Probability.

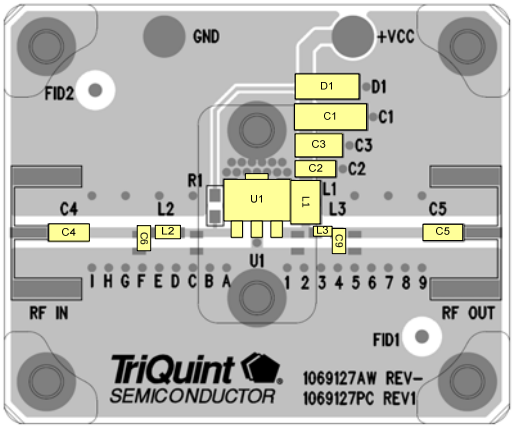


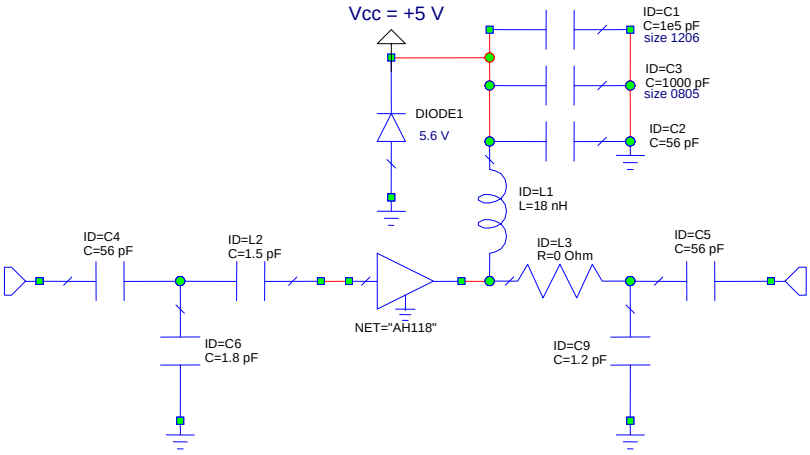






Reference Design 2110-2170 MHz (AH118-89PCB2140)





Note:
1. The diode D1 is used as over-voltage protection on the evaluation boards. It is not specifically required in the final circuit layout in a system using a DC regulator.
2. L2 - the 0 Ω resistor - can be removed (with a thru line) in the final circuit layout.
3. The distance from U1 pin1 pad to the edge of C6 is 253 mil.
4. The distance from U1 pin3 pad to the edge of C9 is 255 mil.

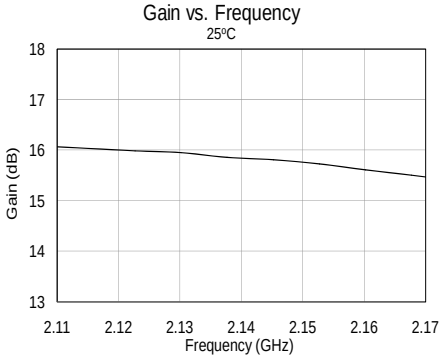
Bill of Material

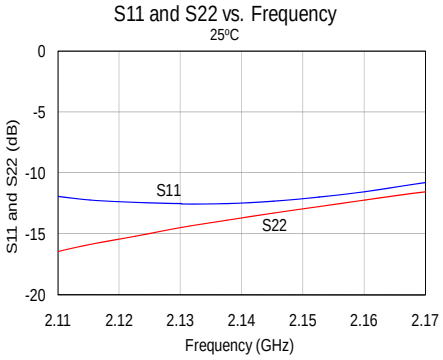
Ref Des	Value	Description	Manufacturer	Part Number
U1		High Linearity Amplifier	TriQuint	AH118-89G
C1	0.1 µF	Cap, Chip, 1206, 50 V, 10%, X7R	various	
C2, C4, C5	56 pF	Cap, Chip, 0603, 50 V, 5%, NPO/COG	various	
C3	1000 pF	Cap, Chip, 0805, 50 V, 5%, NPO	various	
C6	1.8 pF	Cap, Chip, 0603, 200 V, ±0.1 pF, NPO/COG	various	
C9	1.2 pF	Cap, Chip, 0603, 200 V, ±0.1 pF, NPO/COG	various	
L1	18 nH	Ind, Chip, 0603, 5%, Ceramic Core	various	
L2	1.5 pF	Cap, Chip, 0603, 200 V, ±0.1 pF, NPO/COG	various	
L3	0 Ω	Res, 0402, Chip, 5%, 1/16 W	various	
R1		No Load Part		
D1		Zener Diode, SOD-123		

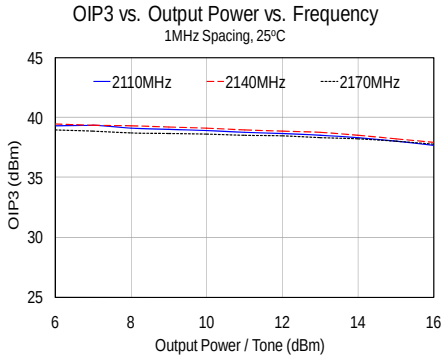
Typical Performance 2110-2170 MHz (AH118-89PCB2140)

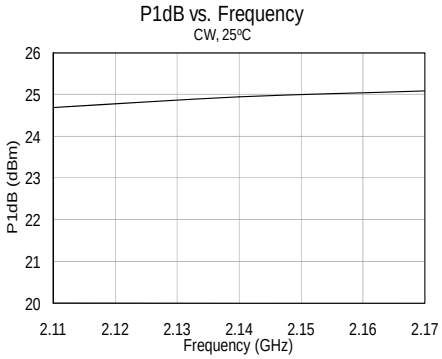
Frequency	MHz	2110	2140	2170
Gain [1]	dB	16.2	16.2	15.8
Input Return Loss	dB	12.4	12.3	10.4
Output Return Loss	dB	15.8	13.3	11.2
Output P1dB	dBm	24.7	24.9	25.0
Output IP3 [2]	dBm	38.8	39.0	38.5
Channel Power @ -45 dBc ACLR [3]	dBc	16.9	17.0	17.2
Noise Figure	dB	4.8	4.9	5.0
Quiescent Current , Icq	mA		160	
Device / Supply Voltage , Vcc	V		+5	

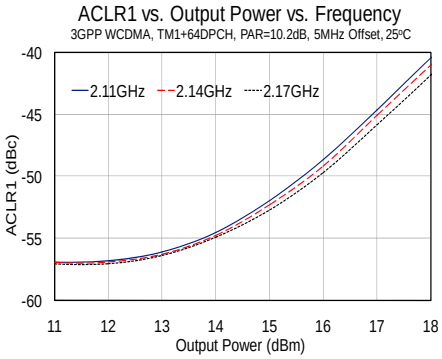
Notes
1. Test conditions unless otherwise noted: 25 ºC, +5V, in tuned application circuit.
2. OIP3 is measured at 11 dBm Pout / tone with 1 MHz spacing.
3. ACLR test set-up: 3GPP WCDMA, TM1+64DPCH, +5MHz Offset, PAR = 10.2 dB @ 0.01% Probability.





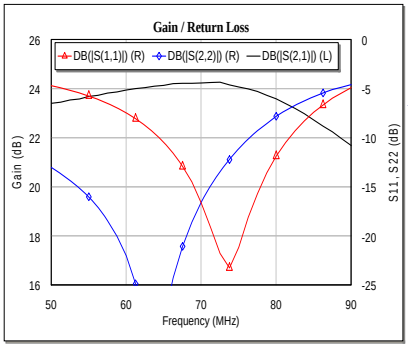


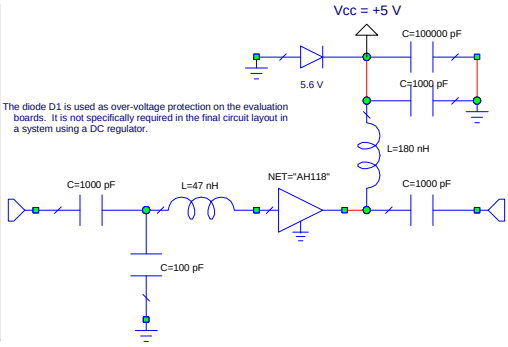




70 MHz Reference Design

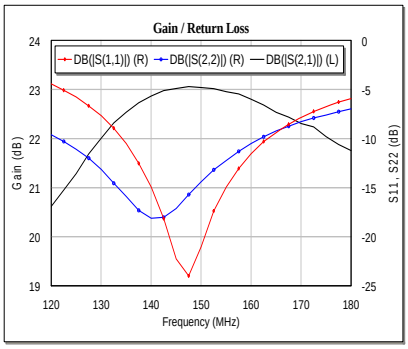
Frequency	70 MHz
Gain	24.2 dB
Input Return Loss	17 dB
Output Return Loss	16 dB
Output P1dB	+23.6 dBm
Output IP3 (+11 dBm / tone, Df=1 MHz)	+41 dBm
Noise Figure	4.8 dB
Supply Voltage	+5 V
Current	160 mA

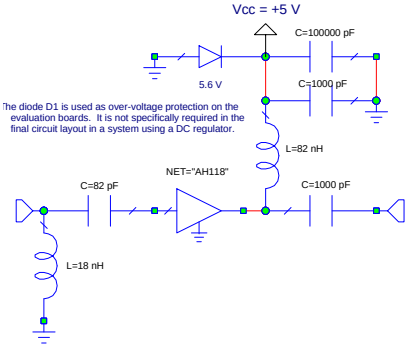




150 MHz Reference Design

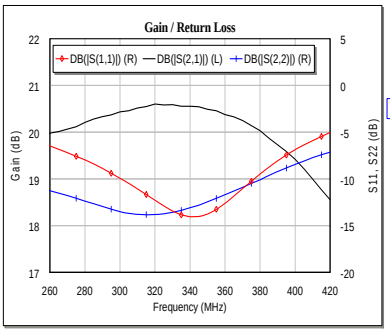
Frequency	150 MHz
Gain	23 dB
Input Return Loss	21 dB
Output Return Loss	14 dB
Output P1dB	+23.5 dBm
Output IP3 (+11 dBm / tone, Df=1 MHz)	+40 dBm
Noise Figure	4.9 dB
Supply Voltage	+5 V
Current	160 mA

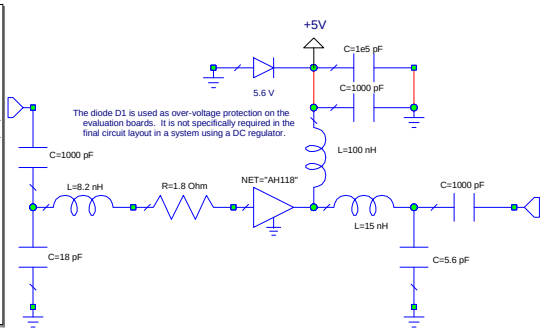




340 MHz Reference Design

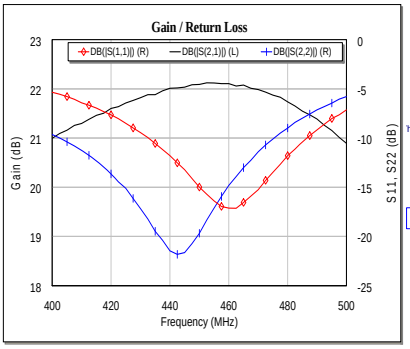
Frequency	340 MHz
Gain	20.6 dB
Input Return Loss	14 dB
Output Return Loss	13 dB
Output P1dB	+24 dBm
Output IP3 (+11 dBm / tone, Df=1 MHz)	+41.4 dBm
Noise Figure	5.1 dB
Supply Voltage	+5 V
Current	160 mA

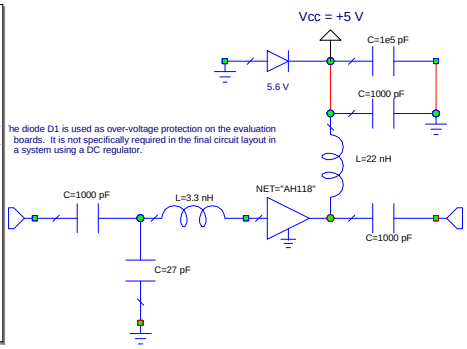




450 MHz Reference Design

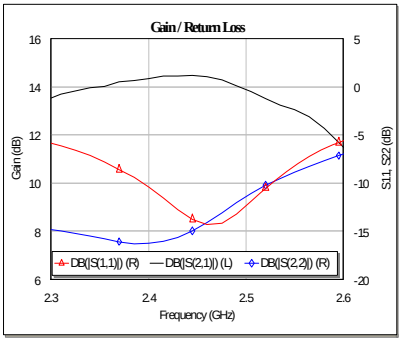
Frequency	450 MHz
Gain	22 dB
Input Return Loss	15 dB
Output Return Loss	19 dB
Output P1dB	+24 dBm
Output IP3 (+11 dBm / tone, Df=1 MHz)	+40 dBm
Noise Figure	5.7 dB
Supply Voltage	+5 V
Current	160 mA

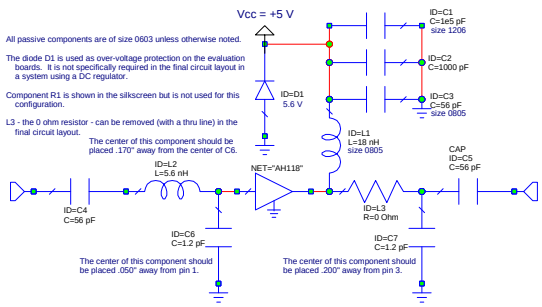




2450 MHz Reference Design

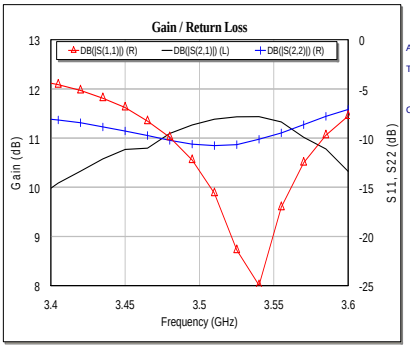
Frequency	2450 MHz
Gain	14.4 dB
Input Return Loss	14 dB
Output Return Loss	15 dB
Output P1dB	+25 dBm
Output IP3 (+11 dBm / tone, Df=1 MHz)	+38 dBm
Supply Voltage	+5 V
Current	160 mA
Gain	14.4 dB

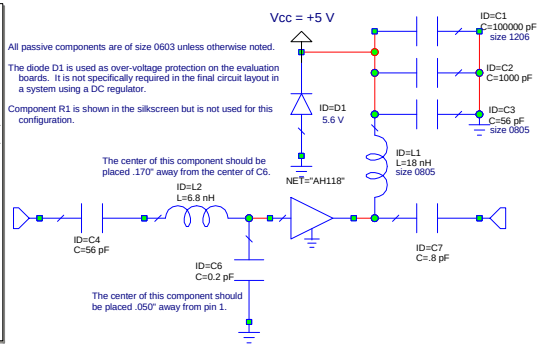




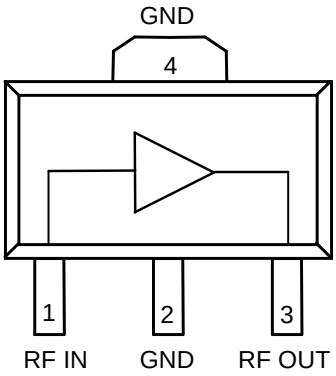
3500 MHz Reference Design

Frequency	3500 MHz
Gain	11 dB
Input Return Loss	14 dB
Output Return Loss	10 dB
Output P1dB	+23.5 dBm
Output IP3 (+11 dBm / tone, Df=1 MHz)	+38.5 dBm
Noise Figure	5.0 dB
Supply Voltage	+5 V
Current	160 mA





Pin Description



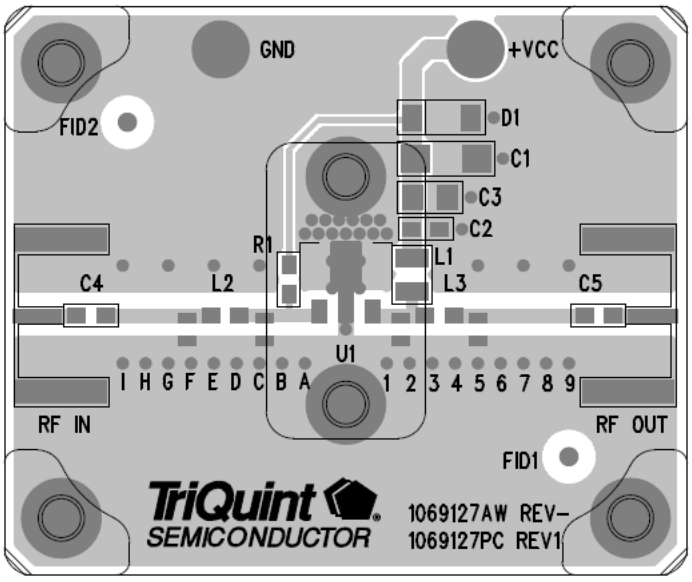
Pin	Symbol	Description
1	RF IN	RF Input. DC voltage present, blocking cap required
2	GND	No electrical connection. Provide an isolated or grounded solder pad for mounting integrity
3	RF OUT	RF Output. DC voltage present, blocking cap required
4	GND PADDLE	Multiple vias should be employed to minimize inductance and thermal resistance

Applications Information

PC Board Layout

Circuit Board Material: .062" total thickness with a .014" Getek top RF layer, 4 layers (other layers added for rigidity), 1 oz copper, Microstrip line details: width = .026", spacing = .026" The silk screen markers 'A', 'B', 'C', etc. and '1', '2', '3', etc. are used as placemarkers for the input and output tuning.

The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.



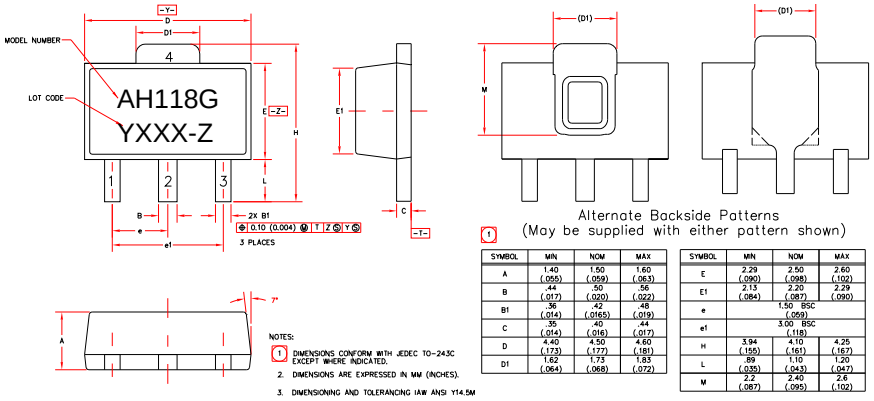
For further technical information, Refer to http://www.triquint.com/prodserv/more_info/default.aspx?prod_id=AH118

Mechanical Information

Package Information and Dimensions

This package is lead-free/Green/RoHS-compliant. It is compatible with both lead-free (maximum 260 °C reflow temperature) and leaded (maximum 245 °C reflow temperature) soldering processes. The plating material on the leads is NiPdAu.

The AH118 will be marked with an "AH118G" designator with a lot code marked below the part designator. The "Y" represents the last digit of the year the part was manufactured, the "XXX" is an auto-generated number, and "Z" refers to a wafer number in a lot batch

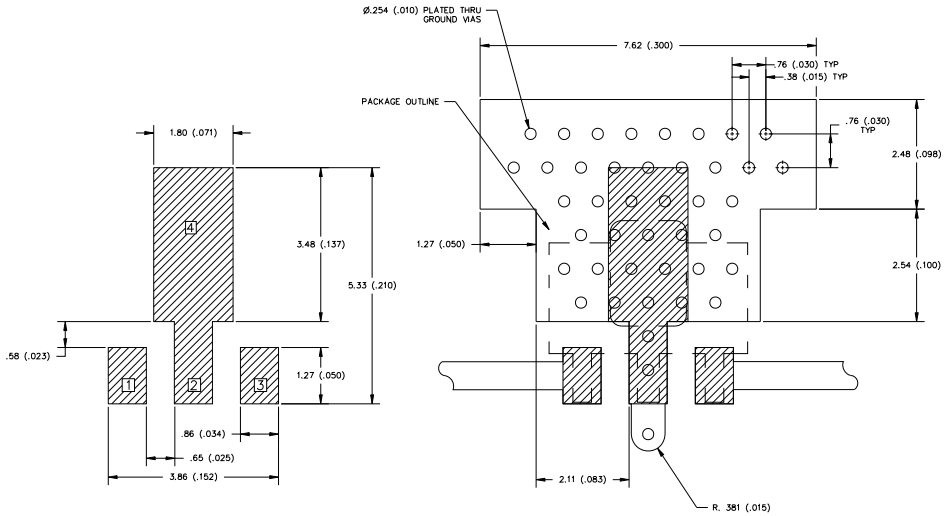


SYMBOL	MIN	NOM	MAX
A	1.40 (.055)	1.50 (.059)	1.60 (.063)
B	.44 (.017)	.50 (.020)	.56 (.022)
B1	.36 (.014)	.42 (.0165)	.48 (.019)
C	.35 (.014)	.40 (.016)	.44 (.017)
D	4.40 (.173)	4.50 (.177)	4.60 (.181)
D1	1.62 (.064)	1.73 (.068)	1.83 (.072)

SYMBOL	MIN	NOM	MAX
E	2.29 (.090)	2.50 (.098)	2.60 (.102)
E1	2.13 (.084)	2.20 (.087)	2.29 (.090)
e		1.50 BSC (.059)	
e1		3.00 BSC (.118)	
H	3.94 (.155)	4.10 (.161)	4.25 (.167)
L	.89 (.035)	1.10 (.043)	1.20 (.047)
M	2.2 (.087)	2.40 (.095)	2.6 (.102)

Mounting Configuration

All dimensions are in millimeters (inches). Angles are in degrees.



Notes:

1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink.
4. Do not put solder mask on the backside of the PC board in the region where the board contacts the heatsink.
5. RF trace width depends upon the PC board material and construction.
6. Use 1 oz. Copper minimum.
7. All dimensions are in millimeters (inches). Angles are in degrees.

Product Compliance Information

ESD Information

Caution! ESD-Sensitive Device

ESD Rating:	Class 1A
Value:	Passes between 250 and 500V.
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114

MSL Rating

Level 3 at +260 °C convection reflow
The part is rated Moisture Sensitivity Level 3 at 260°C per JEDEC standard J-STD-020.

Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260°

This part compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

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Email: info-sales@tqs.com **Fax:** +1.503.615.8902

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