IGLOO PLUS Starter Kit

User's Guide

Actel
POWER MATTERS

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Trademarks

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Introduction

IGLOO PLUS Starter Kit Contents

The RoHS-compliant, environmentally friendly IGLOO® PLUS Starter Kit is packaged in a recyclable cardboard box made from recycled materials. This development kit includes an on-board programmer and demonstrates the ultra-low power of Actel IGLOO PLUS devices. Table 1 lists the contents of the box.

Table 1 · IGLOO PLUS Starter Kit Contents

Quantity	Contents
1	IGLOO PLUS board with AGLP125 IGLOO PLUS FPGA
1	Programmer for use with IGLOO PLUS board
1	5 V power supply
2	USB 2.0 high-speed cables
1	Packet of jumpers
1	Actel Libero® Integrated Design Environment (IDE) DVD
1	Quick Start Guide

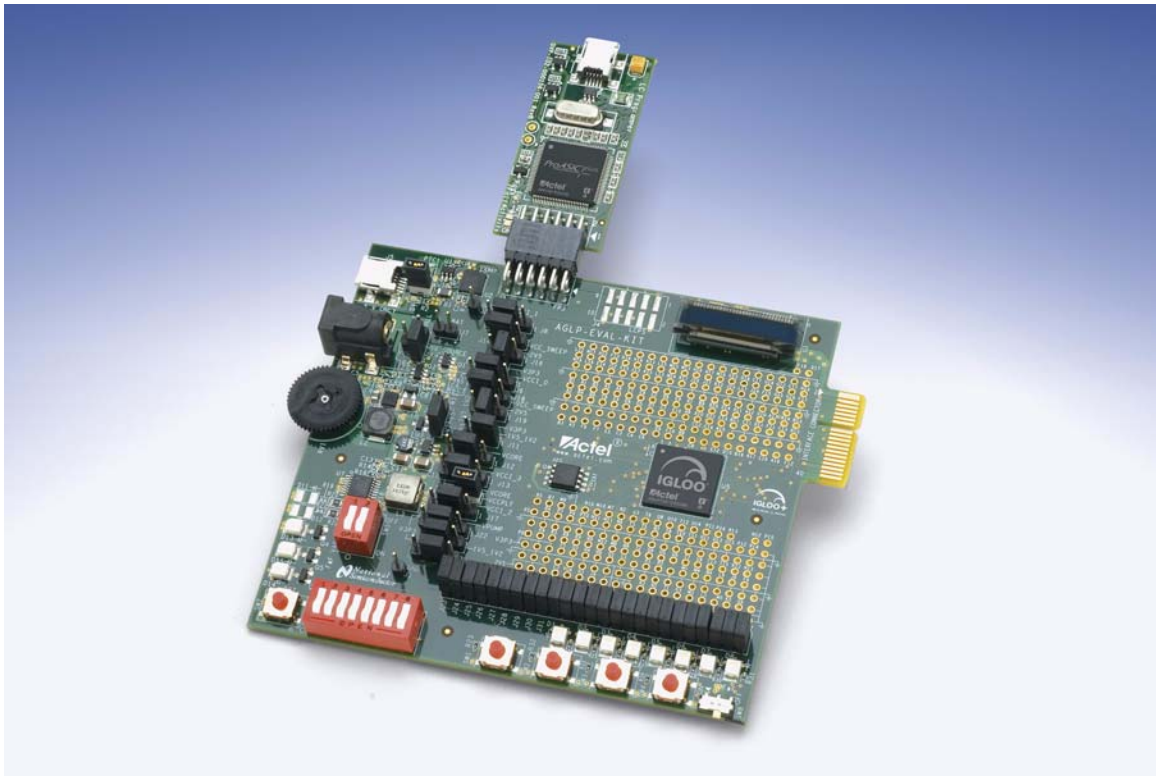


Figure 1 · IGLOO PLUS Starter Kit Board

1 Board Components and Settings

This chapter describes the components and settings for the IGLOO PLUS Starter Kit Board.

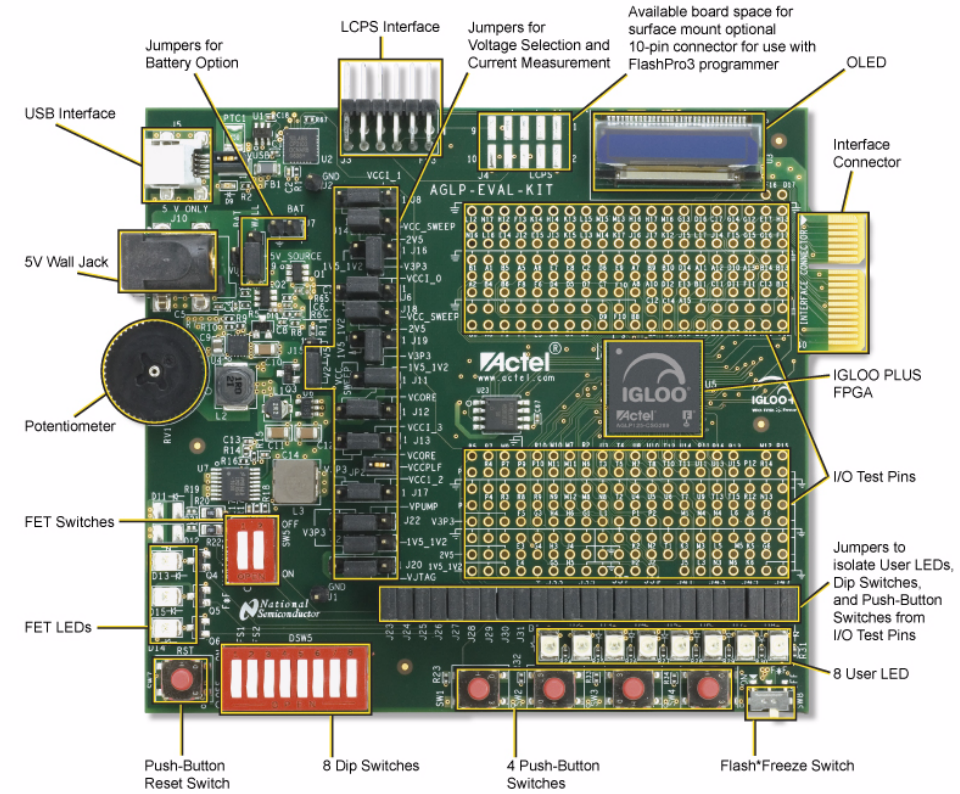
Board Description

The IGLOO PLUS Starter Kit board is intended to provide a low-cost system platform for evaluating IGLOO PLUS (AGLP) technology, such as low power, I/O state preservation during Flash*Freeze mode, and Schmitt Triggered I/Os. Other advanced features include the ability to use the FPGA I/Os of the Expansion Header as hot-swappable and the Schmitt Triggered FPGA inputs for improved noise immunity.

This evaluation board enables you to measure power consumption (dynamic, static, and Flash*Freeze modes) with the core operating between 1.2 V and 1.5 V. When using the board in conjunction with Actel's power analysis tools, you will have a clear picture of application power consumption at each stage in your design. In addition, the Libero® Integrated Design Environment (IDE) tool suite now includes power-driven layout (PDL), which can reduce the power consumption of designs up to 30 percent.

The evaluation board has a small form factor, measuring 3.7 inches by 4 inches, and supports an AGLP125 IGLOO PLUS device in the 14 mm × 14 mm CSG289 package. All components used on the board, such as LEDs, reset (µA range), and oscillator, are low-power components. Also included on the evaluation board is a USB-to-UART interface to allow HyperTerminal on a PC to communicate with the IGLOO PLUS device on the board.

The top of the board has a programming stick header which allows the low-cost programming stick (LCPS) to be attached to the board for programming the IGLOO PLUS AGLP125-CSG289 device (Figure 1-1 on page 7). FPGA I/Os have been wired to test pin pads on the board for debug and expandability.



Note: The clock oscillator for the IGLOO PLUS Starter Kit Board is behind the board.

Figure 1-1 · IGLOO PLUS Starter Kit Board

IGLOO PLUS Board Stackup

The IGLOO PLUS board is built on a 10-layer PCB. Figure 1-2 and Figure 1-3 on page 10 show the top (L1) and bottom (L10) silkscreens. The full PCB design layout is provided on the Actel website, on the IGLOO PLUS Starter Kit page: http://www.actel.com/products/hardware/devkits_boards/iglooplus_starter.aspx. To view the PCB design layout files, you can use the Allegro Free Physical Viewer, which can be downloaded from the Cadence Allegro Downloads page.

1. Top Signal (Figure 1-2 on page 9)
2. GND 1
3. Signal
4. GND 2
5. PWR 1
6. PWR 2
7. GND 3
8. Signal
9. GND 4
10. Bottom Signal (Figure 1-3 on page 10)

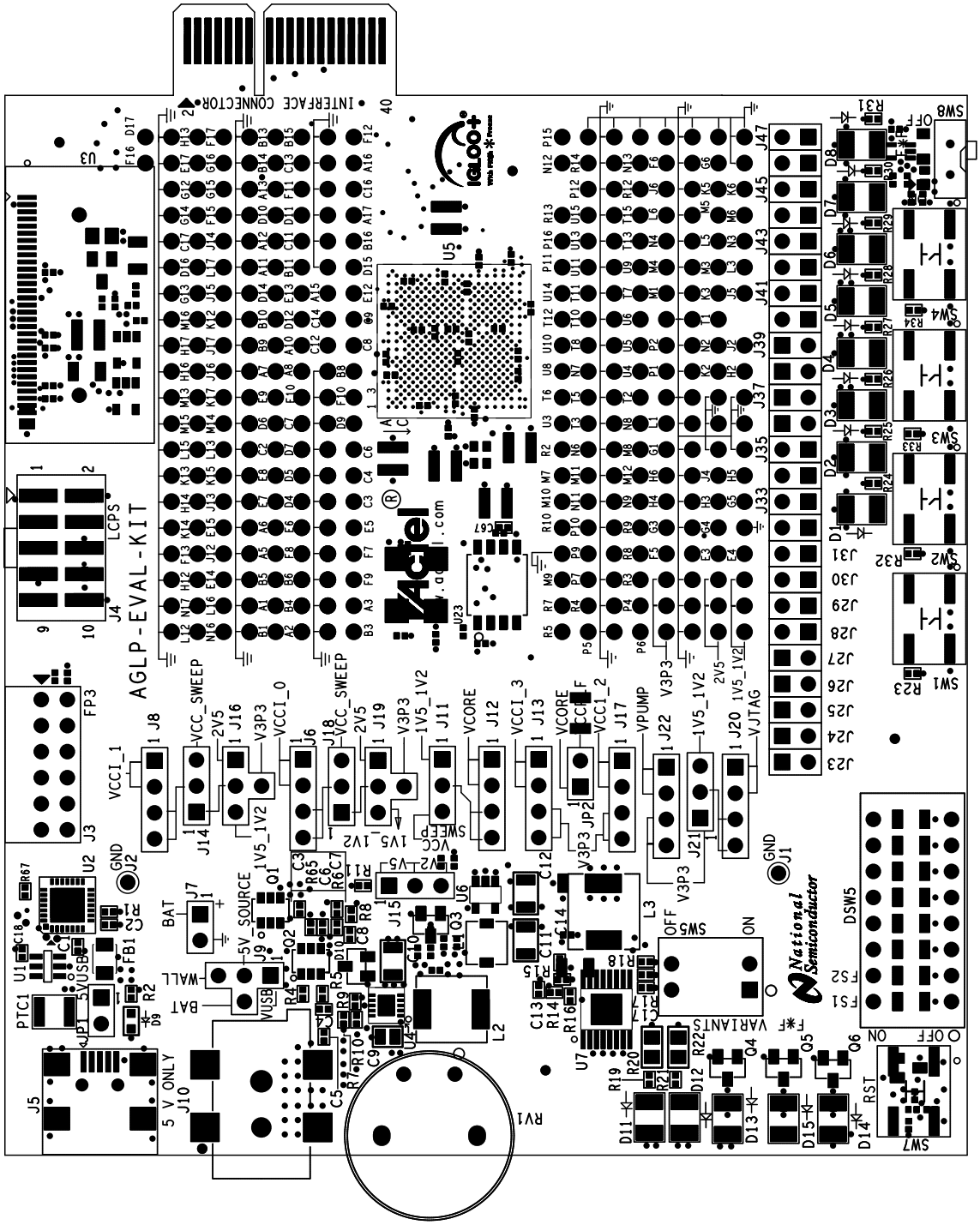


Figure 1-2 · IGLOO PLUS Top Silkscreen (L1)

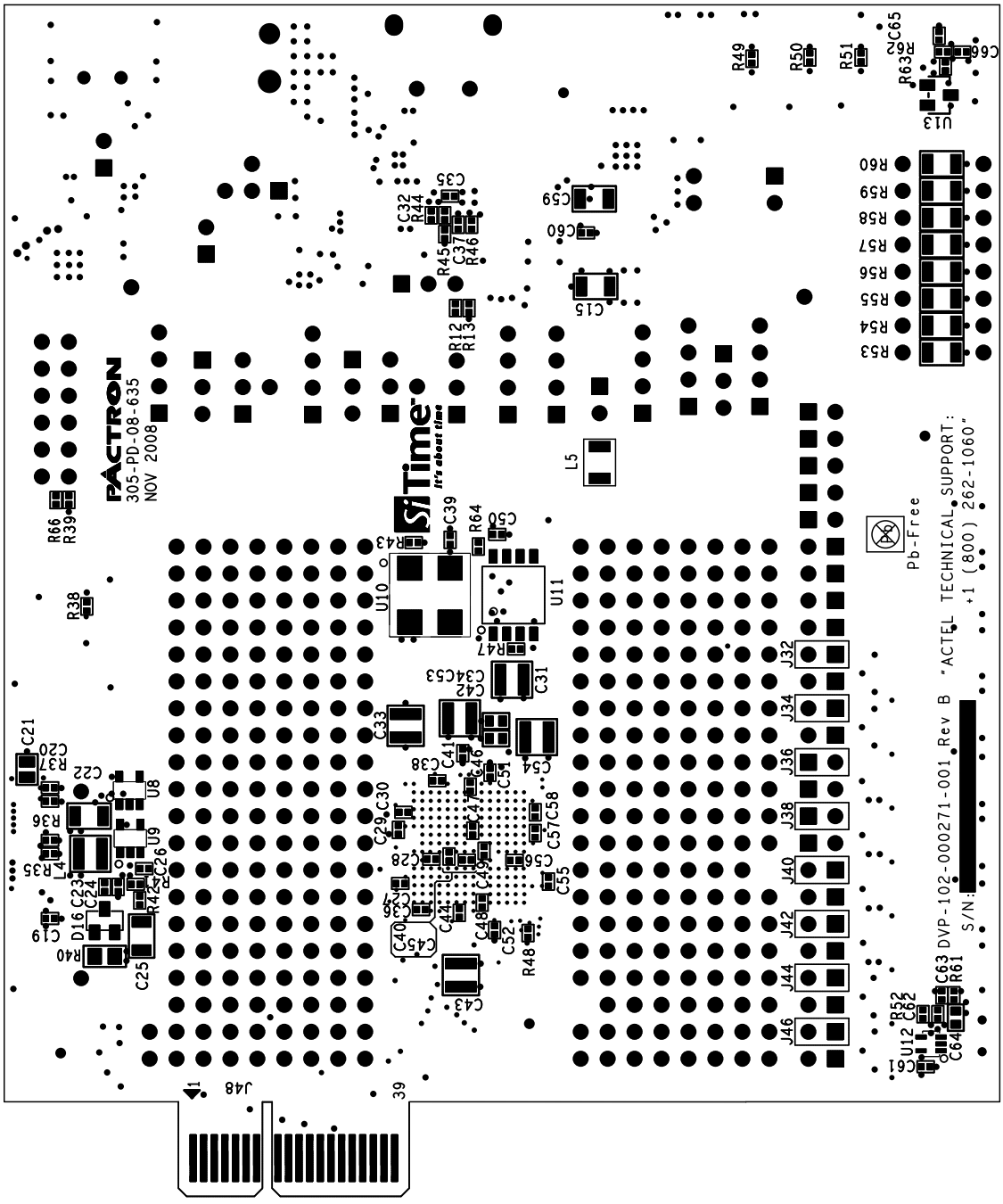


Figure 1-3 · IGLOO PLUS Bottom Silkscreen (L10)

Connectors, Jumpers, and Switch Settings

Recommended default jumper settings are defined in Table 1-1. The voltage selection jumpers are highlighted in grey. Connect jumpers in the default settings described in Table 1-1 to enable the pre-programmed demo design to function correctly.

Table 1-1 · Jumper and Connector Settings

Jumper	Default Setting	Comment
J1		Ground post header
J2		Ground post header
J3		LC JTAG header for programmer
J4		JTAG header
J5		USB mini receptacle
J6	Pin 2-3	Remove jumper to disconnect VCCI_0 power
J7	Remove	Remove jumper to disconnect external battery source
J8	Pin 2-3	Remove jumper to disconnect VCCI_1 power
J9	Pin 1-4	Select WALL, BAT, VUSB for 5V_SOURCE Pin 1-4 = VUSB Pin 2-4 = BAT Pin 3-4 = WALL
J10		5 V Brick
J11	Pin 1-2	Select VCC or VCC_SWEEP for VCORE Pin 1-2 = VCC Pin 3-2 = VCC_SWEEP
J12	Pin 2-3	Current measurement header for VCORE
J13	Pin 2-3	Current measurement header for VCCI_3
J14	Pin 1-2	Select VCC or VCC_SWEEP for VCCI_1 Pin 1-2 = VCC Pin 3-2 = VCC_SWEEP
J15	Pin 3-2	Select VJTAGENB or 3.3 V Pin 3-2 = VJTAGENB Pin 1-2 = 3.3 V
J16	Pin 2-4	Select 3.3 V, 1.5 / 1.2 V, or 2.5 V for VCCI_1 Pin 2-4 = 3.3 V Pin 3-4 = 1.5 V or 1.2 V Pin 1-4 = 2.5 V
J17	Pin 2-3	Current measurement header for VCCI_2
J18	Pin 1-2	Select VCC or VCC_SWEEP for VCCI_0 Pin 1-2 = VCC Pin 3-2 = VCC_SWEEP

Table 1-1 · Jumper and Connector Settings (continued)

Jumper	Default Setting	Comment
J19	Pin 2-4	Select 3.3 V, 1.5 / 1.2 V, or 2.5 V for VCCI_0 Pin 2-4 = 3.3 V Pin 3-4 = 1.5 V or 1.2 V Pin 1-4 = 2.5 V
J20	Pin 2-3	Current measurement header for VJTAG
J21	Pin 1-2	Select 3.3 V or 1.5 / 1.2 V for VJTAG Pin 1-2 = 3.3 V Pin 2-3 = 1.5 V or 1.2 V
J22	Pin 2-3	Current measurement header for VPUMP
J23-J24	Pin 1-2	Remove each jumper to disconnect any of the 2 FET Switches[1:2] from FPGA. J23 = 3V3_SWITCH1 J24 = 3V3_SWITCH2
J25-J27	Pin 1-2	Remove each jumper to disconnect any of the 3 FET LEDs from FPGA. J25 = FET_P1 J26 = FET_N J27 = FET_P2
J28-J35	Pin 1-2	Remove each jumper to disconnect any of the 8 user DIP switches[1:8] from FPGA. J28 = D_SWITCH1 J29 = D_SWITCH2 J30 = D_SWITCH3 J31 = D_SWITCH4 J32 = D_SWITCH5 J33 = D_SWITCH6 J34 = D_SWITCH7 J35 = D_SWITCH8

Table 1-1 · Jumper and Connector Settings (continued)

Jumper	Default Setting	Comment
J36-J39	Pin 1-2	Remove each jumper to disconnect any of the 4 push-button switches[1:4] from FPGA. J36 = SWITCH1 J37 = SWITCH2 J38 = SWITCH3 J39 = SWITCH4
J40-J47	Pin 1-2	Remove each jumper to disconnect any of the 8 user LEDs[1:8] from FPGA. J42 = LED1 J41 = LED2 J40 = LED3 J47 = LED4 J46 = LED5 J45 = LED6 J44 = LED7 J43 = LED8

Table 1-2 · Switch Settings

Switch	Default Setting	Comment
SW1–SW4		Push-button switches for SWITCH[1:4]
SW5	CLOSE	Contains DIP switches for 3V3_SWITCH[1:2]
DSW5	CLOSE	Contains DIP switches for D_SWITCH[1:8]
SW7		Push-button switch for system reset PBRESET_N
SW8	OFF	Flash*Freeze: To enable Flash*Freeze mode, SW8 toward ON. In Flash*Freeze mode, current consumption of FPGA goes below 50 µA.

2 FPGA Description

The IGLOO PLUS board is populated with an IGLOO PLUS AGLP125-CSG289 FPGA.

Key Features of AGLP125-CSG289

- Low power
- 1.2 V to 1.5 V core voltage support for low power
- Supports single-voltage system operation
- 5 µW power consumption in Flash*Freeze mode
- Low-power active FPGA operation
- Flash*Freeze technology enables ultra-low power consumption while maintaining FPGA content
- Configurable hold previous state, tristate, HIGH, or LOW state per I/O in Flash*Freeze mode
- Easy entry to / exit from ultra-low-power Flash*Freeze mode
- Reprogrammable flash technology
- In-system programming (ISP) and security
- High-performance routing hierarchy
- Advanced I/O
- Selectable Schmitt trigger inputs
- Clock conditioning circuit (CCC) and PLL
- Embedded memory

Table 2-1 lists specifications for the AGLP125-CSG289 FPGA.

Table 2-1 · IGLOO PLUS AGLP125-CSG289 FPGA Features

Feature	Specification
System Gates	125,000
Typical Equivalent Macrocells	1,024
VersaTiles (D-flip-flops)	3,120
Flash*Freeze Mode (Typical, µW)	16
RAM kbits (1,024 bits)	36
4,608-Bit Blocks	8
FlashROM (bits)	1 K
Secure (AES) ISP	Yes
Integrated PLLs in CCCs	1
VersaNet Globals	18
I/O Banks	4
Maximum User I/Os	212

For further information, refer to the *IGLOO PLUS datasheet*:
http://www.actel.com/documents/IGLOOPLUS_DS.pdf

Power and Ground Pins

Figure 2-1 shows the power and ground pins for AGLP125-CSG289.

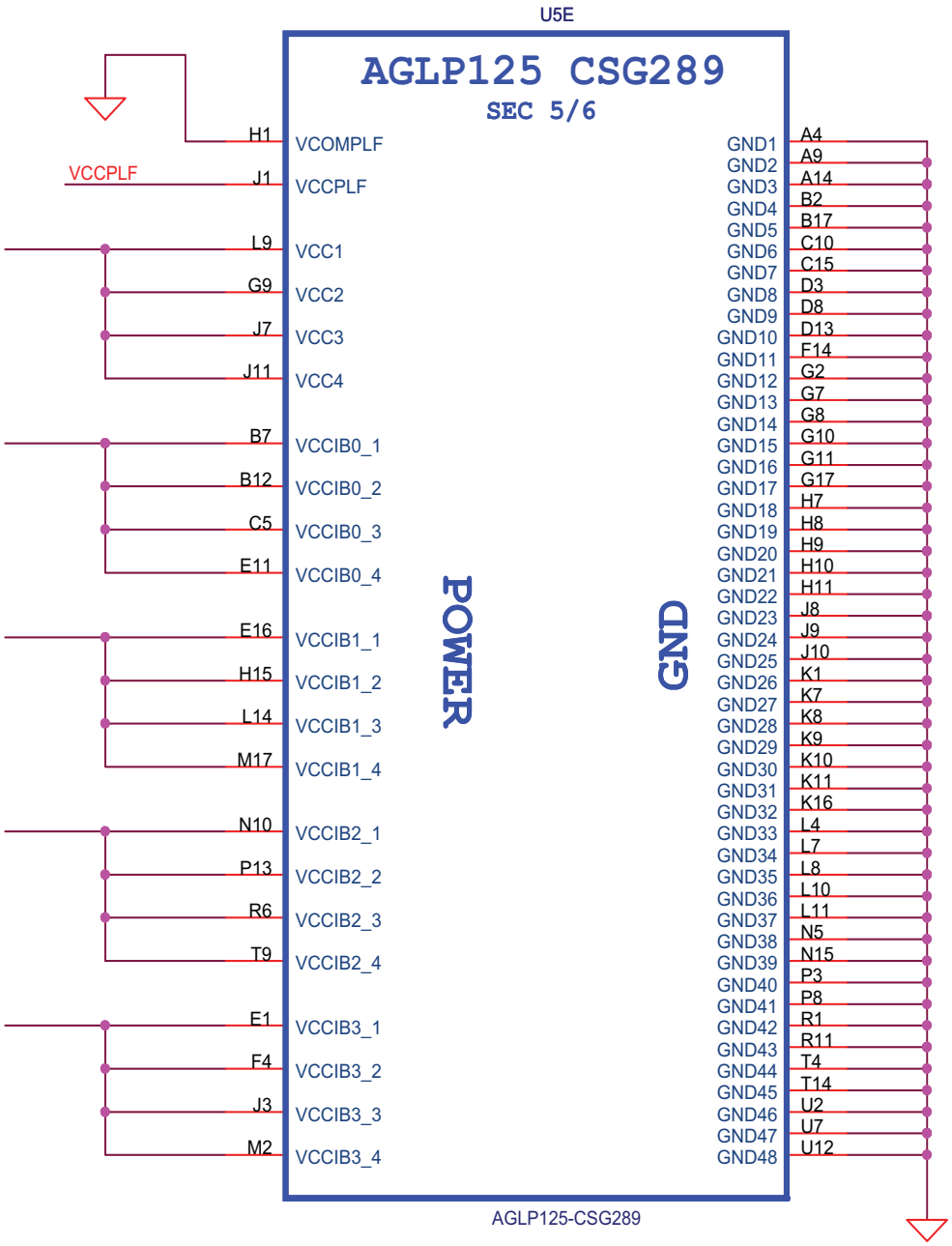


Figure 2-1 · Power and Ground Pins for AGLP125-CSG289

Bank I/O Signals

Figure 2-2 through Figure 2-5 on page 20 show schematics for the bank I/O signals.

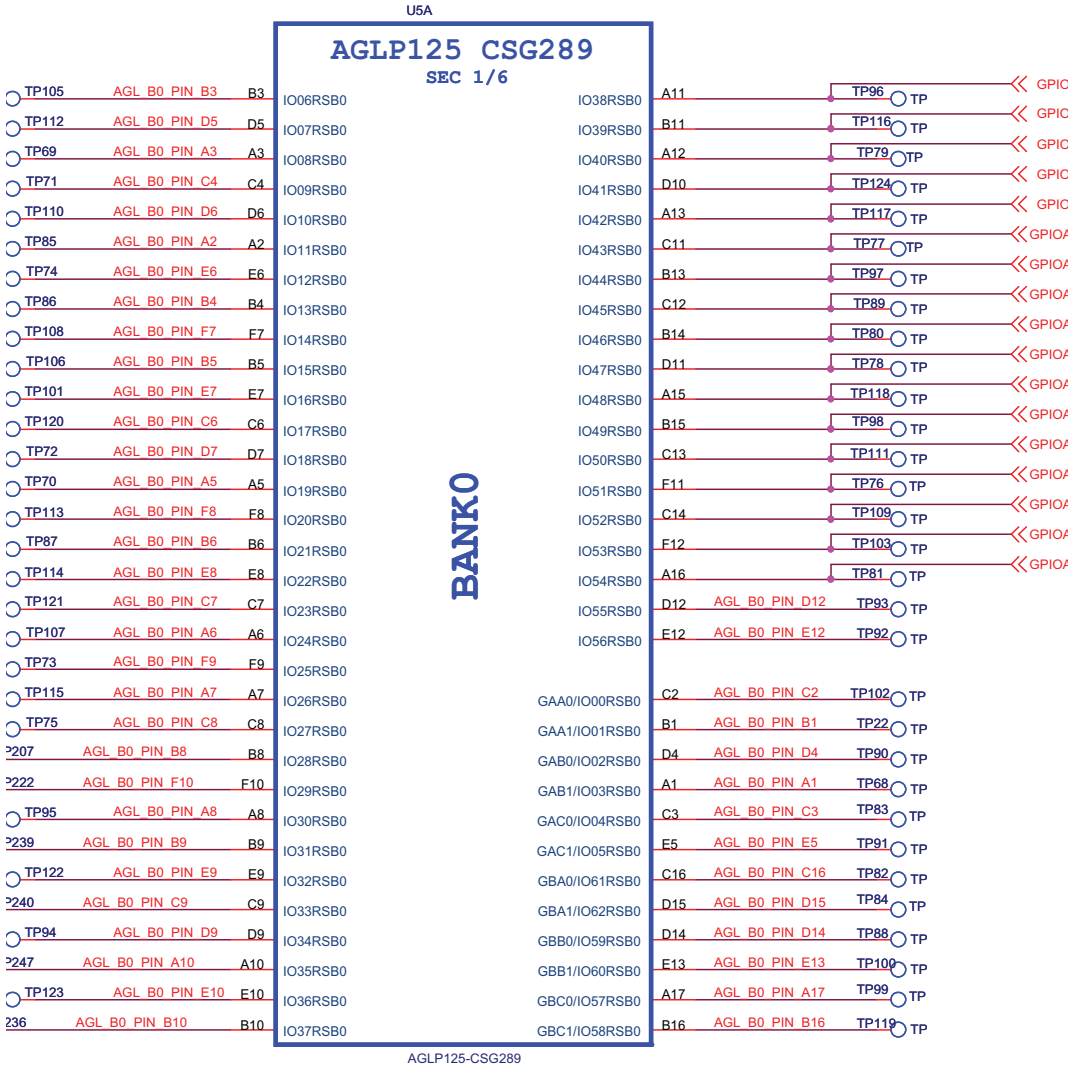


Figure 2-2 · Bank 0 I/O Signals for AGLP125-CSG289

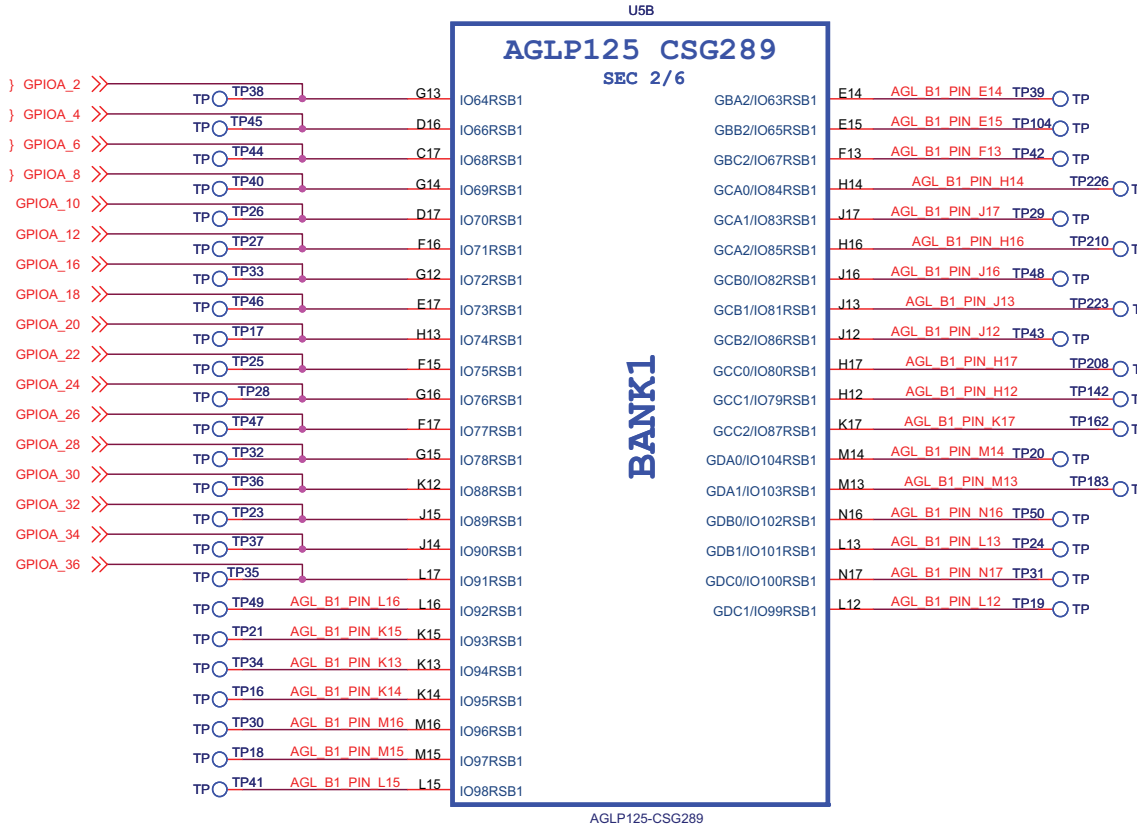


Figure 2-3 · Bank 1 I/O Signals for AGLP125-CSG289

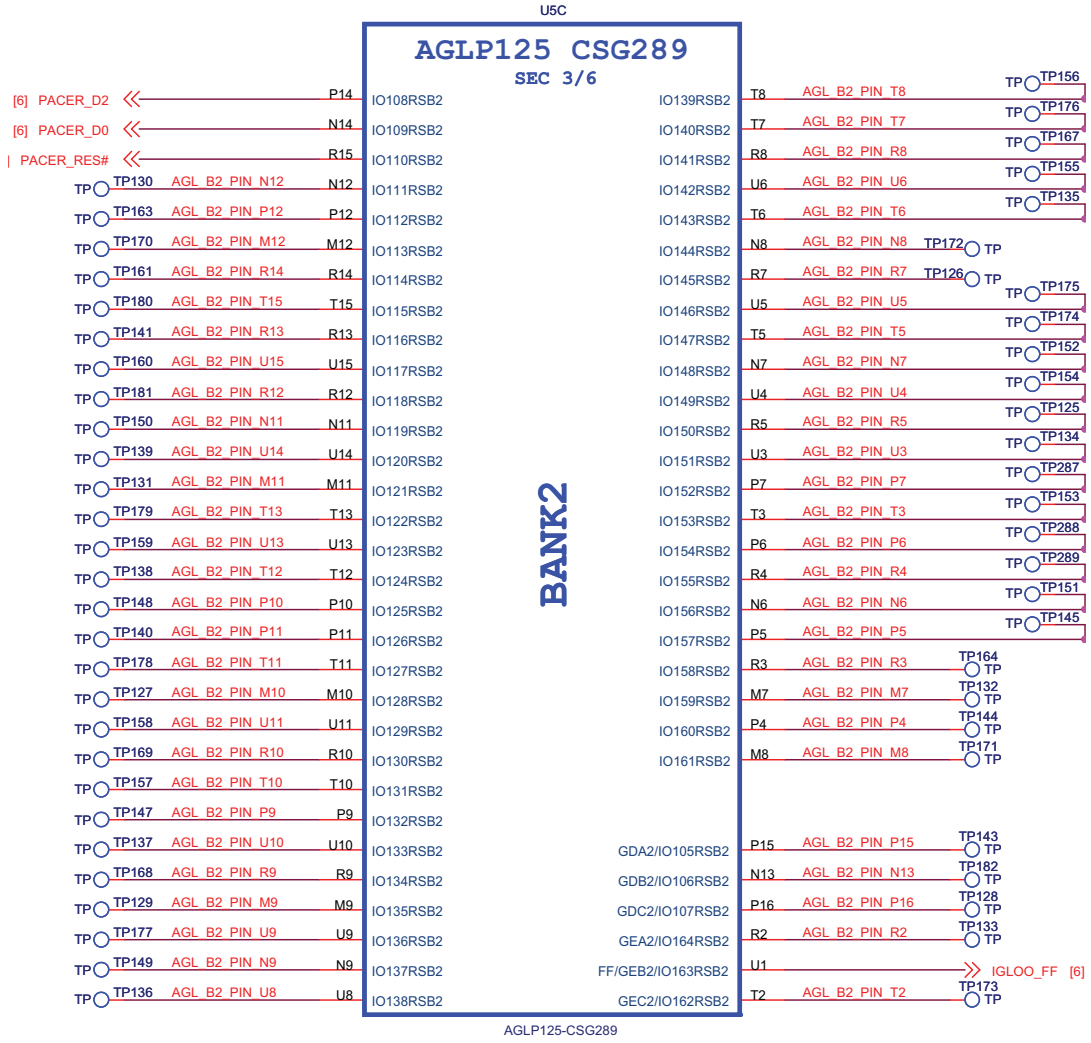


Figure 2-4 · Bank 2 I/O Signals for AGLP125-CSG289

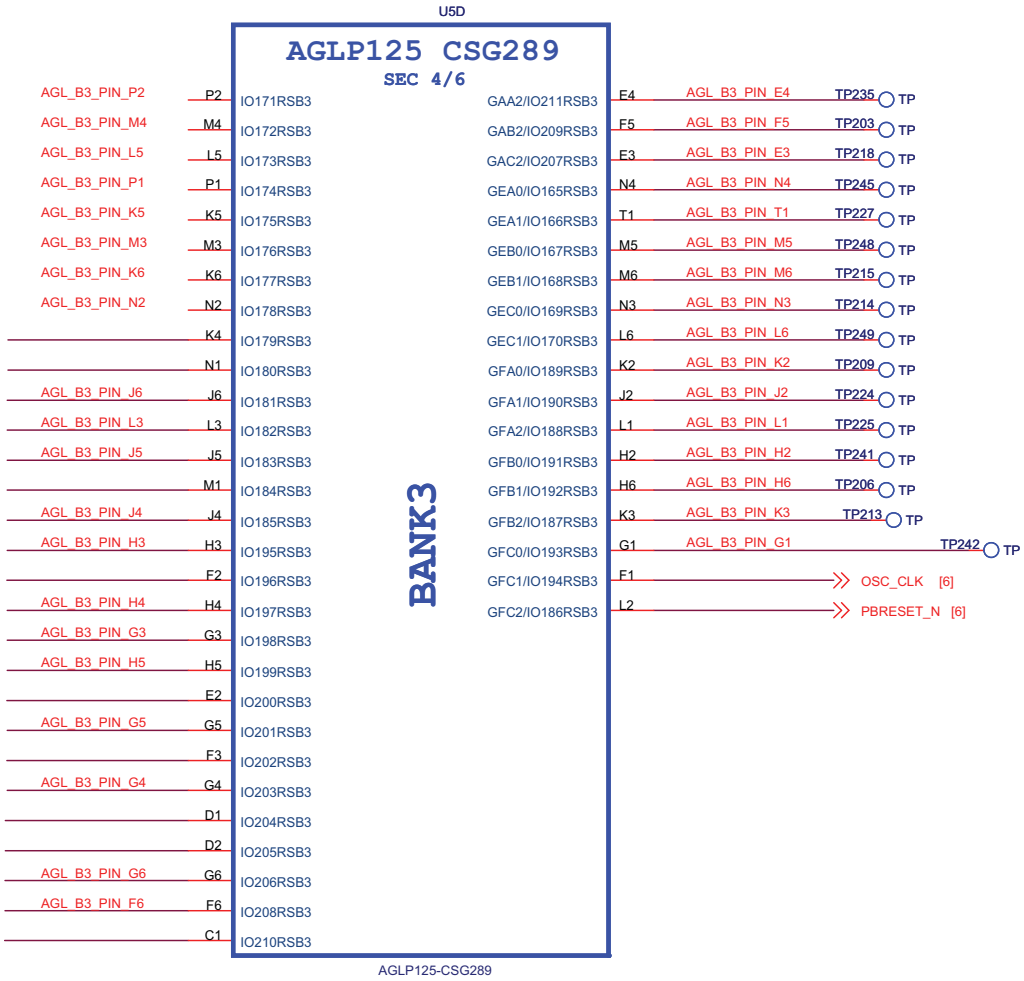


Figure 2-5 · Bank 3 I/O Signals for AGLP125-CSG289

JTAG Pins

The AGLP125-CSG289 has advanced I/O features such as JTAG pins for IEEE 1149.1 JTAG Boundary Scan Test. These pins are utilized during programming of the FPGA (Figure 2-6). Low-power flash devices have a separate bank for these dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). V_{CC} must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; V_{JTAG} alone is insufficient. Both V_{JTAG} and V_{CC} to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used or planned for use, the V_{JTAG} pin together with the TRST pin could be tied to GND.

VJTAG is the ability to switch between 3.3 V and 1.5 V / 1.2 V source using jumper J21. Four-pin headers could be used for current measurement of the V_{JTAG} and V_{PUMP} rails.

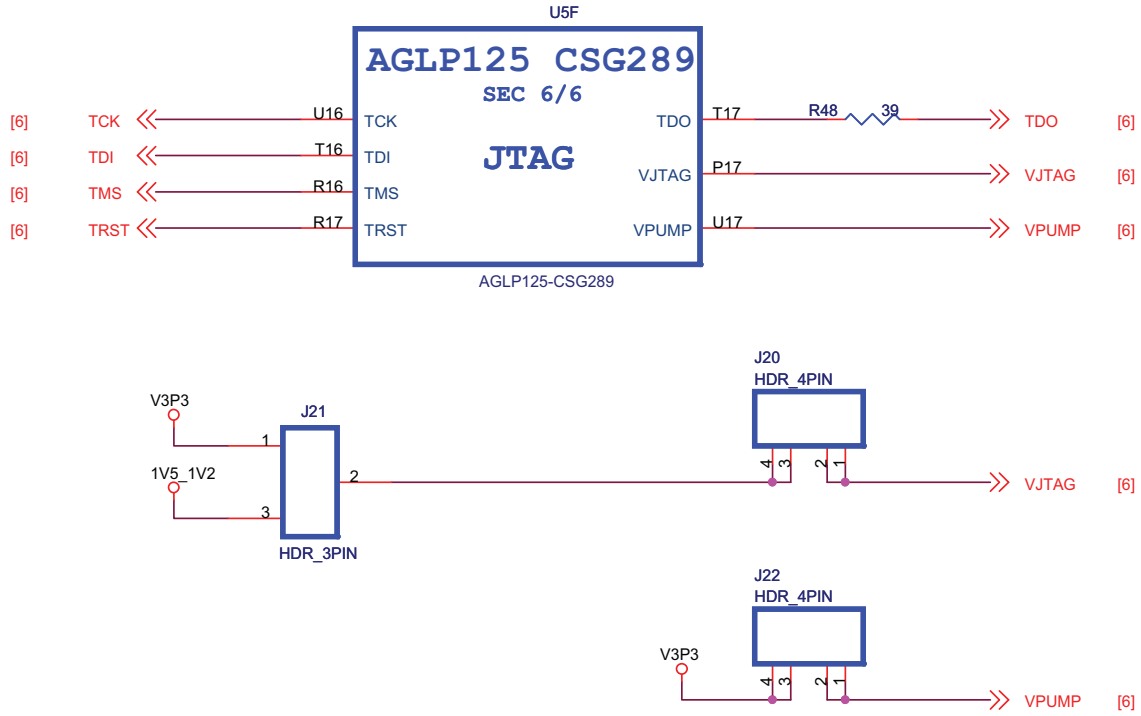


Figure 2-6 · JTAG Pins

Decaps and Ground Post Schematics

The schematics for the decaps and ground post are shown in Figure 2-7.

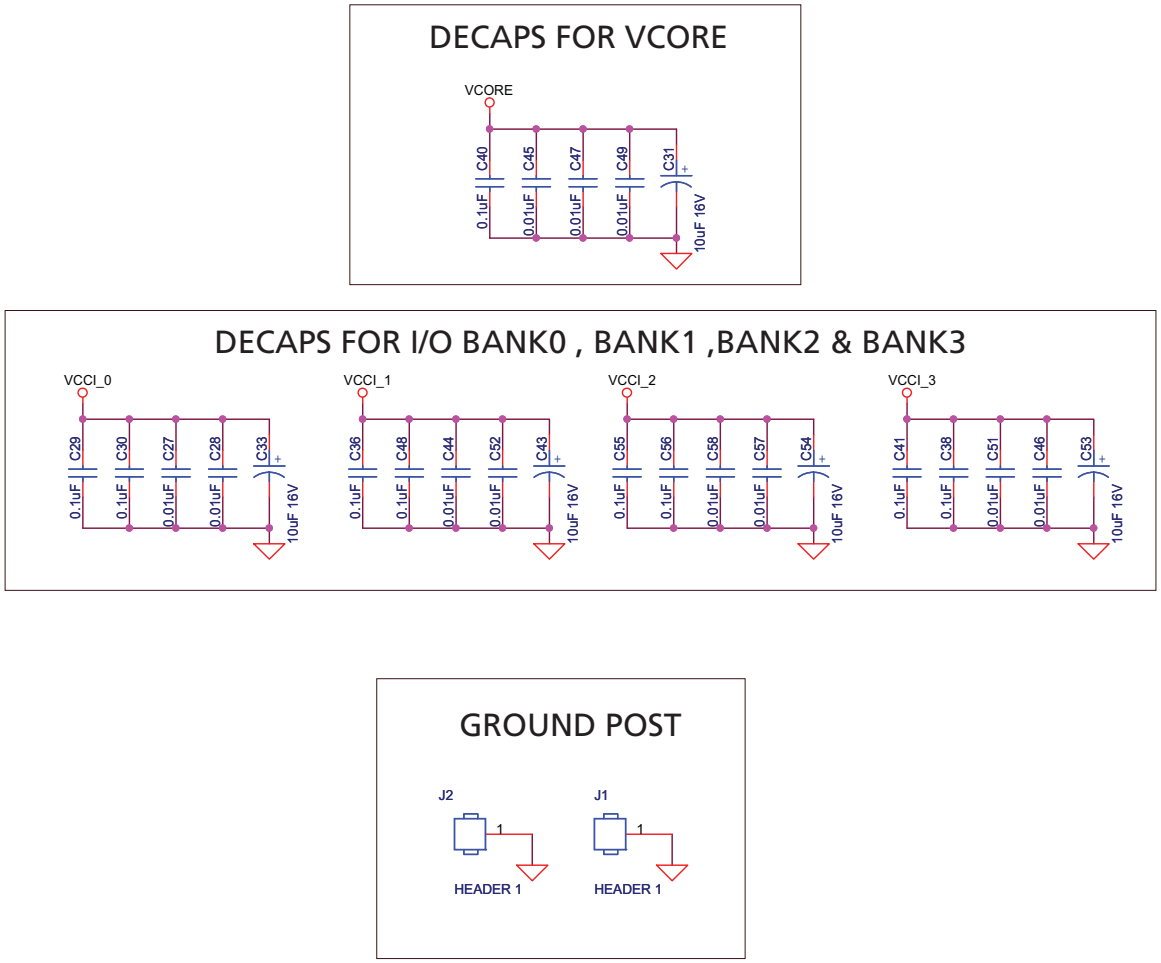


Figure 2-7 · Schematics for Decaps and Ground Post

Power

The IGLOO PLUS development board is powered through an external voltage power brick or USB. The board does not switch seamlessly between the power brick and USB, so the 4-pin header and jumper must be used to select the desired power source. In the USB option, the in-rush current meets the USB specifications (see Figure 3-1). The power brick option is provided in applications when 100% of the total I/Os are utilized and USB power is insufficient. A green LED next to the USB jack is ON whenever the USB power supply is connected.

The development board has an input of a 5 V supply from the power brick or USB. Protection diodes are used to protect against negative voltage. Three voltage rails are provided, as shown in Table 3-1 (3.3 V, 2.5 V, and 1.5 V).

The regulator can be switched between the 1.5 V and 1.2 V rail because the FPGA core functions at 1.2 V, but is programmed at 1.5 V.

Table 3-1 · Power Regulator Current Ratings

Regulator	Current Rating
3.3 V	2 A
2.5V	1 A
1.5 V / 1.2 V	500 mA

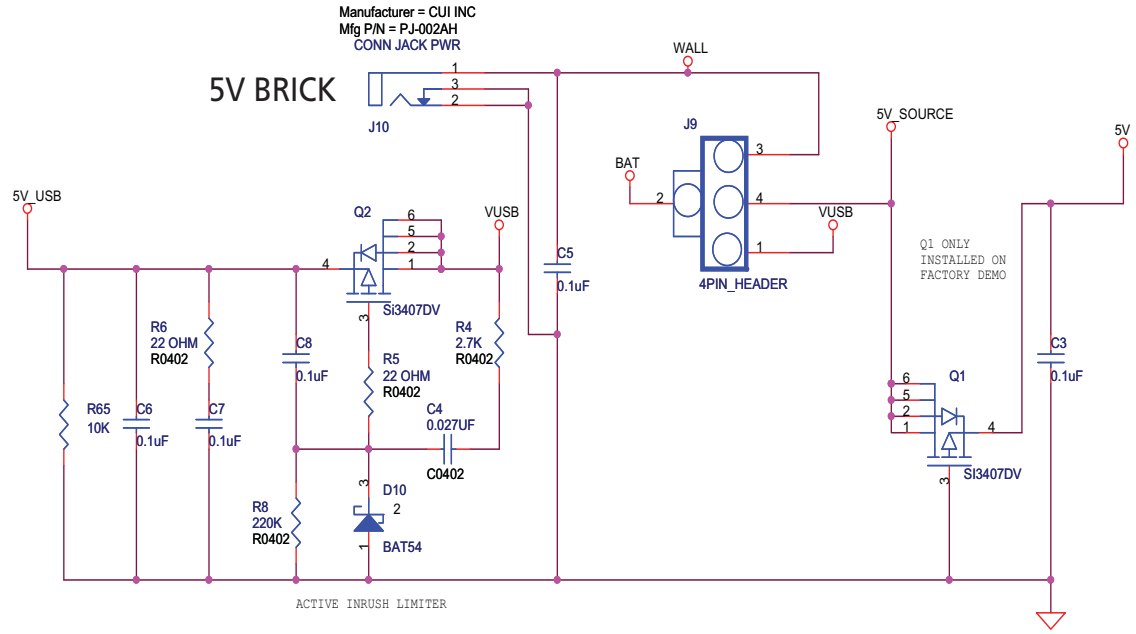


Figure 3-1 · USB Active Inrush Limiter

Power Modes

In addition to the board, the IGLOO PLUS FPGA offers power advantages. Some key power advantages of the IGLOO PLUS FPGAs are as follows:

- Flash*Freeze technology enables easy entry and exit from the static low power mode, where IGLOO consumes as little as 5 µW while retaining the contents of the system memory and data registers.
- Sleep (and shutdown) mode allows the IGLOO PLUS FPGA core power supply (or all power supplies) to be powered down when functionally is not required, while the rest of the system remains powered.
- The user low static ICC macro (ULSICC) reduces IGLOO PLUS FPGA dynamic and static power consumption. The ULSICC macro, when enabled, disables the FlashROM, reducing the overall power of the device.

Table 3-2 gives a summary of the power modes available with IGLOO PLUS devices in general and is extracted from the "Actel's Flash*Freeze Technology and Low Power Modes" chapter of the *IGLOO PLUS FPGA Fabric User's Guide*..

Table 3-2 · Power Modes

Mode		V_{CC}	V_{CCI}	Core	Clocks	ULSICC Macro	To Enter Mode	To Resume Operation	Trigger
Active		On	On	On	On	N/A	Initiate clock	None	–
Static	Idle	On	On	On	Off	N/A	Stop clock	Initiate clock	External
	Flash*Freeze Type 1	On	On	On	On*	N/A	Assert FF pin	Deassert FF pin	External
	Flash*Freeze Type 2	On	On	On	On*	Used to enter Flash*Freeze mode	Assert FF pin and LSICC	Deassert FF pin	External
Sleep		On	Off	Off	Off	N/A	Shut down V_{CC}	Turn on V_{CC} supply	External
Shutdown		Off	Off	Off	Off	N/A	Shut down V_{CC} and V_{CCI} supplies	Turn on V_{CC} and V_{CCI} supplies	External

* *External clocks can be left toggling while the device is in Flash*Freeze mode. Clocks generated by the embedded PLL will be turned off automatically.*

Battery

In addition to the power brick and USB, this board provides the option to power-up via battery. No battery casing is provided on the board. Jumpers should be set correctly to select the option of either powering through a wall/USB or through batteries hooked up externally. To provide a 3 V input source from battery, two AA Alkaline cells may be used. A 2-pin jumper for VBAT and GND must be provided to the input of the main regulator to give the option of either powering through a wall/USB or powering through batteries hooked up externally.

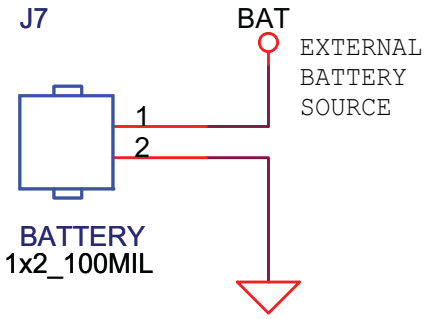


Figure 3-2 · Battery Header and Power Input Schematics

Potentiometer and Voltage-Sweep

A potentiometer is located on the left hand side of the board to provide the voltage-sweep function to sweep V_{CC} (Figure 3-3). One primary function of the potentiometer is to show battery operation on the IGLOO PLUS device and how the FPGA can operate successfully even if V_{CC} experiences a drop in voltage. You can measure the lowest possible V_{CC} for battery operations. When using the potentiometer, you should also monitor the V_{CC} via current measurement headers (Figure 3-4 on page 26) to make sure it does not go beyond the specified value.

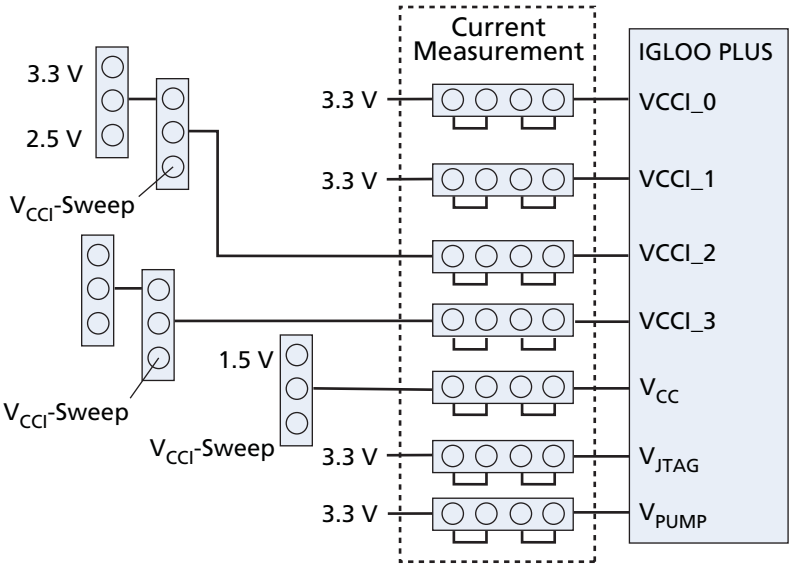


Figure 3-3 · Current Measurement Headers

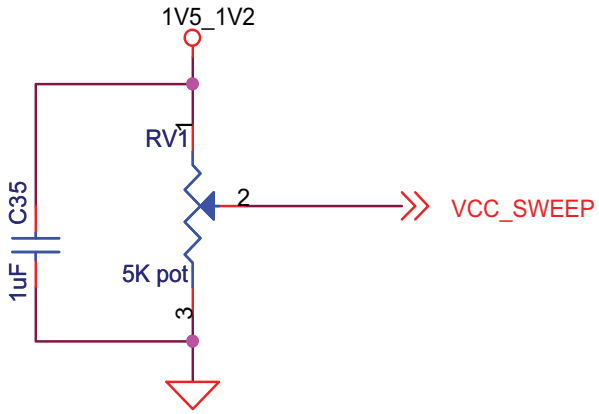
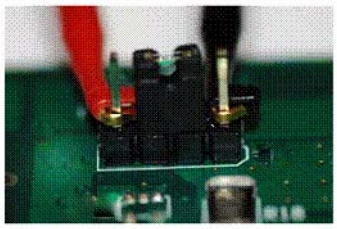


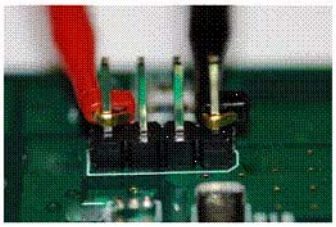
Figure 3-4 · Schematic for Potentiometer

Current Measurement

Once the IGLOO PLUS evaluation board is powered up, you can evaluate power consumption using the current measurement four-pin headers on the board (Figure 3-5). Current measurement can be made without powering down the board.



Set the multimeter to measure current and attach the probes to pins 1 and 4 when the board is in normal operation.



Remove jumper from pins 2-3 for current measurement without powering down.

Figure 3-5 · Current Measurement 4-Pin Headers

Four-pin headers are used for current measurement of the rails shown in Figure 3-6 on page 27. All banks are separated and two of the banks have an option to power-up though a 3.3 V or 2.5 V source, as shown in Figure 3-7 on page 28. Voltage sources can be selected using jumpers or can be selected to sweep between 1.2 V and 1.5 V using the potentiometer on the development board.

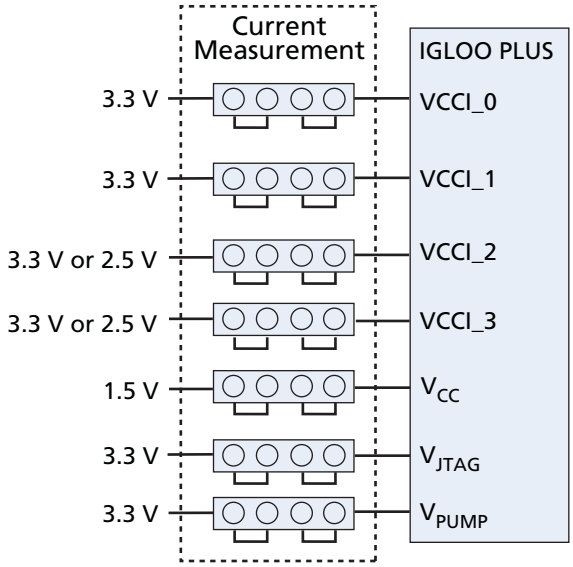


Figure 3-6 · Current Measurement Headers for Power Rails

The schematic in Figure 3-7 shows the options for power-up.

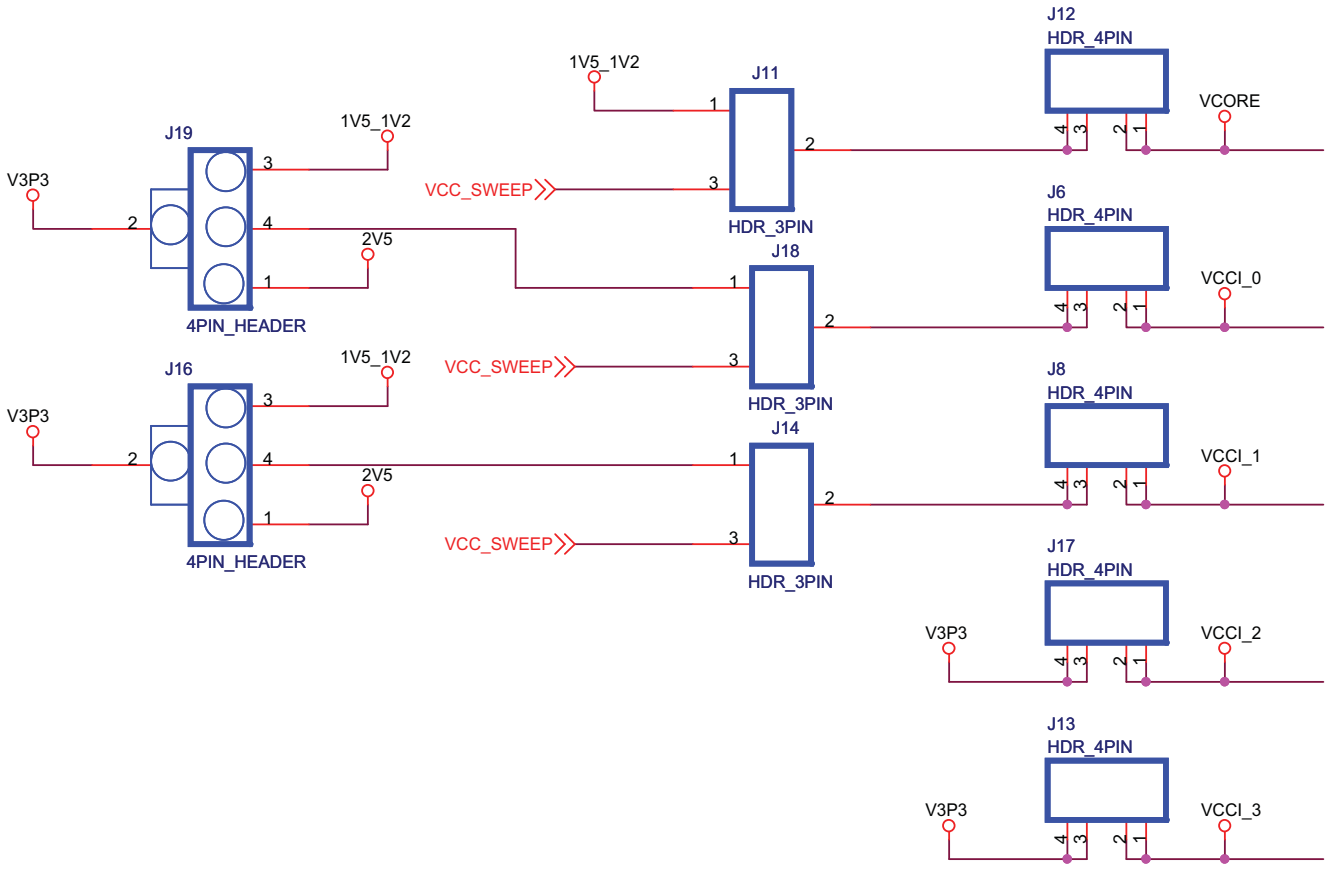


Figure 3-7 · Power-Up Options

4 Operation of Board Components

This chapter describes operation of the IGLOO PLUS evaluation board.

Clock Oscillator

One 20 MHz clock oscillator with 50 PPM is provided on the board. This clock oscillator is connected to the FPGA to provide a system or reference clock. The PLL can be configured and instantiated in the FPGA to generate a wide range of clock frequencies.

Reference

For more information, refer to the IGLOO PLUS Starter Kit website page:

http://www.actel.com/products/hardware/devkits_boards/iglooplus_starter.aspx.

Schematic

Figure 4-1 shows the schematic for the clock oscillator.

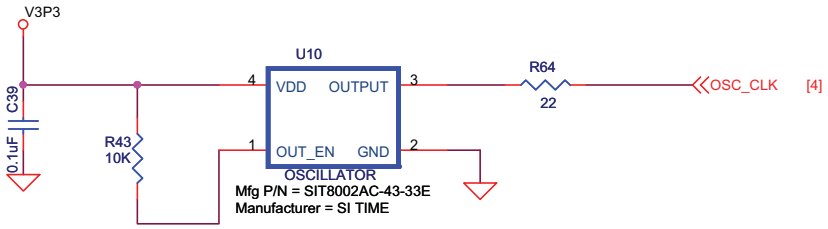


Figure 4-1 · Clock Oscillator Schematic

Reset

An RC type push-button reset switch to the FPGA is provided on-board. The Schmitt Trigger chip (U13), however, is NOT populated. An on-board Schmitt Trigger chip is not required because Schmitt Trigger is one of the many advanced I/O features of the IGLOO PLUS FPGA family. To improve noise immunity, ensure that the Schmitt Trigger option for this reset input pin is enabled in the FPGA design. If the IGLOO PLUS FPGA is swapped out with a device that does not have the advance Schmitt Trigger I/O feature, the Schmitt Trigger chip (U13) should be populated.

Schematic

Figure 4-2 shows the schematic for reset.

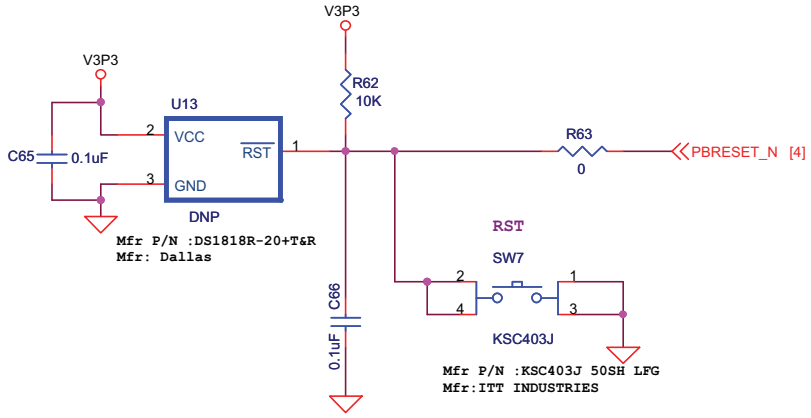


Figure 4-2 · Reset Schematic

Flash*Freeze Mode

The IGLOO PLUS device has an ultra-low-power static mode, called Flash*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation (Figure 4-3).

Flash*Freeze technology enables the user to quickly (within 1 µs) enter and exit Flash*Freeze mode by activating the Flash*Freeze pin while all power supplies are kept at their original values. I/Os, global I/Os, and clocks can still be driven and can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and I/O states. I/Os can be individually configured to either hold their previous state or can be tristated during Flash*Freeze mode.

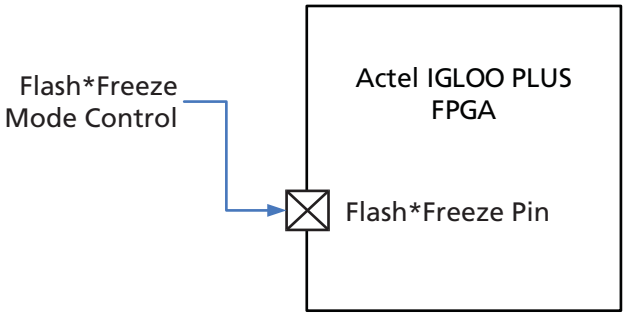


Figure 4-3 · Flash*Freeze Mode Control

There are two ways to use Flash*Freeze mode. In Flash*Freeze type 1, entering and exiting the mode is exclusively controlled by the assertion and deassertion of the FF pin. This enables an external processor or human interface device to directly control Flash*Freeze mode. In Flash*Freeze mode type 2, entering and exiting the mode is controlled by both the FF pin AND user-defined logic. Flash*Freeze management IP can be used in type 2 mode for clock and data management while entering and exiting Flash*Freeze mode.

For more information and detailed usage of Flash*Freeze modes, refer to the "Actel's Flash*Freeze Technology and Low Power Modes" chapter of the *IGLOO PLUS FPGA Fabric User's Guide*.

Flash*Freeze Types

Type 1: Control by dedicated Flash*Freeze Pin.

Type 2: Control by dedicated Flash*Freeze Pin and Internal Logic.

Flash*Freeze Type 1: Control by Dedicated Flash*Freeze Pin

Flash*Freeze type 1 is intended for systems where either the device will be reset upon exiting Flash*Freeze mode, or data and clock are managed externally. The device enters Flash*Freeze mode 1 µs after the dedicated FF pin is asserted (active low), and returns to normal operation when the FF pin is deasserted (high). In this mode, FF pin assertion or deassertion is the only condition that determines entering or exiting Flash*Freeze mode (Figure 4-4). An INBUF_FF I/O buffer macro must be used to identify the Flash*Freeze input in your design.

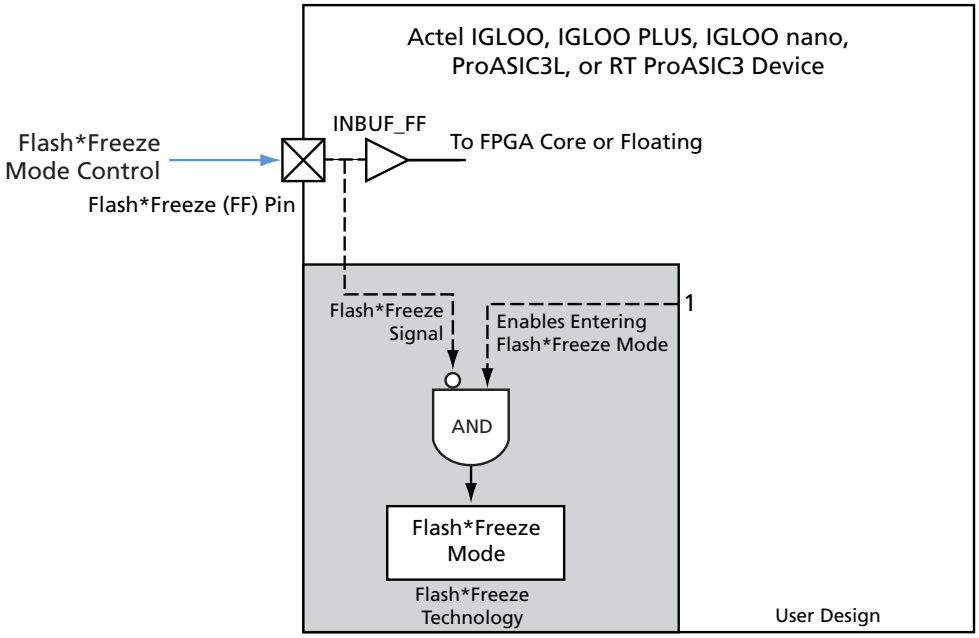


Figure 4-4 · Flash*Freeze Mode Type 1 – Controlled by the Flash*Freeze Pin

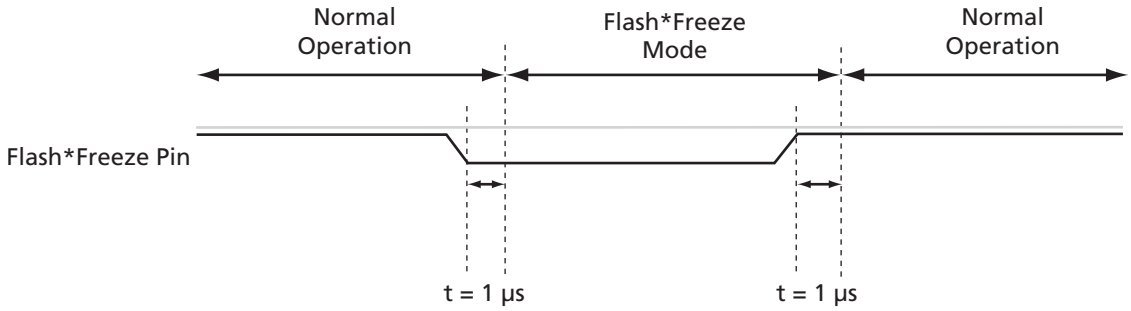


Figure 4-5 · Flash*Freeze Mode Type 1 – Timing Diagram

Flash*Freeze Type 2: Control by Dedicated Flash*Freeze Pin and Internal Logic

The device can be made to enter Flash*Freeze mode by activating the FF pin together with Actel's Flash*Freeze management IP core or user-defined control logic (Figure 4-6) within the FPGA core. This method enables the design to perform important activities before allowing the device to enter Flash*Freeze mode, such as transitioning into a safe state, completing the processing of a critical event. Designers are encouraged to take advantage of Actel's Flash*Freeze Management IP to handle clean entry and exit of Flash*Freeze mode. The device will only enter Flash*Freeze mode when the Flash*Freeze pin is asserted (active low) and the User Low Static ICC (ULSICC) macro input signal, called the LSICC signal, is asserted (high). One condition is not sufficient to enter Flash*Freeze mode type 2; both the FF pin and LSICC signal must be asserted.

Figure 4-7 shows the timing diagram for entering and exiting Flash*Freeze mode type 2. After exiting Flash*Freeze mode type 2 by deasserting the Flash*Freeze pin, the LSICC signal must be deasserted by the user design. This will prevent entering Flash*Freeze mode by asserting the Flash*Freeze pin only. Refer to Table 4-1 on page 33 for Flash*Freeze (FF) pin and LSICC signal assertion and deassertion values.

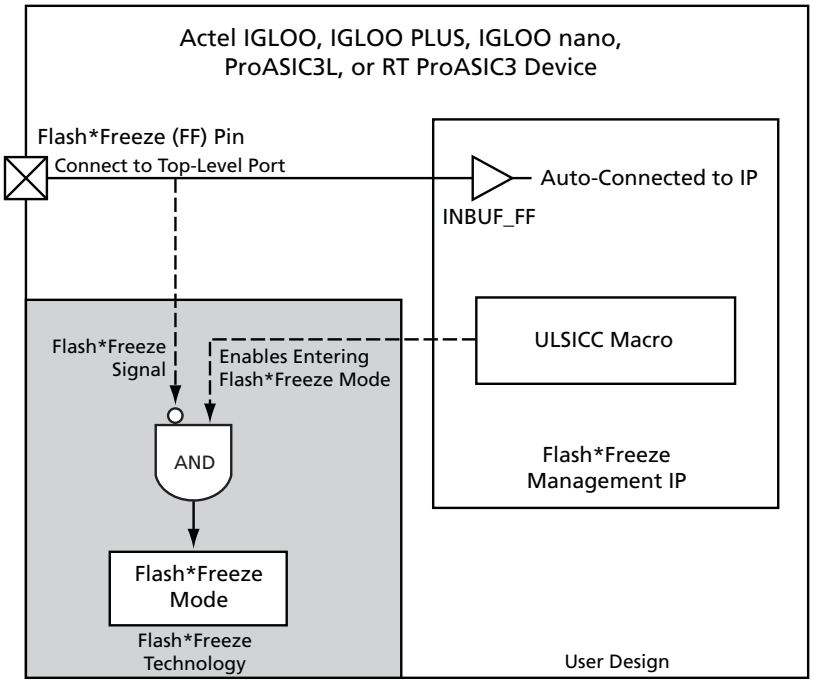


Figure 4-6 · Flash*Freeze Mode Type 2 – Controlled by Flash*Freeze Pin and Internal Logic (LSICC signal)

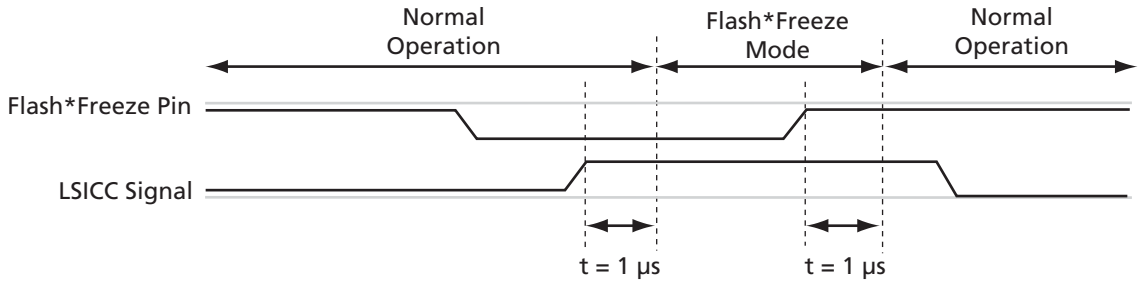


Figure 4-7 · Flash*Freeze Mode Type 2 – Timing Diagram

Table 4-1 · Flash*Freeze Mode Type 1 and Type 2 – Signal Assertion and Deassertion Values

Signal	Assertion Value	Deassertion Value
Flash*Freeze (FF) pin	Low	High
LSICC signal	High	Low

Notes:

1. *The Flash*Freeze (FF) pin is an active-Low signal, and LSICC is an active-High signal.*
2. *The LSICC signal is used only in Flash*Freeze mode type 2.*

IGLOO PLUS I/O State in Flash*Freeze Mode

In IGLOO PLUS devices, users have multiple options in how to configure I/Os during Flash*Freeze mode:

1. Hold the previous state.
2. Set I/O pad to weak pull-up or pull-down.
3. Tristate I/O pads.

The I/O configuration must be configured by the user in the I/O Attribute Editor or in a PDC constraint file, and can be done on a pin-by-pin basis. The output hold feature will hold the output in the last registered state, using the I/O pad weak pull-up or pull-down resistor when the FF pin is asserted. When inputs are configured with the hold feature enabled, the FPGA core side of the input will hold the last valid state of the input pad before the device entered Flash*Freeze mode. The input pad can be driven to any value, configured as tristate, or configured with the weak pull-up or pull-down I/O pad feature during Flash*Freeze mode, without affecting the hold state. If the weak pull-up or pull-down feature is used without the output hold feature, the input and output pads will maintain the configured weak pull-up or pull-down status during Flash*Freeze mode and normal operation. If a fixed weak pull-up or pull-down is defined on an output buffer or as bidirectional in output mode, and a hold state is also defined for the same pin, the pin will be configured in hold state mode during Flash*Freeze mode. During normal operation, the pin will be configured with the predefined weak pull-up or pull-down. Any I/Os that do not use the hold state or I/O pad weak pull-up or pull-down features will be tristated during Flash*Freeze mode and the FPGA core will be driven high by inputs. Inputs that are tristated during Flash*Freeze mode may be left floating without any reliability concern or impact to power consumption.

Table 4-2 shows the I/O pad state based on the configuration and buffer type.

Table 4-2 · IGLOO PLUS Flash*Freeze Mode (type 1 and type 2)—I/O Pad State

Buffer Type	Hold State	I/O Pad Weak Pull-Up/-Down	I/O Pad State in Flash*Freeze Mode
Input	Enabled	Enabled	Weak pull-up/pull-down [1]
	Disabled	Enabled	Weak pull-up/pull-down [2]
	Enabled	Disabled	Tristate [1]
	Disabled	Disabled	Tristate [2]

Notes:

1. *Internal core logic driven by this input buffer will be set to the value this I/O had when entering Flash*Freeze mode.*
2. *Internal core logic driven by this input buffer will be tied High as long as the device is in Flash*Freeze mode.*
3. *For bidirectional buffers: Internal core logic driven by the input portion of the bidirectional buffer will be set to the hold state.*

Table 4-2 · IGLOO PLUS Flash*Freeze Mode (type 1 and type 2)—I/O Pad State (continued)

Buffer Type		Hold State	I/O Pad Weak Pull-Up/-Down	I/O Pad State in Flash*Freeze Mode
Output		Enabled	"Don't care"	Weak pull to hold state
		Disabled	Enabled	Weak pull-up/pull-down
		Disabled	Disabled	Tristate
Bidirectional / Tristate Buffer	E = 0 (input/tristate)	Enabled	Enabled	Weak pull-up/pull-down [1]
		Disabled	Enabled	Weak pull-up/pull-down [2]
		Enabled	Disabled	Tristate [1]
		Disabled	Disabled	Tristate [2]
	E = 1 (output)	Enabled	"Don't care"	Weak pull to hold state [3]
		Disabled	Enabled	Weak pull-up/pull-down
		Disabled	Disabled	Tristate

Notes:

1. *Internal core logic driven by this input buffer will be set to the value this I/O had when entering Flash*Freeze mode.*
2. *Internal core logic driven by this input buffer will be tied High as long as the device is in Flash*Freeze mode.*
3. *For bidirectional buffers: Internal core logic driven by the input portion of the bidirectional buffer will be set to the hold state.*

Flash*Freeze Switch

An F*F switch is provided on the board for designs that utilize the Flash*Freeze technology. Setting the F*F switch to FF_ON will enable the Flash*Freeze mode of the IGLOO PLUS device. Since the Schmitt Trigger chip (U12) is NOT populated on-board for the F*F switch, the Schmitt Trigger feature should be enabled in the FPGA design for the Flash*Freeze input to enhance noise immunity (Figure 4-8). The Schmitt Trigger is an advanced I/O feature of the IGLOO PLUS FPGA family. If the IGLOO PLUS FPGA is swapped out with a device that does not have the advanced Schmitt Trigger I/O feature, the Schmitt Trigger chip (U12) should be populated.

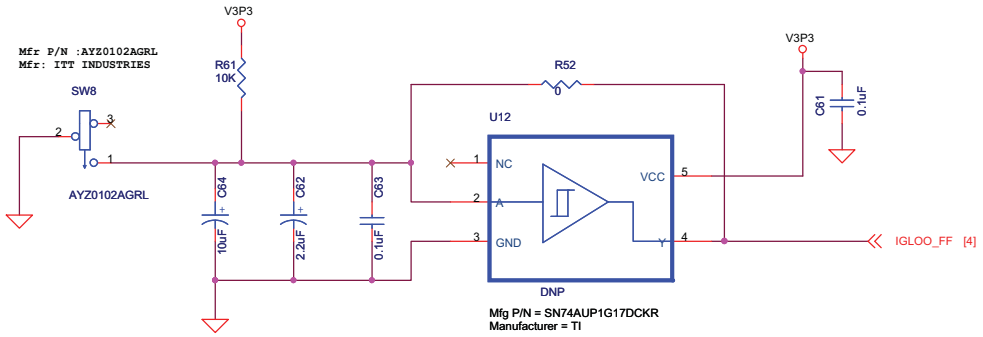


Figure 4-8 · Flash*Freeze Schematic, Schmitt Triggered

Some features on this board are included to demonstrate the Flash*Freeze variants of the IGLOO PLUS FPGA. I/Os can be individually configured to either hold their previous state or be tristated during Flash*Freeze mode. Alternatively, they can be set to a certain state (high or low) using weak pull-up or pull-down I/O attribute configurations. These Flash*Freeze variants can be demonstrated by configuring the I/Os in Designer and using switches as inputs to control the FET LEDs. Refer to the demo design, which provides additional details on demonstrating these Flash*Freeze variants ("IGLOO PLUS Board Demo" on page 51).

Flash*Freeze Variant Dip Switch

Two regular DIP switches are located on the board, next to the FET LEDs (Figure 4-9). The DIP switches can be programmed to help debug or demonstrate the Flash*Freeze variants. Refer to the demo design that demonstrates the Flash*Freeze variants with these switches.

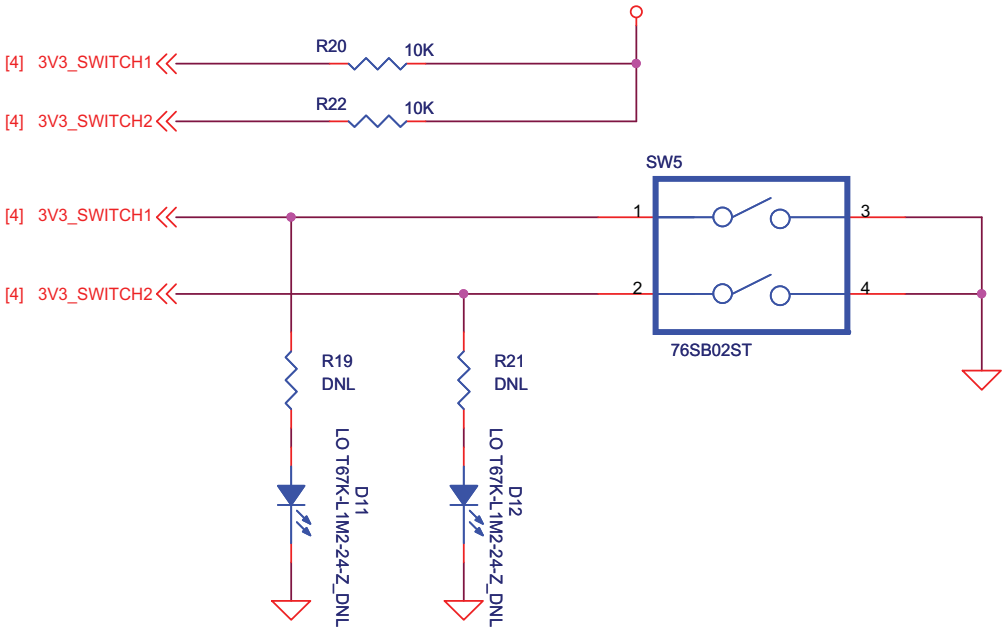


Figure 4-9 · Two I/Os Controlled via DIP Switch Toggling High or Low

Flash*Freeze Variant FET LEDs

These FET LEDs can be used for debugging, such as for viewing the state of I/Os in Flash*Freeze mode. These LEDs can be activated (ON) before entering Flash*Freeze mode, and have the ability to remain activated (ON) in Flash*Freeze mode. In low-power or Flash*Freeze mode, the FET LEDs can continue to function normally. There is one N-Type FET LED and two P-Type FET LEDs on the board (Figure 4-10). Refer to "Demo 4 – Flash*Freeze Variant: Configuration Settings of Demo Design" on page 52, which will help demonstrate the Flash*Freeze variants.

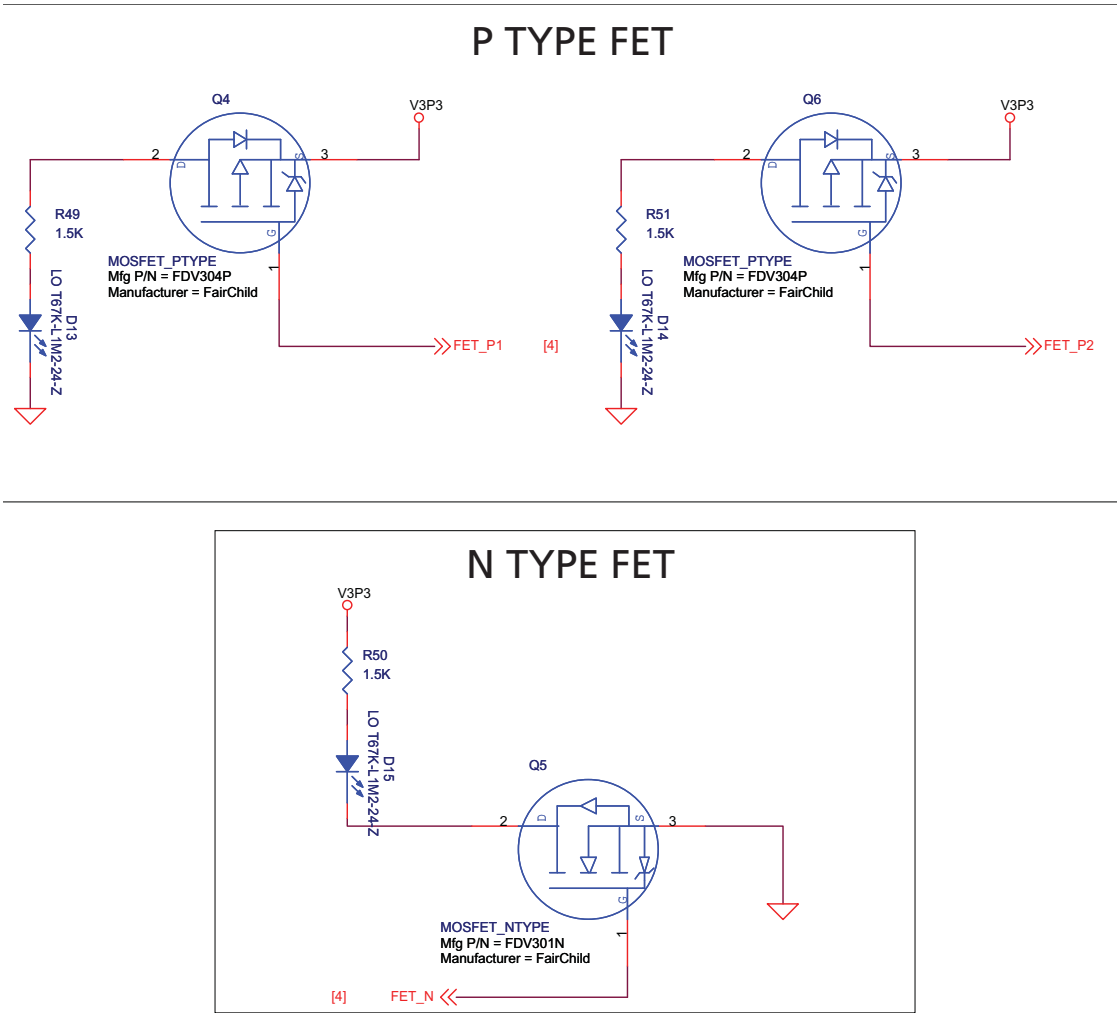


Figure 4-10 · FET LEDs for Debugging

Push-Button Switches

Four active low push-button switches are provided on the board for debug purposes. You can remove the corresponding jumpers to detach or isolate any of the four push-button test switches from the FPGA I/O. Schematics are shown in Figure 4-11 and Figure 4-12.

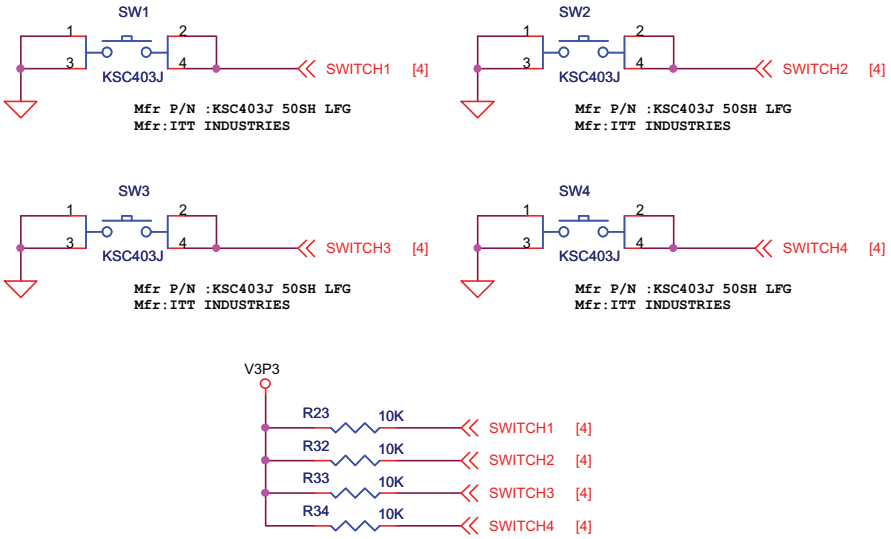


Figure 4-11 · Push-Button Switches Schematic

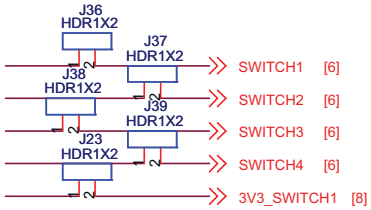


Figure 4-12 · Jumper Header Schematic for Push-Button Switches

DIP Switches

A DIP switch pack (8 switches) is provided on the board (Figure 4-11 and Figure 4-12). You can remove the corresponding jumpers to detach or isolate any of the eight DIP Switches from the FPGA I/Os.

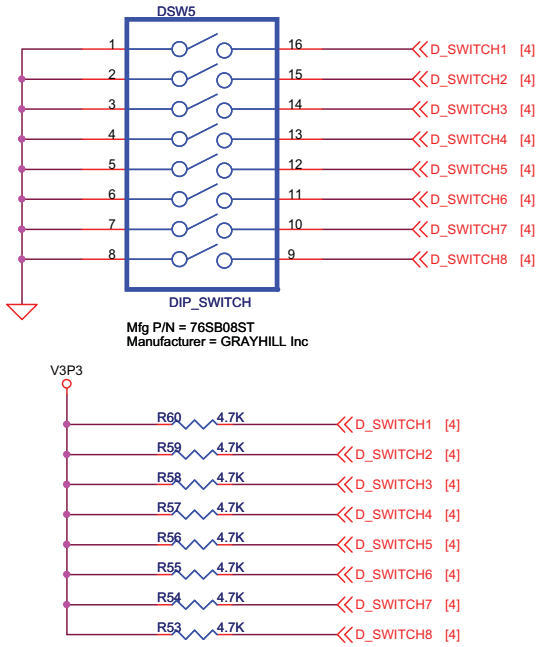


Figure 4-13 · DIP Switches Schematic

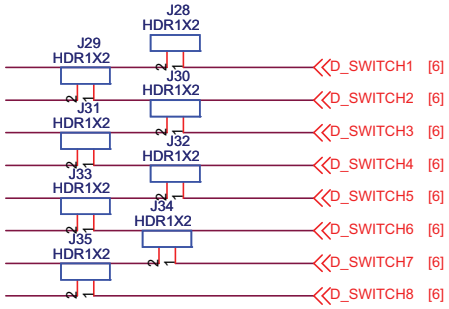


Figure 4-14 · Jumper Header Schematic for DIP Switches

User LEDs

Eight active low debug LEDs are provided on the board (Figure 4-15 and Figure 4-16). You can remove the corresponding jumpers from the 8 × 2 headers to detach or isolate any of the eight LEDs from the FPGA I/Os.

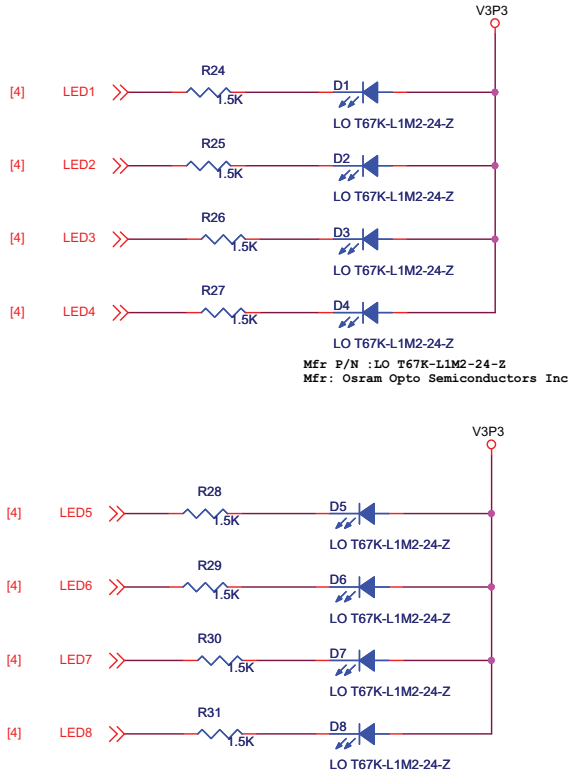


Figure 4-15 · User LEDs Schematic

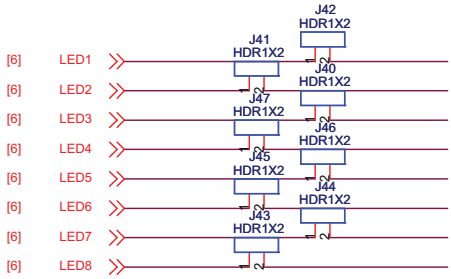


Figure 4-16 · Jumper Header Schematic for User LEDs

I/O Test Pins

All IGLOO PLUS FPGA I/Os are available on headers located on the top and bottom of the device (Figure 4-17 and Figure 4-18). These test pins are multiples of 100 mils apart, so developers can easily attach headers and place an extension card on top with an off-the-shelf breadboard for a low-cost solution for integration. In order to use I/Os assigned to the LEDs, DIP Switches, and push-button switches, the 2-pin jumper on their path must be removed first to disconnect the assignment.

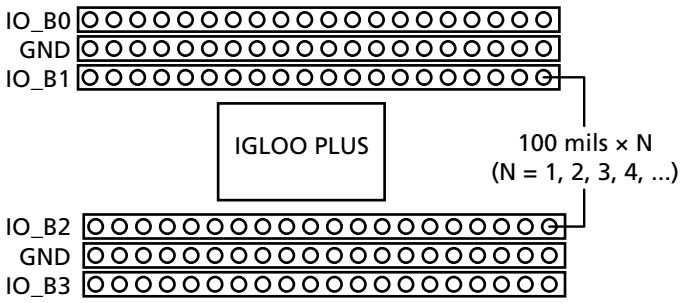


Figure 4-17 · I/O Test Pins

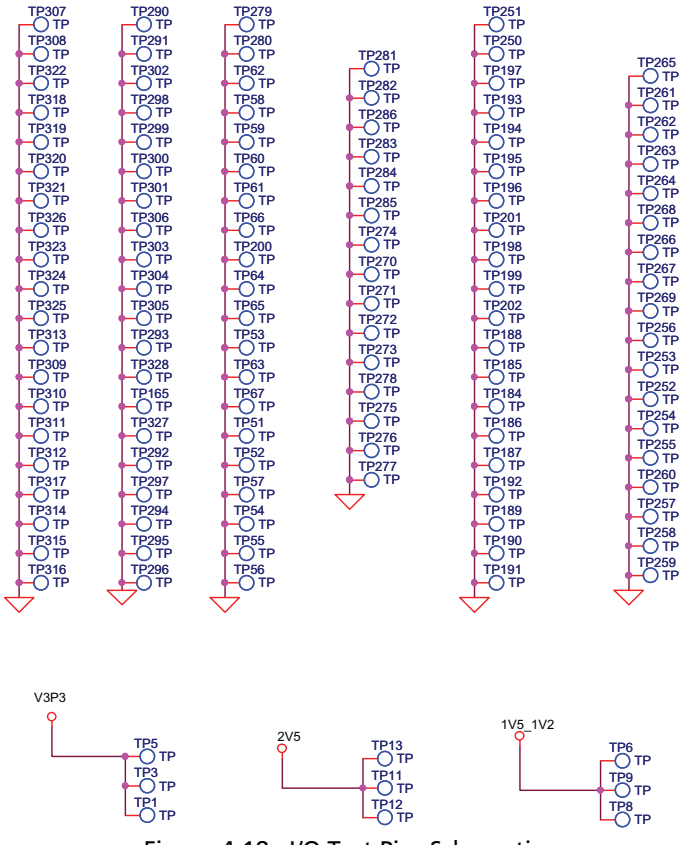


Figure 4-18 · I/O Test Pins Schematic

OLED

A 96 × 16 pixel low-power blue organic light emitting diode (OLED) is available on the board above the IGLOO PLUS FPGA (Figure 4-19). The OLED features a serial I2C interface, and is capable of displaying sharp images or text. The demo design included in this kit contains a roulette game that uses the OLED for display and the push-button switch for game control.

Additional OLED info is available at the IGLOO PLUS Starter Kit website page:

http://www.actel.com/products/hardware/devkits_boards/iglooplus_starter.aspx.

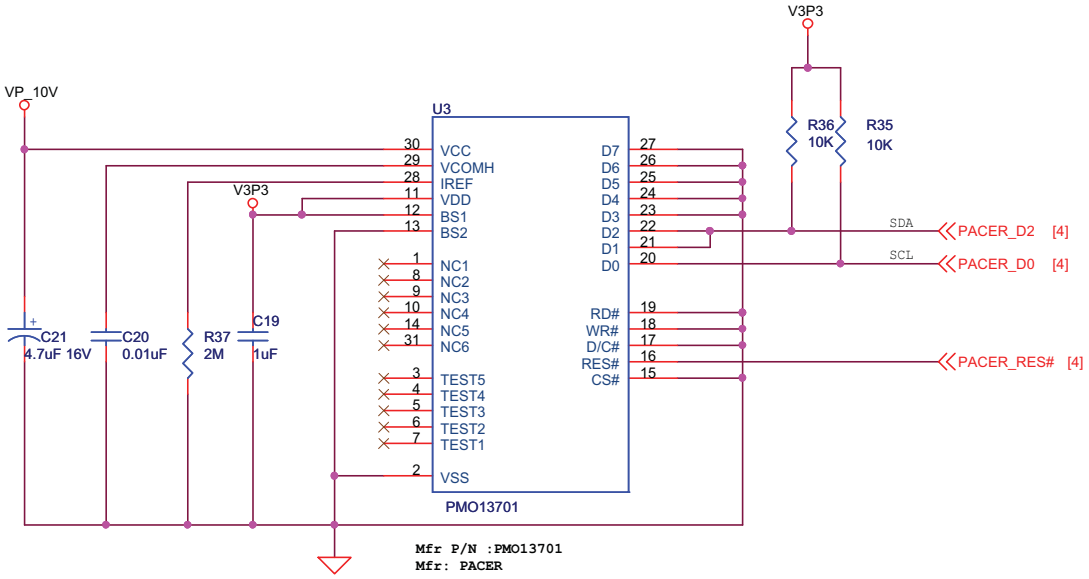


Figure 4-19 · OLED Display Schematic

Interface Connector

A standard interface connector on the board can be used to connect additional daughter cards, some of which are developed by partners and third party vendors (Figure 4-20). The interface possibilities are numerous, such as flash and SRAM memory interfaces, keyboard interfaces for embedded applications, LCD interfaces, and motor control interfaces. GPIOA_1, GPIOA_2, GPIOA_4, and GPIOA_31 pins can be used for critical signals, such as clock and reset, because proper series termination has been provided on these signal lines.

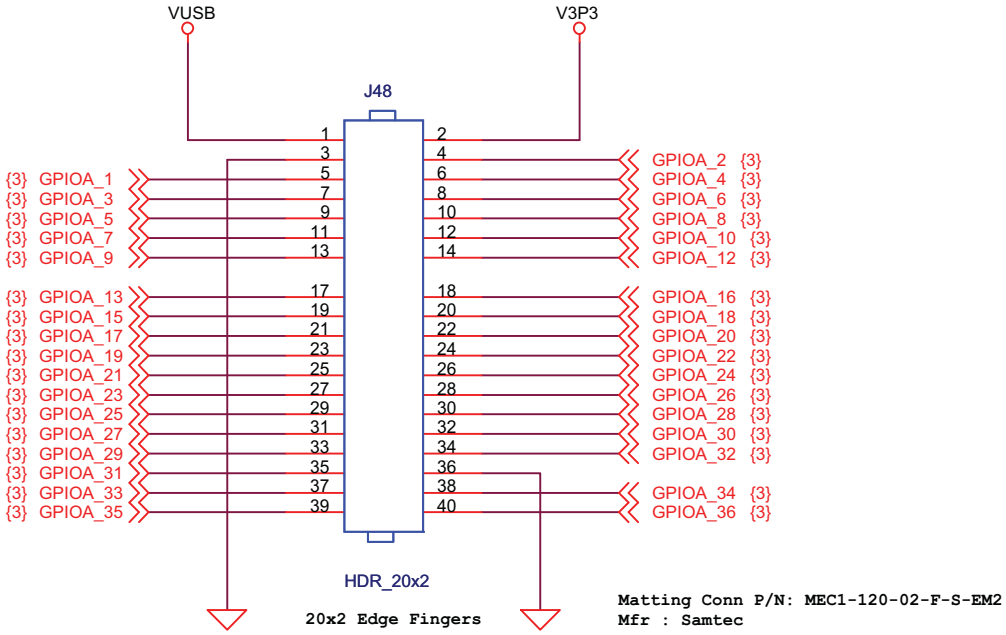


Figure 4-20 · Interface Connector Schematic

USB-to-UART Interface

Included on the starter kit board is a USB-to-UART interface with ESD protection. This interface includes an integrated USB-to-UART bridge controller to provide a standard UART connection with the IGLOO PLUS FPGA. Any standard UART controller can be implemented in the IGLOO PLUS FPGA to allow access with this interface. In addition, Actel IP catalog includes various UART controllers, specifically CoreUART, which can be instantiated in the FPGA design with an embedded processor. CoreUART controller supports both asynchronous and synchronous modes with configurable parameters for various applications.

One application of the USB-to-UART interface is to allow for Hyper-terminal on a PC to communicate with the IGLOO PLUS FPGA. HyperTerminal is a serial communications application program that can be installed in the Windows® operating system. A basic HyperTerminal program is usually distributed with Windows. With an USB driver properly installed, and correct COM port and communication settings selected, you can use the HyperTerminal program to communicate with a design running in the IGLOO PLUS FPGA device.

Information on the USB-to-UART bridge datasheet and device drivers are available at the IGLOO PLUS Starter Kit website page: http://www.actel.com/products/hardware/devkits_boards/iglooplus_starter.aspx.

The USB-to-UART schematic is shown in Figure 4-21.

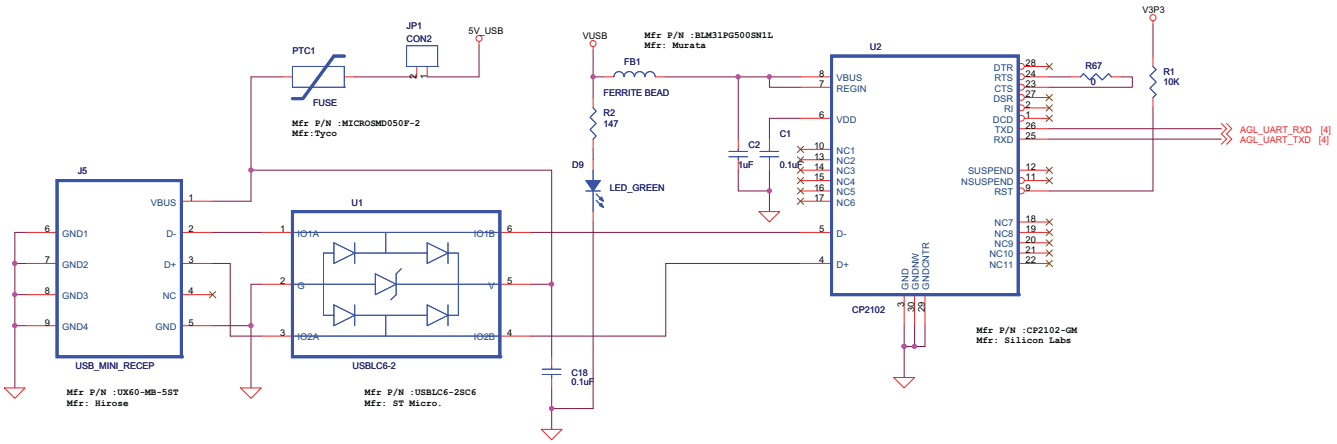


Figure 4-21 · USB-to-UART Interface Schematic

SPI Flash

One 2 Mbyte SPI flash is available on the board and can be used by CoreABC-type applications for access of additional memory. The flash interface, serial peripheral interface bus (SPI), is a synchronous serial data link standard that is used to access the flash memory. Some advantages of the SPI interface are full duplex communication and higher throughput than I2C. In the schematics shown in Figure 4-22, either the Winbond or Atmel 2 Mbyte SPI flash will be populated on-board.

Winbond and Atmel SPI flash datasheets are available at the IGLOO PLUS Starter Kit website page:

http://www.actel.com/products/hardware/devkits_boards/iglooplus_starter.aspx.

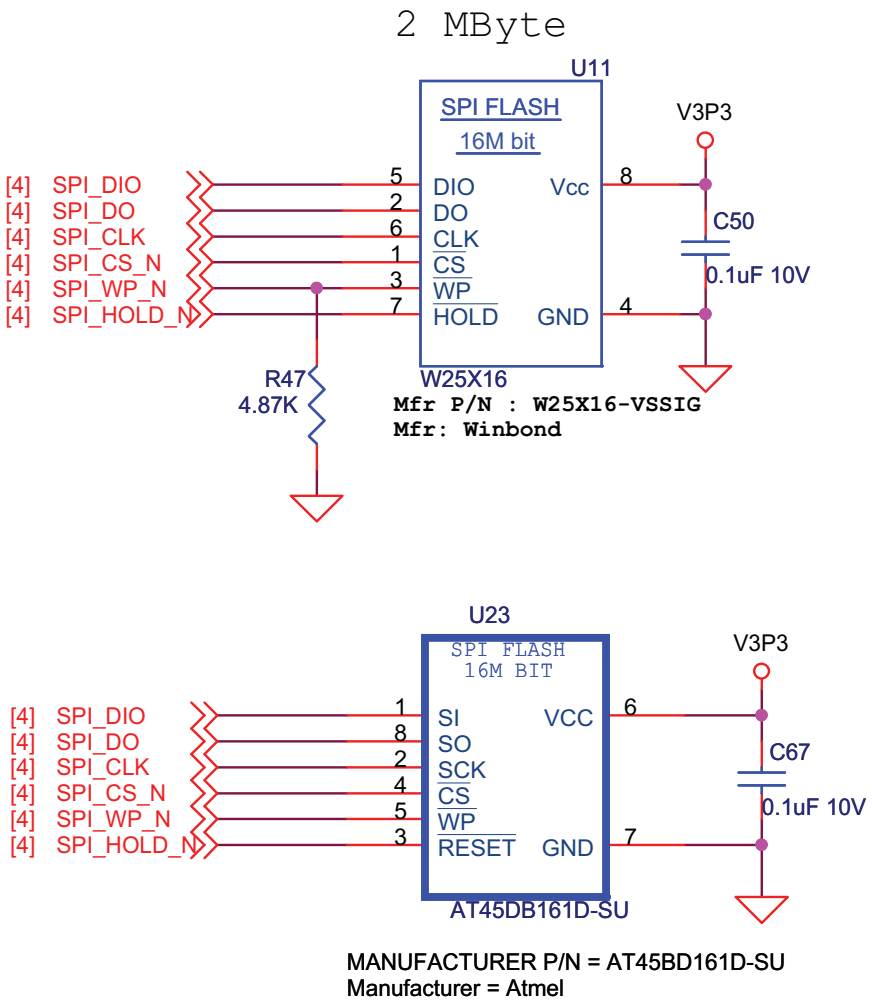


Figure 4-22 · SPI Flash Schematics

Note: Either the Winbond or Atmel SPI flash will be populated on the board.

Low-Cost Programming Stick (LCPS)

Interface

The development board can be programmed by the low-cost programming stick (LCPS) or via a 10-pin FP3 header (Figure 4-24). Regardless of the programming dongle used, IGLOO PLUS is programmed the same way as IGLOO nano, ProASIC3, and Fusion FPGA devices.The LCPS is a special version for the FlashPro3 programming circuitry that is compatible with FlashPro3 and the generic FlashPro programming software. The LCPS, like the IGLOO PLUS board, is RoHS-compliant and is completely lead (Pb) free. To use the LCPS with the FlashPro software, all you need to do is to select the FlashPro3 from the list of programmer types. The LCPS behaves exactly as if it were a regular encased FlashPro3 programmer. The 12-pin female connector socket is designed to interface to the 12-pin right-angle male header on the IGLOO PLUS kit. One of the pins is a special VJTAGENB signal that goes high when programming is taking place and returns to a low level when programming has completed. This signal is connected to the FET on the 1.5 V regulator circuit. The IGLOO PLUS board uses this signal to effect a change in the value of V_{CC} from 1.2 V to 1.5 V, which is required for programming all IGLOO PLUS devices.

You do not need to have the LCPS connected to the IGLOO PLUS board to operate it, after the FPGA has been programmed. The LCPS must be connected to the Actel IGLOO PLUS board only when programming the AGLP125-CSG289.

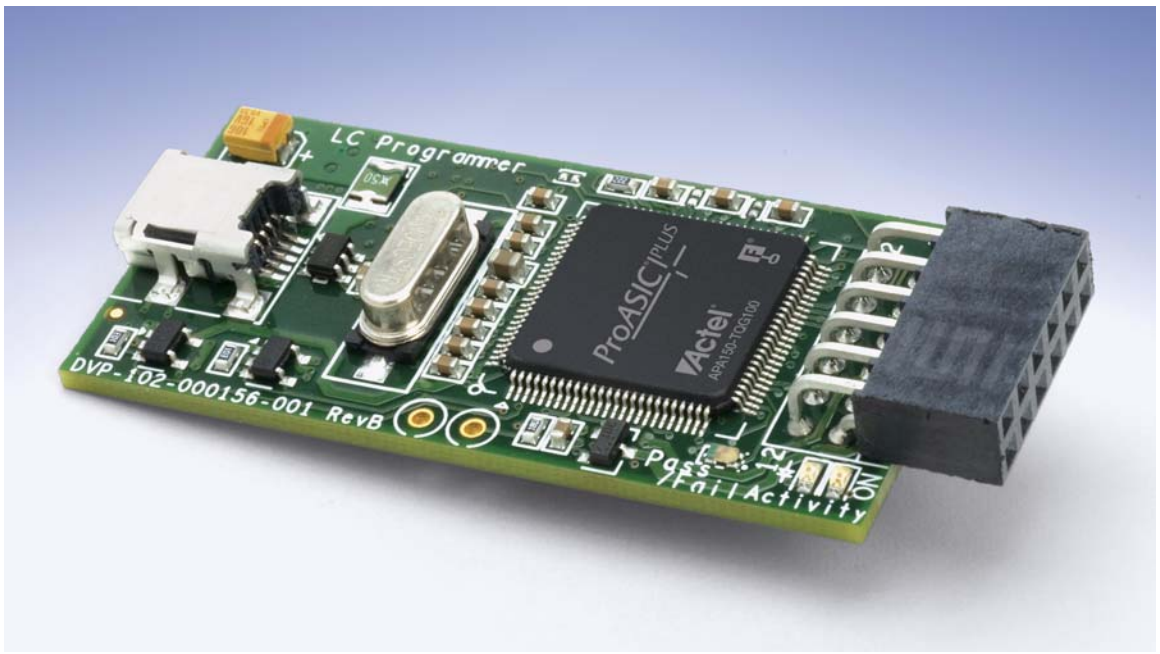


Figure 4-23 · Low-Cost Programming Stick (LCPS)

Note: The LCPS supplied with this kit is intended for use with the IGLOO PLUS Starter Kit. An LCPS supplied for other kits, although electrically and functionally equivalent, may not connect seamlessly with the IGLOO PLUS Starter Kit board.

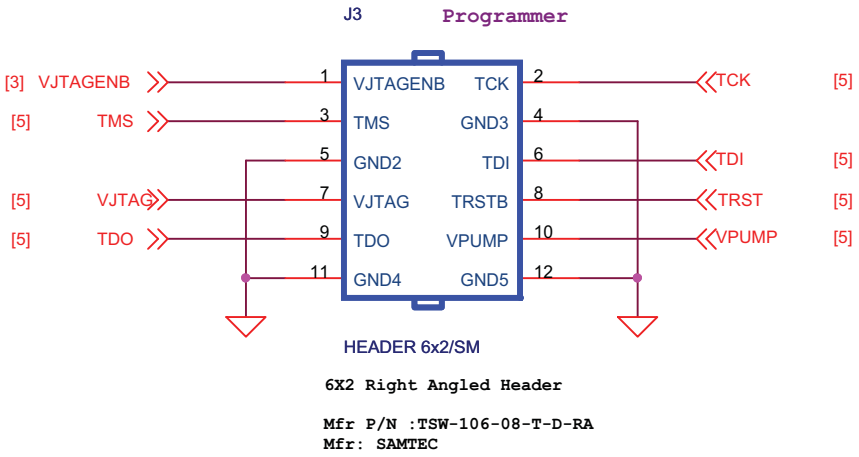


Figure 4-24 · FPGA Programming Headers Schematic

LCPS Stackup

The LCPS is built on a four-layer PCB with the layers arranged in the following stackup:

1. Top signal layer (Figure 4)
2. Ground plane
3. Power plane
4. Bottom signal layer (Figure 4-26 on page 48)

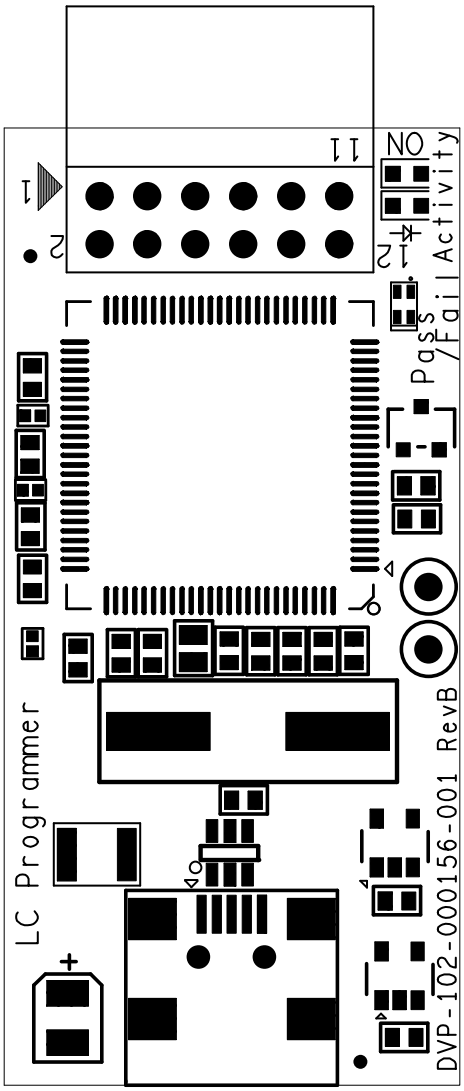


Figure 4-25 · Low-Cost Programming Stick – Top Silkscreen

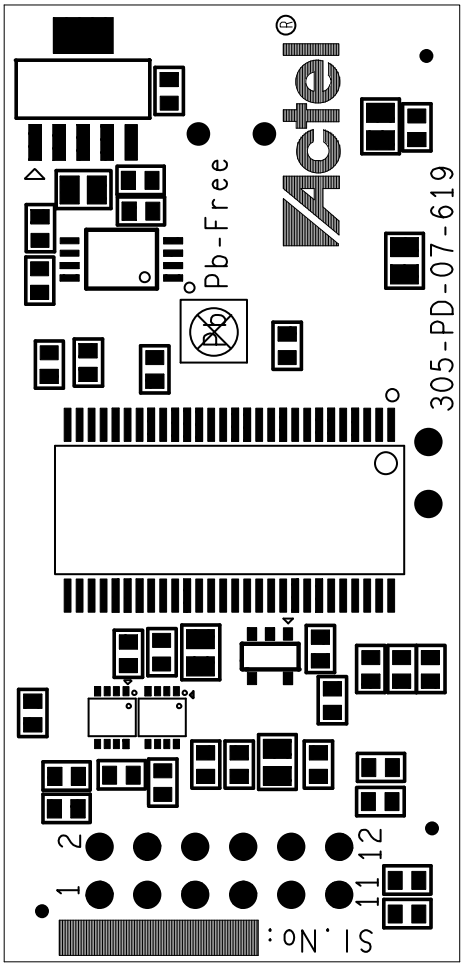


Figure 4-26 · Low-Cost Programming Stick – Bottom Silkscreen

Programming

To program a design into the IGLOO PLUS evaluation board:

1. To program a design into the IGLOO PLUS evaluation board, attach the LCPS board to the IGLOO PLUS evaluation board.
2. Attach a USB cable to the LCPS. This allows a programming data file, in programming database format (*.pdb) or STAPL format (*.stp), to be downloaded via the FlashPro software to the Actel IGLOO PLUS device fitted to the board.
3. A separate USB connection is required for the IGLOO PLUS Board if no other power source (power brick) is attached to the IGLOO PLUS board.
4. When using the FlashPro software, the programmer to select is the FlashPro3. The LCPS is functionally equivalent to a FlashPro programmer but designed specifically for use with the IGLOO PLUS Starter Kit.
5. Alternatively, an option (10-pin FP3 header) is provided to program the FPGA with a FlashPro3 instead (Figure 5-1).

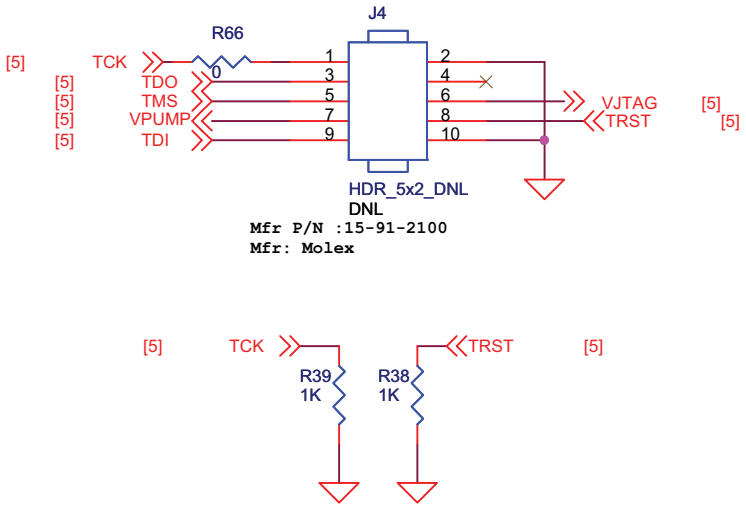


Figure 5-1 · Schematic of JTAG header for Programming Directly with a FlashPro3

6 IGLOO PLUS Board Demo

The IGLOO PLUS FPGA is pre-programmed with a simple demo to quickly get you started. This demo design will provide a quick overview as well as a quick check of this board.

Demos Included in the Starter Kit

There are a few demos included in this starter kit, such as a binary counter to light up the 8 user LEDs. These 8 LEDs retain their count value in Flash*Freeze mode and restart counting from that value after exiting Flash*Freeze mode. During Flash*Freeze mode, the active LEDs will be weakly ON, since they are driven by the weak hold state resistors. Flash*Freeze variants can be demonstrated using the F*F switches and FET LEDs.

The IGLOO PLUS demo design RTL and design files are available at the IGLOO PLUS Starter Kit website page: http://www.actel.com/products/hardware/devkits_boards/iglooplus_starter.aspx. Refer to the *Quick Start Guide* available on the website to run the demo.

Powering Up the Board

1. Before running the demos, refer to Table 1-1 on page 11 to check the default jumper and board settings.
2. The board is powered from the USB connection and no external power supply is required.
   - A 5 V wall-jack connector could be used when USB cable is not available.
   - The board does not switch seamlessly between the power brick and USB, so the power source 4-pin header and jumper must be used to select the desired power source.
3. Once the USB cable is attached securely, verify the green LED next to the USB jack is ON.

Getting Started with the IGLOO PLUS Starter Kit Demo Design

Demo 1 – IGLOO PLUS Counter

1. Before starting Demo 1, check the jumper settings and set all switches to the OFF or CLOSE position. Ensure the F*F switch is in the OFF position.
2. Power-on the IGLOO PLUS Starter Kit board using the power supply or USB cable included in the starter kit.
3. Press and release the System Reset button to reset the IGLOO PLUS FPGA.
4. Observe that LED D1 is ON during Reset.
5. The LEDs D[3:8] represent a binary counter which counts up from 000000 to 111111 and loops back. After reset, LEDs D[3:8] should restart counting from zero.

Table 6-1 · LED[8:1]

LED	Description
LED D1	On during reset
LED D2	On when any push-button is pressed or DIP switch is in the open position
LED D3	Binary Counter[5]
LED D4	Binary Counter[4]
LED D5	Binary Counter[3]
LED D6	Binary Counter[2]
LED D7	Binary Counter[1]
LED D8	Binary Counter[0]

Demo 2 – OLED Interface Demonstration

This demo includes a simple Roulette game provided by Avnet Memec that demonstrates control and operation of the OLED display.

1. Press SW1 to begin a bet and press SW1 again to stop at the number you want to bet on.
2. Once you have selected your number, press SW2 to spin. Your results will display in the OLED.
3. Continue with steps 1 and 2 to bet and play again.

Demo 3 – Simple Flash*Freeze Demonstration

This demo demonstrates the IGLOO PLUS FPGA's ability to save power while holding internal logic state during Flash*Freeze mode.

1. Enter Flash*Freeze mode by switching the F*F switch to ON.
   - In Flash*Freeze mode, observe the LEDs D[1:8] retain the last state they were driven to when Flash*Freeze mode was asserted. They may be weakly ON, since they are driven by the weak hold state resistors.
   - The OLED will remain on, since it is self-powered.
   - See Demo 4 below for the settings and states of LEDs D[13:15] during Flash*Freeze mode.
2. Exit Flash*Freeze mode by switching the F*F switch to OFF.
   - After exiting Flash*Freeze mode, LEDs D[3:8] resume counting from the count value prior to entering Flash*Freeze mode.
3. To measure power of the FPGA core during and after Flash*Freeze mode, simply remove jumper J12 and use a multimeter capable of reading µA current across J12.

Demo 4 – Flash*Freeze Variant: Configuration Settings of Demo Design

One feature of the IGLOO PLUS FPGA family is the ability to hold input and output states during Flash*Freeze mode. This demonstration will showcase this feature by displaying the result of various input and output hold configurations.

In this portion of the design, two inputs named FET Switch 1 and FET Switch 2 are used to drive different logic values into the FPGA. FET Switch 1 directly drives FET LED D13 and FET Switch 2 directly drives FET LED D14 and FET LED D15. FET switches are used on this board to provide the required current to drive the LEDs when the FPGA is in Flash*Freeze mode. FETs are not required to enter Flash*Freeze mode or to take advantage of the I/O hold state feature. The FPGA configurations of the inputs and outputs of this circuit are described in Table 6-2 and Table 6-3 on page 53.

Table 6-2 · FET Input Configuration in Demo Design

Name	I/O Hold	Internal Weak Resister Pull	Description
FET Switch 1	Enabled	Down	Drives FET LED D13 directly
FET Switch 2	Disabled	Down	Drives FET LED D14 and D15 directly

When HOLD is disabled at the output buffer, the output will depend on the resister pull-up or pull-down direction in Flash*Freeze mode. If HOLD is enabled at the output buffer, then the output will depend on the state right before entering Flash*Freeze mode.

Table 6-3 · FET Output Configuration in Demo Design

FET LED	I/O Hold	Internal Weak Resister Pull	Description
FET LED D13	Enabled	Down	P-Type
FET LED D14	Disabled	Down	P-Type
FET LED D15	Disabled	Up	N-Type

1. Similar to Demo 1, before starting Demo 4, check the jumper settings and set all switches to the OFF or CLOSED position. Ensure the F*F switch is in the OFF position.
2. Power-on the IGLOO PLUS Starter Kit board using the power supply or USB cable included in the starter kit.
3. Press and release the System Reset button (SW7) to reset the IGLOO PLUS FPGA.
   - Observe that LED D1 is ON during Reset.
4. Example A: Set both FET Switches [2:1] to the CLOSE position.
   - Based on the logic in this demo design, both P-Type FET LEDs D13 and D14 should be ON and N-Type FET LED D15 should be OFF. Refer to the board schematic for reference on the FET LED connections.
   - Enable Flash*Freeze mode by setting the F*F Switch to ON.

     After entering Flash*Freeze mode, observe that P-Type FET LED D13 stays ON because the HOLD state for this output configuration was enabled.

     Also observe that P-Type FET LED D14 is ON due to the pull-down resister configuration.

     N-Type FET LED D15 turns ON due to the pull-up resister configuration.

     Toggle the FET Switches back and forth.

     Observe that the LEDs are unaffected, because the device is in Flash*Freeze mode. The inputs are not able to pass data into the device.

     Return the FET Switches [2:1] back to the CLOSE position
   - Disable Flash*Freeze mode by setting the F*F Switch to OFF.

     After exiting the Flash*Freeze mode, observe that N-Type FET LED D15 turns OFF.
5. Example B: Set both FET Switches [2:1] to the OPEN position
   - Based on the logic in this demo design, both P-type FET LEDs D13 and D14 should be OFF and N-type FET LED D15 should be ON.
   - Enable Flash*Freeze mode by setting the F*F Switch to ON.

     After entering Flash*Freeze mode, observe that P-Type FET LED D13 remains OFF because the HOLD state for this output configuration was enabled.

     Also observe that P-Type FET LED D14 turns ON due to the pull-down resister configuration.

     N-Type FET LED D15 is ON due to the pull-up resister configuration.
   - Disable Flash*Freeze mode by setting the F*F to OFF.

     After exiting the Flash*Freeze mode, observe that P-Type FET LED D14 turns OFF.

The FET Truth Table (Table 6-4) shows the Flash*Freeze variants based on the FET I/O HOLD and resister pull configured for this demo design. For the output FET LEDs, NORMAL represents the LED state before entering and after exiting Flash*Freeze mode, while F*F Mode represents the LED state during Flash*Freeze mode.

Table 6-4 · FET Truth Table

Input		Output					
FET Switch 1	FET Switch 2	P-Type FET LED D13 (active low): HOLD		P-Type FET LED D14 (active low): Pull-down		N-Type FET LED D15 (active high): Pull-up	
		NORMAL	F*F Mode	Normal	F*F Mode	Normal	F*F Mode
CLOSE (0)	CLOSE (0)	ON (0)	ON (0)	ON (0)	ON (0)	OFF (0)	ON (1)
CLOSE (0)	OPEN (1)	ON (0)	ON (0)	OFF (1)	ON (0)	ON (1)	ON (1)
OPEN (1)	CLOSE (0)	OFF (1)	OFF (1)	ON (0)	ON (0)	OFF (0)	ON (1)
OPEN (1)	OPEN (1)	OFF (1)	OFF (1)	OFF (1)	ON (0)	ON (1)	ON (1)

Resources

IGLOO PLUS Starter Kit

http://www.actel.com/products/hardware/devkits_boards/iglooplus_starter.aspx

IGLOO PLUS Overview

http://www.actel.com/products/iglooplus/default.aspx

IGLOO PLUS Datasheet

http://www.actel.com/documents/IGLOOPLUS_DS.pdf

IGLOO PLUS FPGA Fabric User's Guide

http://www.actel.com/documents/IGLOOPLUS_UG.pdf

Libero IDE Design Software

http://www.actel.com/products/software/libero/default.aspx

B

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From Northwest U.S.A., call **650.318.4434**
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From Europe, call **650.318.4252** or **+44 (0) 1276 401 500**
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You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email

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The technical support email address is tech@actel.com.

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