Title	***Reference Design Report for a 30 W Supply Using TOPSwitch®-JX TOP266VG***
Specification	85 VAC – 264 VAC Input; 12 V, 2.5 A Output
Application	General Purpose
Author	Applications Engineering Department
Document Number	RDR-242
Date	March 1, 2010
Revision	1.2

Summary and Features

- Highly energy efficient
  - Very low no-load input power: < 80 mW at 230 VAC
  - Full load efficiency >84% at 115 VAC / 47 Hz
  - Efficiency >80% above 8% load
  - Average efficiency >84% (25%, 50%, 75%, 100% load points)
  - Simplifies meeting ENERGY STAR 2.0, 80 Plus and EuP requirements
  - 725 V MOSFET rating allowed high turns ratio (V_{OR}) and use of 60 V Schottky output diode
- Low cost, low component count and small PCB footprint solution
  - 132 kHz operation optimizes core size and efficiency performance
  - Low-profile eDIP™ package with no external heatsink
- Integrated Protection and Reliability Features
  - Line undervoltage lock out (UVLO) and line overvoltage shutdown prevents output glitching and improves reliability
  - Primary sensed output overvoltage shutdown (OVP) eliminates second optocoupler
  - Auto recovery output over current (OCP) and short circuit protection
  - Flat overload power with line voltage
  - Meets limited power source (LPS) <100 VA requirement with a single point of failure
  - Accurate thermal shutdown with large hysteresis

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This engineering report describes a power supply employing the Power Integrations® TOPSwitch®-JX TOP266VG. This power supply operates over a universal input range and provides a 12 V, 30 W output. It has been designed and tested to operate open frame with an ambient temperature environment of up to 40 °C.

The TOPSwitch-JX, by design, maintains virtually constant efficiency across a very wide load range without using special operating modes to meet specific load thresholds. This optimizes performance for existing and emerging energy-efficiency regulations. Maintaining constant efficiency ensures design optimization for future energy-efficiency regulation changes without the need for redesign.

The low MOSFET capacitance of TOPSwitch-JX allows a higher switching frequency without the efficiency penalty which occurs with standard discrete MOSFET. The 132 kHz switching frequency (rather than the 70 kHz to 100 kHz frequency used for a discrete MOSFET) reduces the transformer size required, and so reduces cost.

This power supply offers the following protection features:

- Output OVP (including open loop) with latching shutdown
- Auto-recovery type overload protection

This document provides complete design details including specifications, the schematic, bill of materials, and transformer design and construction information. This information includes performance results pertaining to regulation, efficiency, standby, transient load, power-limit data, and conducted EMI scans.

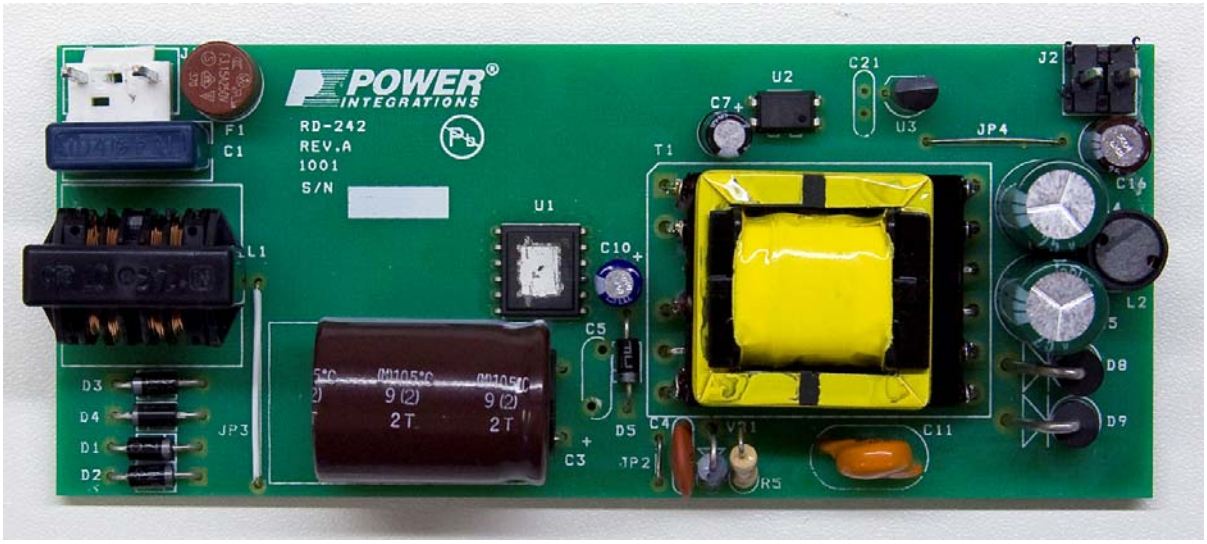

Figure 1 – Populated Circuit Board Photograph, Component Side.

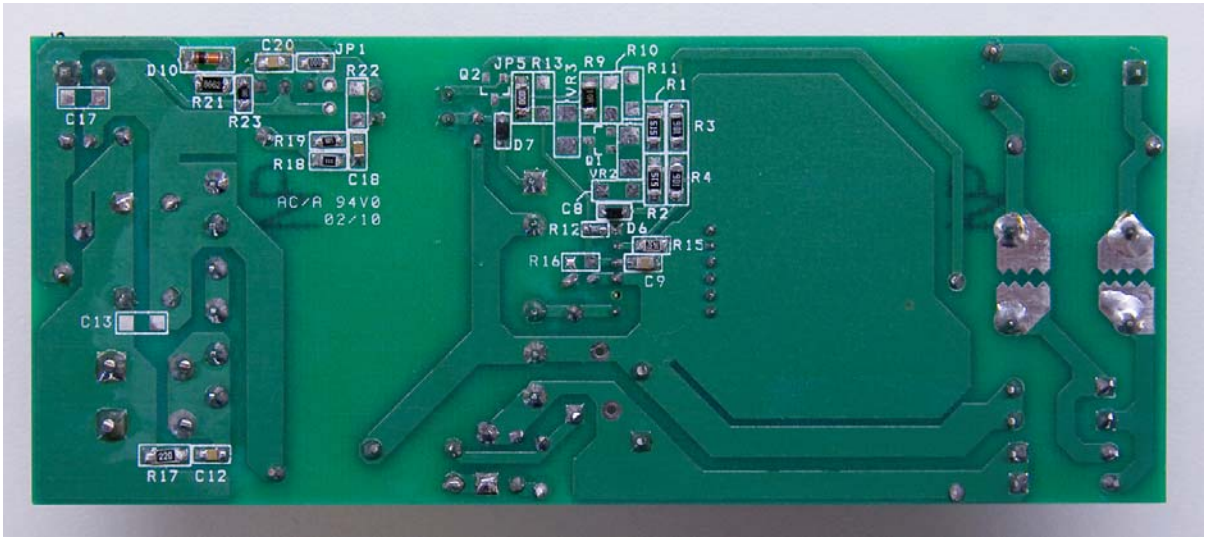

Figure 2 – Populated Circuit Board Photograph, Solder Side.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		264	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	63	Hz	
No-load Input Power (230 VAC)				0.08	W	
Output						
Output Voltage	V_{OUT}	11.4	12	12.6	V	
Output Ripple Voltage	V_{RIPPLE}			120	mV	20 MHz bandwidth
Output Current	I_{OUT}	0		2.5	A	
Total Output Power						
Continuous Output Power	P_{OUT}		30		W	
LPS	P_{OUT_PEAK}			100	W	To meet LPS safety requirement
Efficiency						
Full Load	η	80			%	Measured at P_{OUT} 25 °C, 90 VAC / 60Hz
Required average efficiency at 25, 50, 75 and 100 % of P_{OUT}	$\eta_{ES2.0}$	83			%	Per ENERGY STAR V2.0
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC950 / UL1950 Class II				
Line Surge						1.2/50 μs surge, IEC 1000-4-5, Series Impedance:
Differential Mode (L1-L2)				1	kV	Differential Mode: 2 Ω
Common Mode (L1/L2-PE)				2	kV	Common Mode: 12 Ω
Ambient Temperature	T_{AMB}	0		40	°C	Free convection, sea level

3 Schematic

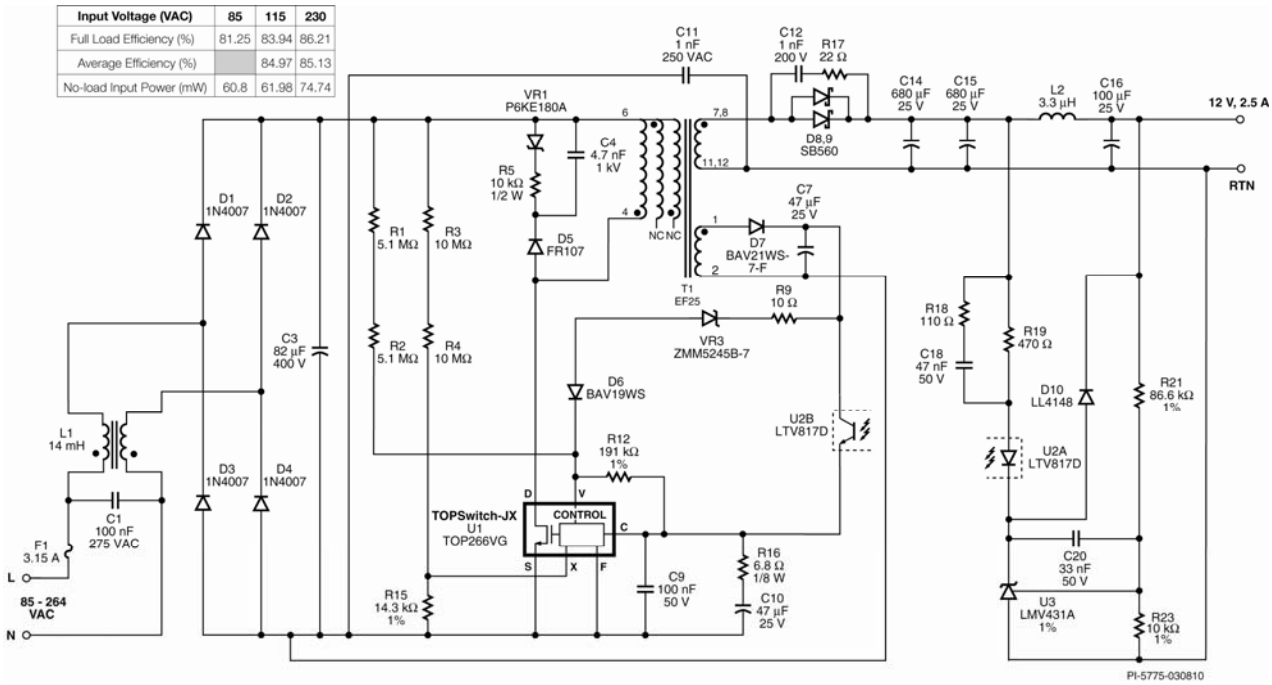

Figure 3 – Schematic.

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4 Circuit Description

This power supply employs a TOP266VG off-line switcher, (U1), in a flyback configuration. IC U1 has an integrated 725 V MOSFET and a multi-mode controller. It regulates the output by adjusting the MOSFET duty cycle, based on the current fed into its CONTROL (C) pin.

4.1 Key Design Decisions

The goals of the design were highest full load efficiency, average efficiency (average of 25%, 50%, 75% and 100% load points) and very low no-load consumption.

Additional requirements included latching output overvoltage shutdown and compliance to safety agency limited power source (LPS) limits. Actual efficiency and no-load performance easily exceeded current energy efficiency requirements.

In order to meet these design goals the following key design decisions were made.

4.1.1 PI part selection

• Ambient of 40 °C allowed one device size smaller than indicated by the power table.

The device selected for this design was based on the 85-265 VAC, Open Frame, PCB heatsinking column of the datasheet power table (Table 1). One device size smaller was selected (TOP266V vs TOP267V) due to the ambient specification of 40 °C (vs. the 50°C assumed in the power table) and the optimum PCB area and layout for the device heatsink. The subsequent thermal and efficiency data confirmed this choice. The maximum device temperature was 107 °C at full load, 40 °C, 85 VAC, 47 Hz (worst case conditions) and average efficiency exceeded 83% ENERGY STAR and EuP Tier 2 requirements.

4.1.2 Transformer Core Selection

• 132 kHz switching frequency allowed the selection of smaller core for lower cost.

The size of the magnetic core is a function of the switching frequency. The choice of the higher switching frequency of 132 kHz allowed for the use of a smaller core size. The higher switching frequency does not negatively impact the efficiency in TOPSwitch-JX designs due its small drain to source capacitance (C_{OSS}) as compared to that of discrete MOSFETs.

4.1.3 Line Sense Resistor Values

• Increasing line sensing resistance from 4 MΩ to 10.2 MΩ to reduce no-load input power dissipation by 16 mW

Line sensing is provided by resistors R1 and R2 and sets the line undervoltage and overvoltage thresholds. The combined value of these resistors was increased from the standard 4 MΩ to 10.2 MΩ. This reduced the resistor, and therefore contribution to no-

load input power, from ~26 mW to ~10 mW. To compensate the resultant change in the UV threshold resistor R12 was added between the CONTROL and VOLTAGE-MONITOR pins. This adds a DC current equal to ~16 mA into the V pin, requiring only 9 μA to be provided via R1 and R2 to reach the V pin UV threshold current of 25 μA and setting the UV threshold to approximately 95 VDC.

This technique does effectively disable the line OV feature as the resultant OV threshold is raised from ~450 VDC to ~980 VDC. However in this design there was no impact as the value of input capacitance (C3) was sufficient to allow the design to withstand differential line surges greater than 1 kV without the peak drain voltage reaching the BV_{DSS} rating of U1.

Specific guidelines and detailed calculations for the value of R12 may be found in the TOPSwitch-JX Application Note AN-47.

4.1.4 Clamp Configuration – RZCD vs RCD

• An RZCD (Zener bleed) was selected over RCD to give higher light load efficiency and lower no-load consumption

The clamp network is formed by VR1, C4, R5 and D5. It limits the peak drain voltage spike caused by leakage inductance to below the BV_{DSS} rating of the internal TOPSwitch-JX MOSFET. This arrangement was selected over a standard RCD clamp to improve light load efficiency and no-load input power.

In a standard RCD clamp C4 would be discharged by a parallel resistor rather than a resistor and series Zener. In an RCD clamp the resistor value of R5 is selected to limit the peak drain voltage under full load and over-load conditions. However under light or no-load conditions this resistor value now causes the capacitor voltage to discharge significantly as both the leakage inductance energy and switching frequency are lower. As the capacitor has to be recharged to above the reflected output voltage each switching cycle the lower capacitor voltage represents wasted energy. It has the effect of making the clamp dissipation appear as a significant load just as if it were connected to the output of the power supply.

The RZCD arrangement solves this problem by preventing the voltage across the capacitor discharging below a minimum value (defined by the voltage rating of VR1) and therefore minimizing clamp dissipation under light and no-load conditions. Zener VR1 is shown as a high peak dissipation capable TVS however a standard lower cost Zener may also be used due to the low peak current that component experiences.

In many designs a resistor value of less than 50 Ω may be used in series with C4 to damp out high frequency ringing and improve EMI but this was not necessary in this case.

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4.1.5 Feedback Configuration

- A high CTR optocoupler was used to reduce secondary bias currents and no-load input power
- Low voltage, low current voltage reference IC used on secondary side to reduce secondary side feedback current and no-load input power.
- Bias winding voltage tuned to ~9 V at no-load, high line to reduce no-load input power

Typically the feedback current into the CONTROL pin at high line is ~3 mA. This current is both sourced from the bias winding (voltage across C10) and directly from the output. Both of these represent a load on the output of the power supply.

To minimize the dissipation from the bias winding under no-load conditions the number of bias winding turns and value of C7 was adjusted to give a minimum voltage across C7 of ~9 V. This was the minimum achievable to keep the optocoupler biased and the output in regulation.

To minimize the dissipation of the secondary side feedback circuit a high CTR (CTR of 300 – 600%) optocoupler type was used. This reduces the secondary side opto-led current from ~3 mA to <~1 mA and therefore the effective load on the output. A standard 2.5 V TL431 voltage reference was replaced with the 1.24 V LMV431 to reduce the supply current requirement of this component from 1 mA to 100 μA

4.1.6 Output Rectifier Choice

- Use of high V_{OR} enabled the use of a 60 V Schottky diode for high efficiency and lower cost

The higher BV_{DSS} rating of the TOPSwitch-JX of 725 V (compared to 600 V or 650 V rating of typical power MOSFETs) allowed a higher transformer primary to secondary turns ratio (reflected output voltage or V_{OR}). This reduced the output diode voltage stress and allowed the use of cheaper and more efficient 60 V (vs 80 V or 100 V) Schottky diodes. The efficiency improvement occurs due the lower forward voltage drop of the lower voltage diodes. Two parallel connected axial 5 A, 60 V Schottky rectifier diodes were selected for both low cost and high efficiency. This allowed PCB heatsinking of the diode for low cost while maintaining efficiency compared to a single higher current TO-220 packaged diode mounted on a heatsink. For this configuration the recommendation is that each diode is rated at twice the output current and that the diodes share a common cathode PCB area for heatsinking so that their temperatures track. In practice the diodes current share quite effectively as can be demonstrated by monitoring their individual temperatures.

4.2 Function Block Descriptions

4.2.1 Input EMI Filtering

Common-mode inductors L1 and X capacitor C1 provides CM and DM noise filtering. The frequency jittering feature of the TOPSwitch-JX allows a very small X capacitor (100 nF) to be used in meeting Class B Emission limits. This also eliminates the need for discharge resistors required for meeting safety standards.

Y capacitor C11, connected between the primary and secondary side in conjunction with T1 shield and cancellation windings provides common mode filtering.

4.2.2 TOPSwitch-JX Primary

The EcoSmart feature of U1 automatically provides constant efficiency over the entire load range. It uses a proprietary Multi-Cycle-Modulation (MCM) function to eliminate the need for special operating modes triggered at specific loads. This simplifies circuit design since it removes the need to design for aberrant or specific operating conditions or load thresholds.

Capacitor C10 provides the auto-restart timing for U1. At startup this capacitor is charged through the DRAIN (D) pin. Once it is charged U1 begins to switch. Capacitor C10 stores enough energy to ensure the power supply starts up. After start-up the bias winding powers the controller via the CONTROL pin. Bypass capacitor C9 is placed as physically close as possible to U1. Resistor R16 provides additional compensation to the feedback loop.

4.2.3 Thermal Overload Protection

IC U1 has an integrated accurate hysteretic thermal overload protection function. When the junction temperature of U1 reaches +142 °C (typical temperature shutdown threshold) during a fault condition, the IC shuts down. It automatically recovers once the junction temperature has decreased by 75 °C.

4.2.4 Output Overvoltage Protection

Open-loop faults cause the output voltage to exceed the specified maximum value. To prevent excessive output voltage levels in such cases, U1 utilizes an output overvoltage shutdown function. An increase in output voltage causes an increase in the bias winding on the primary side, sensed by VR3. A sufficient rise in the bias voltage causes VR3 to conduct and inject current into the VOLTAGE (V) pin of U1. When the current exceeds 336 μA for more than 100 μs, U1 enters the latching overvoltage shutdown mode.

4.2.5 Output Power Limiting with Line Voltage

Resistors R3, R4, and R15 reduce the external current limit of U1 as the line voltage increases. This allows the supply to limit the output power to <100 VA at high line while still delivering the rated output at low line, and to provide a nearly constant output power level with changing line voltages. The line sensing resistors R1 and R2, in conjunction with R12, set the undervoltage and overvoltage thresholds for U1. R12 provides

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additional current to V pin from the bias supply and together with R1 and R2 sets the threshold current for V pin with reduced power loss and thus helps further improvement on the no-load input power.

4.2.6 Output Feedback

Schottky diodes D8 and D9 rectify the output. A snubber network (C12, R17) dampens ringing across the diodes and reduces high frequency conducted and radiated noise. Capacitors C14 and C15 provide output filtering. Resistors R21 and R23 provide a voltage divider and set the DC set point of the output. C20, R21, and R19 provide compensation for the feedback control loop and C18 and R18 is a phase boost network to improve the phase margin of the unit. Resistor R19 limits the gain of the feedback system to ensure power supply stability throughout the range of operation. Diode D10 provides a fast discharge path for C20 when the output turns-off and to allow smooth rise of the output voltage when the unit is turned on again.

4.2.7 Output Inductor Post Filter Soft-Finish

To prevent output overshoot during start-up the voltage that appears across L2 was used to provide a soft-finish function. When the voltage across L2 exceeds the forward drop of U2A and D10 current flows though the optocoupler LED and provides feedback to the primary. This arrangement acts to limit the rate of rise of the output voltage until it reaches regulation and eliminates the capacitor that is typically placed across U3 to provide the same function.

5 PCB Layout

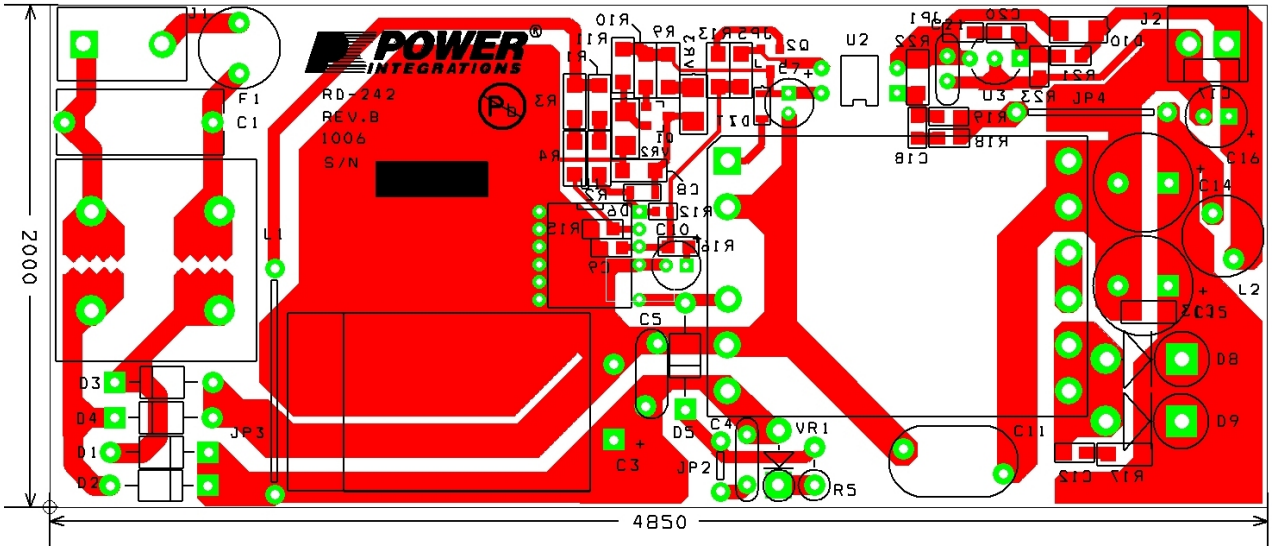

Figure 4 – Printed Circuit Board Layout.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Part Number	Mfg
1	1	C1	100 nF, 275VAC, Film, X2	LE104	OKAYA ELECT
2	1	C3	82 µF, 400 V, Electrolytic, Low ESR, (18 x 25)	EKXG401ELL820MM25S	Nippon Chemi-Con
3	1	C4	4700 pF, 1 kV, Disc Ceramic	562R5GAD47	Vishay
4		C5	Not Used		
5	2	C7, C10	47 µF, 25 V, Electrolytic, Very Low ESR, 300 mΩ, (5 x 11)	EKZE250ELL470ME11D	Nippon Chemi-Con
6		C8	Not Used		
7	1	C9	100 nF, 50 V, Ceramic, X7R, 0805	ECJ-2YB1H104K	Panasonic
8	1	C11	1 nF, Ceramic, Y1	440LD10-R	Vishay
9	1	C12	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX Corp
10		C13 C17	Not Used		
11	2	C14 C15	680 µF, 25 V, Electrolytic, Very Low ESR, 23 mΩ, (10 x 20)	EKZE250ELL681MJ20S	Nippon Chemi-Con
12	1	C16	100 µF, 25 V, Electrolytic, Gen. Purpose, (6.3 x 11)	EKMG250ELL101MF11D	Nippon Chemi-Con
13	1	C18	47 nF, 50 V, Ceramic, X7R, 0805	ECJ-2YB1H473K	Panasonic
14	1	C20	33 nF, 50 V, Ceramic, X7R, 0805	ECJ-2VB1H333K	Panasonic
15		C21	Not Used		
16	4	D1 D2 D3 D4	1000 V, 1 A, Rectifier, DO-41	1N4007-E3/54	Vishay
17	1	D5	Rectifiers 1A 1000 V 150ns	FR107G-B	Rectron
18	1	D6	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diode Inc.
19	1	D7	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diode Inc.
20	2	D8 D9	60 V, 5 A, Schottky, DO-201AD	SB560	Vishay
21	1	D10	75 V, 0.15 A, Fast Switching, 4 ns, MELF	LL4148-13	Diode Inc.
22	1	F1	3.15 A, 250 V, Slow, TR5	3721315041	Wickman
23	1	J1	3 Position (1 x 3) header, 0.156 pitch, Vertical	26-48-1031	Molex
24	1	J2	2 Position (1 x 2) header, 0.156 pitch, Vertical	26-48-1021	Molex
25	1	JP1	0 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEY0R00V	Panasonic
26	1	JP2	Wire Jumper, Non insulated, 22 AWG, 0.2 in	298 SV005	Alpha
27	1	JP3	Wire Jumper, Non insulated, 22 AWG, 0.9 in	298 SV005	Alpha
28	1	JP4	Wire Jumper, Non insulated, 22 AWG, 0.6 in	298 SV005	Alpha
29	1	JP5	0 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEY0R00V	Panasonic
30	1	L1	14 mH, 0.7 A, Common Mode Choke	ELF-17N007A	Panasonic
31	1	L2	3.3 µH, 5.5 A	RL622-3R3K-RC	JW Miller
32		Q1	Not Used		
33		Q2	Not Used		
34	2	R1 R2	5.1 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ515V	Panasonic
35	2	R3 R4	10 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ106V	Panasonic
36	1	R5	10 kΩ, 5%, 1/2 W, Carbon Film	CFR-50JB-10K	Yageo
37	1	R9	10 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ100V	Panasonic

38		R10	Not Used		
39		R11	Not Used		
40	1	R12	191 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1913V	Panasonic
41		R13	Not Used		
42	1	R15	14.3 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1432V	Panasonic
43	1	R16	6.8 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ6R8V	Panasonic
44	1	R17	22 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ220V	Panasonic
45	1	R18	110 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ111V	Panasonic
46	1	R19	470 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ470V	Panasonic
47	1	R21	86.6 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF8662V	Panasonic
48		R22	Not Used		
59	1	R23	10 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1002V	Panasonic
50	1	T1	Bobbin, EF25, Horizontal, 12 pins	YC2504 SNX-R1521	Ying Chin Santronics
51	1	U1	TOP266VG, eDIP-12P	TOP266VG	Power Integrations
52	1	U2	Optocoupler, 35 V, CTR 300-600%, 4-DIP	LTV-817D	Liteon
53	1	U3	1.24V Shunt Reg IC	LMV431ACZ	National Semiconductor
54	1	VR1	180 V, 5 W, 5%, TVS, DO204AC (DO-15)	P6KE180ARLG	On Semi
55		VR2	Not Used		
56	1	VR3	15 V, 5%, 500 mW, DO-213AA (MELF)	ZMM5245B-7	Diodes Inc

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7 Transformer Specification

7.1 Electrical Diagram

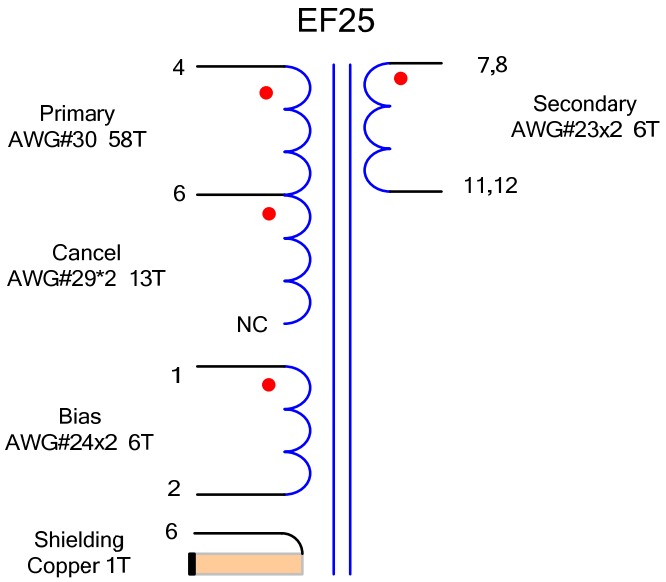

Figure 5 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1-6 to pins 7-12	3000 VAC
Primary Inductance	Pins 4-6, all other windings open, measured at 100 kHz, 0.4 VRMS	712 µH ±10%
Resonant Frequency	Pins 4-6, all other windings open	300 kHz (Min.)
Primary Leakage Inductance	Pins 4-6, with pins 7-12 shorted, measured at 100 kHz, 0.4 VRMS	25 µH (Max.)

7.3 Materials

Item	Description
[1]	Core: PC44 EF25, TDK or equivalent Gapped for AL of 215 nH/T^2
[2]	Bobbin: BEF25, Horizontal, 12 pins, 6/6. Manufacture#: YC-2504.
[3]	Magnet Wire: #30 AWG.
[4]	Magnet Wire: #29 AWG
[5]	Magnet Wire: #23 AWG.
[6]	Magnet Wire: #24 AWG.
[7]	Margin tape: 3M, Polyester web. 3.0 mm wide.
[8]	Teflon Tube.
[9]	Tape: 3M 1298 Polyester Film, 15.3 mm wide.
[10]	Tape: 3M 1298 Polyester Film, 9.3 mm wide.
[11]	Tape: 3M 1298 Polyester Film, 14.0 mm wide.
[12]	Copper Foil Tape: 2.0 mils thick, 9.0 mm wide. See Figure 7 below to prepare.
[13]	Varnish.

7.4 Transformer Build Diagram

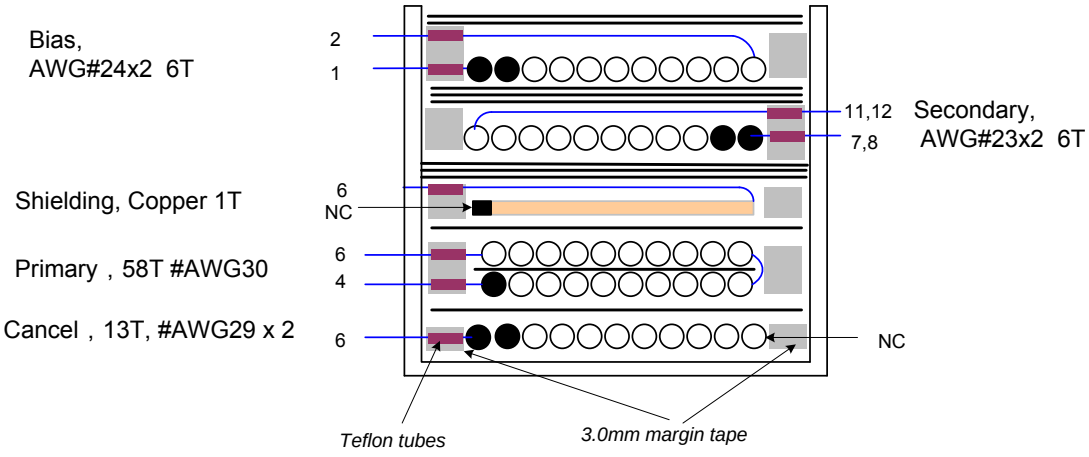

Figure 6 – Transformer Build Diagram.

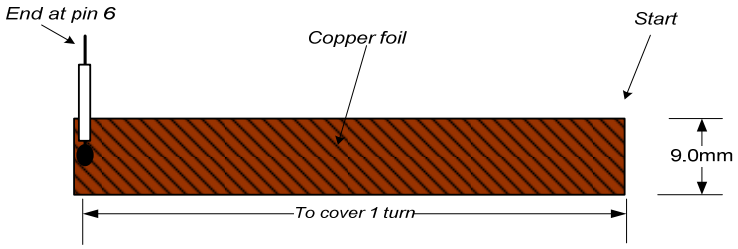

Figure 7 – Shield.

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7.5 Transformer Construction

Winding preparation	Place the bobbin item [2] on the mandrel such that primary side on the left and secondary side on the right. Winding direction is clockwise direction.
Margin	Apply margin tape item [7] on both sides of bobbin and for all windings.
WD1 (Cancel)	Start at pin 6, apply Teflon tubes item [8] at start ends, wind 13 bifilar turns of item [4] from left to right. At the last turn, cut the wires and leave no connect.
Insulation	Apply 1 layer of tape item [9].
WD2 (Primary)	Start at pin 4, apply Teflon tube item [8] at start end, wind 29 turns of item [3] from left to right, place 1 layer of tape item [10]. Continue winding from right to left with another 29 turns, at the last turn also apply Teflon tube item [8] and end at pin 6.
Insulation	Apply 1 layer of tape item [9].
WD3 (Shielding)	Use copper foil tape item [12], see figure 3 above, start with no connect; wind 1 turn (over lapped- but separate with tape to avoid shortage), and end with pin 6.
Insulation	Apply 3 layers of tape item [8].
WD4 (Secondary)	Start at pin 7, 8, apply Teflon tubes item [8] at start ends, wind 6 bifilar turns of item [5] from right to left, at the last turn bring the wires back to the left, also apply Teflon tubes at the wire ends, and finish at pin 11,12.
Insulation	Apply 3 layers of tape item [9].
WD5 (Bias)	Start at pin 1, apply Teflon tubes item [8] at start ends, wind 6 bifilar turns of item [6] from left to right, at the last turn bring the wires back to the left, also apply Teflon tubes at the wire ends, and finish at pin 1.
Outer insulation	Apply 2 layers of tape item [9].
Final Assembly	Grind core. Cover outside the core with tape item [11]. Assemble core and varnish [13]

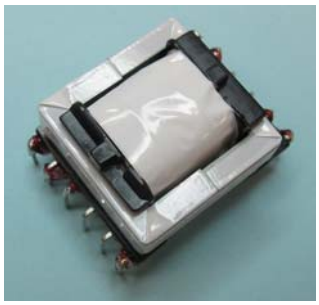

Figure 8 – Completed Transformer.

8 Transformer Design Spreadsheet

ACDC_TOPSwitchJX_020110; Rev.1.2; Copyright Power Integrations 2010	INPUT	INFO	OUTPUT	UNIT	TOP_JX_020110: TOPSwitch-JX Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					**Design title**
VACMIN	85			Volts	Minimum AC Input Voltage
VACMAX	265			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	12.00			Volts	Output Voltage (main)
PO_AVG	30.00	*Warning*		Watts	!!! For low line (VMIN < 200 VDC) designs: Reduce PO_AVG<28.5 W (or use larger device)
PO_PEAK			30.00	Watts	Peak Output Power
Heatsink Type	**PCB**		PCB		Heatsink Type
Enclosure	**Open Frame**				Open Frame enclosure assume sufficienct airflow while adapter means a sealed enclosure.
n	0.80			%/100	Efficiency Estimate
Z	0.50				Loss Allocation Factor
VB	15			Volts	Bias Voltage - Verify that VB is > 8 V at no load and VMAX
tC	3.00			ms	Bridge Rectifier Conduction Time Estimate
CIN	82.0		82	uFarads	Input Filter Capacitor
ENTER TOPSWITCH-JX VARIABLES					
TOPSwitch-JX	**TOP266V**			Universal / Peak	115 Doubled/230V
Chosen Device		*TOP266V*	Power Out	28.5 W / 86 W	39W
KI	0.4725				External Ilimit reduction factor (KI=1.0 for default ILIMIT, KI <1.0 for lower ILIMIT)
ILIMITMIN_EXT			1.120	Amps	Use 1% resistor in setting external ILIMIT
ILIMITMAX_EXT			1.289	Amps	Use 1% resistor in setting external ILIMIT
Frequency (F)=132kHz, (H)=66kHz	**F**		F		Select 'H' for Half frequency - 66kHz, or 'F' for Full frequency - 132kHz
fS			132000	Hertz	TOPSwitch-JX Switching Frequency: Choose between 132 kHz and 66 kHz
fSmin			119000	Hertz	TOPSwitch-JX Minimum Switching Frequency
fSmax			145000	Hertz	TOPSwitch-JX Maximum Switching Frequency
High Line Operating Mode			FF		Full Frequency, Jitter enabled
VOR	120.00			Volts	Reflected Output Voltage
VDS			10	Volts	TOPSwitch on-state Drain to Source Voltage
VD	0.50			Volts	Output Winding Diode Forward Voltage Drop
VDB	0.70			Volts	Bias Winding Diode Forward Voltage Drop
KP	0.62				Ripple to Peak Current Ratio (0.3 < KRP < 1.0 : 1.0< KDP<6.0)
PROTECTION FEATURES					
LINE SENSING					V pin functionality

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VUV_STARTUP			95	Volts	Minimum DC Bus Voltage at which the power supply will start-up
VOV_SHUTDOWN			445	Volts	Typical DC Bus Voltage at which power supply will shut-down (Max)
RLS			4.0	M-ohms	Use two standard, 2 M-Ohm, 5% resistors in series for line sense functionality.
OUTPUT OVERVOLTAGE					
VZ			27	Volts	Zener Diode rated voltage for Output Overvoltage shutdown protection
RZ			5.1	k-ohms	Output OVP resistor. For latching shutdown use 20 ohm resistor instead
OVERLOAD POWER LIMITING					X pin functionality
Overload Current Ratio at VMAX			1.2		Enter the desired margin to current limit at VMAX. A value of 1.2 indicates that the current limit should be 20% higher than peak primary current at VMAX
Overload Current Ratio at VMIN			1.11		Margin to current limit at low line.
ILIMIT_EXT_VMIN			1.01	A	Peak primary Current at VMIN
ILIMIT_EXT_VMAX			0.97	A	Peak Primary Current at VMAX
RIL			12.88	k-ohms	Current limit/Power Limiting resistor.
RPL			N/A	M-ohms	Resistor not required. Use RIL resistor only
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**Auto**		EF25		Core Type
Core		*EF25*		*P/N:*	PC40EF25-Z
Bobbin		*EF25_BOBBIN*		*P/N:*	*
AE			0.518	cm^2	Core Effective Cross Sectional Area
LE			5.78	cm	Core Effective Path Length
AL			2000	nH/T^2	Ungapped Core Effective Inductance
BW			15.6	mm	Bobbin Physical Winding Width
M	0.00			mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	2.00				Number of Primary Layers
NS			6		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			90	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.60		Maximum Duty Cycle (calculated at PO_PEAK)
IAVG			0.42	Amps	Average Primary Current (calculated at average output power)
IP			1.01	Amps	Peak Primary Current (calculated at Peak output power)
IR			0.63	Amps	Primary Ripple Current (calculated at average output power)
IRMS			0.56	Amps	Primary RMS Current (calculated at average output power)

TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			712	uHenries	Primary Inductance
LP Tolerance			10		Tolerance of Primary Inductance
NP			58		Primary Winding Number of Turns
NB			8		Bias Winding Number of Turns
ALG			215	nH/T^2	Gapped Core Effective Inductance
BM			2412	Gauss	Maximum Flux Density at PO, VMIN (BM<3000)
BP			3384	Gauss	Peak Flux Density (BP<4200) at ILIMITMAX and LP_MAX. Note: Recommended values for adapters and external power supplies <=3600 Gauss
BAC			751	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1776		Relative Permeability of Ungapped Core
LG			0.27	mm	Gap Length (Lg > 0.1 mm)
BWE			31.2	mm	Effective Bobbin Width
OD	0.32		0.32	mm	Maximum Primary Wire Diameter including insulation
INS			0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.27	mm	Bare conductor diameter
AWG			30	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			102	Cmils	Bare conductor effective area in circular mils
CMA		*Warning*	182	Cmils/Amp	!!! INCREASE CMA>200 (increase L(primary layers),decrease NS,larger Core)
Primary Current Density (J)			11.00	Amps/mm^2	!!! Decrease current density Use larger wire diameter, increase L or increase core size.
TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT EQUIVALENT)					
Lumped parameters					
ISP			9.70	Amps	Peak Secondary Current
ISRMS			4.36	Amps	Secondary RMS Current
IO_PEAK			2.50	Amps	Secondary Peak Output Current
IO			2.50	Amps	Average Power Supply Output Current
IRIPPLE			3.57	Amps	Output Capacitor RMS Ripple Current
CMS			872	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			20	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.81	mm	Secondary Minimum Bare Conductor Diameter
ODS			2.60	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS			0.89	mm	Maximum Secondary Insulation Wall Thickness

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VOLTAGE STRESS PARAMETERS					
VDRAIN			611	Volts	Maximum Drain Voltage Estimate (Includes Effect of Leakage Inductance)
PIVS			51	Volts	Output Rectifier Maximum Peak Inverse Voltage
PIVB			64	Volts	Bias Rectifier Maximum Peak Inverse Voltage
TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					
1st output					
VO1			12	Volts	Output Voltage
IO1_AVG			2.50	Amps	Average DC Output Current
PO1_AVG			30.00	Watts	Average Output Power
VD1			0.5	Volts	Output Diode Forward Voltage Drop
NS1			6.00		Output Winding Number of Turns
ISRMS1			4.361	Amps	Output Winding RMS Current
IRIPPLE1			3.57	Amps	Output Capacitor RMS Ripple Current
PIVS1			51	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS1			872	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			20	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.81	mm	Minimum Bare Conductor Diameter
ODS1			2.60	mm	Maximum Outside Diameter for Triple Insulated Wire
2nd output					
VO2				Volts	Output Voltage
IO2_AVG				Amps	Average DC Output Current
PO2_AVG			0.00	Watts	Average Output Power
VD2			0.7	Volts	Output Diode Forward Voltage Drop
NS2			0.34		Output Winding Number of Turns
ISRMS2			0.000	Amps	Output Winding RMS Current
IRIPPLE2			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS2			2	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS2			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS2			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2			N/A	mm	Minimum Bare Conductor Diameter
ODS2			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
3rd output					
VO3				Volts	Output Voltage
IO3_AVG				Amps	Average DC Output Current
PO3_AVG			0.00	Watts	Average Output Power
VD3			0.7	Volts	Output Diode Forward Voltage Drop
NS3			0.34		Output Winding Number of Turns
ISRMS3			0.000	Amps	Output Winding RMS Current
IRIPPLE3			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS3			2	Volts	Output Rectifier Maximum Peak Inverse Voltage

CMS3			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS3			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS3			N/A	mm	Minimum Bare Conductor Diameter
ODS3			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
Total Continuous Output Power			30	Watts	Total Continuous Output Power
Negative Output			N/A		If negative output exists enter Output number; eg: If VO2 is negative output, enter 2

Note: The warning displayed for PO_AVG indicates the possibility of a thermal issue however thermal results showed that the selected device could deliver the rated output power at the specified maximum ambient temperature.

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9 Performance Data

All measurements were performed at room temperature, 60 Hz input frequency. All output measurements were taken at the output terminals.

9.1 Active Mode Efficiency

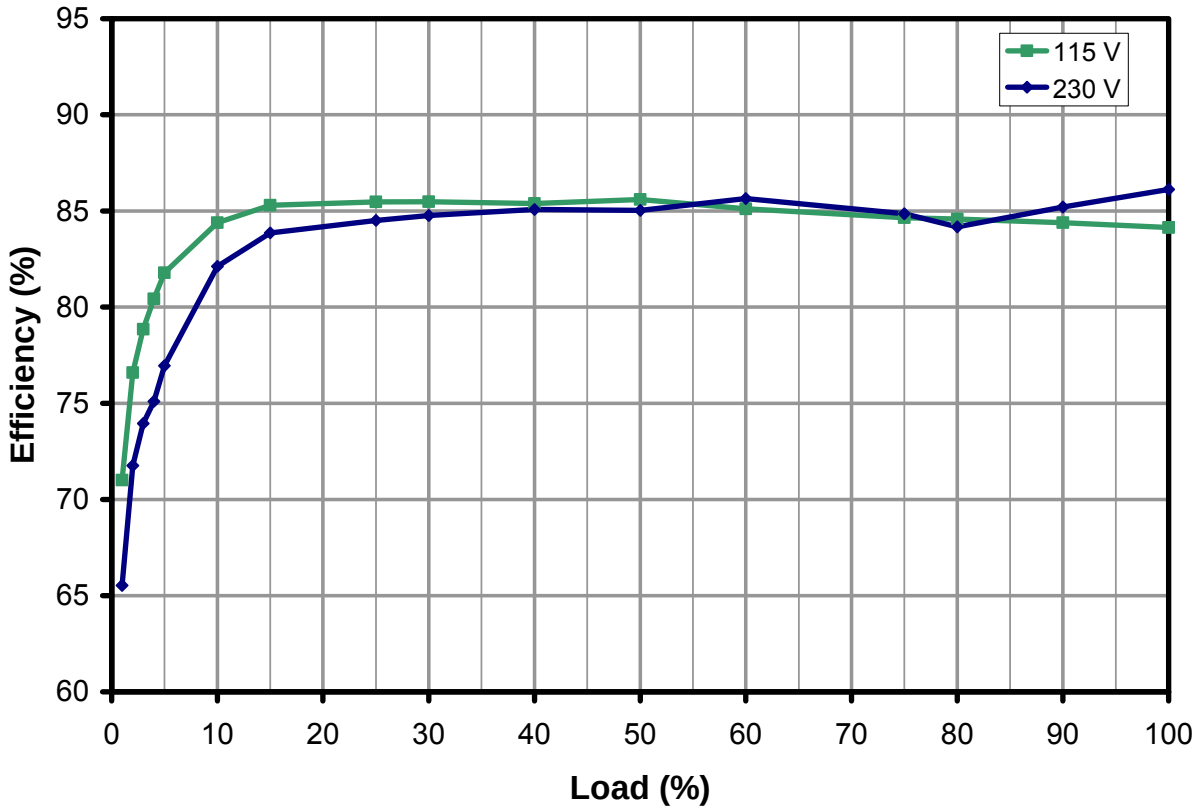

Figure 9 – Efficiency vs. Input Voltage, Room Temperature, 60 Hz.

Load (%)	I_{OUT} (Meas)	V_{OUT} (V)	P_{OUT} (W)	P_{IN} (W)	Efficiency (%)
0	0.000	11.99	0.0000	0.062	
1	0.025	11.99	0.30	0.423	71.00
2	0.050	11.98	0.60	0.782	76.60
3	0.075	11.98	0.90	1.141	78.85
4	0.100	11.98	1.20	1.491	80.43
5	0.125	11.98	1.50	1.831	81.79
10	0.250	11.98	3.00	3.549	84.39
15	0.375	11.98	4.49	5.267	85.30
25	0.625	11.98	7.49	8.760	85.47
30	0.750	11.98	8.99	10.510	85.49
40	1.000	11.98	11.98	14.030	85.39
50	1.249	11.98	14.96	17.480	85.60
60	1.499	11.98	17.96	21.100	85.11
75	1.876	11.98	22.47	26.550	84.65
80	2.005	11.98	24.02	28.400	84.58
90	2.250	11.98	26.96	31.940	84.39
100	2.499	11.98	29.94	35.580	84.14

Table 1 – Data at 115 VAC / 60 Hz for Figure 9.

Load (%)	I_{OUT} (Meas)	V_{OUT} (V)	P_{OUT} (W)	P_{IN} (W)	Efficiency (%)
0	0.000	11.99	0.0000	0.075	
1	0.025	11.99	0.30	0.456	65.52
2	0.050	11.99	0.60	0.837	71.77
3	0.075	11.99	0.90	1.216	73.95
4	0.100	11.98	1.20	1.600	75.10
5	0.125	11.98	1.50	1.946	76.95
10	0.250	11.98	3.00	3.647	82.12
15	0.375	11.98	4.49	5.357	83.86
25	0.625	11.98	7.49	8.860	84.51
30	0.750	11.98	8.99	10.600	84.76
40	1.000	11.98	11.98	14.080	85.09
50	1.250	11.98	14.98	17.610	85.04
60	1.500	11.98	17.97	20.980	85.65
75	1.875	11.98	22.46	26.470	84.86
80	1.999	11.98	23.95	28.450	84.18
90	2.249	11.98	26.94	31.620	85.21
100	2.499	11.98	29.94	34.760	86.13

Table 2 – Data at 230 VAC / 50 Hz for Figure 9.

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Percent of Full Load	Efficiency (%)	
	115 VAC	230 VAC
25	85.47	84.51
50	85.60	85.04
75	84.65	84.86
100	84.14	86.13
Average	**84.97**	**85.13**
US EISA (2007) requirement	81	
ENERGY STAR 2.0 requirement	83	

9.2 Energy Efficiency Requirements

The external power supply requirements below all require meeting active mode efficiency and no-load input power limits. Minimum active mode efficiency is defined as the average efficiency of 25, 50, 75 and 100% of output current (based on the nameplate output current rating).

For adapters that are single input voltage only then the measurement is made at the rated single nominal input voltage (115 VAC or 230 VAC), for universal input adapters the measurement is made at both nominal input voltages (115 VAC and 230 VAC).

To meet the standard the measured average efficiency (or efficiencies for universal input supplies) must be greater than or equal to the efficiency specified by the standard.

The test method can be found here:

http://www.energystar.gov/ia/partners/prod_development/downloads/power_supplies/EPSupplyEffic_TestMethod_0804.pdf

For the latest up to date information please visit the PI Green Room:

http://www.powerint.com/greenroom/regulations.htm

9.2.1 USA Energy Independence and Security Act 2007

This legislation mandates all single output single output adapters, including those provided with products, manufactured on or after July 1st, 2008 must meet minimum active mode efficiency and no load input power limits.

Active Mode Efficiency Standard Models

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
< 1 W	$0.5 \times P_O$
≥ 1 W to ≤ 51 W	$0.09 \times \ln(P_O) + 0.5$
> 51 W	0.85

ln = natural logarithm

No-load Energy Consumption

Nameplate Output (P_O)	Maximum Power for No-load AC-DC EPS
All	≤ 0.5 W

This requirement supersedes the legislation from individual US States (for example CEC in California).

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9.2.2 ENERGY STAR EPS Version 2.0

This specification takes effect on November 1st, 2008.

Active Mode Efficiency Standard Models

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
≤ 1 W	$0.48 \times P_O + 0.14$
> 1 W to ≤ 49 W	$0.0626 \times \ln(P_O) + 0.622$
> 49 W	0.87

ln = natural logarithm

Active Mode Efficiency Low Voltage Models (V_O<6 V and $I_O \geq 550$ mA)

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
≤ 1 W	$0.497 \times P_O + 0.067$
> 1 W to ≤ 49 W	$0.075 \times \ln(P_O) + 0.561$
> 49 W	0.86

ln = natural logarithm

No-load Energy Consumption (both models)

Nameplate Output (P_O)	Maximum Power for No-load AC-DC EPS
0 to < 50 W	≤ 0.3 W
≥ 50 W to ≤ 250 W	≤ 0.5 W

9.3 No-load Input Power

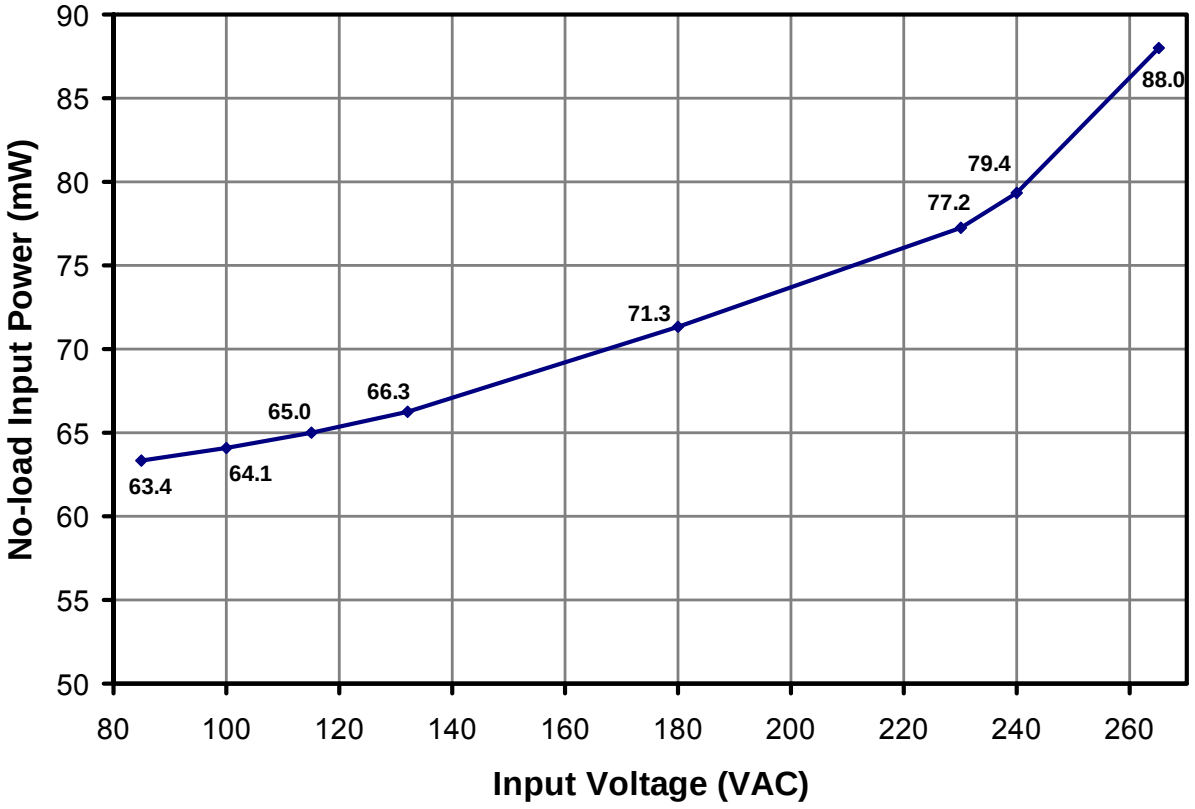

Figure 10 – Zero Load Input Power vs. Input Line Voltage, Room Temperature, 60 Hz.

V_{OUT}	Input Line	P_{IN} (mW)
12	85 V / 50 Hz	63.36
12	100 V / 50 Hz	64.10
12	115 V / 60 Hz	65.00
12	132 V / 60 Hz	66.27
12	180 V / 50 Hz	71.33
12	230 V / 50 Hz	77.23
12	240 V / 50 Hz	79.36
12	264 V / 50 Hz	88.03

Table 3 – No-load Input Power vs. Input Voltage.

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9.4 Available Standby Output Power

The chart below shows the available output power vs. line voltage for an input power of 1 W, 2 W and 3 W.

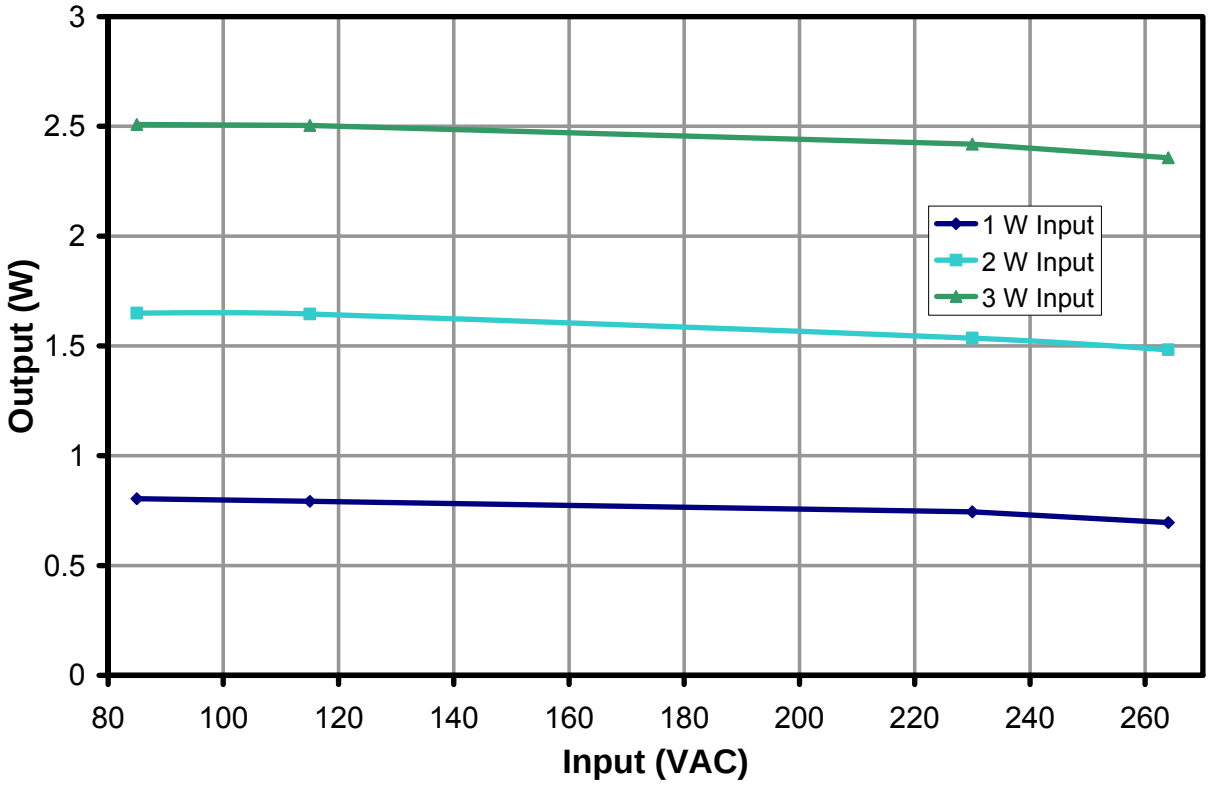

Figure 11 – Available Standby Power.

9.5 Regulation

9.5.1 Load

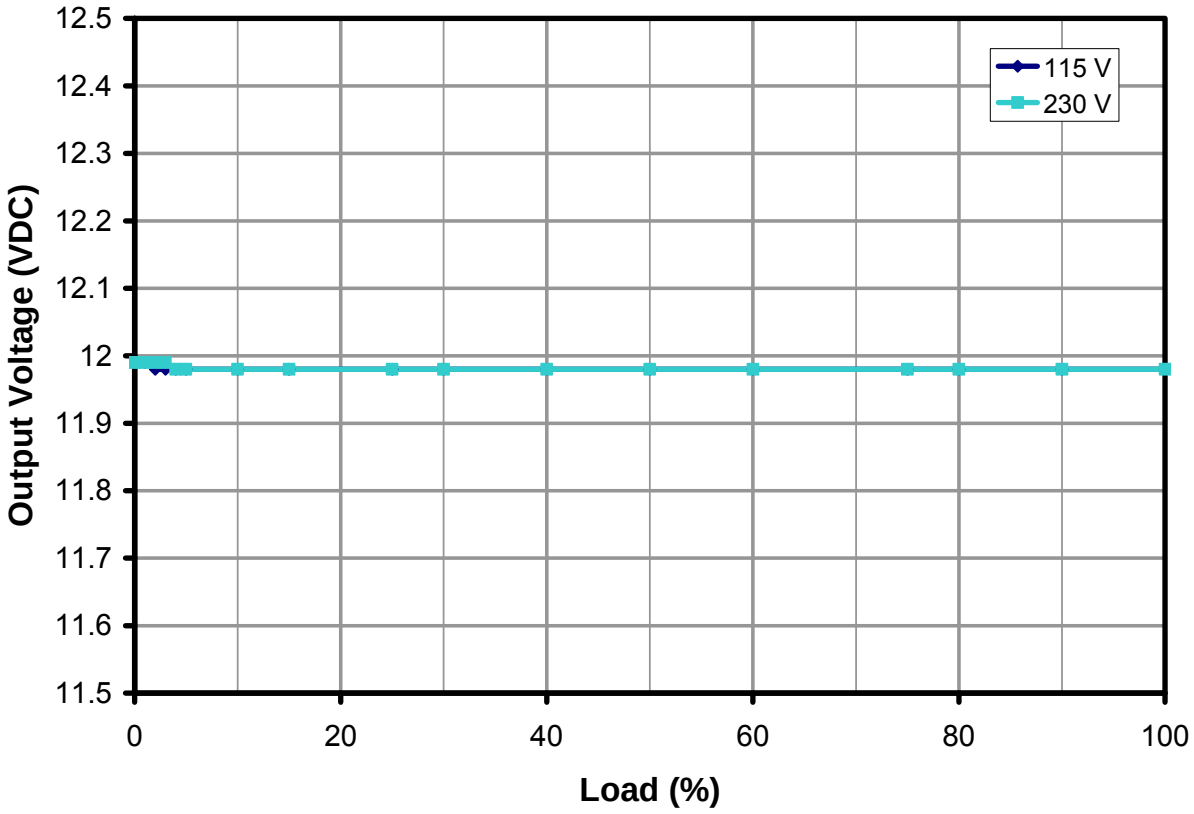

Figure 12 – Load Regulation, Room Temperature.

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9.5.2 Line

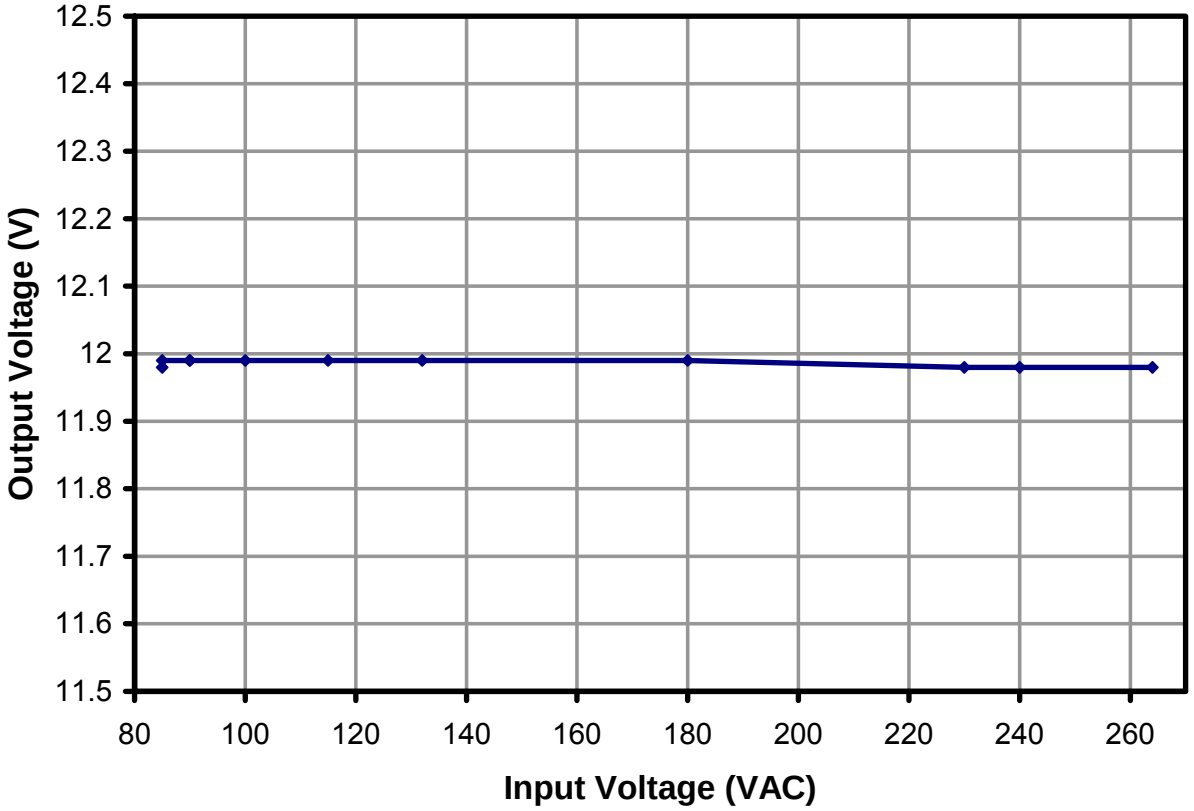

Figure 13 – Line Regulation, Room Temperature, Full Load.

9.6 Efficiency

9.6.1 Load

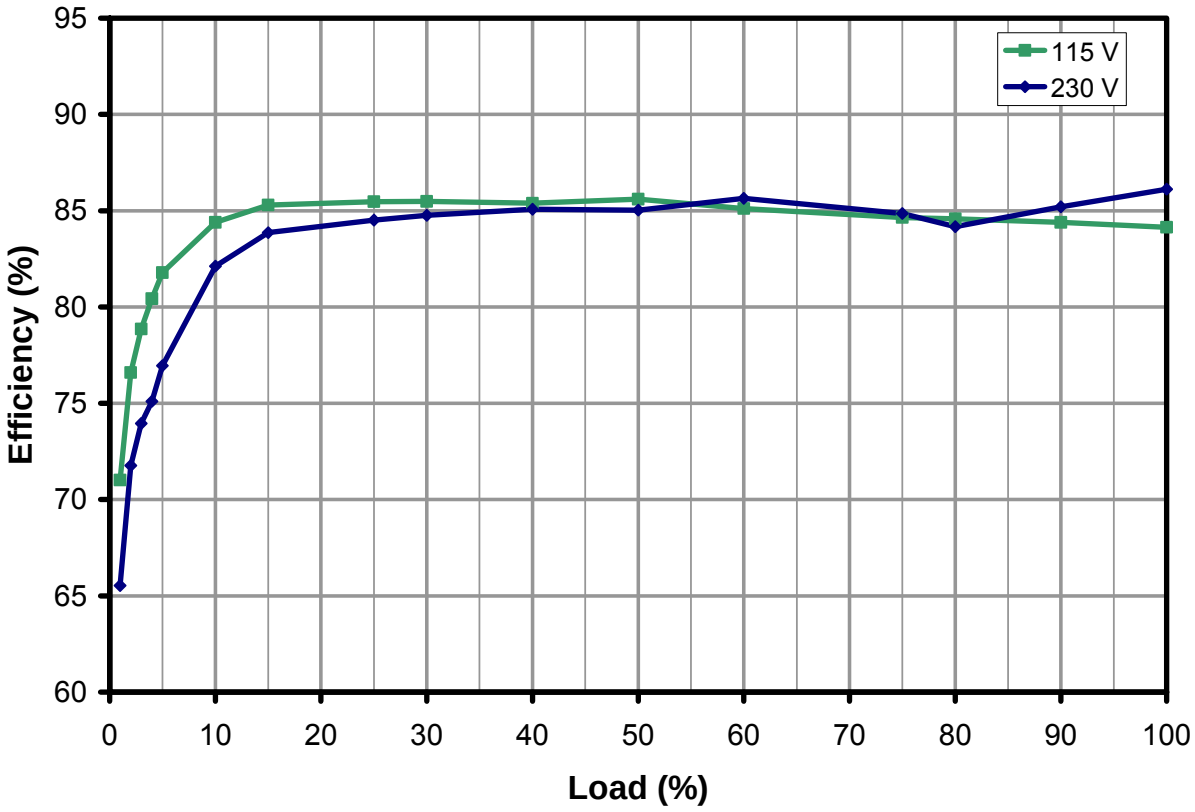

Figure 14 – Load Efficiency, Room Temperature.

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10.6.2 Line

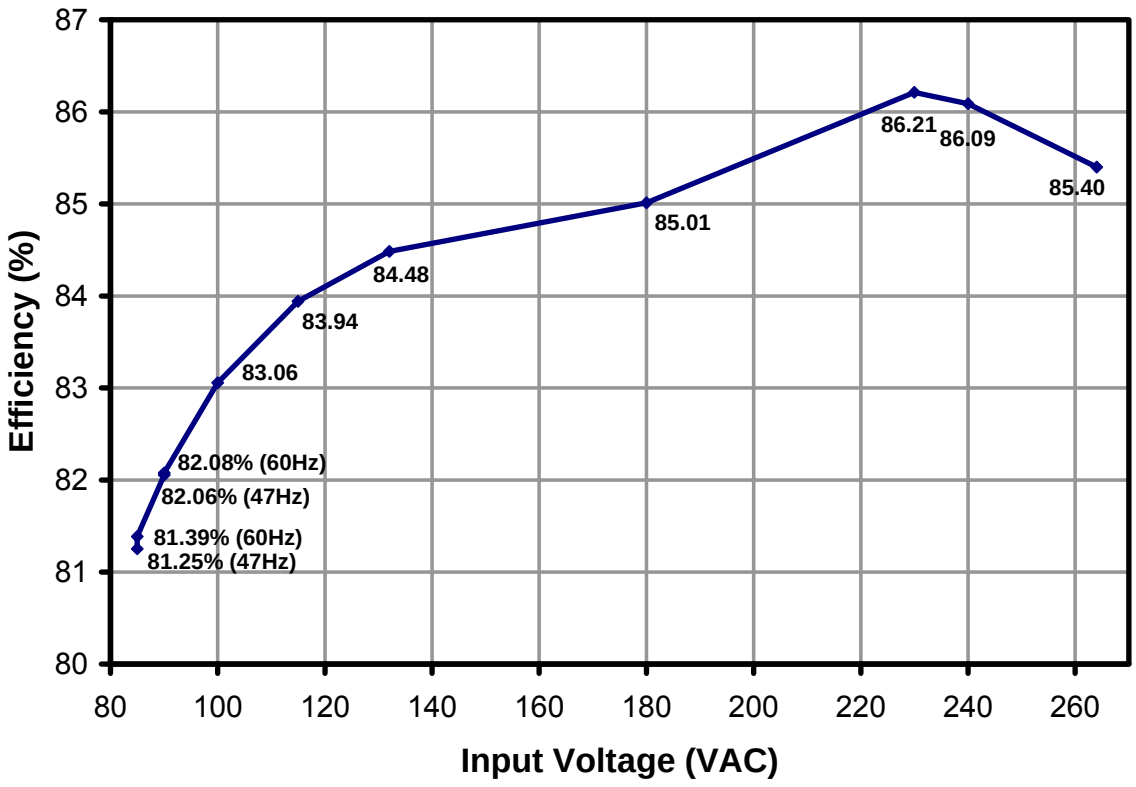

Figure 15 – Line Efficiency at Full-load, Room Temperature.

10 Power Limit

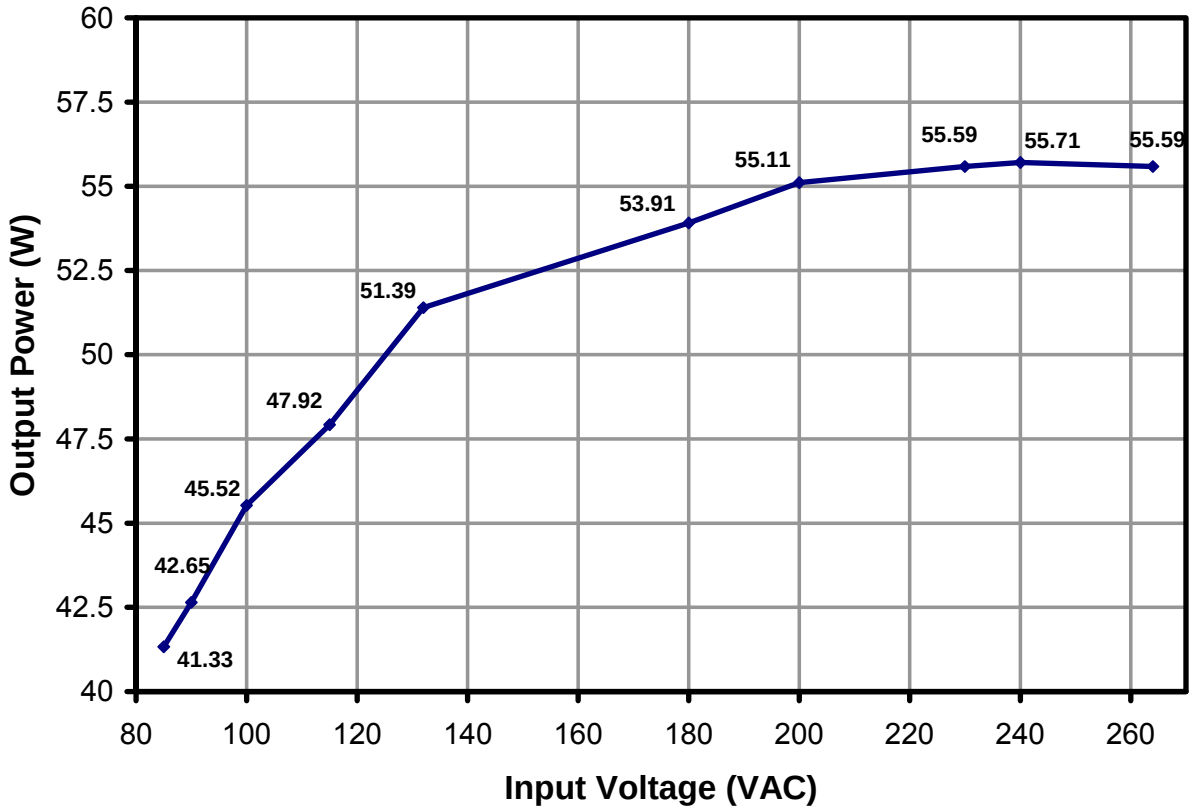

Figure 16 – Maximum Output Power vs. Line Voltage.

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11 Thermal Performance

The power supply was placed inside a small box and then placed inside the chamber. The box protects the unit from being blown directly by the fan inside the chamber. The chamber temperature was controlled to maintain a constant temperature of 40 °C inside the box. The supply was operated at its rated output power (30 W). The transformer winding temperature was taken on the outermost layer.

Item	Ref Des	Description	85 VAC, 47 Hz; T_A = 40 ˚C	264 VAC, 50 Hz; T_A = 40 ˚C
1	L1	Common Mode Choke Core	81	52
2	L1	Common Mode Choke Wire	92	54
3	D1	Bridge Diode	79	54
4	U1	TOPSwitch	107	78
5	T1	Transformer wire	86	82
6	T1	Transformer core	75	74
7	C14	Output Capacitor	54	54
8	C15	Output Capacitor	61	60
9	D8	Output Diode	81	80
10	D9	Output Diode	80	80
11	VR1	Zener Clamp	70	63

12 Waveforms

12.1 Drain Voltage and Current, Normal Operation

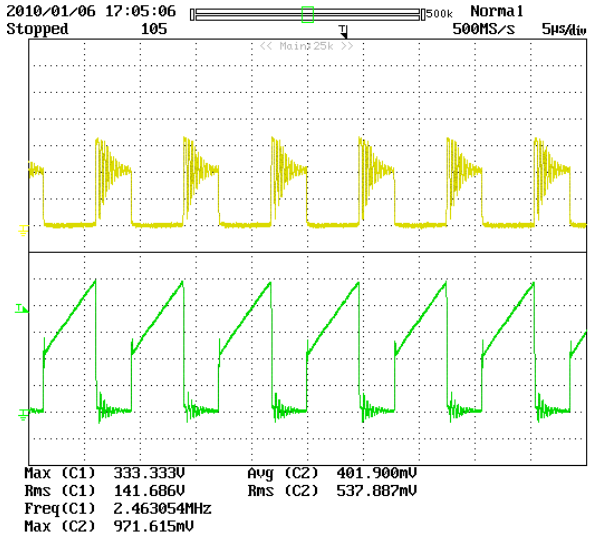

Figure 17 – 85 VAC 47 Hz, Full Load.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 0.2 A, 5 µs / div.

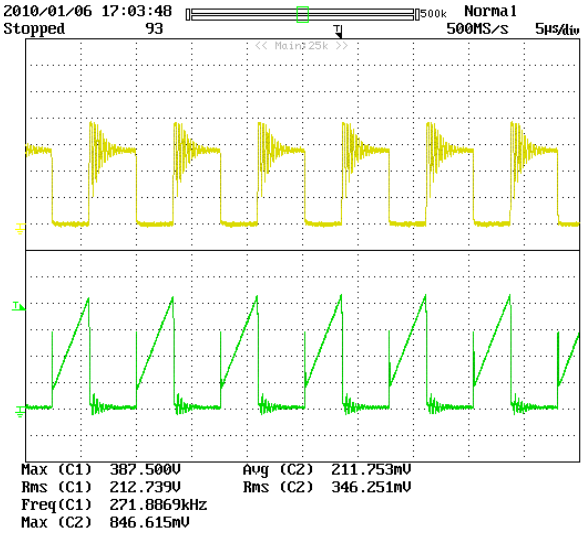

Figure 18 – 115 VAC 60 Hz, Full Load.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 0.2 A, 5 µs / div.

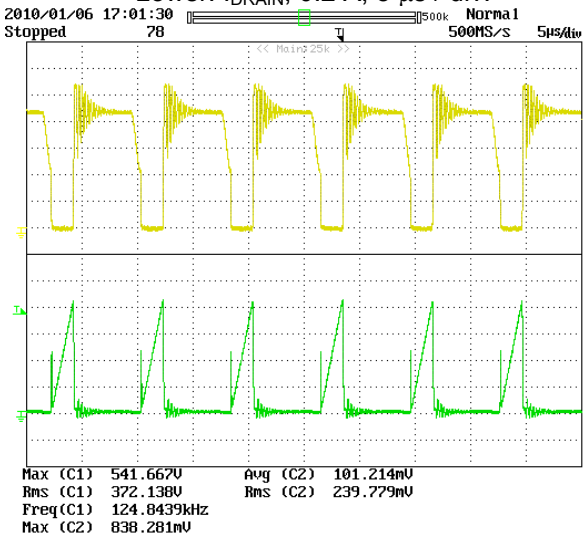

Figure 19 – 230 VAC 50 Hz, Full Load.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 0.2 A, 5 µs / div.

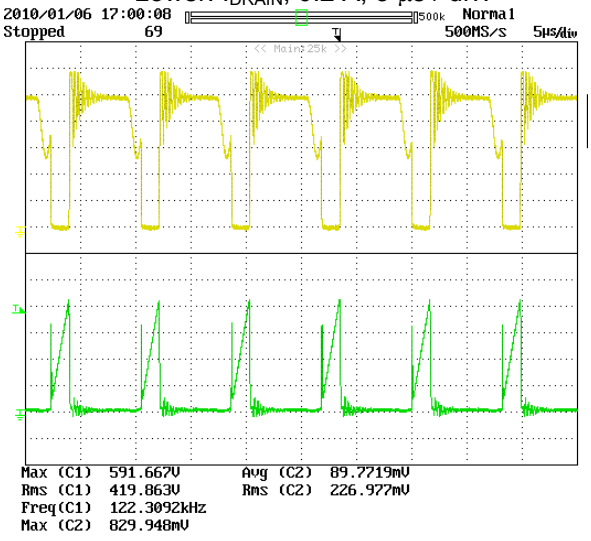

Figure 20 – 264 VAC 50 Hz, Full Load.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 0.2 A, 5 µs / div.

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12.2 V_{OUT} and Drain Current Start-up Profile

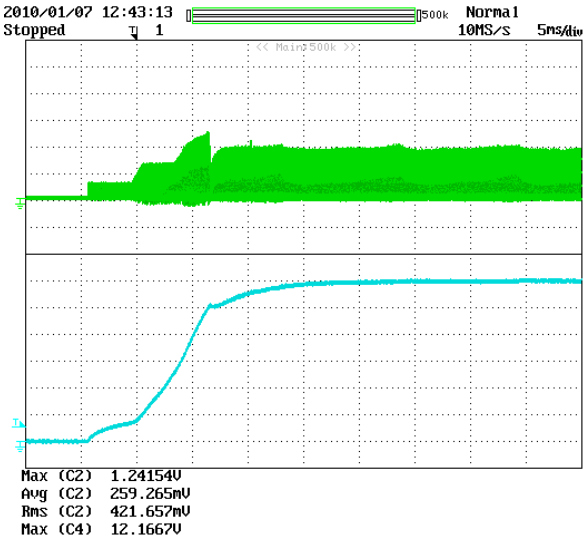

Figure 21 – 85 VAC 47 Hz, Full Load.
Upper: I_{DRAIN}, 0.5 A / div.
Lower: V_{OUT}, 2 V, 5 ms / div.

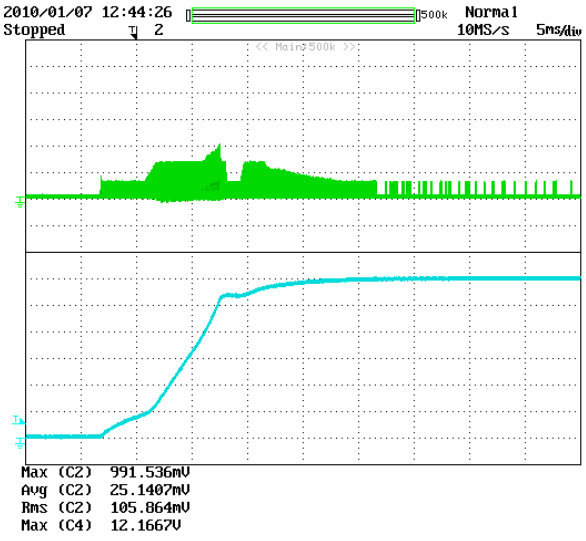

Figure 22 – 85 VAC 47 Hz, No-load.
Upper: I_{DRAIN}, 0.5 A / div.
Lower: V_{OUT}, 2 V, 5 ms / div.

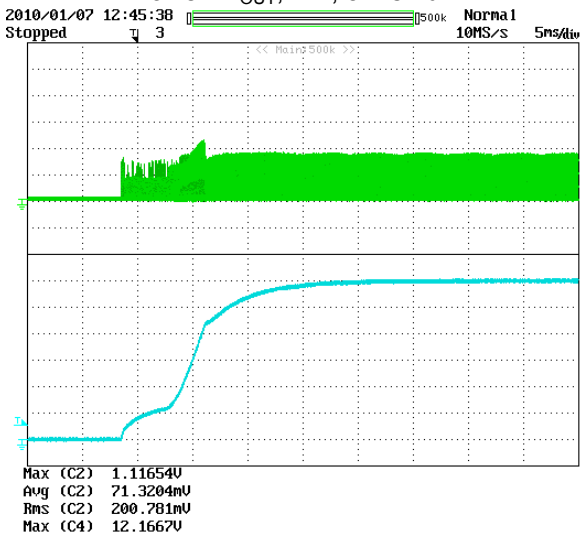

Figure 23 – 264 VAC 50 Hz, Full Load.
Upper: I_{DRAIN}, 0.5 A / div.
Lower: V_{OUT}, 2 V, 5 ms / div.

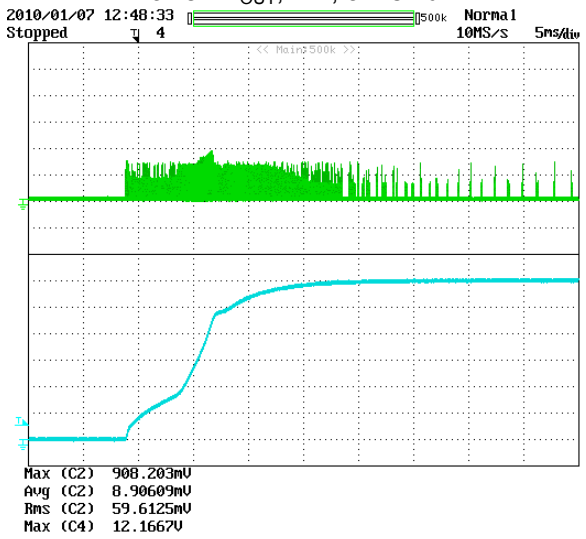

Figure 24 – 264 VAC 50 Hz, Full Load.
Upper: I_{DRAIN}, 0.5 A / div.
Lower: V_{OUT}, 2 V, 5 ms / div.

12.3 V_{OUT} and Drain Voltage Start-up Profile

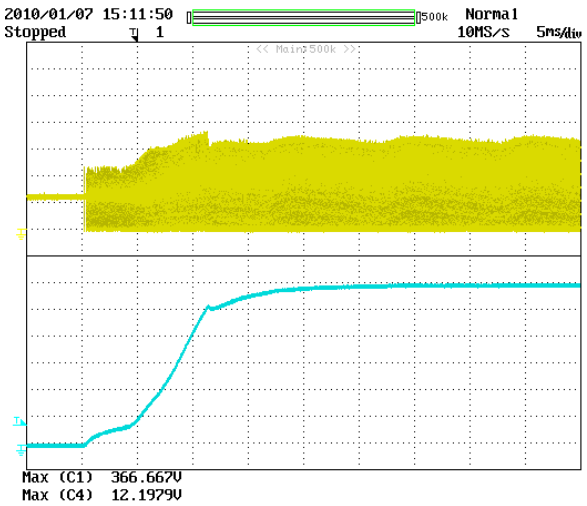

Figure 25 – 85 VAC 47 Hz, Full Load.
Upper: V_{DRAIN}, 100V / div.
Lower: V_{OUT}, 2 V, 5 ms / div.

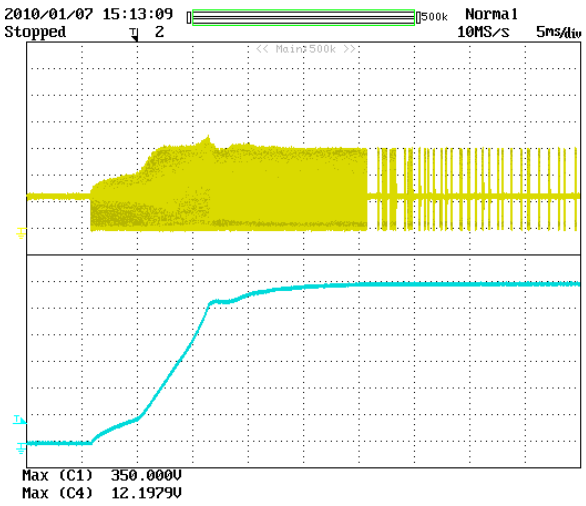

Figure 26 – 85 VAC 47 Hz, No-load.
Upper: V_{DRAIN}, 100V / div.
Lower: V_{OUT}, 2 V, 5 ms / div.

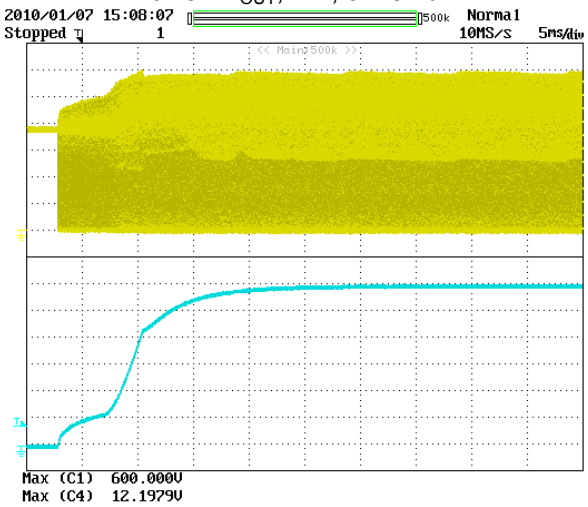

Figure 27 – 264 VAC 50 Hz, Full Load.
Upper: V_{DRAIN}, 100V / div.
Lower: V_{OUT}, 2 V, 5 ms / div.

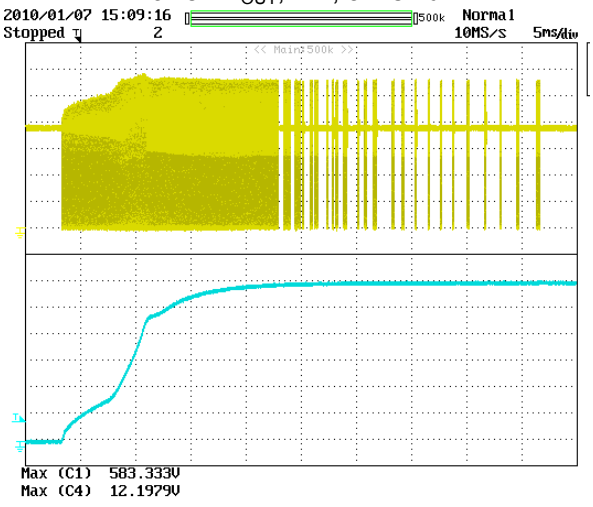

Figure 28 – 264 VAC 50 Hz, No-load.
Upper: V_{DRAIN}, 100V / div.
Lower: V_{OUT}, 2 V, 5 ms / div.

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12.4 Over Current Protection

The waveform below shows V_{DRAIN}, I_{DRAIN}, I_{OUT}, and V_{OUT} when output is shorted. Maximum V_{DRAIN} and I_{DRAIN} are within the maximum allowable limits.

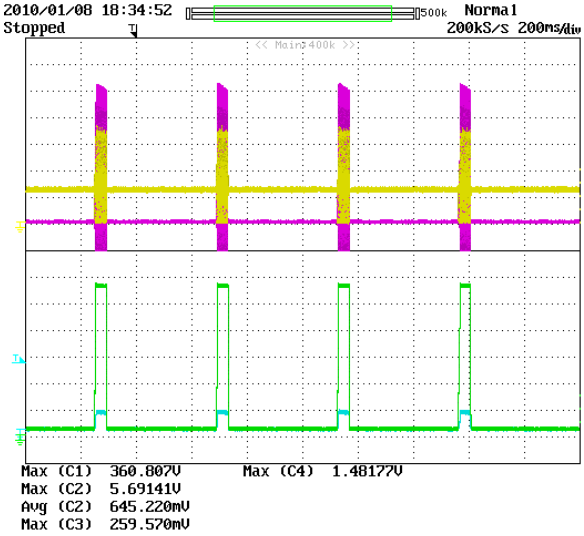

Figure 29 – 85 VAC 60 Hz.
CH1: V_{DRAIN}, 100 V / div.
CH3: I_{DRAIN}, 0.25 A / div.
CH2: I_{OUT}, 1 A / div.
CH4: V_{OUT}, 2 V / div.
Input Power = 2.2 W.

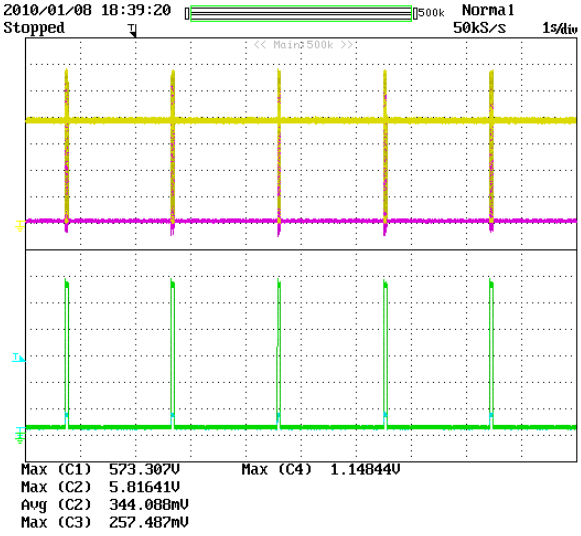

Figure 30 – 264 VAC 63 Hz.
CH1: V_{DRAIN}, 100 V / div.
CH3: I_{DRAIN}, 0.25 A / div.
CH2: I_{OUT}, 1 A / div.
CH4: V_{OUT}, 2 V / div.
Input Power = 0.4 W.

The output diodes had the highest recorded temperature during an output short circuit at 85 VAC, 60 Hz (input power of 2.2 W). A temperature of 45 °C was well within the temperature limits of the diodes.

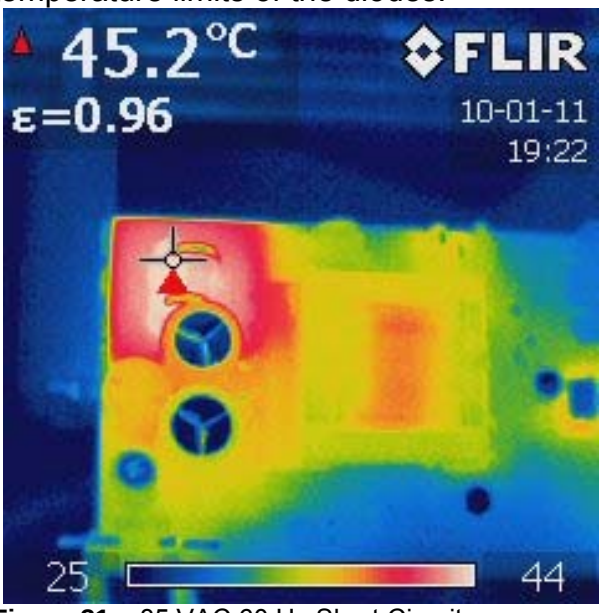

Figure 31 – 85 VAC 60 Hz Short Circuit
D8, D9 : 45.2˚C (T_A = 25˚C).

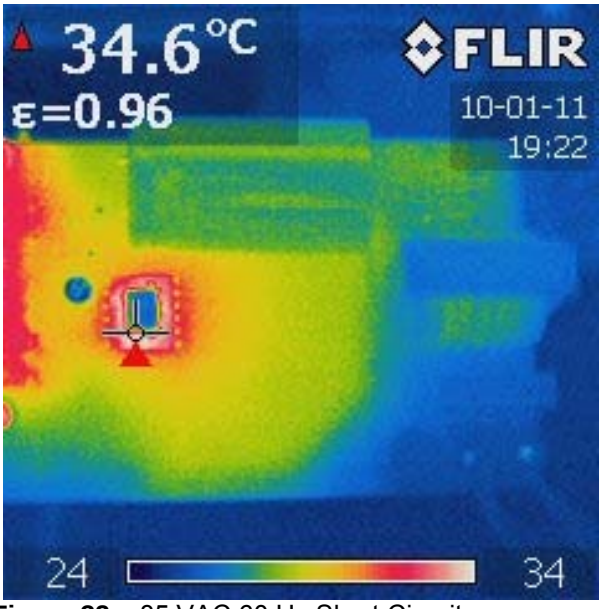

Figure 32 – 85 VAC 60 Hz Short Circuit
U1 : 34.6˚C (T_A = 25˚C).

12.5 VDS & ID at Maximum Power

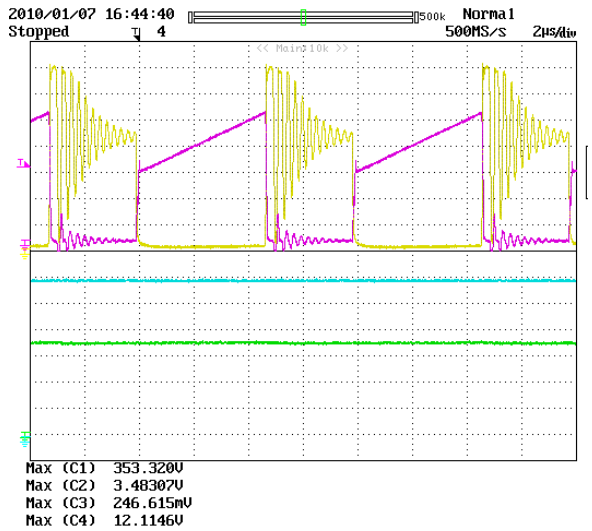

Figure 33 – ~ 42 W at 85 VAC.
CH1: V_{DRAIN}, 100 V / div.
CH3: I_{DRAIN}, 0.25 A / div.
CH2: I_{OUT}, 1 A / div.
CH4: V_{OUT}, 2 V / div.

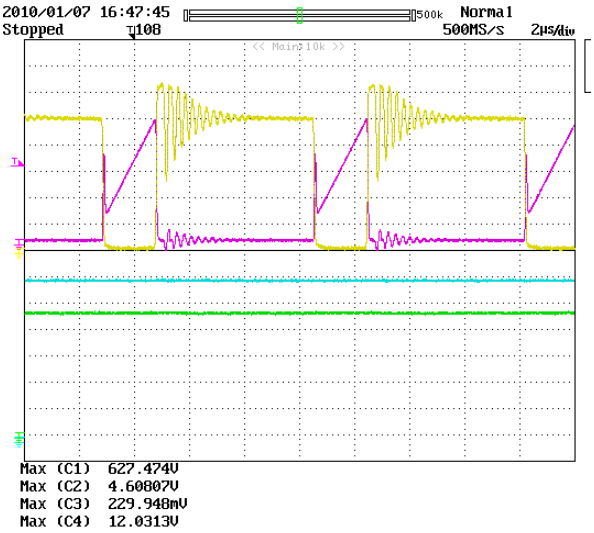

Figure 34– ~ 55.32 W at 264 VAC.
CH1: V_{DRAIN}, 100 V / div.
CH3: I_{DRAIN}, 0.25 A / div.
CH2: I_{OUT}, 1 A / div.
CH4: V_{OUT}, 2 V / div.

12.6 Voltage Stress

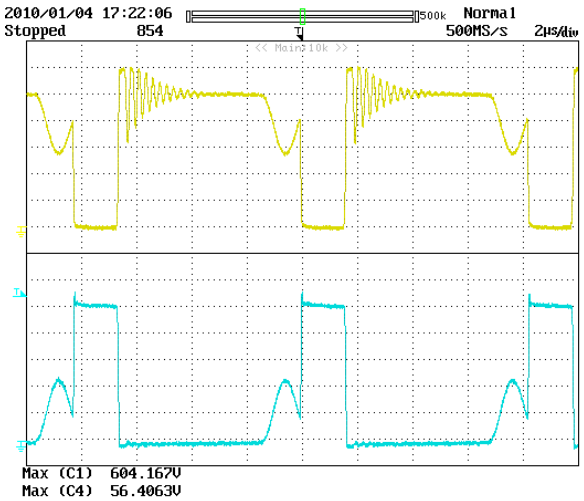

Figure 35 – 264 VAC Full Load.
V_{DRAIN}: 604.17 V.
PIVS: 56.41 V.

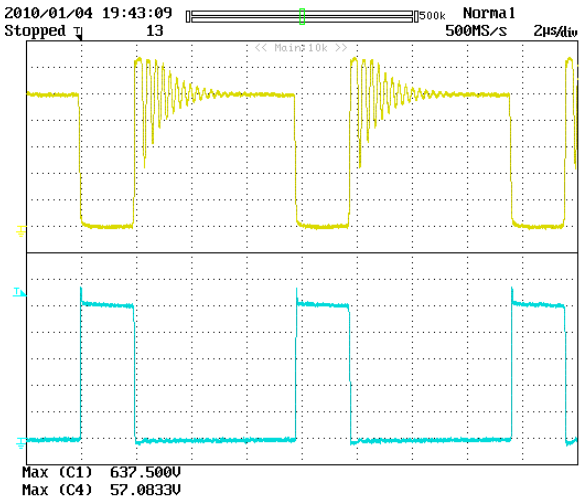

Figure 36 – 264 VAC Max Power.
V_{DRAIN}: 637.5 V.
PIVS: 57.08 V.

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12.7 Overvoltage Protection (Open Loop Test)

OVP is initiated by shorting the LED of U2. This constitutes an open loop condition and causes the output voltage, and bias voltage to rise. OVP is sensed in the primary by sensing the bias winding.

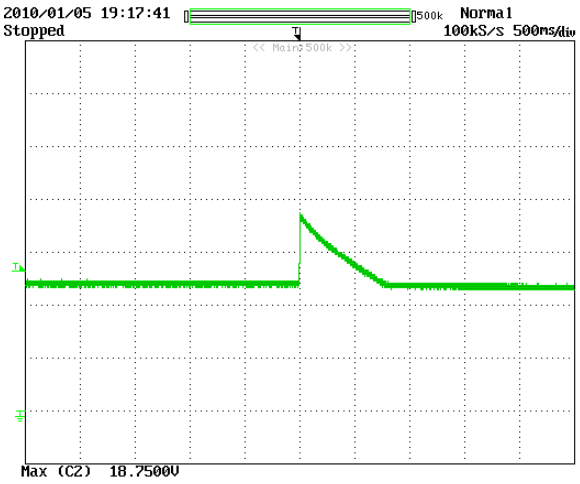

Figure 37 – OVP at 85 VAC, No-load.
OVP Trip Point = 18.75 V.

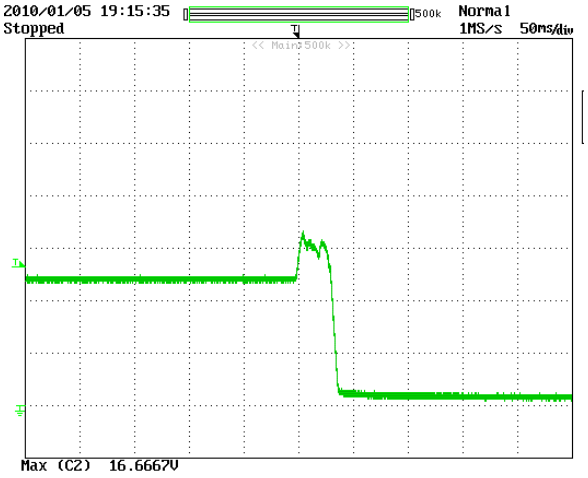

Figure 38 – OVP at 85 VAC, Full Load.
OVP Trip Point = 16.67 V.

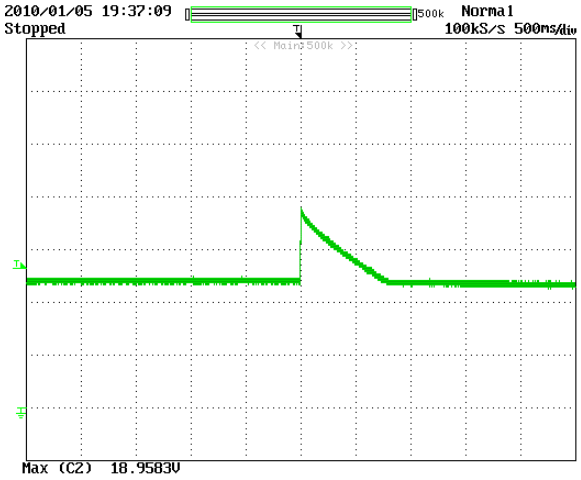

Figure 39 – OVP at 264 VAC, No-load.
OVP Trip Point = 18.96 V.

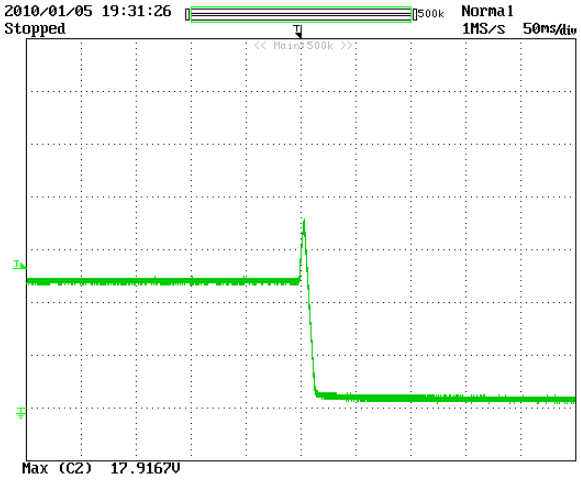

Figure 40 – OVP at 264 VAC, Full Load.
OVP Trip Point = 17.92 V.

12.8 Load Transient Response

In the figures shown below, the output was AC coupled to view the load transient response. The oscilloscope was triggered using the load current step as a trigger source.

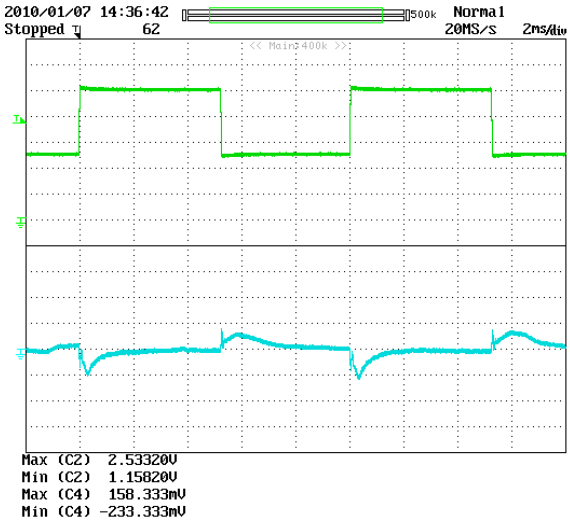

Figure 41 – Transient Response, 115 VAC, 50%↔100% Step Load. Top: Load Current, 0.5 A / div. Bottom: V_{OUT} , 200 mV / div. Time Scale: 2 ms / div.

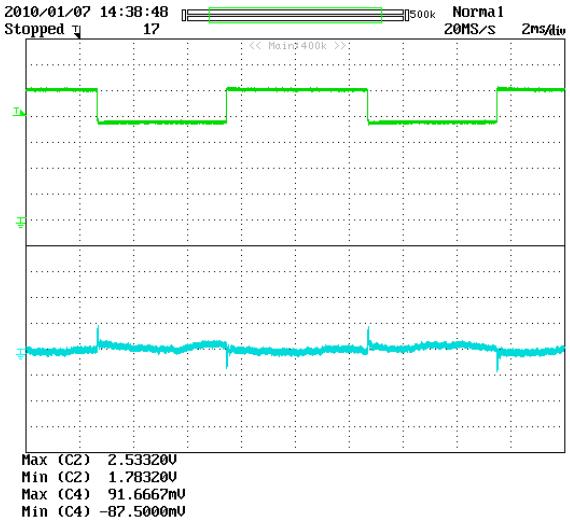

Figure 42 – Transient Response, 115 VAC, 75%↔100% Step Load. Top: Load Current, 0.5 A / div. Bottom: V_{OUT} , 100 mV / div. Time Scale: 2 ms / div.

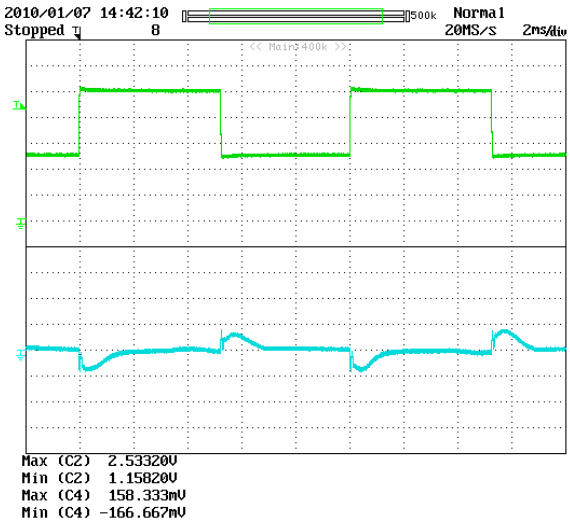

Figure 43 – Transient Response, 230 VAC 50%↔100% Step Load. Top: Load Current, 0.5 A / div. Bottom: V_{OUT} , 200 mV / div. Time Scale: 2 ms / div.

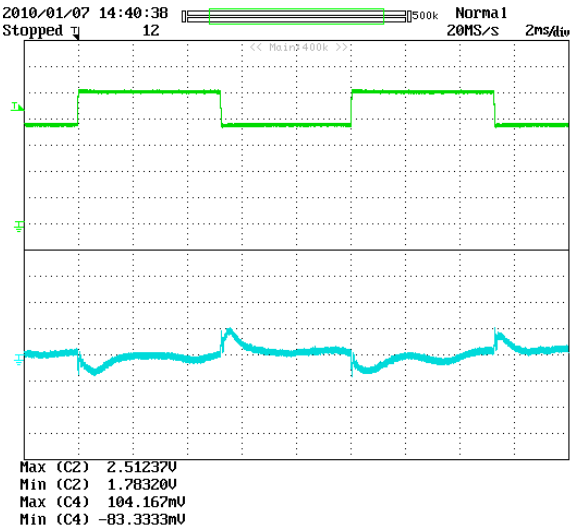

Figure 44 – Transient Response, 230 VAC, 75%↔100% Step Load. Top: Load Current, 0.5 A / div. Bottom: V_{OUT} , 100 mV / div. Time Scale: 2 ms / div.

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12.9 Output Ripple Measurements

12.9.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 47.0 μF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

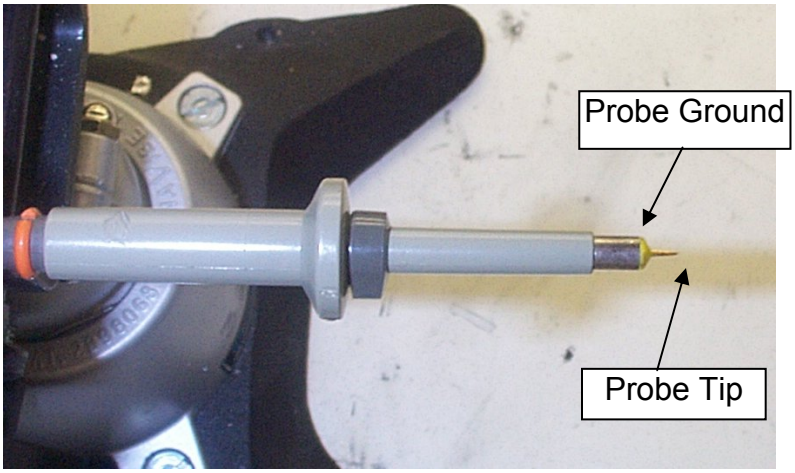

Figure 45 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

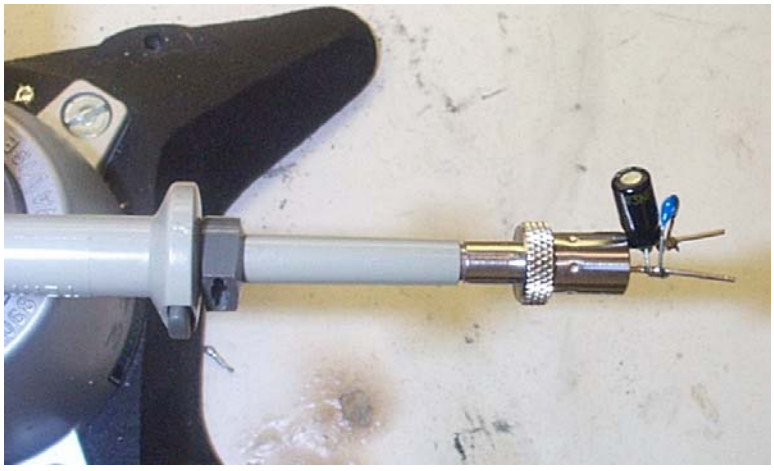

Figure 46 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter.
(Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

12.9.2 Ripple and Noise Measurement Results

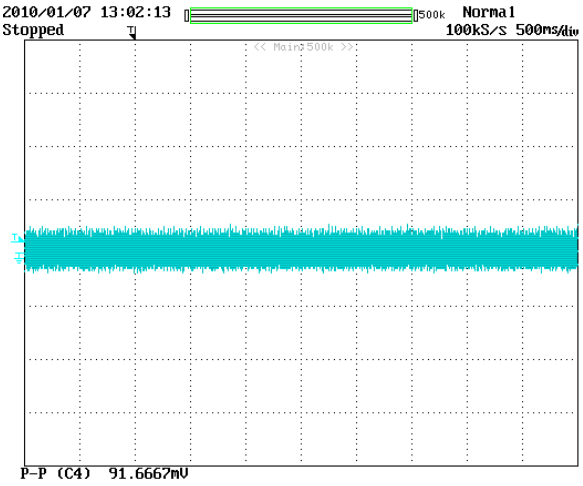

Figure 47 – Ripple, 85 VAC 47 Hz, Full Load.
500 ms, 100 mV / div.

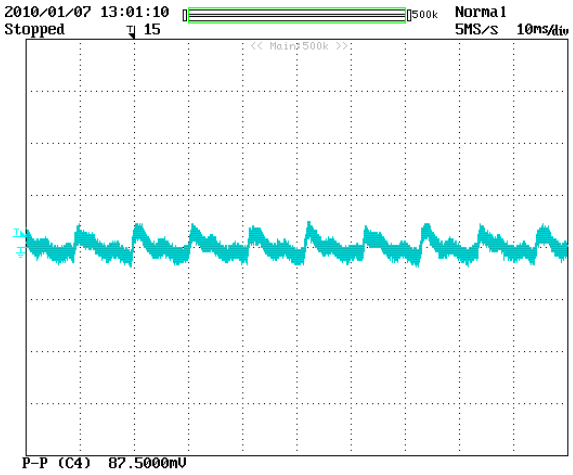

Figure 48 – Ripple, 85 VAC 47 Hz, Full Load.
10 ms, 100 mV / div.

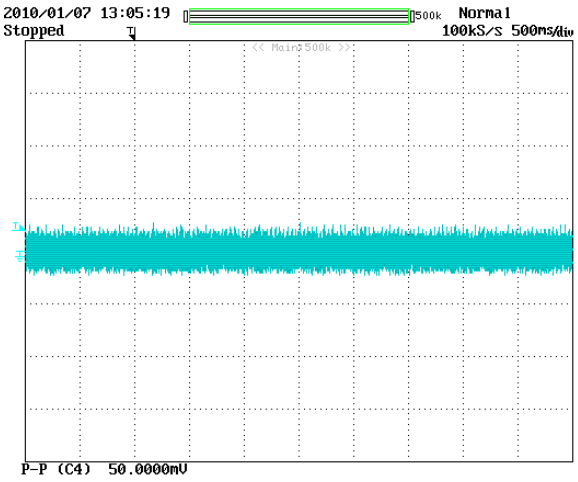

Figure 49 – Ripple, 264 VAC 50 Hz, Full Load.
500 ms, 50 mV /div.

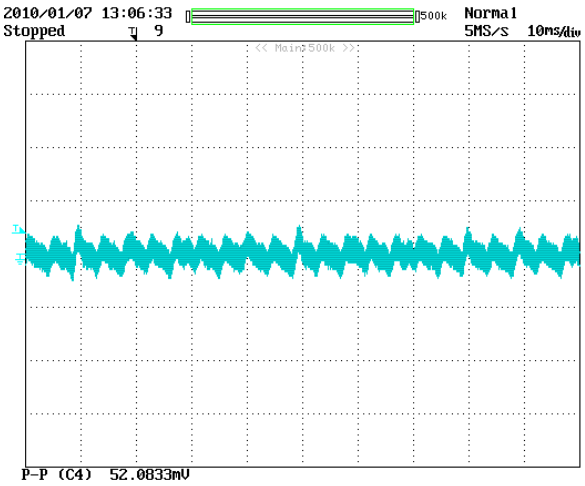

Figure 50 – Ripple, 264 VAC 50 Hz, Full Load.
10 ms, 50 mV /div.

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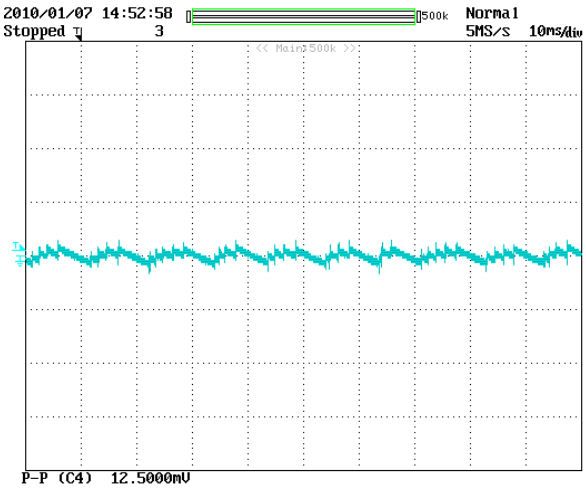

Figure 51 – Ripple, 85 VAC, No-load.
10 ms, 20 mV / div.

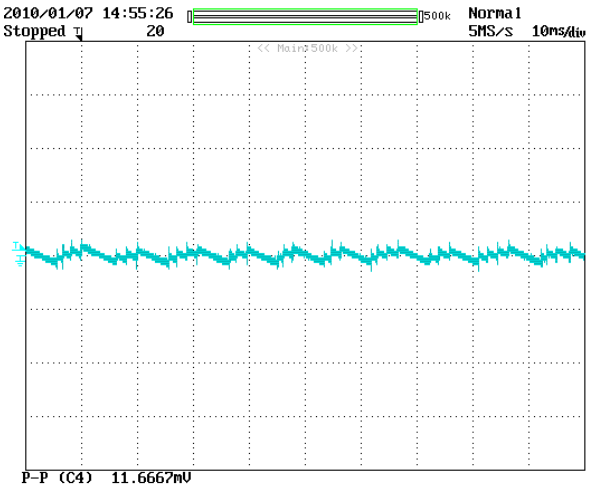

Figure 52 – Ripple, 115 VAC, No-load.
10 ms, 20 mV / div.

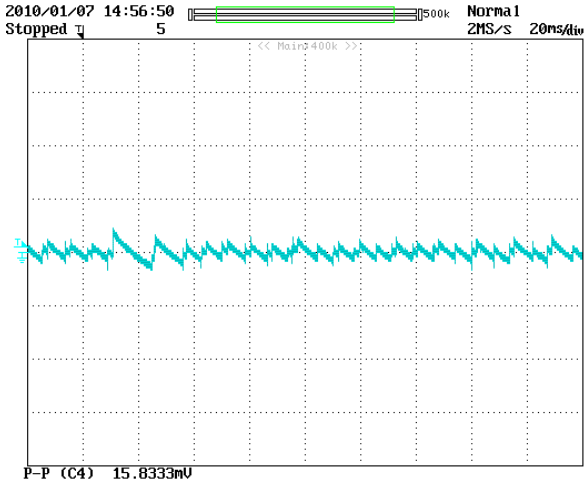

Figure 53– Ripple, 230 VAC, No-load.
10 ms, 20 mV / div.

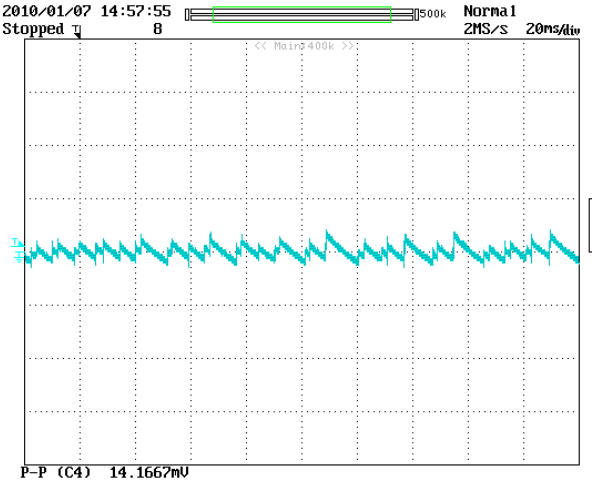

Figure 54 – Ripple, 264 VAC, No-load.
10 ms, 20 mV / div.

13 Control Loop Measurements

13.1 115 VAC Maximum Load

Figure 55 – Gain-Phase Plot, 115 VAC, Maximum Steady State Load.
Crossover Frequency = 3.5 kHz Phase Margin = 51.5°.

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13.2 230 VAC Maximum Load

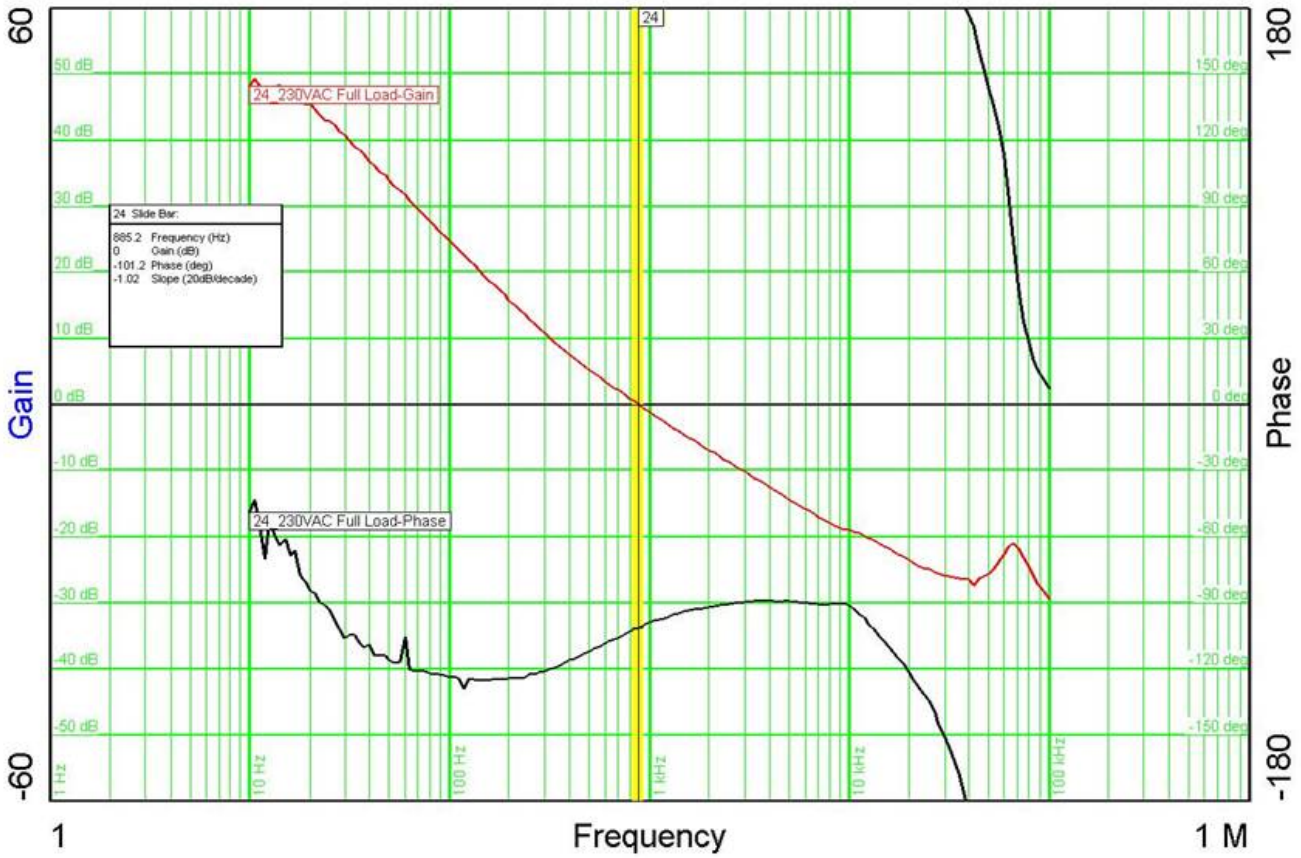

Figure 56 – Gain-Phase Plot, 230 VAC, Maximum Steady State Load.
Crossover Frequency = 637.8 Hz, Phase Margin = 71.7°.

14 Conducted EMI

Conducted EMI were measured using a resistive load of 4.8 Ω. Measurements were taken with output grounded and with output floating conditions. Quasi peak and average measurement have both ≥10 dB of margin to Class B limits.

14.1 Output Grounded

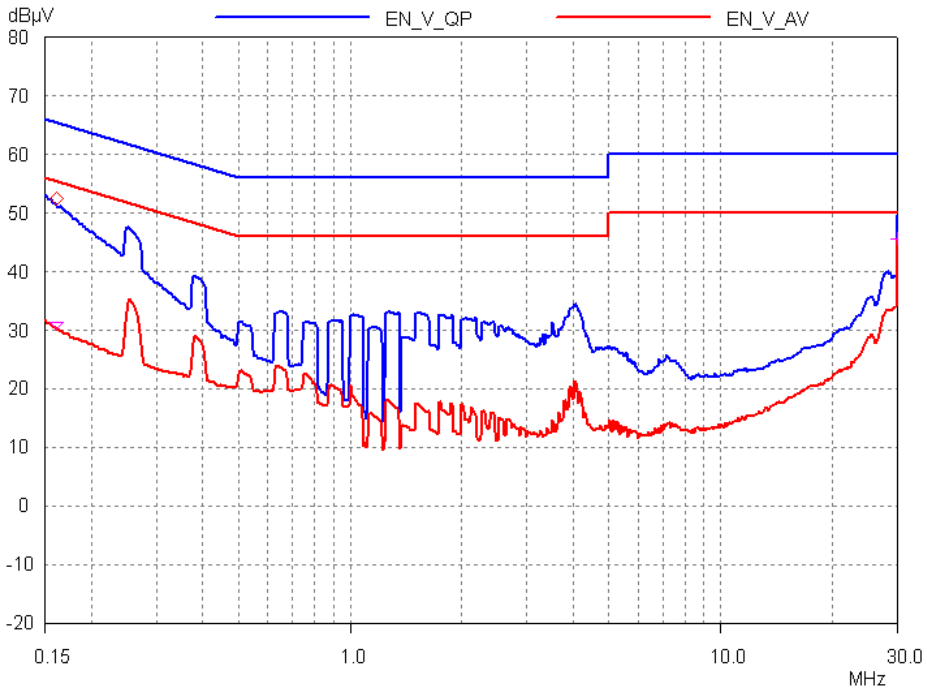

Figure 57 – Phase L1: Conducted EMI, Maximum Steady State Load, 115 VAC, 60 Hz, and EN55022 B Limits. Output Terminal Grounded.

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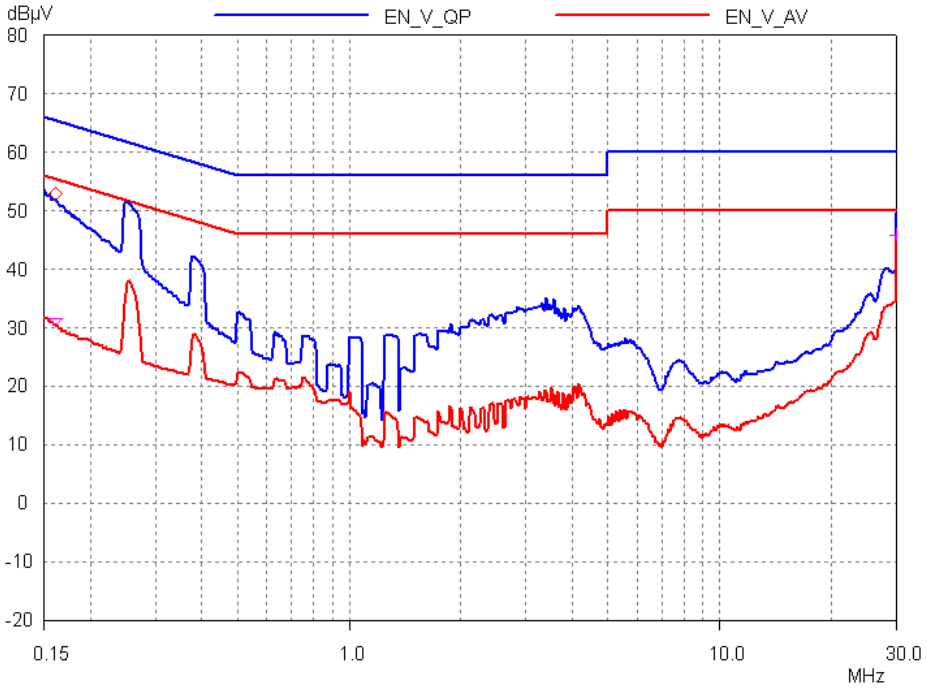

Figure 58 – Phase N: Conducted EMI, Maximum Steady State Load, 115 VAC, 60 Hz, and EN55022 B Limits. Output Terminal Grounded.

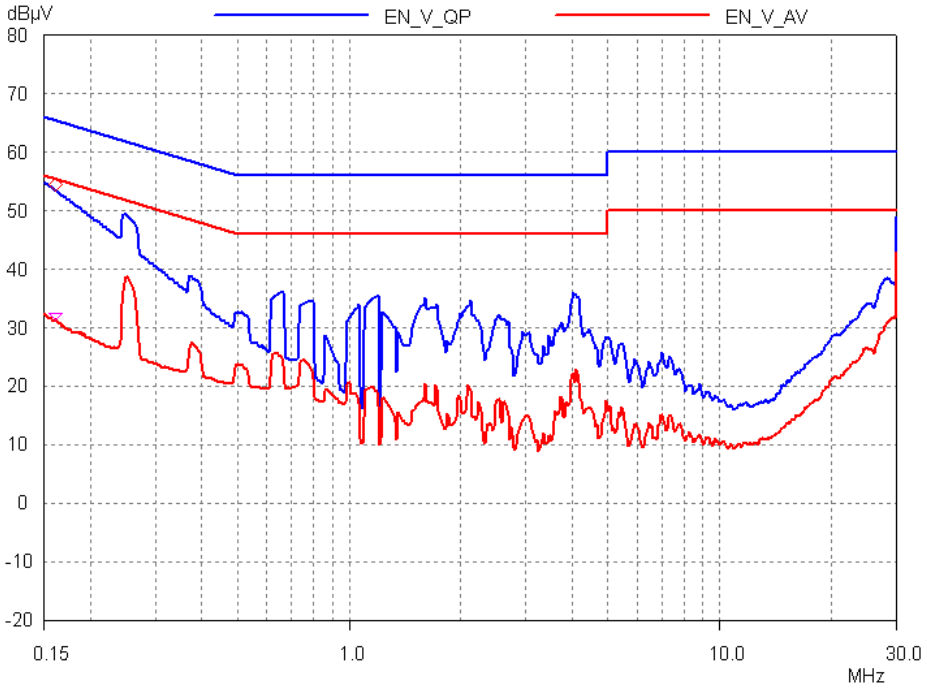

Figure 59 – Phase L1: Conducted EMI, Maximum Steady State Load, 230 VAC, 60 Hz, and EN55022 B Limits. Output Terminal Grounded

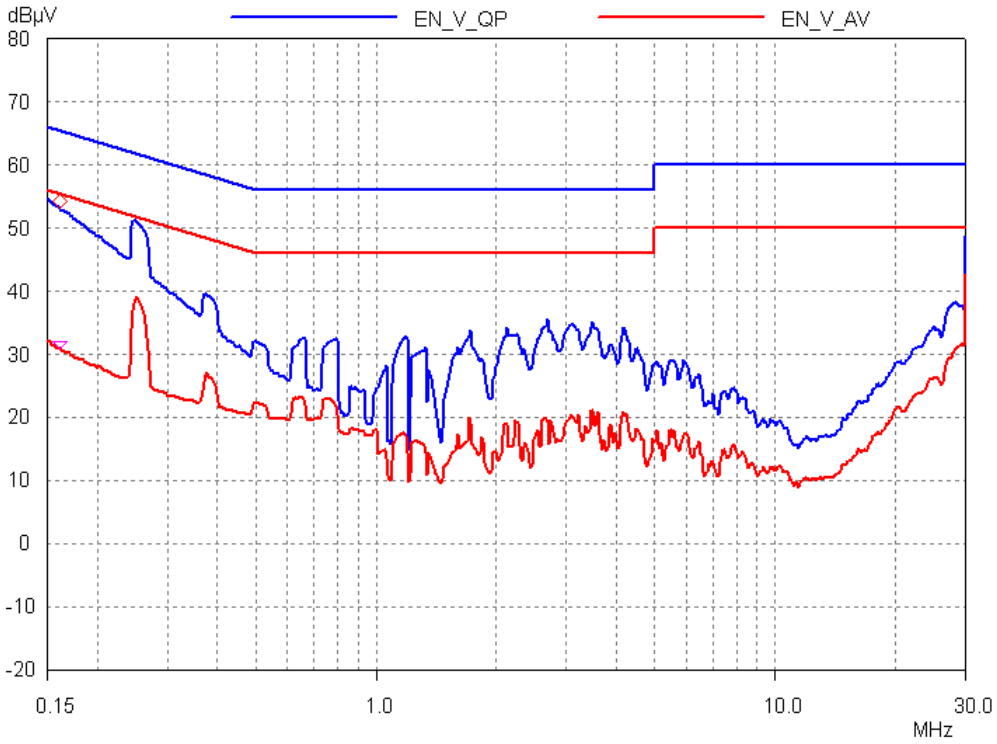

Figure 60 – Phase N: Conducted EMI, Maximum Steady State Load, 230 VAC, 60 Hz, and EN55022 B Limits. Output Terminal Grounded.

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14.2 Output Floating

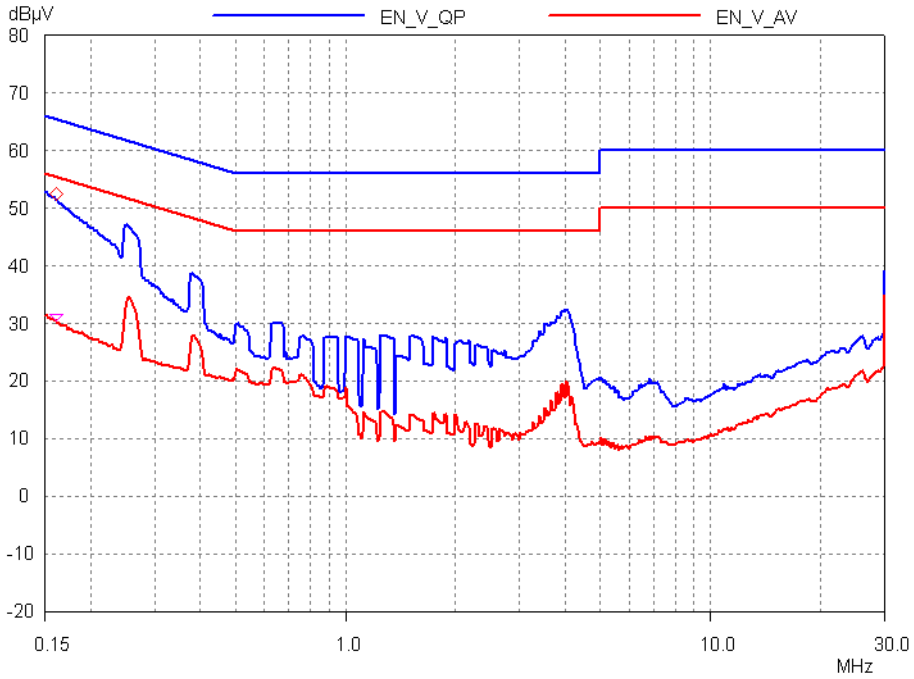

Figure 61 – Phase L1: Conducted EMI, Maximum Steady State Load, 115 VAC, 60 Hz, and EN55022 B Limits. Output Terminal Floating.

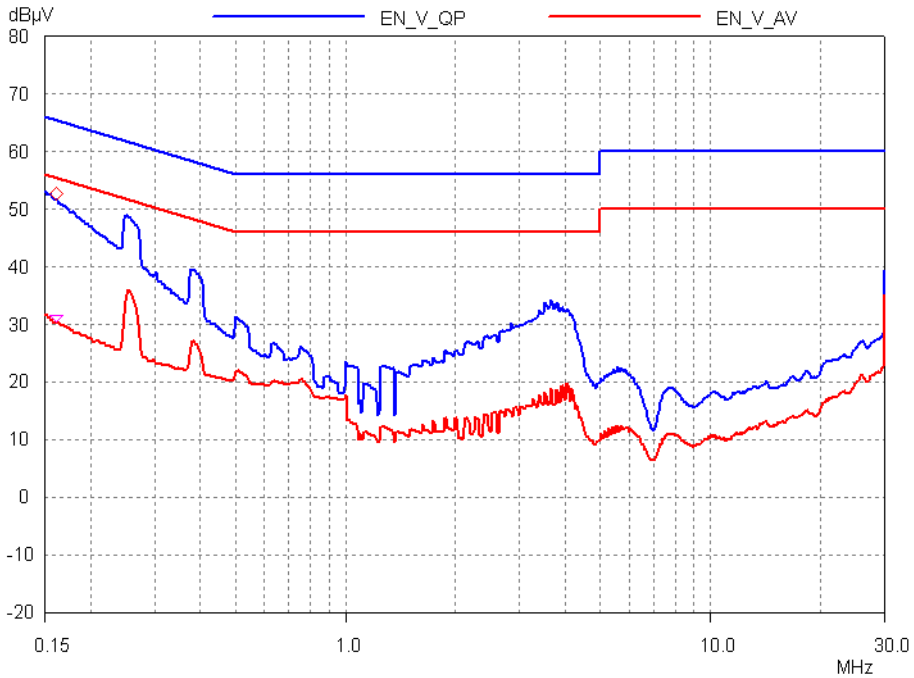

Figure 62 – Phase N: Conducted EMI, Maximum Steady State Load, 115 VAC, 60 Hz, and EN55022 B Limits. Output Terminal Floating.

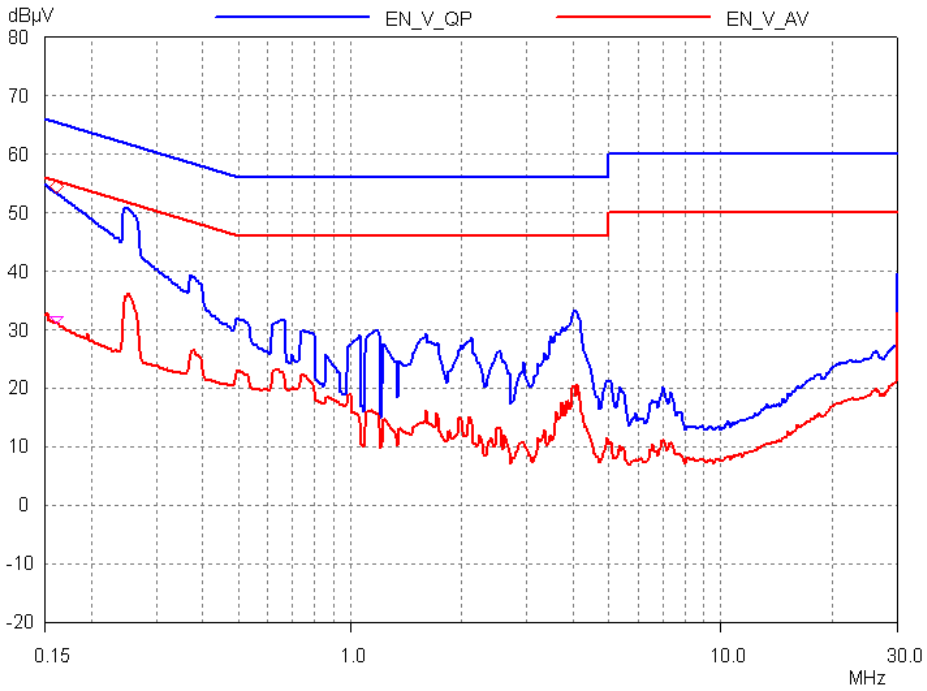

Figure 63 – Phase L1: Conducted EMI, Maximum Steady State Load, 230 VAC, 60 Hz, and EN55022 B Limits. Output Terminal Floating.

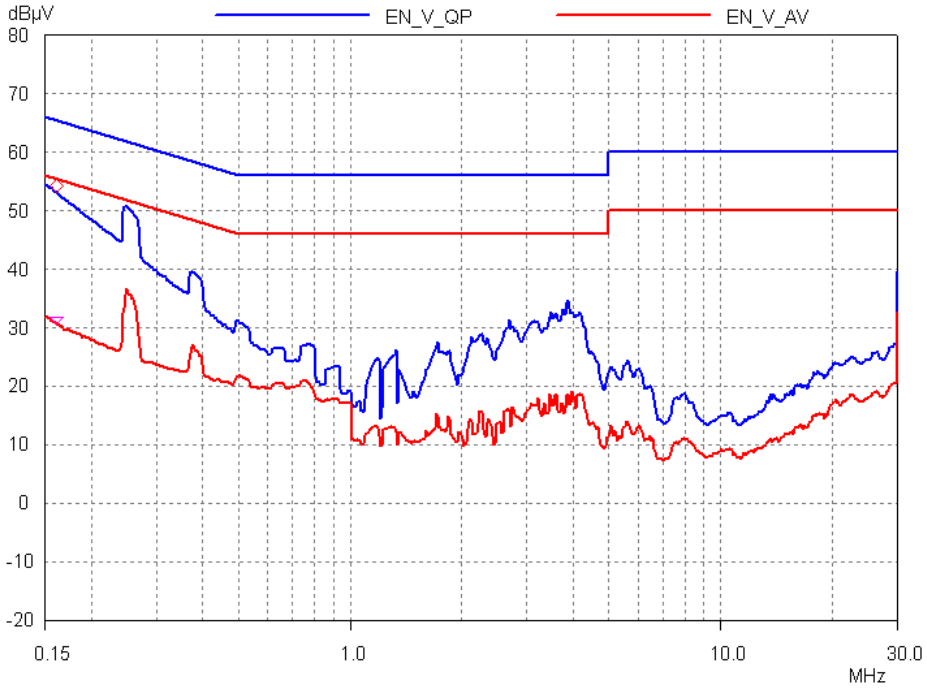

Figure 64 – Phase N: Conducted EMI, Maximum Steady State Load, 230 VAC, 60 Hz, and EN55022 B Limits. Output Terminal Floating.

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15 AC Surge

The input voltage for the supply under test was 115 VAC and 230 VAC, and the supply was loaded to the maximum continuous output power using resistive loads on each output. An LED was used to monitor the presence of output voltage and to detect output interruptions. A test failure was defined as a non-recoverable interruption of output voltage requiring supply repair or recycling of input AC voltage.

15.1 Common Mode Surge, 1.2 / 50 μsec

Surge Voltage (kV)	Phase Angle (°)	Generator Impedance (Ω)	Number of Strikes	Test Result
2	90	12	10	PASS
2	270	12	10	PASS
2.2	90	12	10	PASS
2.2	270	12	10	PASS
2.4	90	12	10	PASS
2.4	270	12	10	PASS

15.2 Differential Mode Surge, 1.2 / 50 μsec

Surge Voltage (kV)	Phase Angle (°)	Generator Impedance (Ω)	Number of Strikes	Test Result
1	90	2	10	PASS
1	270	2	10	PASS
1.2	90	2	10	PASS
1.2	270	2	10	PASS

16 Appendix A: Fast AC Reset

The TOPSwitch-JX family has a simplified fast AC Reset Function which can be configured on the X pin. Should a latching OVP condition occur, the circuit below connected to the X pin will force I_X to exceed $I_{X(TH)}$ = -27 μA (typ) and reset the latch when the AC input is disconnected or falls below a set threshold value.

In the circuit below R1, R2 and C1 sets the time after AC is removed before the latch is reset. A higher gain BJT Q_R is desirable to allow using a higher resistance R1 and lower capacitance C1, and thus minimize the circuit dissipation.

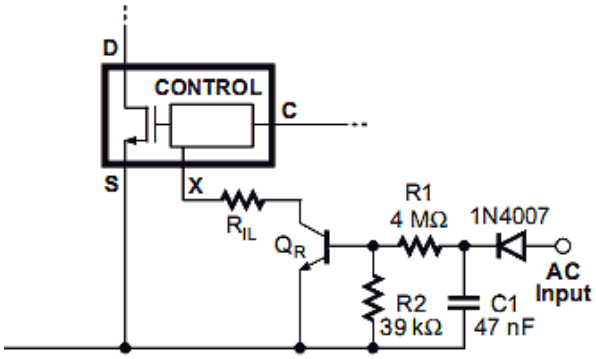

Figure 65 – Fast AC Reset Circuit Implementation for TOPSwitch-JX.

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17 Appendix B: Circuit Modification for Reduced No-load Input Power and Enhanced Output OVP Performance

The TOPSwitch-JX family is designed to achieve very low no-load input power by reducing the CONTROL pin current $I_{C(OFF)}$ = 3.5 mA (typical for TOP266VG, 132 kHz) during MCM operation. The value of $I_{C(OFF)}$ and the bias voltage dictates the power loss in the primary control circuit which contributes to no-load input power losses. This primary circuit loss can be optimized by properly selecting bias voltage to be low enough to minimize the V_{BIAS} x $I_{C(OFF)}$ product but high enough to maintain supply on the CONTROL pin, typically $V_{BIAS(VALLEY)}$ ~7 V. Note that the bias voltage is at minimum during no-load condition at highest AC input/

Another circuit block to look for power savings is the secondary control circuit dissipation during no-load. Power loss associated with the secondary control circuit is related to the output voltage and the control current that flows in the optocoupler diode. The optocoupler diode current is inversely proportional to the CTR of the optocoupler (I_{DOPTO} ~ $I_{C(OFF)}$/CTR), and therefore a higher CTR optocoupler will result in lower secondary side power consumption. In the circuit below, Q2 is added to form a Darlington pair with the optocoupler transistor which now gives a very high equivalent CTR and thus reduces the optocoupler current. This configuration will dramatically improve the no-load power loss savings as shown in the data below. Note that this configuration will result in a higher open loop gain and thus compensation circuit must be redesigned to maintain the necessary stability margins (increasing the value of R19).

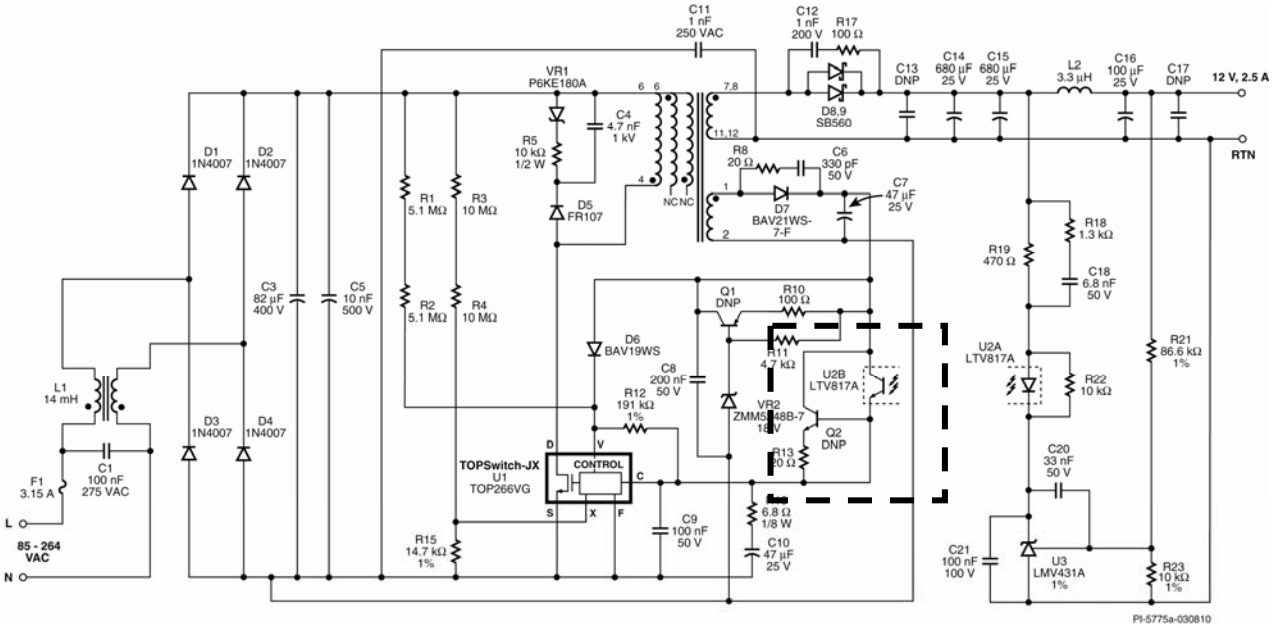

Figure 66 – Optocoupler Darlington Configuration to Reduce Feedback Current and No-load Input Power.

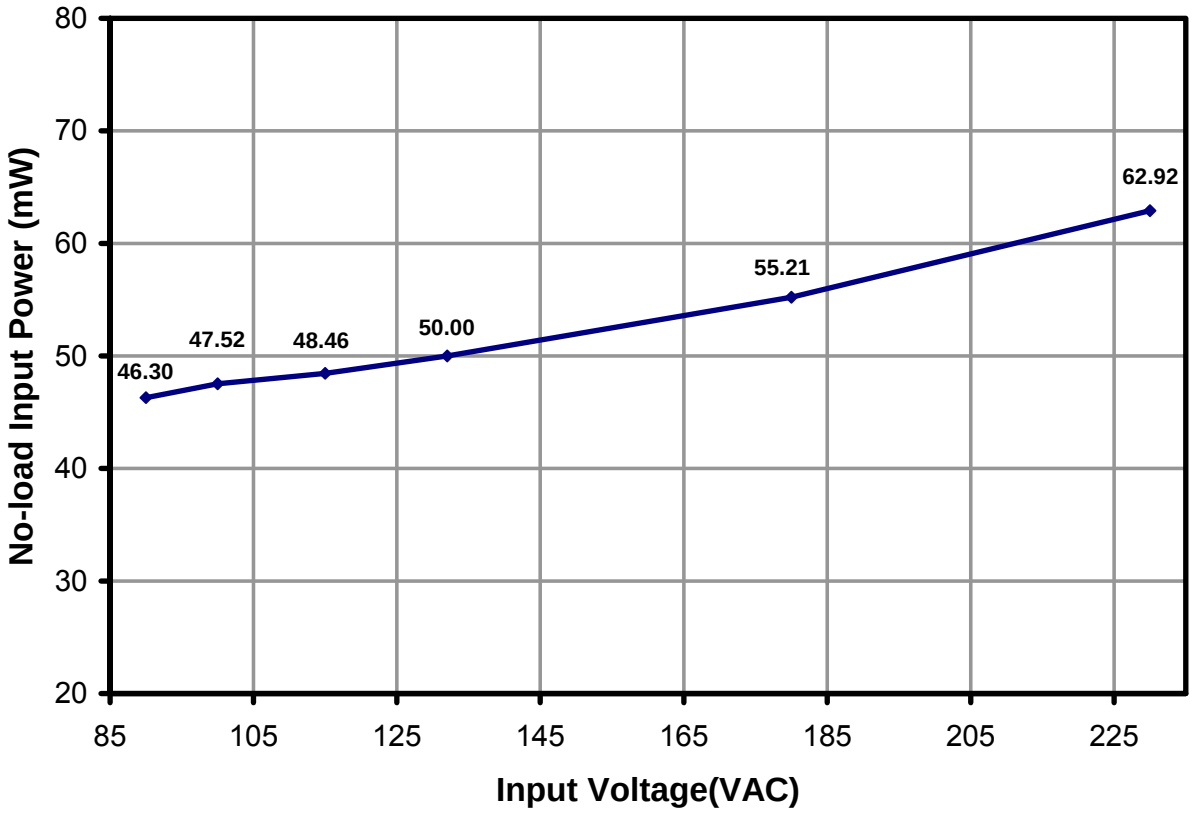

Figure 67 – Zero Load Input Power with Darlington Configuration.

V_{OUT}	Input Line	P_{IN} (mW)
12	85 V / 50 Hz	46.30
12	100 V / 50 Hz	47.52
12	115 V / 60 Hz	48.46
12	132 V / 60 Hz	50.00
12	180 V / 50 Hz	55.21
12	230 V / 50 Hz	62.92
12	240 V / 50 Hz	64.28
12	264 V / 50 Hz	67.17

Table 4 – No-load Input Power vs. Input Voltage.

17.1 Enhanced Output OVP Latch Sensitivity

The network of Q1, R10, R100, C8, and VR2 in Figure 66 guarantees that OVP will latch during low-line over load condition. This circuit will ensure that the required latching current $I_{OV(LS)}$ = 336 μA (typ) is delivered to the V pin for at least 100 μs.

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18 Revision History

Date	Author	Revision	Description & changes	Reviewed
01-Mar-10	CA	1.2	Initial Release	Apps & Mktg

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