

HCPL3700

AC/DC to Logic Interface Optocoupler

Features

- AC or DC input
- Programmable sense voltage
- Logic level compatibility
- Threshold guaranteed over temperature (0°C to 70°C)
- Optoplanar™ construction for high common mode immunity
- UL recognized (file # E90700)
- VDE certified – ordering option 'V', e.g., HCPL3700V

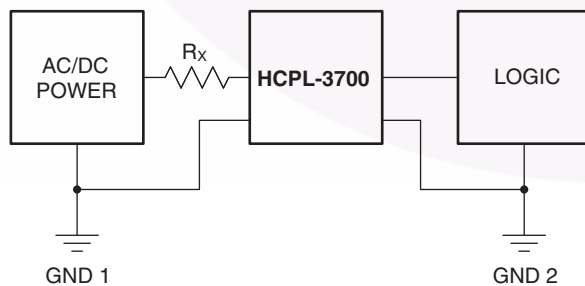
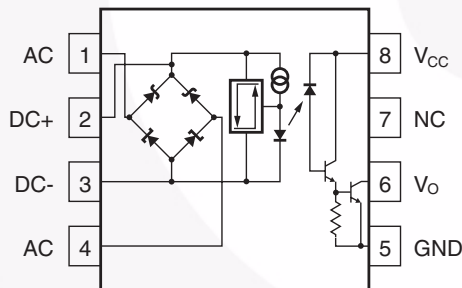
Applications

- Low voltage detection
- 5 V to 240 V AC/DC voltage sensing
- Relay contact monitor
- Current sensing
- Microprocessor Interface
- Industrial controls

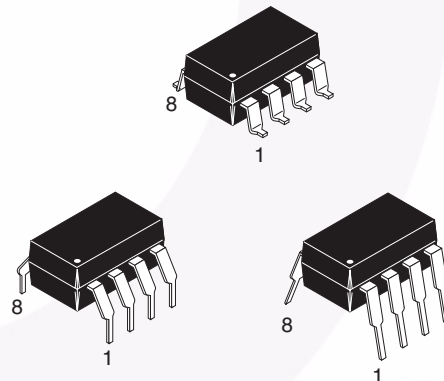
Description

The HCPL-3700 voltage/current threshold detection optocoupler consists of an AlGaAs LED connected to a threshold sensing input buffer IC which are optically coupled to a high gain darlington output. The input buffer chip is capable of controlling threshold levels over a wide range of input voltages with a single resistor. The output is TTL and CMOS compatible.

Schematics



Package Outlines



TRUTH TABLE
(Positive Logic)

| Input | Output |
|-------|--------|
| H | L |
| L | H |

A 0.1µF bypass capacitor must be connected between pins 8 and 5.

Absolute Maximum Ratings (No derating required up to 70°C)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | | Value | Units |
|------------------|--|-----------------------------------|----------------|-------|
| T _{STG} | Storage Temperature | | -55 to +125 | °C |
| T _{OPR} | Operating Temperature | | -40 to +85 | °C |
| T _{SOL} | Lead Solder Temperature | | 260 for 10 sec | °C |
| EMITTER | | | | |
| I _{IN} | Input Current | Average | 50 (Max.) | mA |
| | | Surge, 3ms, 120Hz Pulse Rate | 140 (Max.) | |
| | | Transient, 10µs, 120Hz Pulse Rate | 500 (Max.) | |
| V _{IN} | Input Voltage (Pins 2-3) | | -0.5 (Max.) | V |
| P _{IN} | Input Power Dissipation ⁽¹⁾ | | 230 (Max.) | mW |
| P _T | Total Package Power Dissipation ⁽²⁾ | | 305 (Max.) | mW |
| DETECTOR | | | | |
| I _O | Output Current (Average) ⁽³⁾ | | 30 (Max.) | mA |
| V _{CC} | Supply Voltage (Pins 8-5) | | -0.5 to 20 | V |
| V _O | Output Voltage (Pins 6-5) | | -0.5 to 20 | V |
| P _O | Output Power Dissipation ⁽⁴⁾ | | 210 (Max.) | mW |

Notes:

1. Derate linearly above 70°C free-air temperature at a rate of 1.8 mW/°C.
2. Derate linearly above 70°C free-air temperature at a rate of 2.5 mW/°C.
3. Derate linearly above 70°C free-air temperature at a rate of 0.6 mA/°C.
4. Derate linearly above 70°C free-air temperature at a rate of 1.9 mW/°C.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Min. | Max. | Units |
|-----------------|-----------------------|------|------|-------|
| V _{CC} | Supply Voltage | 2 | 18 | V |
| T _A | Operating Temperature | 0 | 70 | °C |
| f | Operating Frequency | 0 | 4 | kHz |

Electrical Characteristics ($T_A = 0^\circ\text{C}$ to 70°C Unless otherwise specified)

| Symbol | Parameter | | Test Conditions | Min. | Typ. | Max. | Unit |
|------------|------------------------------|------------------|---|------|-------|------|---------------|
| I_{TH+} | Input Threshold Current | | $V_{IN} = V_{TH+}$, $V_{CC} = 4.5\text{ V}$ | 1.96 | 2.4 | 3.11 | mA |
| I_{TH-} | | | $V_O = 0.4\text{ V}$, $I_O \geq 4.2\text{ mA}^{(5)}$ | 1.00 | 1.2 | 1.62 | mA |
| V_{TH+} | Input Threshold Voltage | DC (Pins 2,3) | $V_{IN} = V_2 - V_3$ (Pins 1 & 4 Open) $V_{CC} = 4.5\text{ V}$, $V_O = 0.4\text{ V}^{(5)}$ $I_O \geq 4.2\text{ mA}$ | 3.35 | 3.8 | 4.05 | V |
| V_{TH-} | | | $V_{IN} = V_2 - V_3$ (Pins 1 & 4 Open) $V_{CC} = 4.5\text{ V}$, $V_O = 2.4\text{ V}^{(5)}$ $I_O \geq 100\mu\text{A}$ | 2.01 | 2.5 | 2.86 | V |
| V_{TH+} | | AC (Pins 1,4) | $ V_{IN} = V_1 - V_4 $ (Pins 2 & 3 Open) $V_{CC} = 4.5\text{ V}$, $V_O = 0.4\text{ V}^{(5)}$ $I_O \geq 4.2\text{ mA}$ | 4.23 | 5.0 | 5.50 | V |
| V_{TH-} | | | $ V_{IN} = V_1 - V_4 $ (Pins 2 & 3 Open) $V_{CC} = 4.5\text{ V}$, $V_O = 2.4\text{ V}^{(5)}$ $I_O \leq 100\mu\text{A}$ | 2.87 | 3.7 | 4.20 | V |
| I_{HYS} | Hysteresis | | $I_{HYS} = I_{TH+} - I_{TH-}$ | | 1.2 | | mA |
| V_{HYS} | | | $V_{HYS} = V_{TH+} - V_{TH-}$ | | 1.3 | | V |
| V_{IHC1} | Input Clamp Voltage | | $V_{IHC1} = V_2 - V_3$, $V_3 = \text{GND}$ $I_{IN} = 10\text{ mA}$, Pins 1 & 4 connected to Pin 3 | 5.4 | 6.3 | 6.6 | V |
| V_{IHC2} | | | $V_{IHC2} = V_1 - V_4 $, $ I_{IN} = 10\text{ mA}$ (Pins 2 & 3 Open) | 6.1 | 7.0 | 7.3 | V |
| V_{IHC3} | | | $V_{IHC3} = V_2 - V_3$, $V_3 = \text{GND}$, $I_{IN} = 15\text{ mA}$ (Pins 1 & 4 Open) | | 12.5 | 13.4 | V |
| V_{ILC} | | | $V_{ILC} = V_2 - V_3$, $V_3 = \text{GND}$, $I_{IN} = -10\text{ mA}$ | | -0.75 | | V |
| I_{IN} | Input Current | | $V_{IN} = V_2 - V_3 = 5.0\text{ V}$ (Pins 1 & 4 Open) | 3.0 | 3.7 | 4.4 | mA |
| $V_{D1,2}$ | Bridge Diode Forward Voltage | | $I_{IN} = 3\text{ mA}$ | | 0.65 | | V |
| $V_{D3,4}$ | | | $I_{IN} = 3\text{ mA}$ | | 0.65 | | V |
| V_{OL} | Logic LOW Output Voltage | | $V_{CC} = 4.5\text{ V}$, $I_{OL} = 4.2\text{ mA}^{(5)}$ | | 0.04 | 0.4 | V |
| I_{OH} | Logic HIGH Output Current | | $V_{OH} = V_{CC} = 18\text{ V}^{(5)}$ | | | 100 | μA |
| I_{CCL} | Logic LOW Supply Current | | $V_2 - V_3 = 5.0\text{ V}$, $V_O = \text{Open}$, $V_{CC} = 5\text{ V}$ | | 1.0 | 4 | mA |
| I_{CCH} | Logic HIGH Supply Current | | $V_{CC} = 18\text{ V}$, $V_O = \text{Open}$ | | 0.01 | 4 | μA |
| C_{IN} | Input Capacitance | | $f = 1\text{ MHz}$, $V_{IN} = 0\text{ V}$ (Pins 2 & 3, Pins 1 & 4 Open) | | 50 | | pF |

Note:

5. Logic LOW output level at pin 6 occurs when $V_{IN} \geq V_{TH+}$ and when $V_{IN} > V_{TH-}$ once V_{IN} exceeds V_{TH+} .
 Logic HIGH output level at pin 6 occurs when $V_{IN} \leq V_{TH-}$ and when $V_{IN} < V_{TH+}$ once V_{IN} decreases below V_{TH-} .

Switching Characteristics ($T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$ Unless otherwise specified)

| Symbol | AC Characteristics | Test Conditions | Min. | Typ. | Max. | Unit |
|------------|---|--|------|------|------|------------------------|
| T_{PHL} | Propagation Delay Time (to Output Low Level) | $R_L = 4.7\text{k}\Omega$, $C_L = 30\text{pF}^{(6)}$ | | 6.0 | 15 | μs |
| T_{PLH} | Propagation Delay Time (to Output High Level) | $R_L = 4.7\text{k}\Omega$, $C_L = 30\text{pF}^{(6)}$ | | 25.0 | 40 | μs |
| t_r | Output Rise Time (10–90%) | $R_L = 4.7\text{k}\Omega$, $C_L = 30\text{pF}$ | | 45 | | μs |
| t_f | Output Fall Time (90–10%) | $R_L = 4.7\text{k}\Omega$, $C_L = 30\text{pF}$ | | 0.5 | | μs |
| ICM_{HI} | Common Mode Transient Immunity (at Output High Level) | $I_{IN} = 0\text{ mA}$, $R_L = 4.7\text{k}\Omega$, $V_{O\text{ min}} = 2.0\text{ V}$, $V_{CM} = 1400\text{V}^{(7)(8)}$ | | 4000 | | $\text{V}/\mu\text{s}$ |
| ICM_{LI} | Common Mode Transient Immunity (at Output Low Level) | $I_N = 3.11\text{mA}$, $R_L = 4.7\text{k}\Omega$, $V_{O\text{ max}} = 0.8\text{V}$, $V_{CM} = 140\text{V}^{(7)(8)}$ | | 600 | | $\text{V}/\mu\text{s}$ |

Package Characteristics ($T_A = 0^\circ\text{C}$ to 70°C Unless otherwise specified)

| Symbol | Characteristics | Test Conditions | Min. | Typ. | Max. | Unit |
|-----------|-------------------------------|--|------|-----------|------|-------------|
| V_{ISO} | Withstand Insulation Voltage | Relative humidity < 50%, $T_A = 25^\circ\text{C}$, $t = 1\text{ min}$, $I_{I-O} \leq 2\mu\text{A}^{(9)(10)}$ | 2500 | | | V_{RMS} |
| R_{I-O} | Resistance (input to output) | $V_{IO} = 500\text{Vdc}^{(9)}$ | | 10^{12} | | Ω |
| C_{I-O} | Capacitance (input to output) | $f = 1\text{MHz}$, $V_{IO} = 0\text{Vdc}$ | | 0.6 | | pF |

Notes:

- T_{PHL} propagation delay is measured from the 2.5V level of the leading edge of a 5.0V input pulse (1 μs rise time) to the 1.5 V level on the leading edge of the output pulse. T_{PLH} propagation delay is measured on the trailing edges of the input and output pulse. (Refer to Fig. 9)
- Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse signal V_{CM} , to assure that the output will remain in a logic high state (i.e., $V_O > 2.0\text{ V}$). Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{CM} , to assure that the output will remain in a logic low state (i.e., $V_O < 0.8\text{ V}$). Refer to Fig. 10.
- In applications where dV_{cm}/dt may exceed 50,000 $\text{V}/\mu\text{s}$ (Such as static discharge), a series resistor, R_{CC} , should be included to protect the detector chip from destructive surge currents. The recommended value for R_{CC} is 240V per volt of allowable drop in V_{CC} (between pin 8 and V_{CC}) with a minimum value of 240 Ω .
- Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
- The 2500 $V_{RMS}/1\text{ min.}$ capability is validated by a 3.0 $\text{kV}_{RMS}/1\text{ sec.}$ dielectric voltage withstand test.
- AC voltage is instantaneous voltage for V_{TH+} & V_{TH-} .
- All typicals at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$ unless otherwise specified.

Typical Performance Curves

Fig. 1 Logic Low Supply Current vs. Operating Supply Voltage

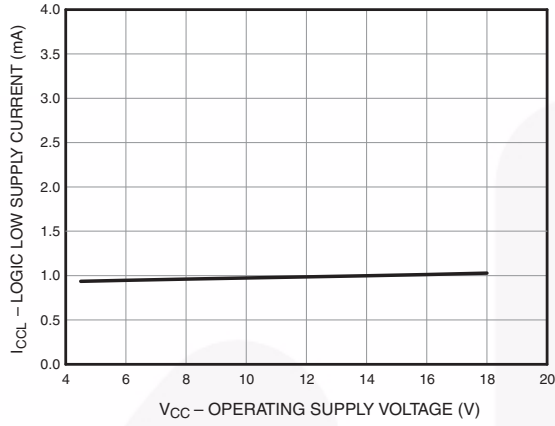


Fig. 2 Input Current vs. Input Voltage

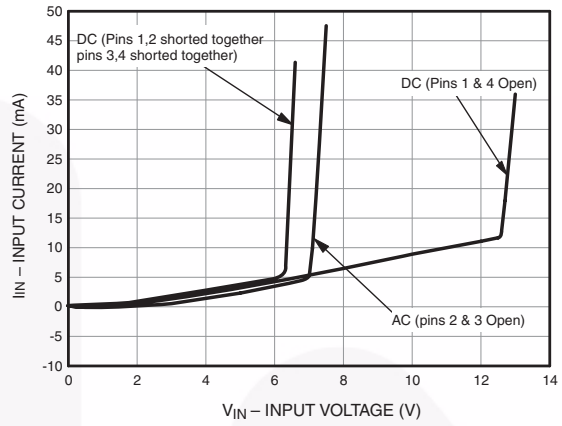


Fig. 3 Input Current/Low Level Output Voltage vs. Temperature

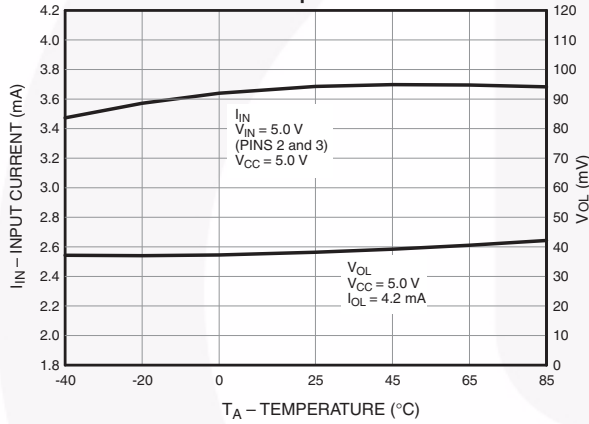


Fig. 4 Current Threshold/Voltage Threshold vs. Temperature

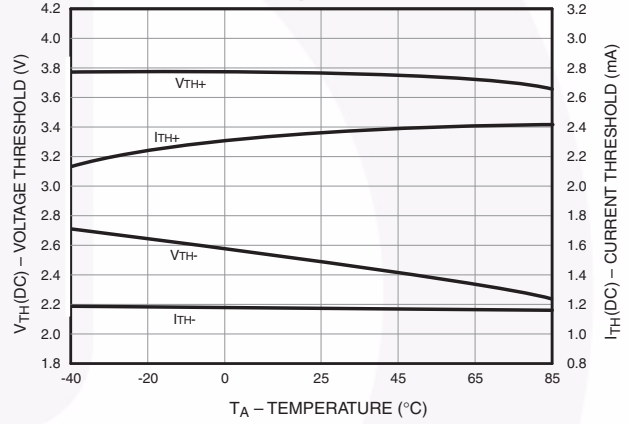


Fig. 5 Propagation Delay vs. Temperature

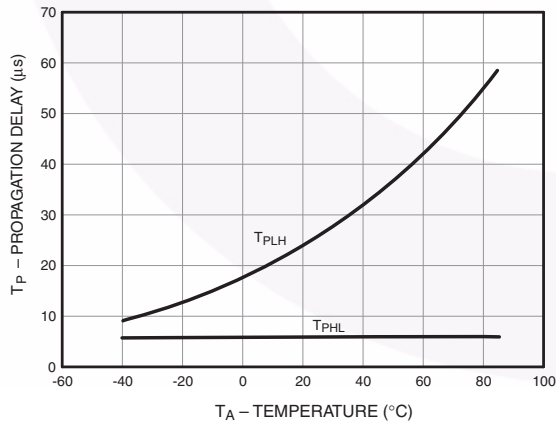
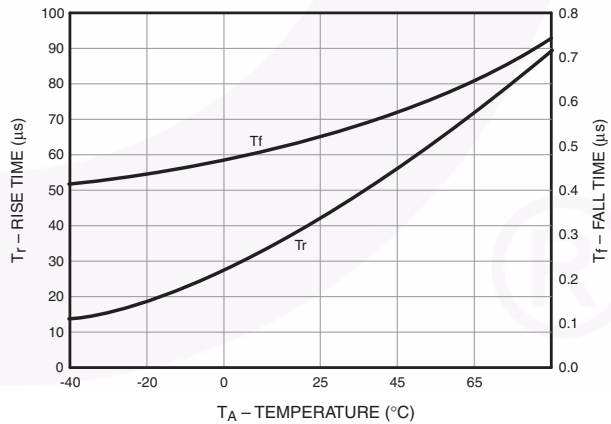


Fig. 6 Rise and Fall Time vs. Temperature



Typical Performance Curves (Continued)

Fig. 7 Logic High Supply Current vs. Temperature

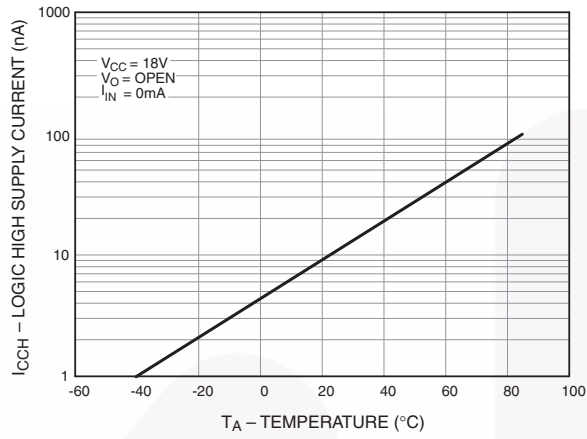
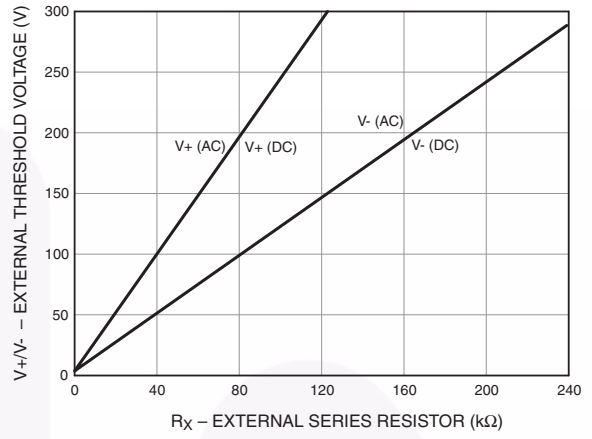
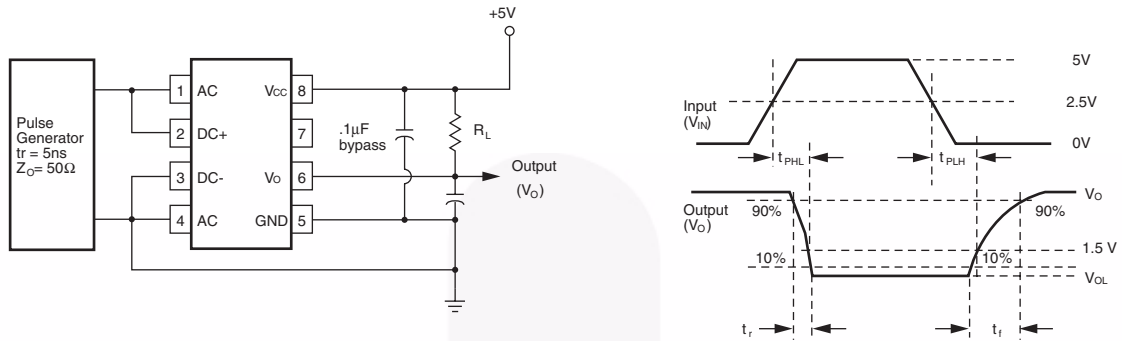


Fig. 8 External Threshold Characteristics V+/V- vs. R_x



Test Circuits



V_{IN}
 Pulse Amplitude = 50V
 Pulse Width = 1ms
 $f = 100\text{Hz}$
 $T_r = T_f = 1.0\mu\text{s}$ (10%–90%)

Fig. 9. Switching Test Circuit

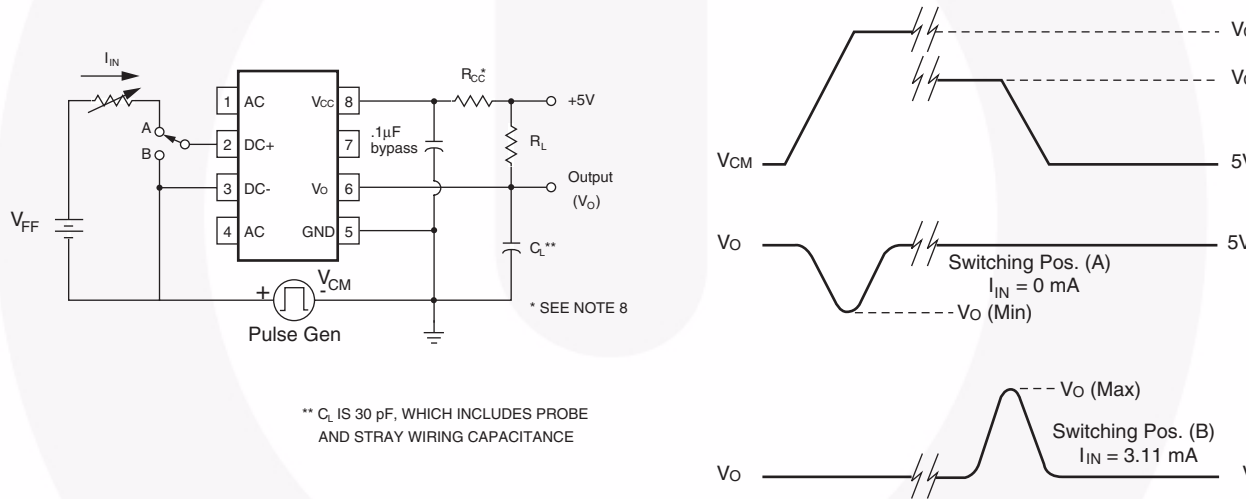
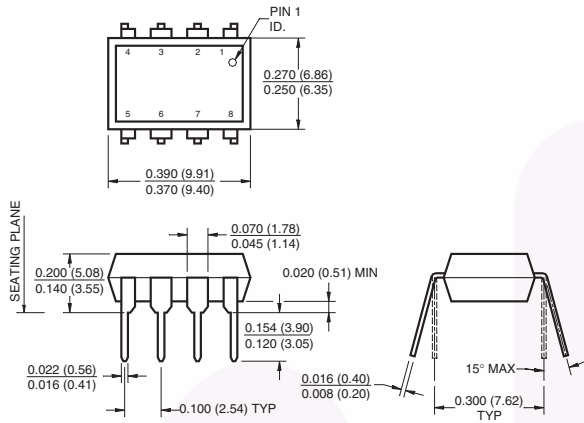


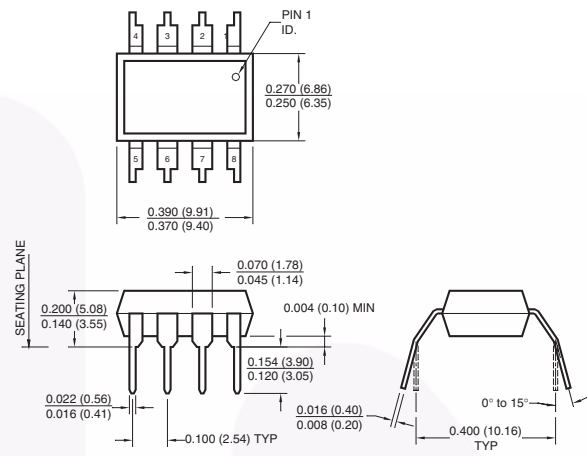
Fig. 10. Test Circuit for Common Mode Transient Immunity and Typical Waveforms

Package Dimensions

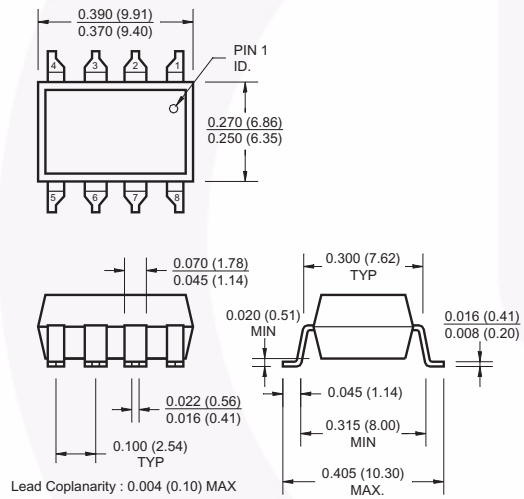
Through Hole



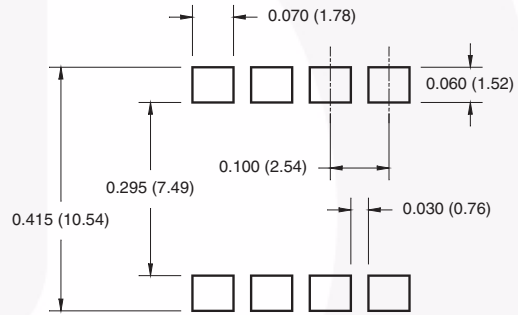
0.4" Lead Spacing



Surface Mount



8-Pin DIP – Land Pattern



Note:

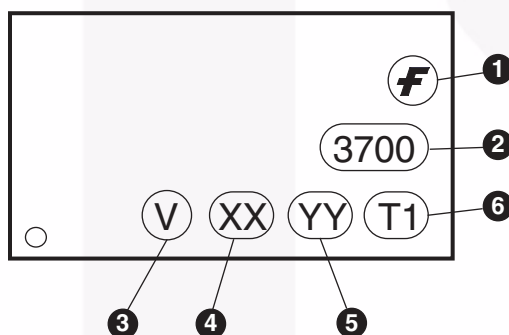
All dimensions are in inches (millimeters)



Ordering Information

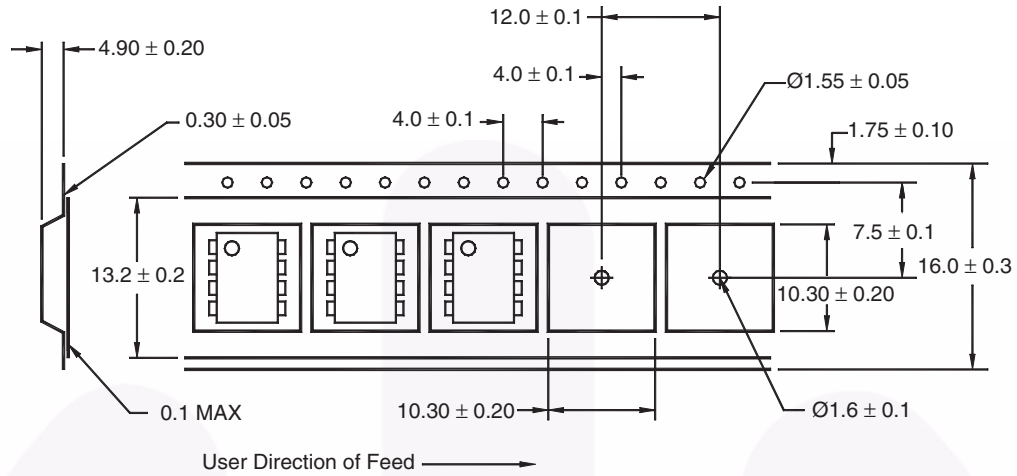
| Option | Example Part Number | Description |
|-----------|---------------------|---------------------------------------|
| No Suffix | HCPL3700 | Shipped in Tubes |
| S | HCPL3700S | Surface Mount Lead Bend |
| SD | HCPL3700SD | Surface Mount; Tape and Reel |
| W | HCPL3700W | 0.4" Lead Spacing |
| V | HCPL3700V | VDE0884 |
| WV | HCPL3700WV | VDE0884; 0.4" Lead Spacing |
| SV | HCPL3700SV | VDE0884; Surface Mount |
| SDV | HCPL3700SDV | VDE0884; Surface Mount; Tape and Reel |

Marking Information



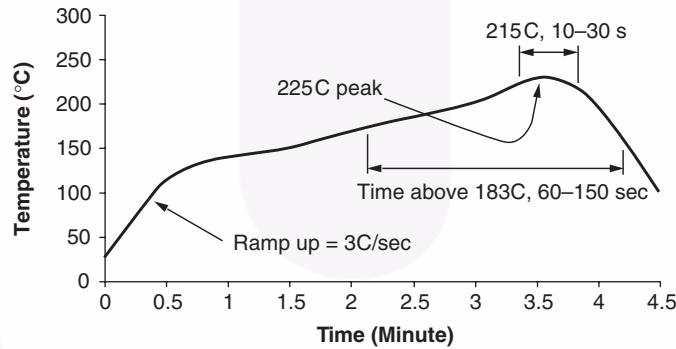
| Definitions | |
|-------------|--|
| 1 | Fairchild logo |
| 2 | Device number |
| 3 | VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table) |
| 4 | Two digit year code, e.g., '07' |
| 5 | Two digit work week ranging from '01' to '53' |
| 6 | Assembly package code |

Carrier Tape Specifications



Note:
All dimensions are in inches (millimeters)

Reflow Profile






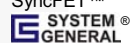
- Peak reflow temperature: 225C (package surface temperature)
- Time of temperature higher than 183C for 60–150 seconds
- One time soldering reflow is recommended





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| Datasheet Identification | Product Status | Definition |
|--------------------------|-----------------------|---|
| Advance Information | Formative / In Design | Datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
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