ACPL-M60L

Small Outline, 5 Leads, High CMR, High Speed, Logic Gate Optocouplers

AVAGO TECHNOLOGIES

Data Sheet

Lead (Pb) Free
RoHS 6 fully
compliant

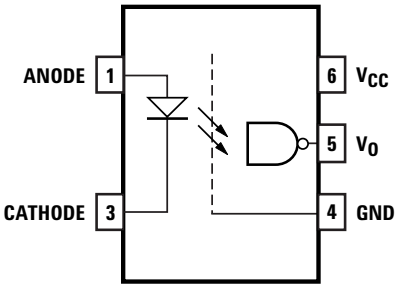
Description

The ACPL-M60L is an optically coupled gate that combines a GaAsP light emitting diode and an integrated high gain photo detector. The output of the detector IC is an open collector Schottky-clamped transistor. The internal shield provides a guaranteed common mode transient immunity specification of 15 kV/µs at 3.3V operation.

This unique design provides maximum AC and DC circuit isolation while achieving LVTTL/LVCMOS compatibility. The optocoupler AC and DC operational parameters are guaranteed from –40˚C to +85˚C, allowing trouble-free system performance.

These optocouplers are suitable for high speed logic interfacing, input/output buffering, as line receivers in environments that conventional line receivers cannot tolerate and are recommended for use in extremely high ground or induced noise environments.

Functional Diagram



Features

- Dual Voltage Operation (3.3V/5V)
- Low power consumption
- 15 kV/µs minimum Common Mode Rejection (CMR) at V_{CM} = 1000 V (3.3V operating voltage)
- High speed: 15 MBd typical
- LVTTL/LVCMOS compatible
- Low input current capability: 5 mA
- Guaranteed AC and DC performance over temperature: –40˚C to +85˚C
- Safety approvals; UL, CSA, IEC/EN/DIN EN 60747-5-2
- Surface mountable
- Very small, low profile JEDEC Registered package outline

Applications

- Isolated line receiver
- Computer-peripheral interfaces
- Microprocessor system interfaces
- Digital isolation for A/D, D/A conversion
- Switching power supply
- Instrument input/output isolation
- Ground loop elimination
- Pulse transformer replacement
- Field buses

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Ordering Information

ACPL-xxxx is UL Recognized with 3750 Vrms for 1 minute per UL1577 and is approved under CSA Component Acceptance Notice #5, File CA 88324.

Part Number	Option RoHS Compliant	Package	Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-2	Quantity
ACPL-M60L	-000E	SO-5	X			100 per tube
	-500E		X	X		1500 per reel

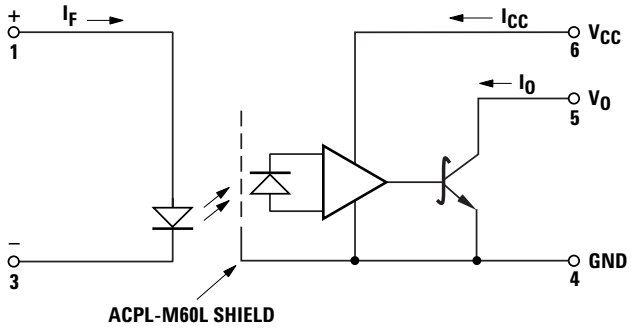
To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry. Combination of Option 020 and Option 060 is not available.

Example 1:

ACPL-M60L-500E to order product of Surface Mount SO-5 in Tape and Reel packaging with RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Schematic

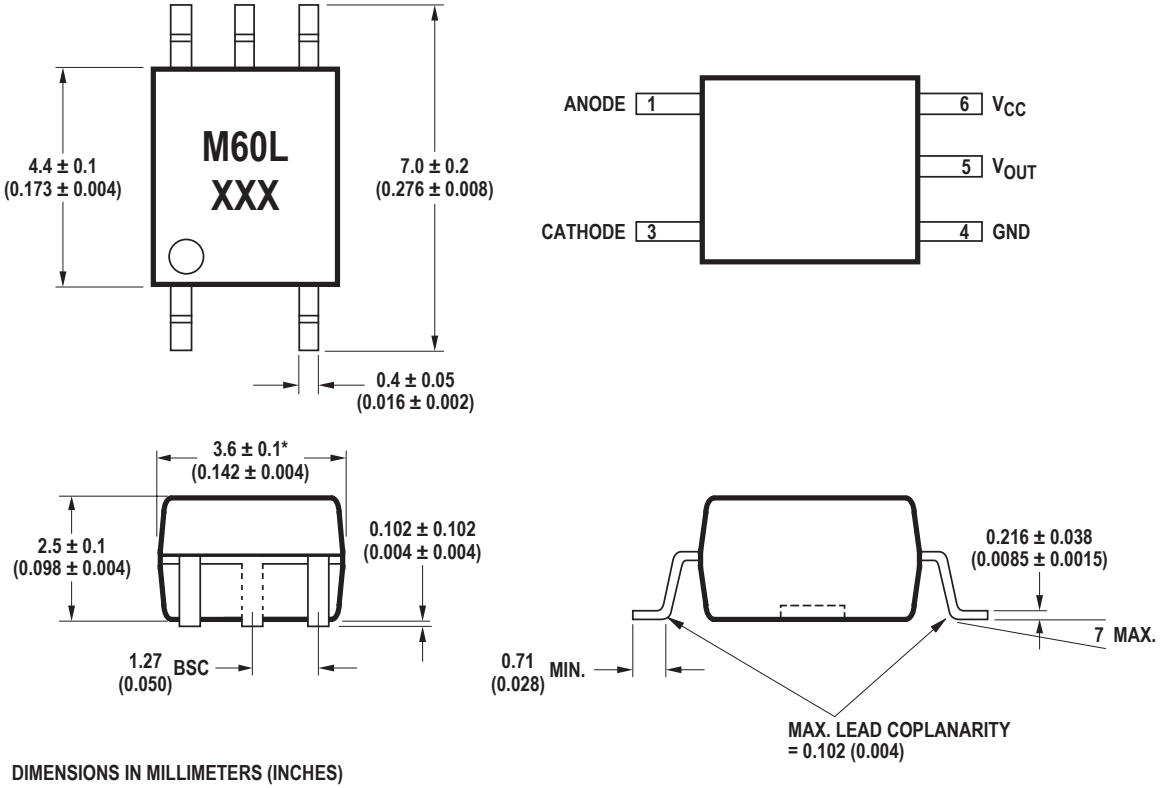


USE OF A 0.1 µF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 6 AND 4 (SEE NOTE 1).

TRUTH TABLE (POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

Package Outline Drawing

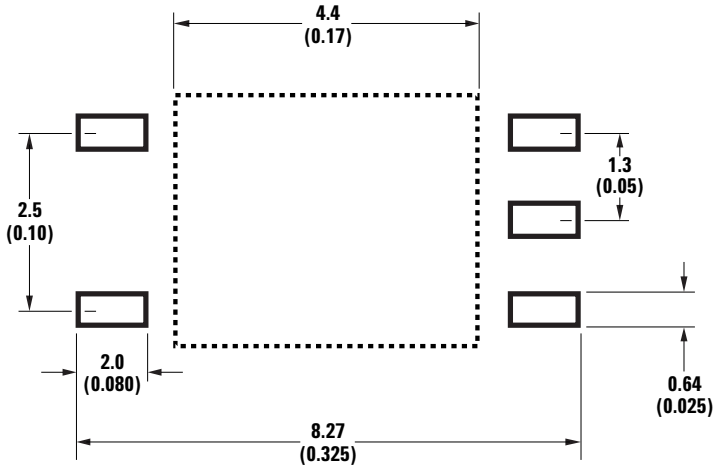


DIMENSIONS IN MILLIMETERS (INCHES)

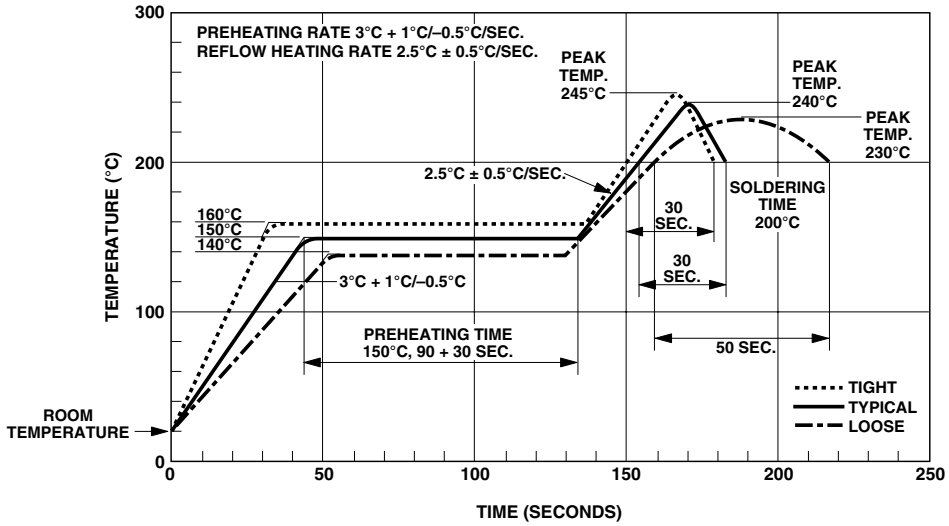
* MAXIMUM MOLD FLASH ON EACH SIDE IS 0.15 mm (0.006)

NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

Land Pattern

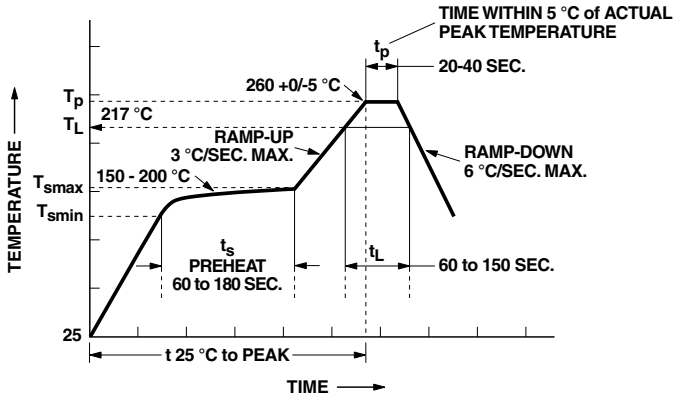


Solder Reflow Temperature Profile



Note: Non-halide flux should be used

Recommended PB-Free IR Profile



NOTES:
THE TIME FROM 25 °C to PEAK TEMPERATURE = 8 MINUTES MAX.
T_{smax} = 200 °C, T_{smin} = 150 °C

Note: Non-halide flux should be used

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L (I01)	≥ 5	mm	Measured from input terminals to output terminals
Minimum External Tracking Path (Creepage)	L (I02)	≥ 5	mm	Measured from input terminals to output terminals
Minimum Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance, conductor to conductor
Tracking Resistance	CTI	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

Absolute Maximum Ratings (No Derating Required up to 85˚C)

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	–55	125	˚C	
Operating Temperature†	T_A	–40	85	˚C	
Average Forward Input Current	I_F		20	mA	1
Reverse Input Voltage	V_R		5	V	
Input Power Dissipation	P_I		40	mW	
Supply Voltage (1 minute maximum)	V_{CC}		7	V	
Output Collector Current	I_O		50	mA	
Output Collector Voltage	V_O		7	V	
Output Collector Power Dissipation	P_O		85	mW	
Solder Reflow Temperature Profile		See Package Outline Drawings section			

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{FL}*	0	250	µA
Input Current, High Level[1]	I_{FH}**	5	15	mA
Power Supply Voltage	V_{CC}	2.7 4.5	3.6 5.5	V V
Operating Temperature	T_A	–40	85	˚C
Fan Out (at R_L = 1 kΩ)[1]	N		5	TTL Loads
Output Pull-up Resistor	R_L	330	4 k	Ω

*The off condition can also be guaranteed by ensuring that $V_{FL} \leq 0.8$ volts.
**The initial switching threshold is 5 mA or less. It is recommended that 6.3 mA to 10 mA be used for best performance and to permit at least a 20% LED degradation guardband.

Electrical Specifications

Over recommended Operating Condition (T_A = –40°C to +85°C , 2.7V ≤ V_{DD} ≤ 3.6V) unless otherwise specified. All Typicals at V_{CC} = 3.3 V, T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}*		4.5	50	µA	V_{CC} = 3.3 V, V_O = 3.3 V I_F = 250 µA	1	
Input Threshold Current	I_{TH}		3.0	5.0	mA	V_{CC} = 3.3 V, V_O = 0.6 V, I_{OL} (Sinking) = 13 mA		
Low Level Output Voltage	V_{OL}*		0.35	0.6	V	V_{CC} = 3.3 V, I_F = 5 mA I_{OL} (Sinking) = 13 mA	2	
High Level Supply Current	I_{CCH}		4.7	7.0	mA	I_F = 0 mA, V_{CC} = 3.3 V		
Low Level Supply Current	I_{CCL}		7.0	10.0	mA	I_F = 10 mA, V_{CC} = 3.3 V		
Input Forward Voltage	V_F	1.4	1.5	1.75*	V	T_A = 25˚C, I_F = 10 mA	5	
Input Reverse Breakdown Voltage	BV_R*	5			V	I_R = 10 µA		
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$		–1.6		mV/˚C	I_F = 10 mA		
Input-Output Insulation	V_{ISO}	3750			V_{RMS}	R_H ≤ 50%, t = 1 min.		12, 13
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0 V		

*The JEDEC Registration specifies 0˚C to +70˚C. Avago specifies –40˚C to +85˚C.

Electrical Specifications

Over recommended temperature (T_A = –40°C to +85°C , 4.5V ≤ V_{DD} ≤ 5.5V) unless otherwise specified. All Typical specification at V_{CC} = 5V, T_A = 25 °C

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}		5.5	100	µA	V_{CC} = 5.5 V, V_O = 5.5 V I_F = 250 µA	1	
Input Threshold Current	I_{TH}		2	5	mA	V_{CC} = 5.5 V, I_O ≥13 mA, V_O = 0.6 V		
Low Level Output Voltage	V_{OL}		0.4	0.6	V	V_{CC} = 5.5 V, I_F = 5 mA, I_{OL} (Sinking) = 13 mA	2	
High Level Supply Current	I_{CCH}		4	7.5	mA	V_{CC} = 5.5 V, I_F = 0 mA,		
Low Level Supply Current	I_{CCL}		6	10.5		V_{CC} = 5.5 V, I_F = 10 mA,		
Input Forward Voltage	V_F	1.4	1.5	1.75	V	T_A = 25°C, I_F = 10 mA	5	
		1.3		1.85		I_F = 10 mA		
Input Reverse Breakdown Voltage	BV_R	5				I_R = 10 µA		
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$		-1.6		mV/°C	I_F = 10 mA		
Input-Output Insulation	V_{ISO}	3750			V_{RMS}	R_H ≤ 50%, t = 1 min.		12, 13
Input Capacitance	C_{IN}		60		pF	V_F = 0V, f = 1 MHz		

*All typicals at T_A = 25°C, V_{CC} = 5 V.

Switching Specifications

Over recommended temperature (T_A = –40°C to +85°C), V_{CC} = 3.3 V, I_F = 7.5 mA unless otherwise specified. All Typicals at T_A = 25°C, V_{CC} = 3.3 V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}			90	ns	R_L = 350 Ω C_L = 15 pF	6, 7, 8	5
Propagation Delay Time to Low Output Level	t_{PHL}			75	ns	R_L = 350 Ω C_L = 15 pF	6, 7, 8	6
Pulse Width Distortion	$\|t_{PHL} - t_{PLH}\|$			25	ns	R_L = 350 Ω C_L = 15 pF	9	8
Propagation Delay Skew	t_{PSK}			40	ns	R_L = 350 Ω C_L = 15 pF		
Output Rise Time (10-90%)	t_r		45		ns	R_L = 350 Ω C_L = 15 pF		
Output Fall Time (90-10%)	t_f		20		ns	R_L = 350 Ω C_L = 15 pF		

*JEDEC registered data for the 6N137.

Switching Specifications

Over recommended temperature (T_A = -40°C to 85°C), V_{CC} = 5 V, I_F = 7.5 mA unless otherwise specified. All Typicals at T_A = 25°C, V_{CC} = 5 V.

Parameter	Symbol	Min.	Typ.*	Max.	Unit	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}	20	48	75 100	ns	T_A = 25°C, R_L=350 Ω C_L=15pF R_L=350 Ω, C_L=15pF	6, 7, 8	5
Propagation Delay Time to Low Output Level	t_{PHL}	25	50	75 100	ns	T_A = 25°C, R_L=350 Ω C_L=15pF R_L=350 Ω, C_L=15pF	6, 7, 8	6
Pulse Width Distortion	$\|t_{PHL} - t_{PLH}\|$		3.5	35	ns	R_L= 350 Ω C_L = 15 pF	9	8
Propagation Delay Skew	t_{PSK}			40	ns	R_L= 350 Ω C_L = 15 pF		
Output Rise Time (10%-90%)	t_{rise}		24		ns	R_L= 350 Ω C_L = 15 pF		
Output Fall Time (10%-90%)	t_{fall}		10		ns	R_L= 350 Ω C_L = 15 pF		

*All typicals at T_A = 25°C, V_{CC} = 5 V.

Parameter	Sym.	Device	Min.	Typ.	Units	Test Conditions		Fig.	Note
Logic High Common Mode Transient Immunity	$\|CM_H\|$	ACPL-M60L	15,000	25,000	V/µs	$\|V_{CM}\|$ = 1000 V	V_{CC} = 3.3 V, I_F = 0 mA, $V_{O(MIN)}$ = 2 V, R_L = 350 Ω, T_A = 25°C	9	9, 11
			10,000	15,000			V_{CC} = 5 V, I_F = 0 mA, $V_{O(MIN)}$ = 2 V, R_L = 350 Ω, T_A = 25°C	9	9, 11
Logic Low Common Mode Transient Immunity	$\|CM_L\|$	ACPL-M60L	15,000	25,000	V/µs	$\|V_{CM}\|$ = 1000 V	V_{CC} = 3.3 V, I_F = 7.5 mA, $V_{O(MAX)}$ = 0.8 V, R_L = 350 Ω, T_A = 25°C	9	10, 11
			10,000	15,000			V_{CC} = 5 V, I_F = 7.5 mA, $V_{O(MIN)}$ = 0.8 V, R_L = 350 Ω, T_A = 25°C	9	10, 11

Notes:
1. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 20 mA.
2. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 15 mA.
3. Derate linearly above +80°C free-air temperature at a rate of 2.7 mW/°C for the SOIC-5 package.
4. Bypassing of the power supply line is required, with a 0.1 µF ceramic disc capacitor adjacent to each optocoupler as illustrated in Figure 11. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20 mm.
5. The t_{PLH} propagation delay is measured from the 3.75 mA point on the falling edge of the input pulse to the 1.5 V point on the rising edge of the output pulse.
6. The t_{PHL} propagation delay is measured from the 3.75 mA point on the rising edge of the input pulse to the 1.5 V point on the falling edge of the output pulse.
7. t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature and specified test conditions.
8. See test circuit for measurement details.
9. CM_H is the maximum tolerable rate of rise on the common mode voltage to assure that the output will remain in a high logic state (i.e., V_O > 2.0 V).
10. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_O < 0.8 V).
11. For sinusoidal voltages, $(|dV_{CM}| / dt)_{max} = \pi f_{CM} V_{CM}$ (p-p).
12. Device considered a two terminal device: pins 1 and 3 shorted together, and pins 4, 5 and 6 shorted together.
13. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 V_{RMS} for 1 second (Leakage detection current limit, I_{I-O} ≤ 5 µA).

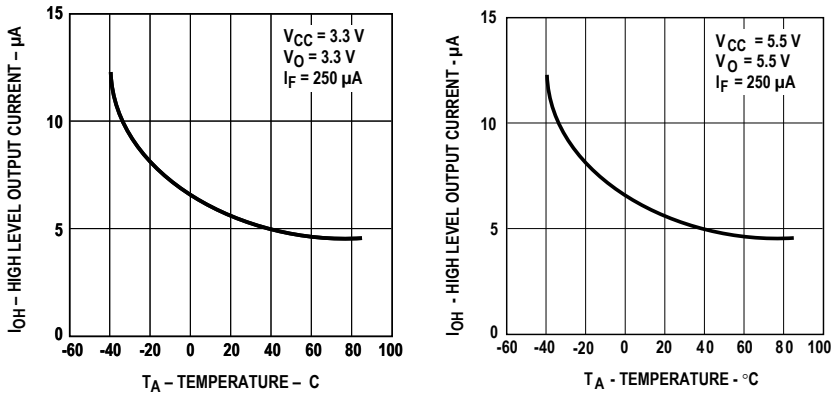


Figure 1. Typical high level output current vs. temperature.

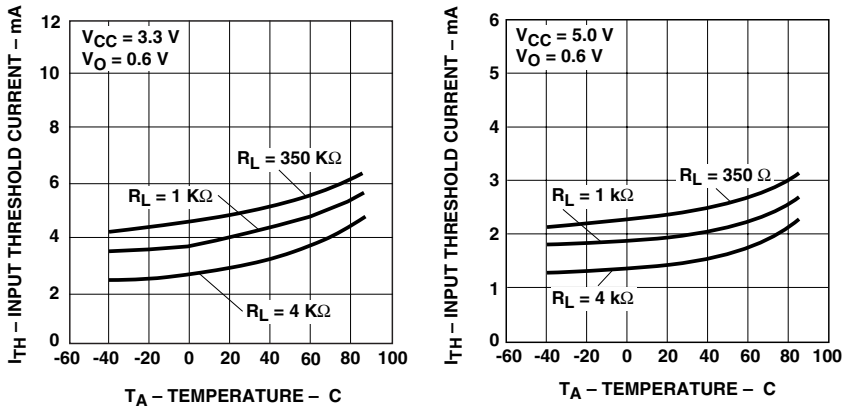


Figure 2. Typical input threshold current vs. Temperature

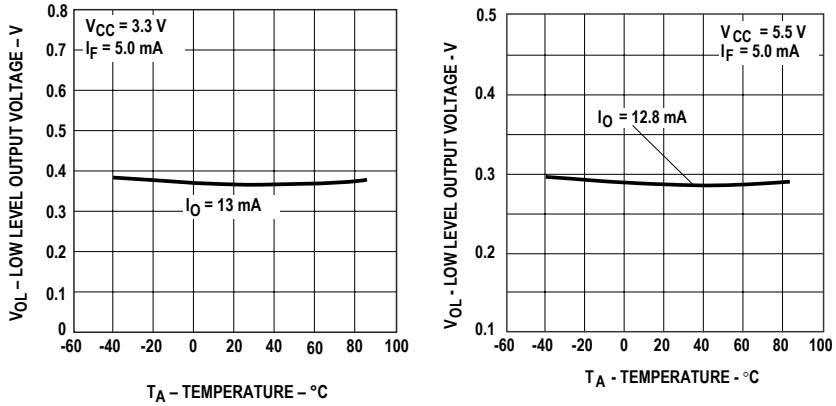


Figure 3. Typical low level output voltage vs. temperature.

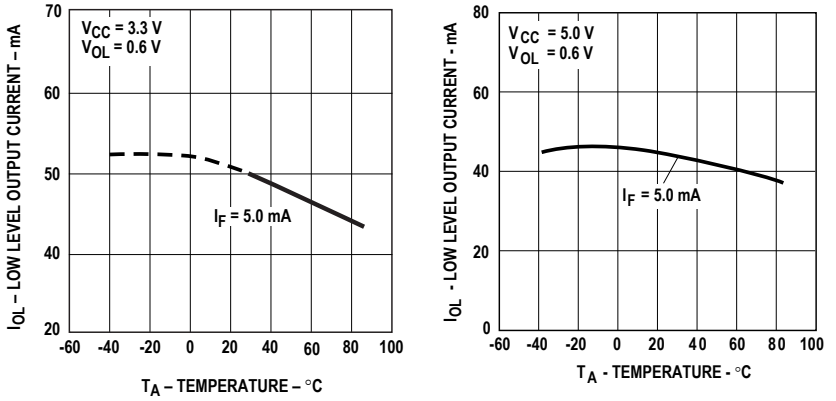


Figure 4. Typical low level output current vs. temperature.

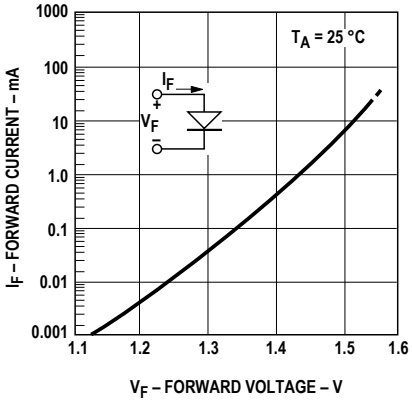


Figure 5. Typical input diode forward characteristic.

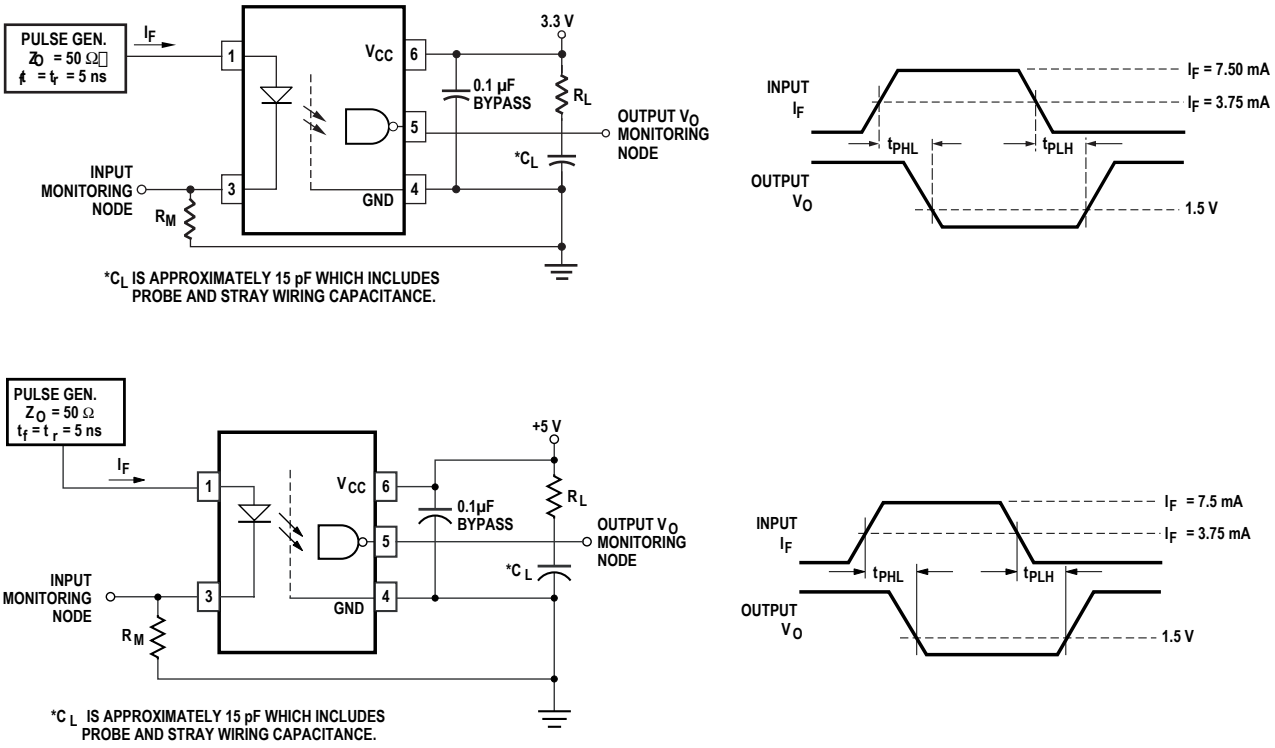


Figure 6. Test circuit for t_{PHL} and t_{PLH}.

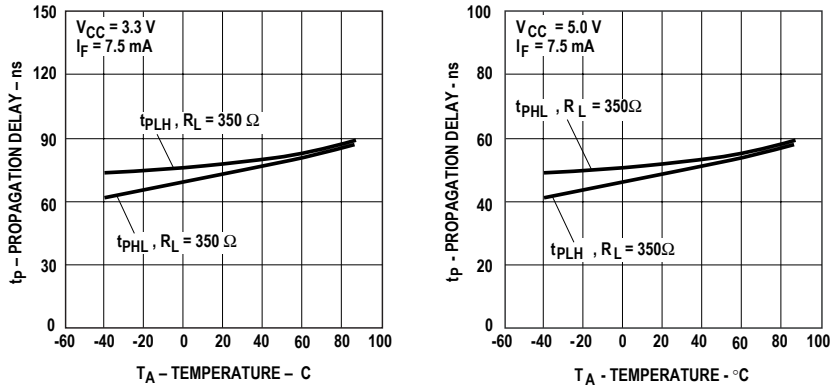


Figure 7. Typical propagation delay vs. temperature.

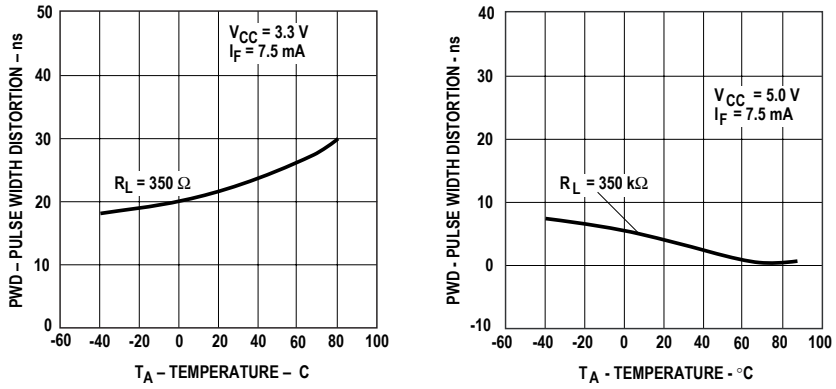


Figure 8. Typical pulse width distortion vs. temperature.

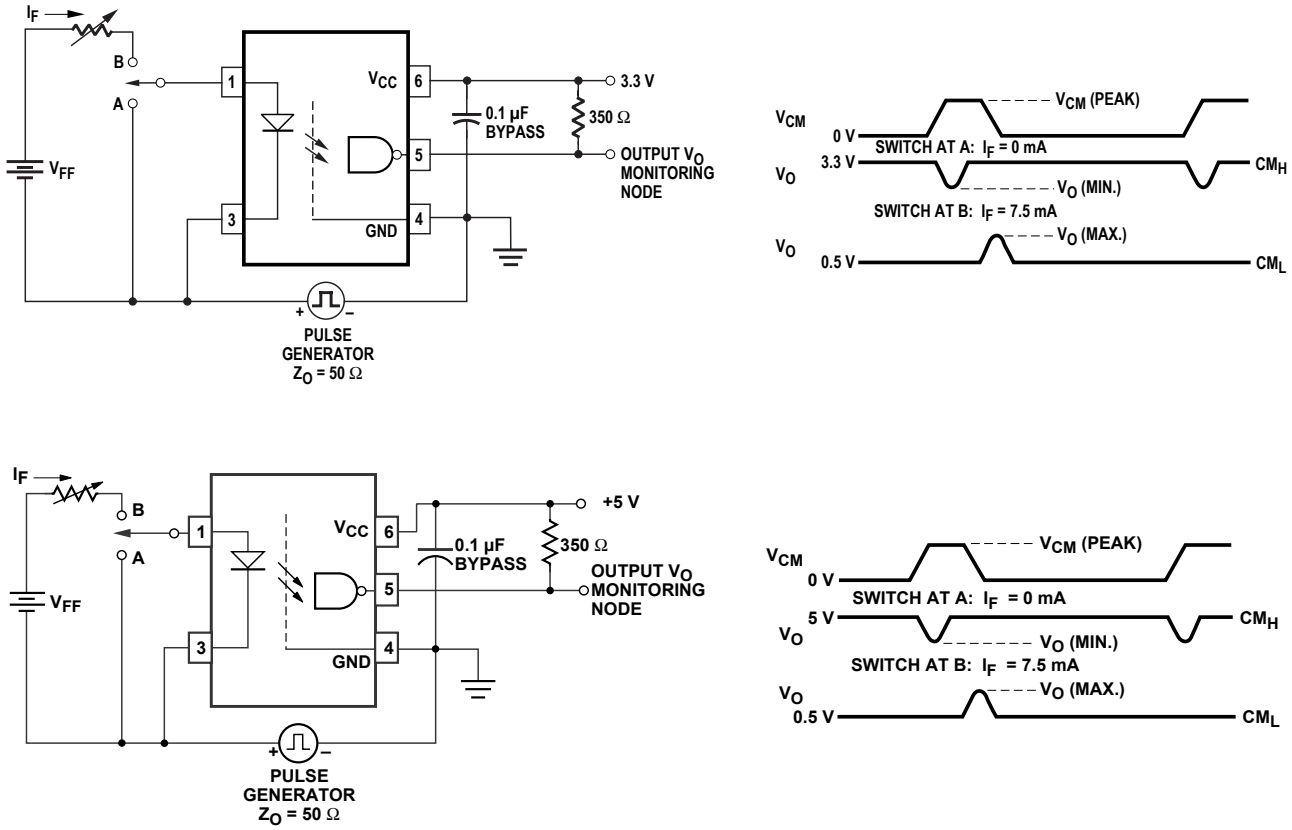


Figure 9. Test circuit for common mode transient immunity and typical waveforms.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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