Switch-mode LED Driver IC With High Current Accuracy and Hiccup Mode Protection

Features

- Switch mode controller for single switch drivers
  - Buck
  - Boost
  - Buck-boost and SEPIC
- Works with high side current sensors
- Closed loop control of output current
- High PWM dimming ratio
- Internal 90V linear regulator (can be extended using external Zener diodes)
- Internal 2% voltage reference ($0°C < T_A < 85°C$)
- Constant frequency operation
- Programmable slope compensation
- Linear & PWM dimming
- +0.2A/-0.4A gate drive
- Hiccup mode protection for both short circuit and open circuit conditions
- Synchronization capability
- Pin compatible with HV9911

Applications

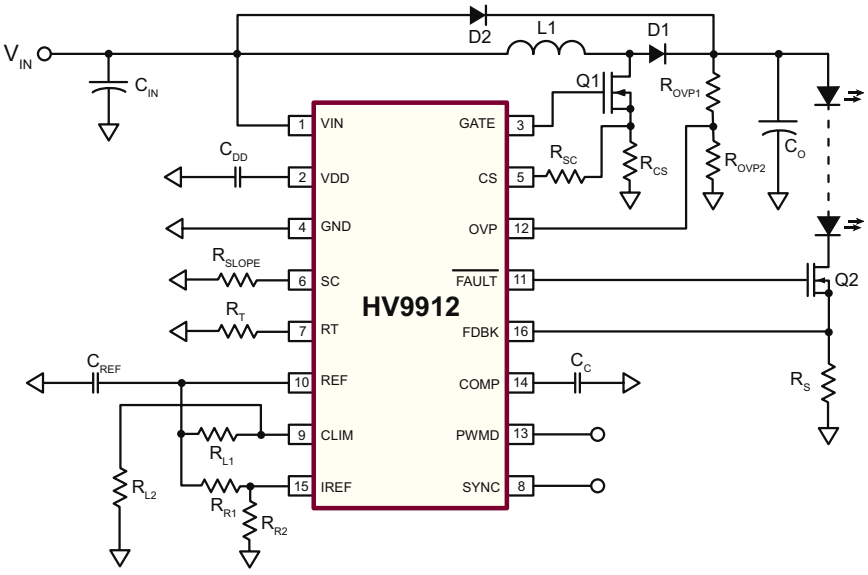
- LED backlight applications
- General LED lighting applications
- Battery powered LED lamps

General Description

The HV9912 is a current mode control LED driver IC designed to control single switch PWM converters (buck, boost, buck-boost or SEPIC) in a constant frequency mode. The controller uses a peak current-mode control scheme with programmable slope compensation and includes an internal transconductance amplifier to control the output current in closed loop enabling high output current accuracy (in the case of buck and buck-boost converters, the output current can be sensed using a high side current sensor like the HV7800). In the constant frequency mode, multiple HV9912 ICs can by synchronized to each other or to an external clock using the SYNC pin. Programmable MOSFET current limit enables current limiting during input under voltage and output overload conditions. The IC also includes a 0.2A source and 0.4A sink gate driver that makes the HV9912 suitable for high power applications. An internal 90V linear regulator powers the IC eliminating the need for a separate power supply for the IC. The IC also provides a $\overline{\text{FAULT}}$ output, which can be used to disconnect the LEDs in case of a fault condition using an external disconnect FET. HV9912 also provides a TTL compatible, low-frequency PWM dimming input that can accept an external control signal with a duty ratio of 0-100% and a frequency of up to a few kilohertz. The HV9912 includes hiccup protection from both short and open circuits, with automatic recovery after the fault condition is cleared.

The HV9912 is a pin compatible replacement to Supertex's HV9911. It is compatible with existing HV9911 designs which have an input voltage of less than 90V by changing R_{OVP1}, R_{OVP}, and R_T.

Typical Application Circuit - Boost



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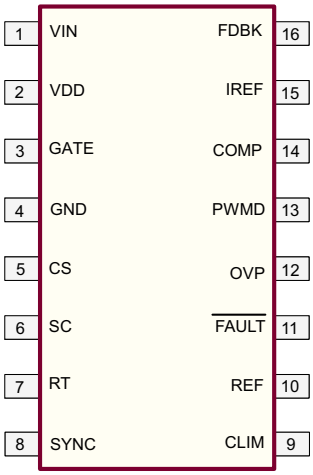
Ordering Information

DEVICE	Package Option
	16-Lead SOIC *9.90x3.90mm body* *1.75mm height (max)* *1.27mm pitch*
HV9912	HV9912NG-G

-G indicates package is RoHS compliant ('Green')

Pin Configuration



16-Lead SOIC (NG)
(top view)

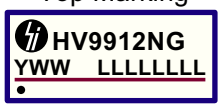
Absolute Maximum Ratings

Parameter	Value
V_{IN} to GND	-0.5V to +100V
V_{DD} to GND	-0.3V to +13.5V
CS to GND	-0.3V to (V_{DD} + 0.3V)
PWMD to GND	-0.3V to (V_{DD} + 0.3V)
GATE to GND	-0.3V to (V_{DD} + 0.3V)
All other pins to GND	-0.3V to (V_{DD} + 0.3V)
Continuous power dissipation (T_A = +25°C)	1200mW
Thermal impedance (θ_{ja})	82°C/W
Junction temperature	+150°C
Storage temperature range	-65°C to +150°C

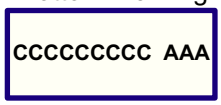
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Product Marking

Top Marking



Bottom Marking



Y = Last Digit of Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
____ = "Green" Packaging

**May be part of top marking*

Package may or may not include the following marks: Si or

16-Lead SOIC (NG)

Electrical Characteristics

*(The * denotes the specifications which apply over the full operating ambient temperature range of -40°C < T_A < +125°C, otherwise the specifications are at T_A = 25°C. V_{IN} = 12V, unless otherwise noted.)*

Sym	Parameter		Min	Typ	Max	Units	Conditions
Input							
V_{INDC}	Input DC supply voltage range	*	(1)	-	90	V	DC input voltage
I_{INSD}	Shut-down mode supply current	*	-	-	1.5	mA	PWMD connected to GND
Internal Regulator							
V_{DD}	Internally regulated voltage	*	7.25	7.75	8.25	V	V_{IN} = 9.0 - 90V, PWMD connected to GND
$UVLO_{RISE}$	V_{DD} undervoltage lockout threshold	-	6.5	-	7.0	V	V_{DD} rising
$UVLO_{HYST}$	V_{DD} undervoltage lockout hysteresis	-	-	500	-	mV	V_{DD} falling

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Electrical Characteristics *(cont.)*

*(The * denotes the specifications which apply over the full operating ambient temperature range of -40°C < T_A < +125°C, otherwise the specifications are at T_A = 25°C. V_{IN} = 12V, unless otherwise noted.)*

Sym	Parameter		Min	Typ	Max	Units	Conditions
Reference							
V_{REF}	REF pin voltage	-	1.225	1.250	1.285	V	REF bypassed with a 0.1µF capacitor to GND; I_{REF} = 0; PWMD = GND; 0°C < T_A < +85°C
		-	1.225	1.250	1.290		REF bypassed with a 0.1µF capacitor to GND; I_{REF} = 0; PWMD = GND; -40°C < T_A < +125°C
$V_{REFLINE}$	Line regulation of reference voltage	-	0	-	20	mV	REF bypassed with a 0.1µF capacitor to GND; I_{REF} = 0; V_{DD} = 7.25 – 12V; PWMD = GND
$V_{REFLOAD}$	Load regulation of reference voltage	-	0	-	10	mV	REF bypassed with a 0.1µF capacitor to GND; I_{REF} = 0-500µA; PWMD = GND
PWM Dimming							
$V_{PWMD(lo)}$	PWMD input low voltage	*	-	-	0.8	V	---
$V_{PWMD(hi)}$	PWMD input high voltage	*	2.0	-	-	V	---
R_{PWMD}	PWMD pull-down resistance	-	50	100	150	kΩ	V_{PWMD} = 5.0V
GATE							
I_{SOURCE}	GATE short circuit current	-	0.2	-	-	A	V_{GATE} = 0V
I_{SINK}	GATE sinking current	-	0.4	-	-	A	V_{GATE} = V_{DD}
T_{RISE}	GATE output rise time	-	-	50	85	ns	C_{GATE} = 1.0nF
T_{FALL}	GATE output fall time	-	-	25	45	ns	C_{GATE} = 1.0nF
Over Voltage Protection							
$V_{OVP, RISING}$	Over voltage rising trip point	-	4.75	5.00	5.25	V	OVP rising
$V_{OVP, HYST}$	Over voltage Hysteresis	-	-	0.50	-	V	OVP falling
Current Sense							
T_{BLANK}	Leading edge blanking	-	100	-	280	ns	0°C < T_A < +85°C
		-	100	-	330		-40°C < T_A < +125°C
T_{DELAY1}	Delay to output of C_{OMP} comparator	-	-	-	200	ns	COMP = V_{DD} ; C_{LIM} = REF; C_{SENSE} = 0 to 600mV step
T_{DELAY2}	Delay to output of C_{LIMIT} comparator	-	-	-	200	ns	COMP = V_{DD} ; C_{LIM} = 300mV; C_{SENSE} = 0 to 400mV step
V_{OFFSET}	Comparator offset voltage	-	-10	-	10	mV	---
Internal Transconductance Opamp							
GB	Gain bandwidth product	#	-	1.0	-	MHz	75pF capacitance at OP pin
A_V	Open loop DC gain	-	60	-	-	dB	Output open

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Electrical Characteristics *(cont.)*

(Over recommended operating conditions. V_{IN} = 24V, T_A = 25°C, unless otherwise specified)

Sym	Parameter		Min	Typ	Max	Units	Conditions
V_{CM}	Input common-mode range	#	-0.3	-	3.0	V	---
V_O	Output voltage range	#	0.7	-	6.75	V	---
G_M	Transconductance	-	450	550	650	µA/V	---
V_{OFFSET}	Input offset voltage	-	-5.0	-	5.0	mV	---
I_{BIAS}	Input bias current	#	-	0.5	1.0	nA	---
Oscillator							
f_{OSC1}	Oscillator frequency	*	99	106	118	kHz	R_T = 500kΩ
f_{OSC2}	Oscillator frequency	*	510	580	650	kHz	R_T = 96kΩ
D_{MAX}	Maximum duty cycle	-	87	-	93	%	---
V_{SYNCH}	SYNC input high	-	2.0	-	-	V	---
V_{SYNCL}	SYNC input low	-	-	-	0.8	V	---
$I_{OUTSYNC}$	SYNC output current	-	-	18	-	µA	---
Output Short Circuit							
G_{SC}	Gain for short circuit comparator	-	1.9	2.0	2.1	V	---
V_{OMIN}	Minimum output voltage of the gain stage	-	0.125	-	0.25	V	$0^oC < T_A < +85^oC$, I_{REF} = GND
		-	0.125	-	0.26		$-40^oC < T_A < +125^oC$, I_{REF} = GND
T_{OFF}	Propagation time for short circuit detection	-	-	-	250	ns	PWMD = V_{DD}, I_{REF} = 400mA; FDBK step from 0 to 900mV; $\overline{FAULT}$ goes from high to low
$T_{RISE,FAULT}$	Fault output rise time	-	-	-	300	ns	330pF capacitor at $\overline{FAULT}$ pin
$T_{FALL,FAULT}$	Fault output fall time	-		-	300	ns	330pF capacitor at $\overline{FAULT}$ pin
$T_{BLANK,SC}$	Blanking time	-	480	-	900	ns	---
I_{HICCUP}	Current source at COMP pin used for hiccup mode protection	-		5.0	-	µA	---
Slope Compensation							
I_{SLOPE}	Current sourced out of SC pin	*	0	-	100	µA	---
G_{SLOPE}	Internal current mirror ratio	-	1.80	2.00	2.26	-	I_{SLOPE} = 50µA ; R_{SC} = 1.0kΩ

Notes:

(1) See Application Information for Minimum Input Voltage.

* *The specifications which apply over the full operating temperature range at $-40^oC < T_A < +125^oC$ are guaranteed by design and characterization.*

\# *Denotes specifications guaranteed by design.*

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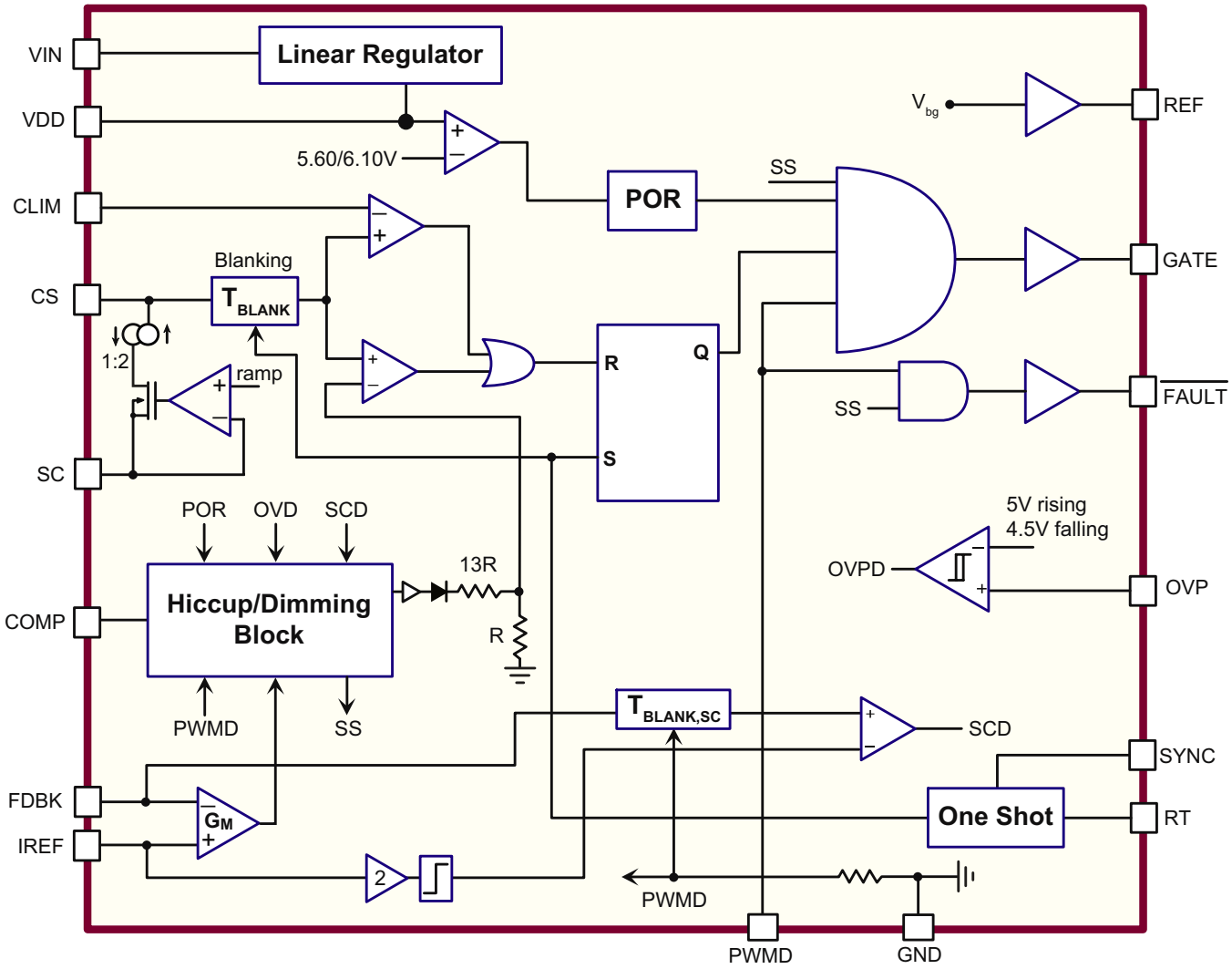
Functional Block Diagram



Functional Description

Power Topology

The HV9912 is a switch-mode converter LED driver designed to control a continuous conduction mode buck or boost in a constant frequency (or constant off-time) mode. The IC includes an internal linear regulator, which operates from input voltages up to 90V eliminating the need for an external power supply for the IC. The IC includes features typically required in LED drivers like open LED protection, output short circuit protection, linear and PWM dimming, programmable input current limiting and accurate control of the LED current. A high current gate drive output enables the controller to be used in high power converters.

The HV9912 is an enhanced version of the HV9911 with hysteretic over-voltage protection and hiccup mode short circuit protection. The IC includes a blanking network controlled by the PWMD input to prevent the short circuit protection from triggering prematurely during PWM dimming due to the parasitic capacitance of the LED string. It also allows the IREF pin to be pulled all the way down to GND without triggering the short circuit protection. It is a pin compatible replacement to the HV9911.

Linear Regulator

The HV9912 can be powered directly from its VIN pin that withstands a voltage up to 90V. When a voltage is applied at the VIN pin, the HV9912 tries to maintain a constant 7.75V (typ) at the VDD pin. The regulator also has a built in under-voltage lockout which shuts off the IC if the voltage at the VDD pin falls below the UVLO threshold.

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The VDD pin must be bypassed by a low ESR capacitor (≥0.1µF) to provide a low impedance path for the high frequency current of the output gate driver.

The input current drawn from the VIN pin is a sum of the 1.5mA current drawn by the internal circuit and the current drawn by the gate driver (which in turn depends on the switching frequency and the gate charge of the external FET).

$$I_{IN} = 1.5mA + (Q_G \times f_S) \quad \text{(Eqn. 1)}$$

In the above equation, fs is the switching frequency and Q_G is the gate charge of the external FET (which can be obtained from the datasheet of the FET).

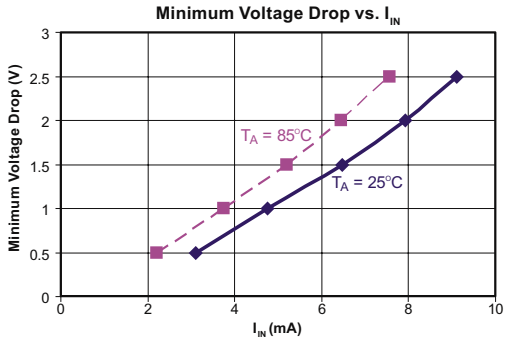
Minimum Input Voltage at VIN pin

The minimum input voltage at which the converter will start and stop depends on the minimum voltage drop required for the linear regulator. The internal linear regulator will regulate the voltage at the VDD pin when VIN is between 9V and 90V. However, when VIN is less than 9V, the converter will still function as long as VDD is greater than the under voltage lockout. Thus, the converter might be able to start at lower than 9V. The start/stop voltages at the VIN pin can be determined using the minimum voltage drop across the linear regulator as a function of the current drawn. This data is shown in Fig. 1 for ambient temperatures of 25ºC and 85ºC.

Assume an ambient temperature of 85ºC. Assuming the IC is driving a 15nC gate charge FET at 200kHz, the total input current is estimated to be 4.5mA (using Eqn. 1). At this input current, the minimum voltage drop from Fig. 1 can be approximately estimated to be V_{DROP} = 1.25V. However, before the IC starts switching the current drawn will be 1.5mA. At this current level, the voltage drop is approximately V_{DROP1} = 0.3V. Thus, the start/stop VIN voltages can be computed to be:

$$\begin{aligned} VIN_{START} &= UVLO_{MAX} + V_{DROP1} \quad \text{(Eqn. 2)} \\ &= 7.0V + 0.3V \\ &= 7.3V \\ VIN_{STOP} &= UVLO_{MAX} - \Delta UVLO + V_{DROP} \\ &= 7.0V - 0.5V + 1.25V \\ &= 7.75V \end{aligned}$$

Fig. 1 Headroom vs Input Current



In this case, the gate drive draws too much current and VIN_{START} is less than VIN_{STOP}. In such cases, the IC will oscillate between ON and OFF if the input voltage is between the start and stop voltages. In these circumstances, it is recommended that the input voltage be kept higher than VIN_{STOP}.

Reference

HV9912 includes a 2% accurate, 1.25V reference, which can be used as the reference for the output current as well as to set the switch current limit. The reference is buffered so that it can deliver a maximum of 500µA external current to drive the external circuitry. The reference should be bypassed with at least a 10nF low ESR capacitor.

Note: *In order to avoid abnormal start-up conditions, the bypass capacitor at the REF pin should not exceed 0.1µF.*

Oscillator

Connecting a resistor between R_T and GND will program the time period.

In both cases, resistor R_T sets the current which charges an internal oscillator capacitor. The capacitor voltage ramps up linearly and when the voltage increases beyond the internal set voltage, a comparator triggers the SET input of the internal SR flip-flop. This starts the next switching cycle. The time period of the oscillator can be computed as:

$$T_S \approx R_T \times 18pF \quad \text{(Eqn. 3)}$$

Synchronization

The SYNC pin is an input/output (I/O) port to a fault tolerant peer-to-peer and/or master clock synchronization circuit. For synchronization, the SYNC pins of multiple HV9912 based converters can be connected together and may also be connected to the open drain output of a master clock. When connected in this manner, the oscillators will lock to the device with the highest operating frequency. When synchronizing multiple ICs, it is recommended that the same timing resistor be (corresponding to the switching frequency) be used in all the HV9912 circuits.

In rare occasions, given the length of the connecting lines for the SYNC pins, a resistor between SYNC and GND may be required to damp any ringing due to parasitic capacitances. It is recommended that the resistor chosen be greater than 300kΩ.

When synchronized in this manner, a permanent HIGH or LOW condition on the SYNC pin will result in a loss of synchronization, but the HV9912 based converters will continue to operate at their individually set operating frequency. Since loss of synchronization will not result in total system failure, the SYNC pin is considered fault tolerant.

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Slope Compensation

For continuous conduction mode converters operating in the constant frequency mode, slope compensation becomes necessary to ensure stability of the peak current mode controller, if the operating duty cycle is greater than 0.5. Choosing a slope compensation which is one half of the down slope of the inductor current ensures that the converter will be stable for all duty cycles.

Slope compensation can be programmed by two resistors R_{SLOPE} and R_{SC}. Assuming a down slope of DS (A/µs) for the inductor current, the slope compensation resistors can be computed as:

$$R_{SC} = \frac{R_{SLOPE} \times DS \times 10^6 \times T_S \times R_{CS}}{10} \qquad \text{(Eqn. 4)}$$

where R_{CS} is the current sense resistor which senses the switching FET current.

Note: *The maximum current that can be sourced out of the SC pin is limited to 100µA. This limits the minimum value of the R_{SLOPE} resistor to 25kΩ. If the equation for slope compensation produces a value of R_{SLOPE} less than this value, then R_{SC} would have to be reduced accordingly. It is recommended that R_{SLOPE} be chosen in the range of 25 - 50kΩ.*

Current Sense

The current sense input of the HV9912 includes a built in 100ns (minimum) blanking time to prevent spurious turn off due to the initial current spike when the FET turns on.

The HV9912 includes two high-speed comparators - one is used during normal operation and the other is used to limit the maximum input current during input under voltage or overload conditions.

The IC includes an internal resistor divider network, which steps down the voltage at the COMP pin by a factor of 15. This stepped-down voltage is given to one of the comparators as the current reference. The reference to the other comparator, which acts to limit the maximum inductor current, is given externally.

It is recommended that the sense resistor R_{CS} be chosen so as to provide about 250mV current sense signal.

Current Limit

Current limit has to be set by a resistor divider from the 1.25V reference available on the IC. Assuming a maximum operating inductor current I_{PK} (including the ripple current), the maximum voltage at the CLIM pin can be set as:

$$V_{CLIM} \geq 1.2 \times I_{PK} \times R_{CS} + \frac{5 \times R_{CS}}{R_{SLOPE}} \times 0.9 \qquad \text{(Eqn. 5)}$$

Note that this equation assumes a current limit at 120% of the maximum input current. Also, if V_{CLIM} is greater than 450mV, the saturation of the internal opamp will determine the limit on the input current rather than the CLIM pin. In such a case, the sense resistor R_{CS} should be reduced till V_{CLIM} reduces below 550mV.

It is recommended that no capacitor be connected between CLIM and GND.

Internal 1MHz Transconductance Amplifier

HV9912 includes a built in 1MHz transconductance amplifier, with tri-state output, which can be used to close the feedback loop. The output current sense signal is connected to the FDBK pin and the current reference is connected to the IREF pin.

The output of the opamp is controlled by the signal applied to the PWMD pin. When PWMD is high, the output of the opamp is connected to the COMP pin. When PWMD is low, the output is left open. This enables the integrating capacitor to hold the charge when the PWMD signal has turned off the gate drive. When the IC is enabled, the voltage on the integrating capacitor will force the converter into steady state almost instantaneously.

The output of the opamp is buffered and connected to the current sense comparator using a 15:1 divider. The buffer helps to prevent the integrator capacitor from discharging during the PWM dimming state.

PWM Dimming

PWM dimming can be achieved by driving the PWMD pin with a TTL compatible square wave source. The PWM signal is connected internally to the three different nodes - the transconductance amplifier, the FLT output and the GATE output.

When the PWMD signal is high, the GATE and FLT pins are enabled and the output of the transconductance opamp is connected to the external compensation network. Thus, the internal amplifier controls the output current. When the PWMD signal goes low, the output of the transconductance amplifier is disconnected from the compensation network. Thus, the integrating capacitor maintains the voltage across it. The GATE is disabled, so the converter stops switching and the FLT pin goes low, turning off the disconnect switch.

The output capacitor of the converter determines the PWM dimming response of the converter, since it has to get charged and discharged whenever the PWMD signal goes high or low. In the case of a buck converter, since the inductor current is continuous, a very small capacitor is used across the LEDs. This minimizes the effect of the capacitor on the PWM dimming response of the converter. However, in the case of a boost converter, the output current is dis-

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continuous and a very large output capacitor is required to reduce the ripple in the LED current. Thus, this capacitor will have a significant impact on the PWM dimming response. By turning off the disconnect switch when PWMD goes low, the output capacitor is prevented from being discharged and thus the PWM dimming response of the boost converter is greatly improved.

Note that in case of continuous conduction mode boost converters, disconnecting the capacitor might cause a sudden spike in the capacitor voltage as the energy in the inductor is dumped into the capacitor. This increase in the capacitor voltage might cause the OVP comparator to trip if the OVP point is set too close to the maximum operating voltage. Thus, either the capacitor has to be larger to absorb this energy without increasing the capacitor voltage significantly or the OVP set point has to be increased.

False Triggering of the Short Circuit Comparator During PWM Dimming

During PWM dimming, the parasitic capacitance of the LED string causes a spike in the output current when the disconnect FET is turned on. With the HV9911, this parasitic spike in the output current caused the IC to falsely detect an over current condition and shut down. To prevent this false shutdown, an R-C filter was used at the FDBK pin to filter this spike.

To prevent this false triggering in the HV9912, there is a built-in 500ns blanking network for the short circuit comparator, which eliminates the need for the external R-C low pass filter. This blanking network is activated when the PWMD input goes high. Thus, the short circuit comparator will not see the spike in the LED current during the PWM Dimming turn-on transition. Once the blanking timer is completed, the short circuit comparator will start monitoring the output current. Thus, the total delay time for detecting a short circuit will depend on the condition of the PWMD input.

If the output short circuit exists before the PWMD signal goes high, the total detection time will be:

$$t_{detect1} = t_{blank,SC(max)} + t_{delay(max)} \approx 900 + 250 \approx 1150ns(max) \quad \text{(Eqn. 6)}$$

If the short circuit occurs when the PWMD signal is already high, the time to detect will be:

$$t_{detect1} = t_{delay(max)} \approx 250ns(max) \quad \text{(Eqn. 7)}$$

Hiccup Timer

The HV9912 reuses the compensation network on the COMP pin to create a timer which is activated upon startup or when a detected fault has been cleared. When a fault is detected (either open circuit or short circuit) or upon startup, the COMP pin is disconnected from the G_M amplifier and the GATE and FLT pins are pulled low disabling the LED driver. When the fault has cleared, a 5.0µA current source is activated which pulls the COMP network up to 5.0V. Once the voltage at the COMP network reaches 5.0V, the 5.0µA sourcing current is disconnected and a 5.0µA sinking current is activated which pulls the COMP pin low. When the voltage at the COMP pin reaches 1.0V, the sinking current is disconnected and the G_M amplifier is reconnected to the COMP pin. The FLT pin goes high and the GATE pin is now allowed to switch. The closed loop control then takes over the control of the LED current.

Startup Condition

The startup waveforms are shown in Fig. 2.

Assuming a pole-zero R-C network at the COMP pin (series combination of R_Z and C_Z in parallel with C_C), the start-up delay time can be approximately computed as

$$t_{delay} \approx t_{POR} + (C_C + C_Z) \times \frac{9V}{5\mu A} \quad \text{(Eqn. 8)}$$

This equation assumes that the voltage drop across R_Z can be neglected compared to the voltage swing at the COMP pin, which is true in most of the cases (R_Z < 100kΩ). The POR time (t_{POR}) for the HV9912 is 10µs.

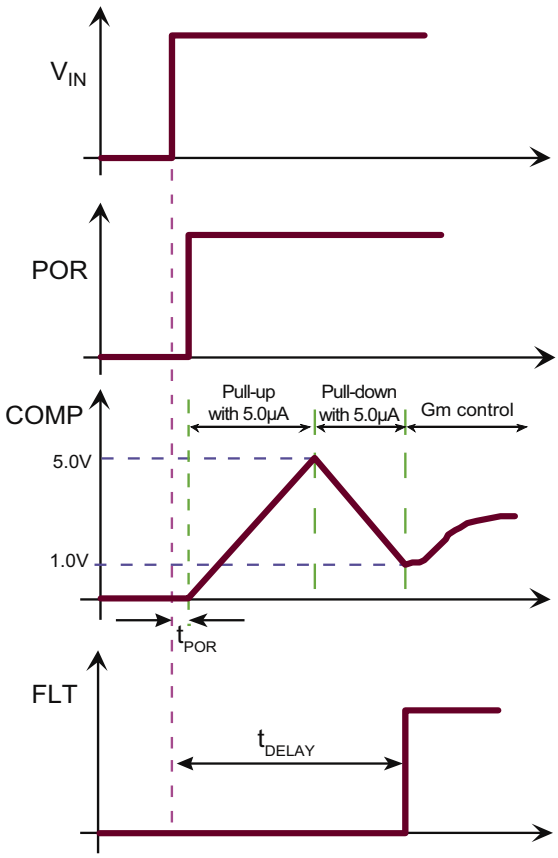

Fig. 2 Waveforms During Startup

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FAULT Condition

In the case of a fault condition (either open circuit or short circuit), the same sequence is repeated with the only difference being that the COMP pin voltage does not start from zero, but rather from its steady-state condition.

Short Circuit Protection

When a short circuit condition is detected (output current becomes higher than twice the steady state current), the GATE and FLT outputs are pulled low. As soon as the disconnect FET is turned off, the output current goes to zero and the short circuit condition disappears. At this time, the hiccup timer is started (Fig. 3). Once the timing is complete, the converter attempts to restart. If the fault condition still persists, the converter shuts down and goes through the cycle again. If the fault condition is cleared (due to a momentary output short) the converter will start regulating the output current normally. This allows the LED driver to recover from accidental shorts without having to reset the IC.

The hiccup time will depend on the steady state voltage of the COMP pin (V_{COMP}). This is typically in the range of 3 - 4V. The hiccup time can be approximately computed as:

$$t_{HICCUP} \approx (C_C + C_Z) \times \frac{9V - V_{COMP}}{5\mu A} \qquad \text{(Eqn. 9)}$$

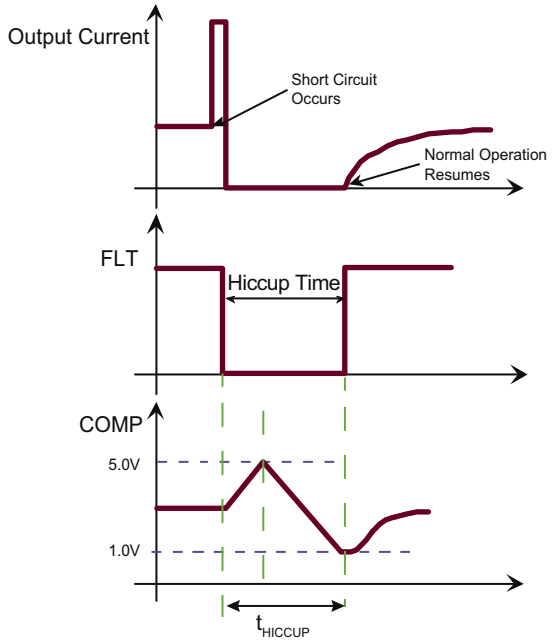

Fig. 3 Short Circuit Protection

Over Voltage Protection

The HV9912 provides hysteretic over voltage protection allowing the IC to recover in case the LED load is disconnected momentarily.

When the load is disconnected in a boost converter, the output voltage rises as the output capacitor starts charging. When the output voltage reaches the OVP rising threshold, the HV9912 detects an over voltage condition and turns off the converter. The converter is turned back on only when the output voltage falls below the falling OVP threshold (which is 10% lower than the rising threshold). This time is mostly dictated by the R-C time constant of the output capacitor Co and the resistor network used to sense over voltage (R_{OVP1} + R_{OVP2}). In case of a persistent open circuit condition, this cycle keeps repeating maintaining the output voltage within a 10% band.

In most designs, the lower threshold voltage of the over voltage protection when the converter will be turned on will be more than the LED string voltage. Thus, when the LED load is reconnected to the output of the converter, the voltage differential between the actual output voltage and the LED string voltage will cause a spike in the output current when the FLT signal goes high. This causes a short circuit to be detected and the HV9912 will go into short circuit protection. This behavior continues till the output voltage becomes lower than the LED string voltage, at which point no fault will be detected and normal operation of the circuit will commence (Fig. 4).

The various delay times can be computed as follows:

$$t_{RC} \approx 0.1 \times (R_{OVP1} + R_{OVP2}) \times C_O \qquad \text{(Eqn. 10)}$$

$$t_{HICCUP1} \approx (C_C + C_Z) \times \frac{9V - V_{COMP}}{5\mu A} \qquad \text{(Eqn. 11)}$$

$$t_{HICCUP2\text{-}n} \approx (C_C + C_Z) \times \frac{9V}{5\mu A} \qquad \text{(Eqn. 12)}$$

Note that the number of hiccup cycles might be more than two.

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Linear Dimming

Linear dimming can be accomplished by varying the voltage at the IREF pin, as the output current is proportional to the voltage at the IREF pin. This can be done either by using a potentiometer from the REF pin or by applying an external voltage source at the IREF pin.

In the HV9911, due to the offset voltage of the short circuit comparator as well as the non-linearity of the X2 gain stage, pulling the IREF pin very close to GND will cause the internal short circuit comparator to trigger and shut down the IC.

To overcome this in the HV9912, the minimum output of the gain stage is limited to 125 ~ 250mV, allowing the IREF pin to be pulled all the way to 0V without triggering the short circuit comparator.

Note: Since this control IC is a peak current mode controller, pulling the IREF pin to zero will not cause the LED current to become zero. The converter will still be operating at its minimum on-time causing a very small current to flow through the LEDs. To get zero LED current, the PWMD input has to be pulled to GND.

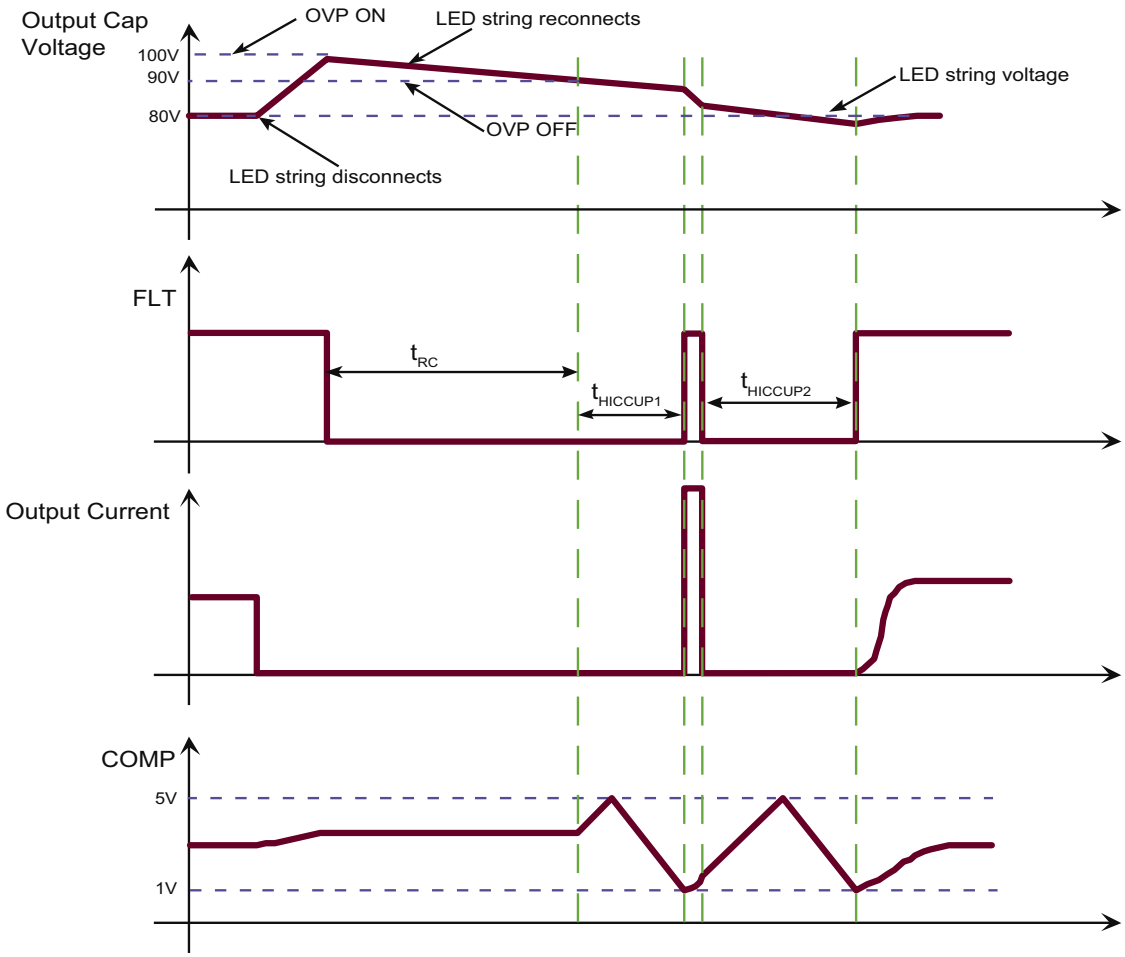

Fig. 4 Open Circuit Protection

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Pin Description

Pin #	Pin	Description
1	VIN	This pin is the input of a 90V high voltage regulator.
2	VDD	This is a power supply pin for all internal circuits. It must be bypassed with a low ESR capacitor to GND (at least 0.1µF).
3	GATE	This pin is the output gate driver for an external N-channel power MOSFET.
4	GND	Ground return for all the low power analog internal circuitry. This pin must be connected to the return path from the input.
5	CS	This pin is used to sense the source current of the external power FET. It includes a built-in 100ns (min) blanking time.
6	SC	This pin is used to set the slope compensation.
7	RT	This pin sets the frequency of the power circuit. A resistor between RT and GND will program the circuit in constant frequency mode.
8	SYNC	This I/O pin may be connected to the SYNC pin of other HV9912 circuits and will cause the oscillators to lock to the highest frequency oscillator.
9	CLIM	This pin provides a programmable input current limit for the converter. The current limit can be set by using a resistor divider from the REF pin.
10	REF	This pin provides 2% accurate reference voltage. It must be bypassed with a 0.01 – 0.1µF capacitor to GND.
11	$\overline{\text{FAULT}}$	This pin is pulled to ground when there is an output short circuit condition or output over voltage condition. This pin can be used to drive an external MOSFET in the case of boost converters to disconnect the load from the source.
12	OVP	This pin provides the over voltage protection for the converter. When the voltage at this pin exceeds 5.0V, the gate output of the HV9912 is turned off and FLT goes low. The IC will turn on when the voltage at the pin goes below 4.5V.
13	PWMD	When this pin is pulled to GND (or left open), switching of the HV9912 is disabled. When an external TTL high level is applied to it, switching will resume.
14	COMP	Stable Closed loop control can be accomplished by connecting a compensation network between COMP and GND. This capacitor also controls the hiccup time.
15	IREF	The voltage at this pin sets the output current level. The current reference can be set using a resistor divider from the REF pin.
16	FDBK	This pin provides output current feedback to the HV9912 by using a current sense resistor.

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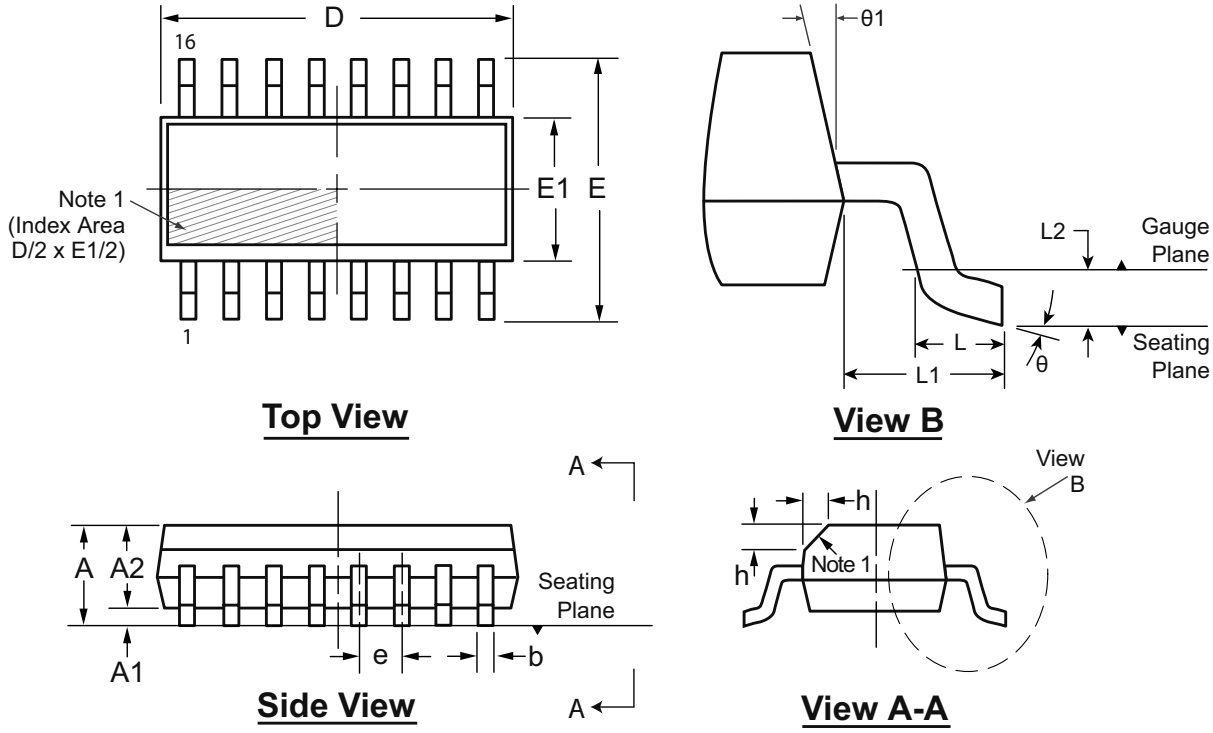
16-Lead SOIC (Narrow Body) Package Outline (NG)

9.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note:

1. *This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	9.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	9.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	10.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AC, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
***Supertex Doc. #:** DSPD-16SONG, Version G041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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