

High Voltage Liquid Crystal Shutter Driver

Features

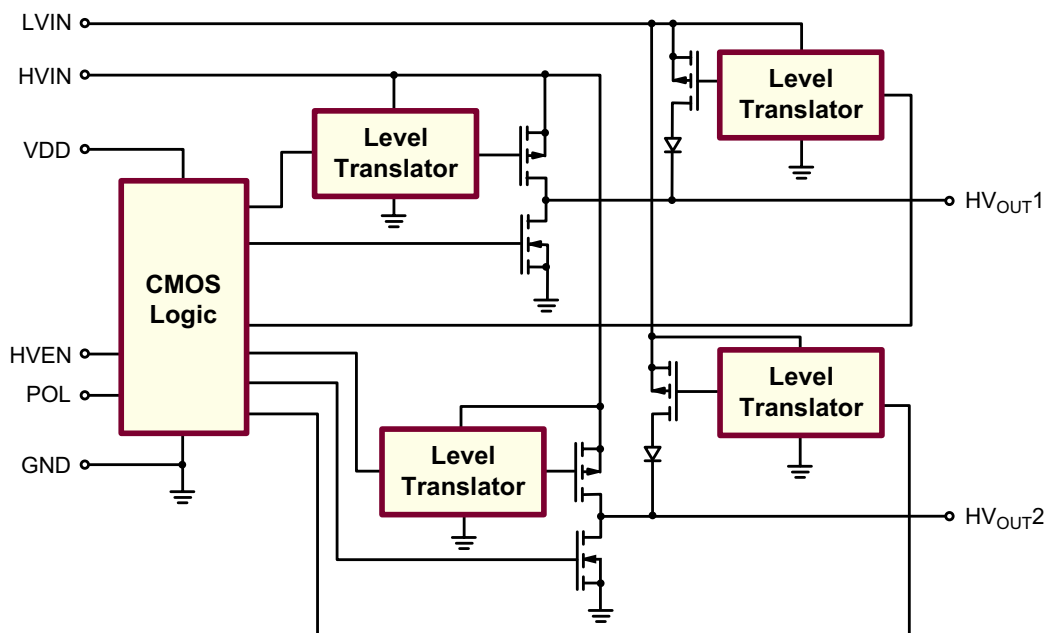
- ▶ HVCMOS® technology for high performance
- ▶ Logic-selectable output voltage
- ▶ 100nF drive capability
- ▶ Up to 90V_{P-P}
- ▶ 25µs response time

General Description

The Supertex HV508 is a 45V liquid crystal shutter driver in an 8-Lead SOIC surface mount package. It consists of two outputs that provide square waves of opposite phase. The liquid crystal shutter is connected between the two outputs. Its equivalent load can be approximated as a resistor in parallel with a capacitor. Minimum resistance is 1.0MΩ and maximum capacitance is 0.1µF.

The HV508 has three input supply voltages, HV_{IN}, LV_{IN}, and V_{DD}. The output's amplitude will be either LV_{IN} or HV_{IN}. A logic high on the HV_{EN} input will set the output to operate from the HV_{IN} supply. A logic low on the HV_{EN} input will set the output to operate from the LV_{IN} supply. The output frequency is set by the logic input frequency applied on the POL input.

Block Diagram



Ordering Information

Device	8-Lead SOIC (Narrow Body) 4.90x3.90mm body, 1.75mm height (max) 1.27mm pitch
HV508	HV508LG-G

-G indicates package is RoHS compliant ('Green')



Absolute Maximum Ratings

Parameter	Value
HV_{IN} , high voltage input	+60V
LV_{IN} , low voltage input	+7.5V
V_{DD} , logic supply voltage	+12V
Operating temperature	-5.0°C to +60°C
Storage temperature	-65°C to +150°C
Soldering temperature ¹	+300°C
Power dissipation ²	700mW

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Notes:

- Distance of 1.6mm from case for 10 seconds.
- For operation above 25°C ambient, derate linearly at 6.0mW/°C.

Recommended Operating Conditions

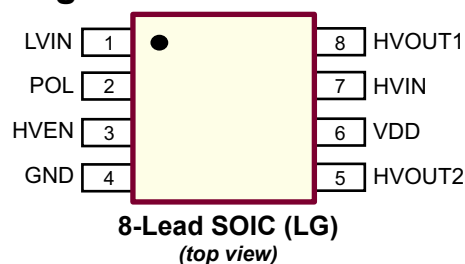
Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Logic supply voltage	5.0	-	10.0	V	---
LV_{IN}	Low output supply voltage	3.0	-	6.0	V	---
HV_{IN}	High output supply voltage	5.0	-	45	V	---
V_{IL}	Logic input voltage low	0	-	0.3 V_{DD}	V	---
V_{IH}	Logic input voltage high	0.7 V_{DD}	-	V_{DD}	V	---
T_A	Ambient temperature	-5.0	-	+60	°C	---

DC Electrical Characteristics (over operating supply voltages unless otherwise specified, $T_A = -5^\circ\text{C}$ to $+60^\circ\text{C}$)

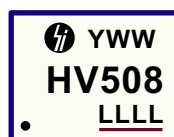
Sym	Parameter	Min	Typ	Max	Units	Conditions
I_{HVQ}	HV_{IN} quiescent current	-	-	10	µA	---
I_{LVQ}	LV_{IN} quiescent current	-	-	10	µA	---
I_{DDQ}	V_{DD} quiescent current	-	-	10	µA	---
I_{HV}	HV_{IN} operating current	-	-	2.8	mA	POL = 100Hz, HV_{EN} = high, $T_A = 25^\circ\text{C}$, Load = 1MΩ in parallel with 0.1µF between HV_{OUT1} and HV_{OUT2}
I_{LV}	LV_{IN} operating current	-	-	380	µA	POL = 100Hz, HV_{EN} = low, $T_A = 25^\circ\text{C}$, Load = 1MΩ in parallel with 0.1µF between HV_{OUT1} and HV_{OUT2}
I_{IL}	Logic input current low	-5.0	-	-	µA	---
I_{IH}	Logic input current high	-	-	5.0	µA	---
C_{LOAD}	Output capacitive load*	0	-	0.25	µF	C_{LOAD} in parallel with a 1.0MΩ resistor

* The device can operate continuously in this range without damage. AC limits are not implemented.

Pin Configuration



Product Marking



Y = Last Digit of Year Sealed
 WW = Week Sealed
 L = Lot Number
 _____ = "Green" Packaging

Package may or may not include the following marks: Si or

8-Lead SOIC (LG)

AC Electrical Characteristics ($HV_{IN} = 45V$, $LV_{IN} = 6.0V$, $V_{DD} = 5.0V$, $T_A = -5.0^{\circ}C$ to $+60^{\circ}C$)

Sym	Parameter	Min	Typ	Max	Units	Conditions
f_{POL}	POL input frequency	0	-	100	Hz	---
$t_{HV(ON)}$	Turn-on time when high voltage is enabled	-	-	16	μs	Load = 1.0M Ω in parallel with 0.1 μF between HV _{OUT1} and HV _{OUT2} , HV _{EN} = high, outputs rise to HV _{IN} . See Fig.1.
$t_{HV(OFF)}$	Turn-off time when high voltage is enabled	-	-	16	μs	
$t_{LV(ON)}$	Turn-on time when high voltage is disabled	-	-	40	μs	Load = 1.0M Ω in parallel with 0.1 μF between HV _{OUT1} and HV _{OUT2} , HV _{EN} = low, outputs rise to HV _{IN} . See Fig.1.
$t_{LV(OFF)}$	Turn-off time when high voltage is disabled	-	-	6.0	μs	
$t_{EN(ON)}$	Turn-on time from HV _{EN} to HV _{OUT}	-	-	25	μs	Load = 1.0M Ω in parallel with 0.1 μF between HV _{OUT1} and HV _{OUT2} . See Fig.2.

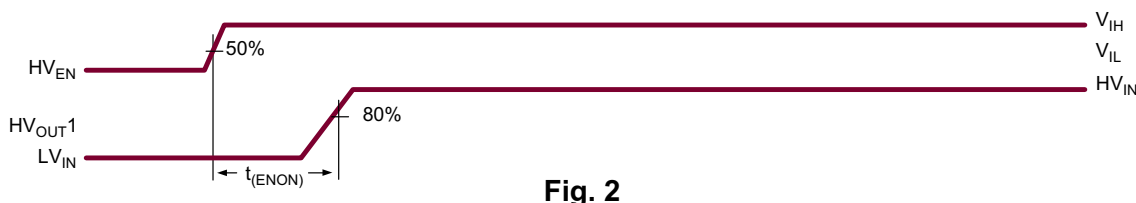
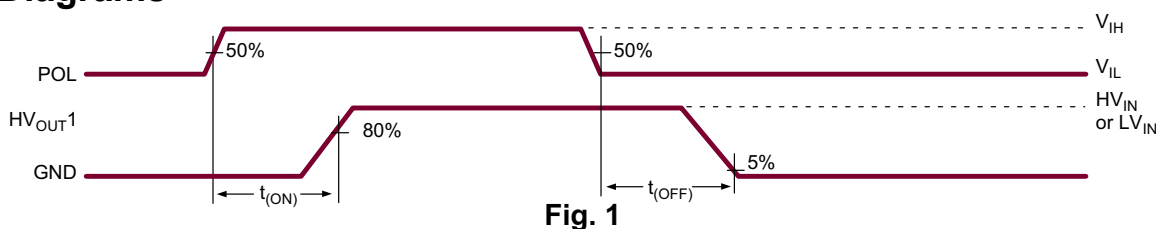
Power-Up/ Power-Down Sequences

Power-up sequence should be the following:

1. Connect GND
2. Connect V_{DD}
3. Connect logic inputs
4. Connect HV_{IN}
5. and connect LV_{IN}

Power-down sequence should be the reverse.

Timing Diagrams

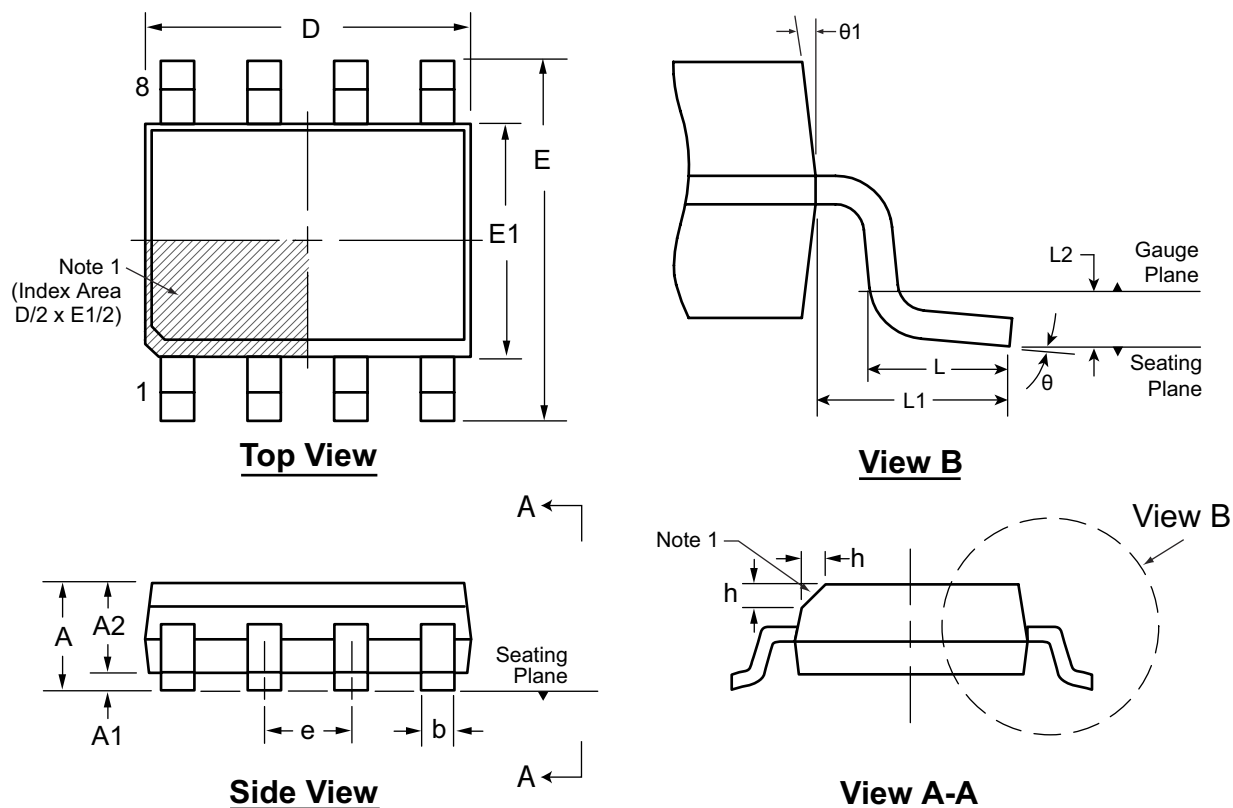


Logic Truth Table

HV _{EN}	POL	HV _{OUT1}	HV _{OUT2}
H	H	HV _{IN}	GND
H	L	GND	HV _{IN}
L	H	LV _{IN}	GND
L	L	GND	LV _{IN}

8-Lead SOIC (Narrow Body) Package Outline (LG)

4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note:
 1. This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol	A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1	
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

Supertex Doc. #: DSPD-8SOLGTG, Version I041309.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

Supertex inc. does not recommend the use of its products in life support applications, and will not knowingly sell them for use in such applications unless it receives an adequate "product liability indemnification insurance agreement." Supertex inc. does not assume responsibility for use of devices described, and limits its liability to the replacement of the devices determined defective due to workmanship. No responsibility is assumed for possible omissions and inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications refer to the Supertex inc. website: <http://www.supertex.com>.