

10-Channel, Serial-Input Latched Display Driver

Features

- ▶ High output voltage 80V
- ▶ High speed 5MHz @5.0V_{DD}
- ▶ Low power I_{BB} ≤ 0.1mA (all high)
- ▶ Active pull down 100µA min @25°C
- ▶ Output source current 25mA @60V V_{BB}
- ▶ Each device drives 10 lines
- ▶ High-speed serially-shifted data input
- ▶ 5.0V CMOS-compatible inputs
- ▶ Latches on all driver outputs
- ▶ Pin-compatible replacement for UCN5810A and TL4810A, TL4810B

Applications

- ▶ High speed dot matrix print head driver
- ▶ VFD (vacuum fluorescent display) driver

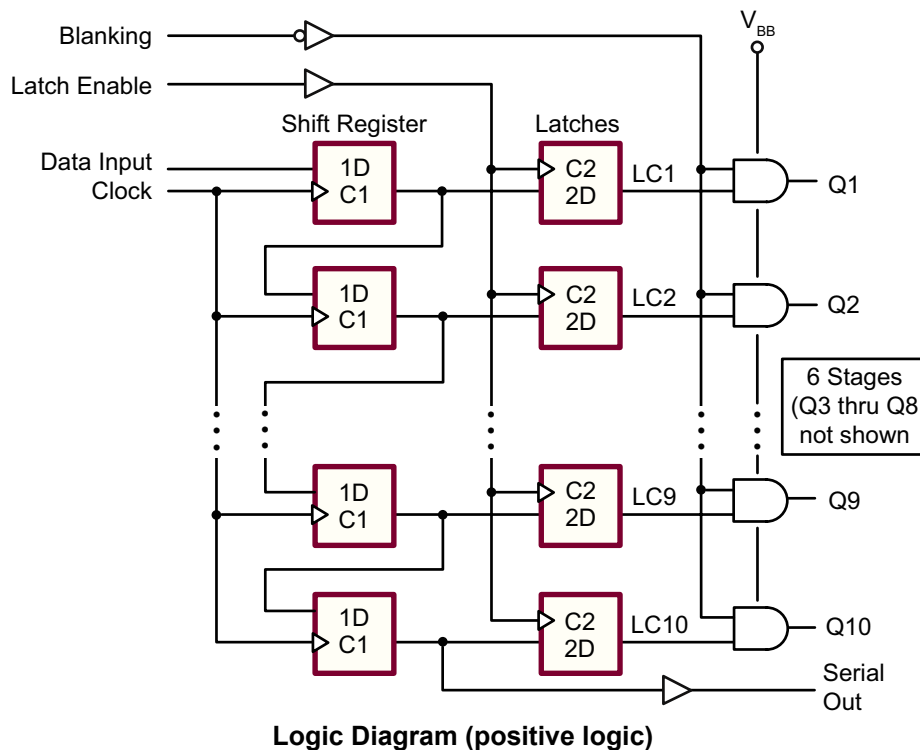
General Description

The HV6810 is a monolithic integrated circuit designed to drive a dot matrix or segmented vacuum fluorescent display (VFD). These devices feature a serial data output to cascade additional devices for large displays.

A 10-bit data word is serially loaded into the shift register on the positive-going transition of the clock. Parallel data is transferred to the output buffers through a 10-bit D-type latch while the latch enable input is high, and is latched when the latch enable is low. When the blanking input is high, all of the outputs are low.

Outputs are structures formed by double-diffused MOS (DMOS) transistors with output voltage ratings of 80V and 25mA source-current capability. All inputs are compatible with CMOS levels.

Functional Block Diagram



Ordering Information

Device	Package Options	
	20-Lead PLCC .353x.353in body .180in height (max) .050in pitch	20-Lead SOW 12.80x7.50mm body 2.65mm height (max) 1.27mm pitch
HV6810	HV6810PJ-G	HV6810WG-G

-G indicates package is RoHS compliant ("Green")



Absolute Maximum Ratings¹

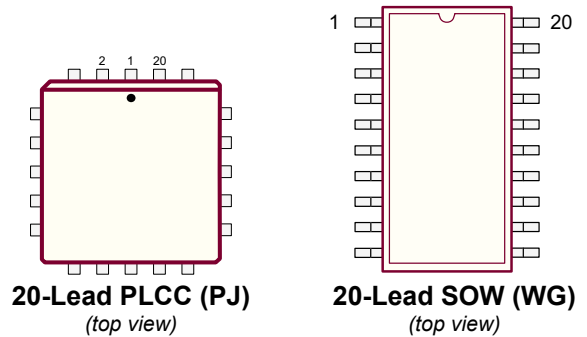
Parameter	Value
Logic supply voltage, V_{DD}^2	7.5V
Driver supply voltage, V_{BB}^2	90V
Output voltage	90V
Input voltage ¹	-0.3V to $V_{DD} + 0.3V$
Continuous total power dissipation at 25°C free-air temperature: ³	
20-Lead PLCC (PJ) ¹	1500mW
20-Lead SOW (WG) ¹	1500mW ¹
Operating temperature range	-45°C +85°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. All voltages are referenced to GND.

Notes:

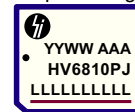
- Over operating free-air temperature
- All voltages are referenced to V_{SS}
- For operation above 25°C ambient derate linearly to 85°C at 15mW/°C

Pin Configuration



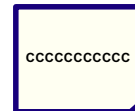
Product Marking

Top Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
A = Assembler ID
C = Country of Origin*

Bottom Marking



— = "Green" Packaging
*May be part of top marking

Package may or may not include the following marks: Si

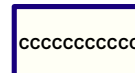
20-Lead PLCC (PJ)

Top Marking



YY = Year Sealed
WW = Week Sealed
A = Assembler ID
L = Lot Number
C = Country of Origin*

Bottom Marking



— = "Green" Packaging
*May be part of top marking

Package may or may not include the following marks: Si

20-Lead SOW (WG)

Recommended Operating Conditions

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Supply voltage	4.5	-	5.5	V	---
V_{BB}	High supply voltage	20	-	80	V	---
V_{SS}	Supply voltage	-	0	-	V	---
V_{IH}	High-level input voltage (for $V_{DD} = 5.0V$)	3.5	-	5.3	V	---
V_{IL}	Low-level input voltage	-0.3	-	0.8	V	---
I_{OH}	Continuous high-level Q output current	25	-	-	mA	---
f_{CLK}	Clock frequency	-	-	5.0	MHz	---
T_A	Operating ambient temperature	-40	-	+85	°C	---

DC Electrical Characteristics

($V_{DD} = 5.0V$, $V_{BB} = 60V$, $V_{SS} = 0V$, $T_A = 25^\circ C$ unless otherwise noted)

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	High level output voltage	Q outputs	57.5	58	-	V $I_O = +25mA$ $V_{DD} = +4.5V$, $I_{OL} = +100\mu A$
		Serial output	4.0	4.5	-	
V_{OL}	Low level output voltage	Q outputs	-	0.15	1.0	V $I_O = -100\mu A$, blanking input at V_{DD} $V_{DD} = +4.5V$, $I_O = -100\mu A$
		Serial output	-	0.05	0.1	
I_{OL}	Low level Q output current (pull-down current)	60	80	-	μA	$T_A = Max$, $V_{OL} = +0.7V$
$I_{O(OFF)}$	Off-state output current	-	-1.0	-15	μA	$V_O = 0V$, blanking input at V_{DD}
I_{IH}	High level input current	-		1.0	μA	$V_{IN} = V_{DD}$
I_{DD}	Supply current from V_{DD} (standby)	-	10	50	μA	All inputs at 0V, one Q output high
		-	10	50		All inputs at 0V, all Q outputs low
I_{BB}	Supply current from V_{BB}	-	0.05	0.1	mA	All outputs low, all Q outputs open
		-	0.05	0.1		All outputs high, all Q outputs open

* All typical values are at $T_A = 25^\circ C$ except for I_{OL} and $I_{O(OFF)}$

AC Electrical Characteristics

(Timing requirements over recommended operating conditions)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$t_{W(CKH)}$	Pulse duration, clock high	100	-	-	ns	---
$t_{W(LEH)}$	Pulse duration, latch enable high	100	-	-	ns	---
$t_{SU(D)}$	Setup time, data before clock	50	-	-	ns	---
$t_{H(D)}$	Hold time, data after clock	50	-	-	ns	---
$t_{CKH-LEH}$	Delay time, clock to latch enable high	50	-	-	ns	---
t_{PD}^*	Propagation delay time, latch enable to output	-	300	-	ns	---

* Switching characteristics, $V_{BB} = 60V$, $T_A = 25^\circ C$

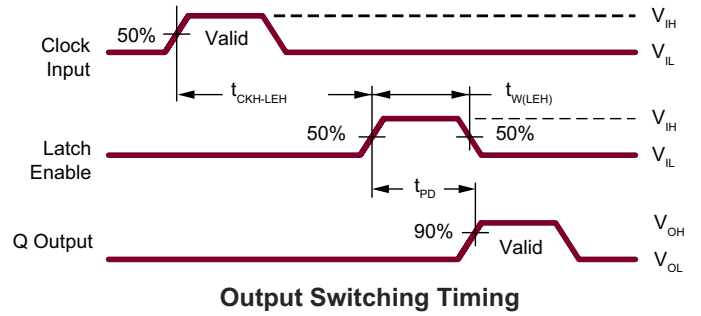
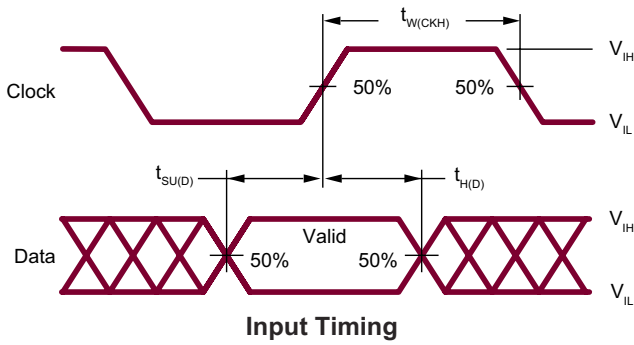
Power-up sequence should be the following:

1. Connect ground V_{SS}
2. Apply V_{DD}
3. Set all inputs (Data, CLK, Enable, etc.) to a known state
4. Apply V_{BB}

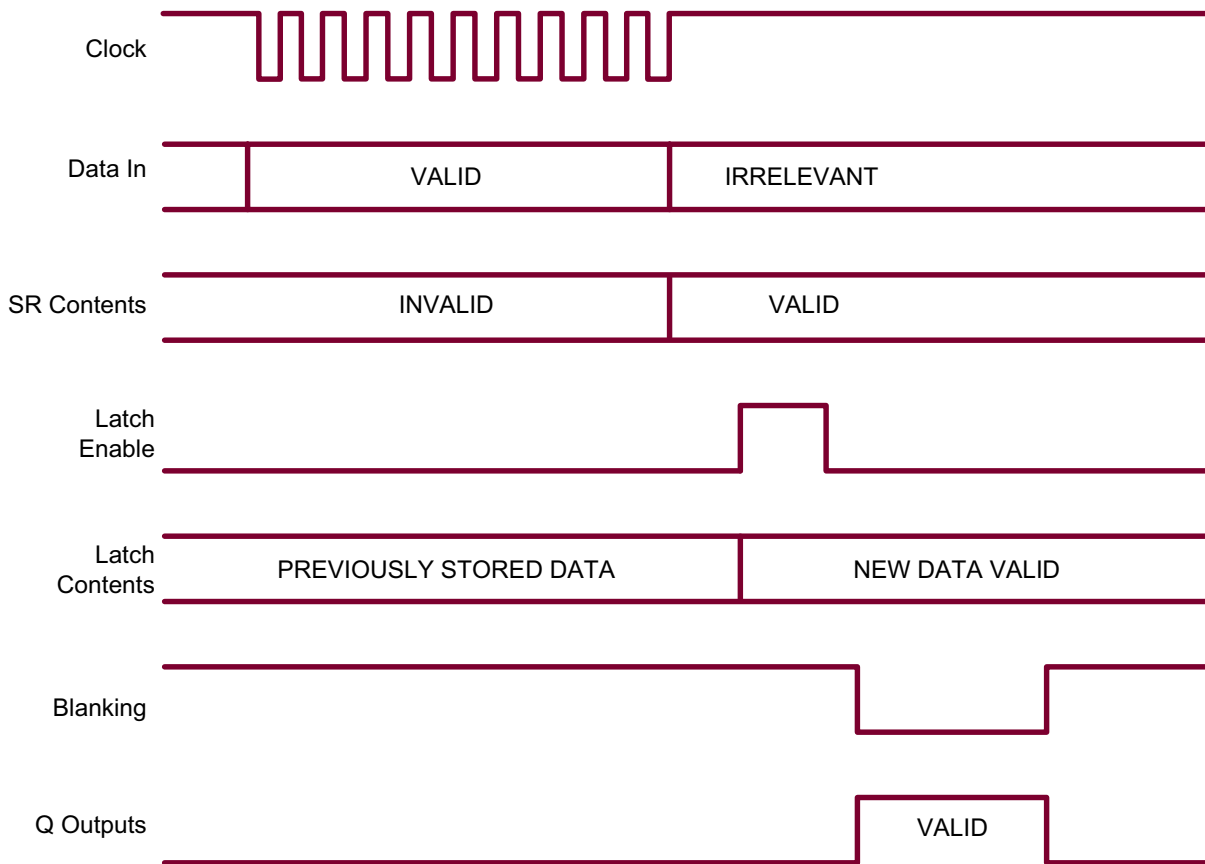
The V_{BB} should not drop below V_{DD} or float during operation.

Power-down sequence should be the reverse of the above.

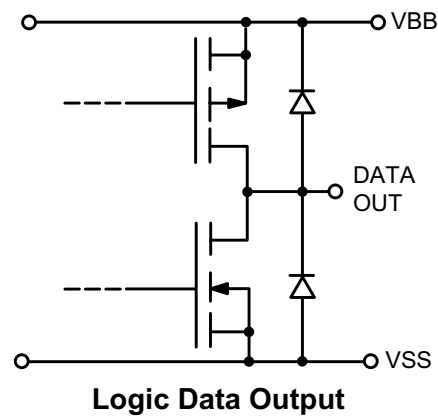
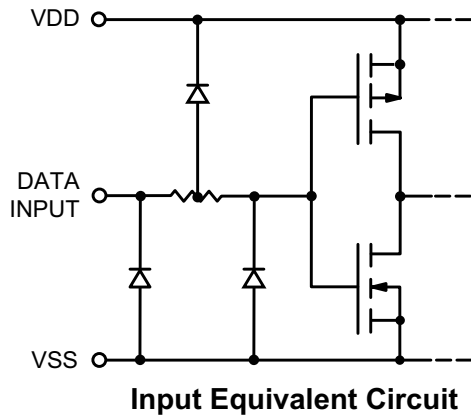
Switching Waveforms



Timing Diagram



Input and Output Equivalent Circuits



Function Table

Serial Data Input	Clock Input	Shift Register Contents		Serial Data Output	LE Strobe Input	Latch Contents		Blanking Input	Output Contents	
		I_1 I_2 I_3 ... I_{N-1} I_N	R_1 R_2 ... R_{N-2} R_{N-1}			I_1 I_2 I_3 ... I_{N-1} I_N	R_1 R_2 R_3 ... R_{N-1} R_N		O_1 O_2 O_3 ... O_{N-1} O_N	P_1 P_2 P_3 ... P_{N-1} P_N
H		H	R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}	---	---	---	---	---	---
L		L	R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}						
X		X	R_1 R_2 R_3 ... R_{N-1} R_N	R_N						
---	---	X	X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N	L	---	P_1 P_2 P_3 ... P_{N-1} P_N	
		P	P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N				
		---	---	---	---	X X X ... X X				H

Notes:

L = Low logic level, H = High logic level, X = Don't care, P = Present state, R = Previous state

= Low to high transition

= High to low transition

Pin Descriptions

20-Lead PLCC (PJ)

Pin #	Function	Description
1	Q8	High voltage output.
2	Q7	
3	Q6	
4	CLOCK	Input data is shifted into the data shift register on the positive edge of the clock.
5	N/C	No connection.
6	VSS	Usually $V_{SS} = 0V$, ground connection.
7	VDD	Low voltage power supply.
8	LE (STROBE)	When LE is high, the shift register output is latched to Q output. When LE stays high, the latches are in transparent mode.
9	Q5	High voltage output.
10	Q4	
11	Q3	
12	Q2	
13	Q1	
14	BLANKING	When blanking is high, all Q's are forced to a low state, regardless of data in each channel.
15	DATA IN	Input data for the input shift register.
16	N/C	No connection.
17	VBB	High voltage power supply.
18	SERIAL DATA OUT	Output data from the shift register.
19	Q10	High voltage output.
20	Q9	

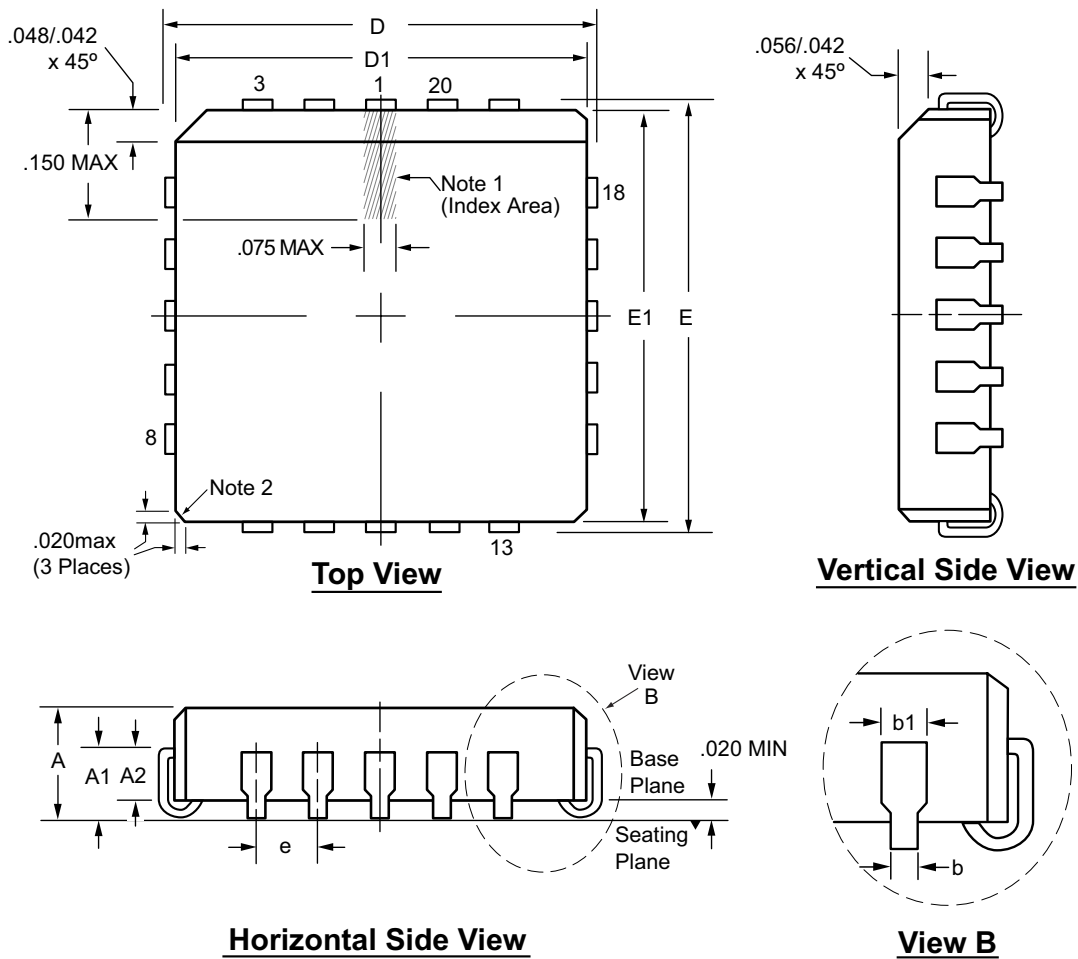
Pin Descriptions

20-Lead SOW (WG)

Pin #	Function	Description
1	Q8	High voltage output.
2	Q7	
3	Q6	
4	CLOCK	Input data are shifted into the data shift register on the positive edge of the clock.
5	VSS	Usually $V_{SS} = 0V$, ground connection.
6	N/C	No connection.
7	VDD	Low voltage power supply.
8	LE (STROBE)	When LE is high, the shift register output is latched to Q output. When LE stays high, the latches are in transparent mode.
9	Q5	High voltage output.
10	Q4	
11	Q3	
12	Q2	
13	Q1	
14	BLANKING	When blanking is high, all Q's are forced to a low state, regardless of data in each channel.
15	DATA IN	Input data for the input shift register.
16	VBB	High voltage power supply.
17	SERIAL DATA OUT	Output data from the shift register.
18	N/C	No connection.
19	Q10	High voltage output.
20	Q9	

20-Lead PLCC Package Outline (PJ)

.353x.353in body, .180in height (max), .050in pitch



Notes:

- A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
- Actual shape of this feature may vary.

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.385	.350	.385	.350	.050 BSC
	NOM	.172	.105	-	-	-	.390	.353	.390	.353	
	MAX	.180	.120	.083	.021	.032	.395	.356	.395	.356	

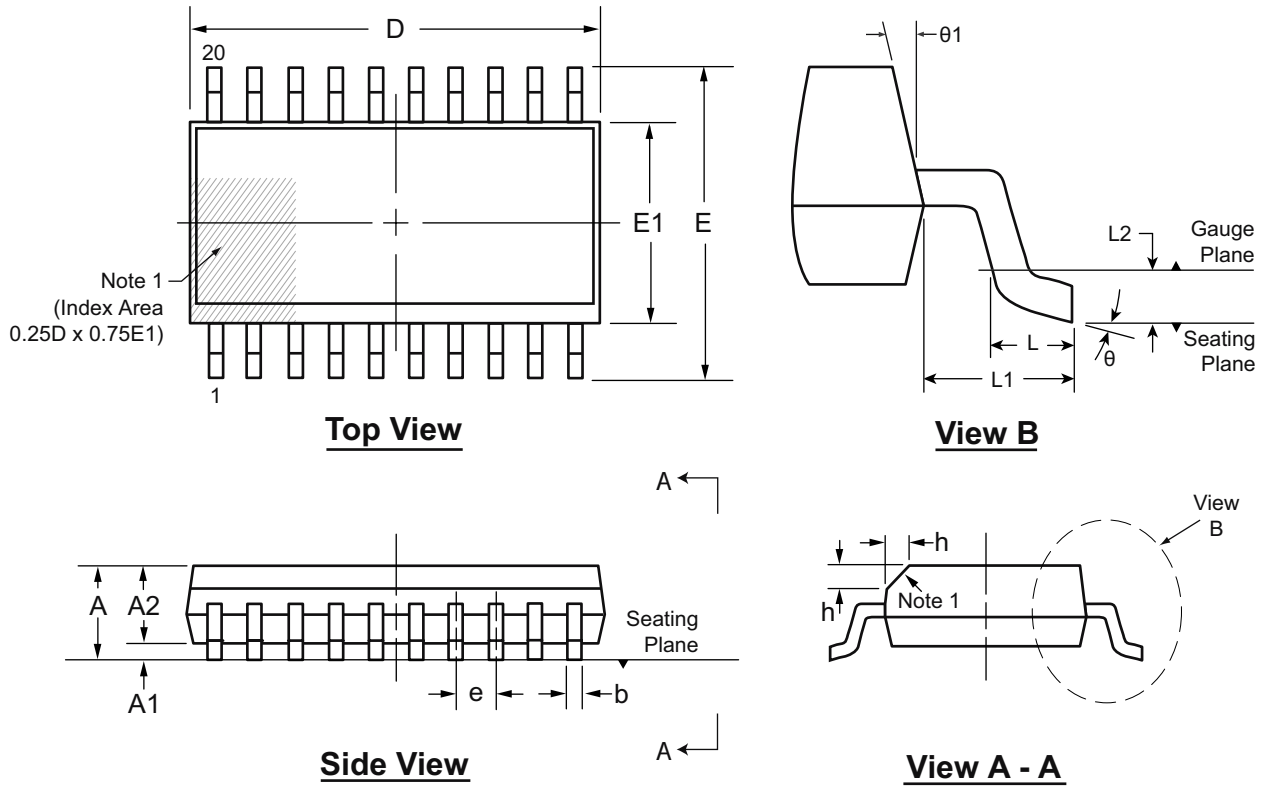
JEDEC Registration MS-018, Variation AA, Issue A, June, 1993.

Drawings not to scale.

Supertex Doc. #: DSPD-20PLCCPJ, Version B092408

20-Lead SOW (Wide Body) Package Outline (WG)

12.80x7.50mm body, 2.65mm height (max), 1.27mm pitch



Note:
 1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	2.15*	0.10	2.05	0.31	12.60*	9.97*	7.40*	1.27 BSC	0.25	0.40	1.40 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	12.80	10.30	7.50		-	-			-	-
	MAX	2.65	0.30	2.55*	0.51	13.00*	10.63*	7.60*		0.75	1.27			8°	15°

JEDEC Registration MS-013, Variation AC, Issue E, Sep. 2005.

* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

Supertex Doc. #: DSPD-20SOWWG, Version D041309.

(The package drawings in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

Supertex inc. does not recommend the use of its products in life support applications, and will not knowingly sell them for use in such applications unless it receives an adequate "product liability indemnification insurance agreement." Supertex inc. does not assume responsibility for use of devices described, and limits its liability to the replacement of the devices determined defective due to workmanship. No responsibility is assumed for possible omissions and inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications refer to the Supertex inc. (website: <http://www.supertex.com>)