National Semiconductor

January 14, 2011

DS90UB903Q/DS90UB904Q

10 - 43MHz 18 Bit Color FPD-Link III Serializer and Deserializer with Bidirectional Control Channel

General Description

The DS90UB903Q/DS90UB904Q chipset offers a FPD-Link III interface with a high-speed forward channel and a bidirectional control channel for data transmission over a single differential pair. The DS90UB903Q/904Q incorporates differential signaling on both the high-speed forward channel and bidirectional control channel data paths. The Serializer/ Deserializer pair is targeted for direct connections between graphics host controller and displays modules. This chipset is ideally suited for driving video data to displays requiring 18-bit color depth (RGB666 + HS, VS, and DE) along with bidirectional control channel bus. The primary transport converts 21 bit data over a single high-speed serial stream, along with a separate low latency bidirectional control channel transport that accepts control information from an I²C port. Using National's embedded clock technology allows transparent full-duplex communication over a single differential pair, carrying asymmetrical bidirectional control channel information in both directions. This single serial stream simplifies transferring a wide data bus over PCB traces and cable by eliminating the skew problems between parallel data and clock paths. This significantly saves system cost by narrowing data paths that in turn reduce PCB layers, cable width, and connector size and pins.

In addition, the Deserializer inputs provide equalization control to compensate for loss from the media over longer distances. Internal DC balanced encoding/decoding is used to support AC-Coupled interconnects.

The Serializer is offered in a 40-pin lead in LLP and Deserializer is offered in a 48-pin LLP packages.

Features

- 10 MHz to 43 MHz input PCLK support
- 210 Mbps to 903 Mbps data throughput
- Single differential pair interconnect
- Bidirectional control interface channel with I²C support
- Embedded clock with DC Balanced coding to support AC-coupled interconnects
- Capable to drive up to 10 meters shielded twisted-pair
- I²C compatible serial interface
- Single hardware device addressing pin
- Up to 4 General Purpose Input (GPI)/ Output (GPO)
- LOCK output reporting pin and AT-SPEED BIST diagnosis feature to validate link integrity
- Integrated termination resistors
- 1.8V- or 3.3V-compatible parallel bus interface
- Single power supply at 1.8V
- ISO 10605 ESD and IEC 61000-4-2 ESD compliant
- Automotive grade product: AEC-Q100 Grade 2 qualified
- Temperature range −40°C to +105°C
- No reference clock required on Deserializer
- Programmable Receive Equalization
- EMI/EMC Mitigation
  - DES Programmable Spread Spectrum (SSCG) outputs
  - DES Receiver staggered outputs

Applications

- Automotive Display Systems
  - Central Information Displays
  - Navigation Displays
  - Rear Seat Entertainment
  - Touch Screen Displays

Typical Application Diagram

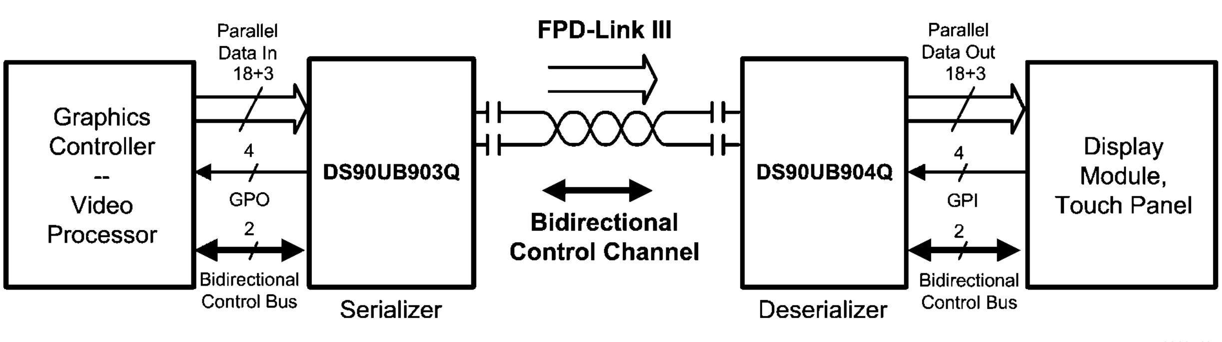

FIGURE 1. Typical Application Circuit

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Block Diagrams

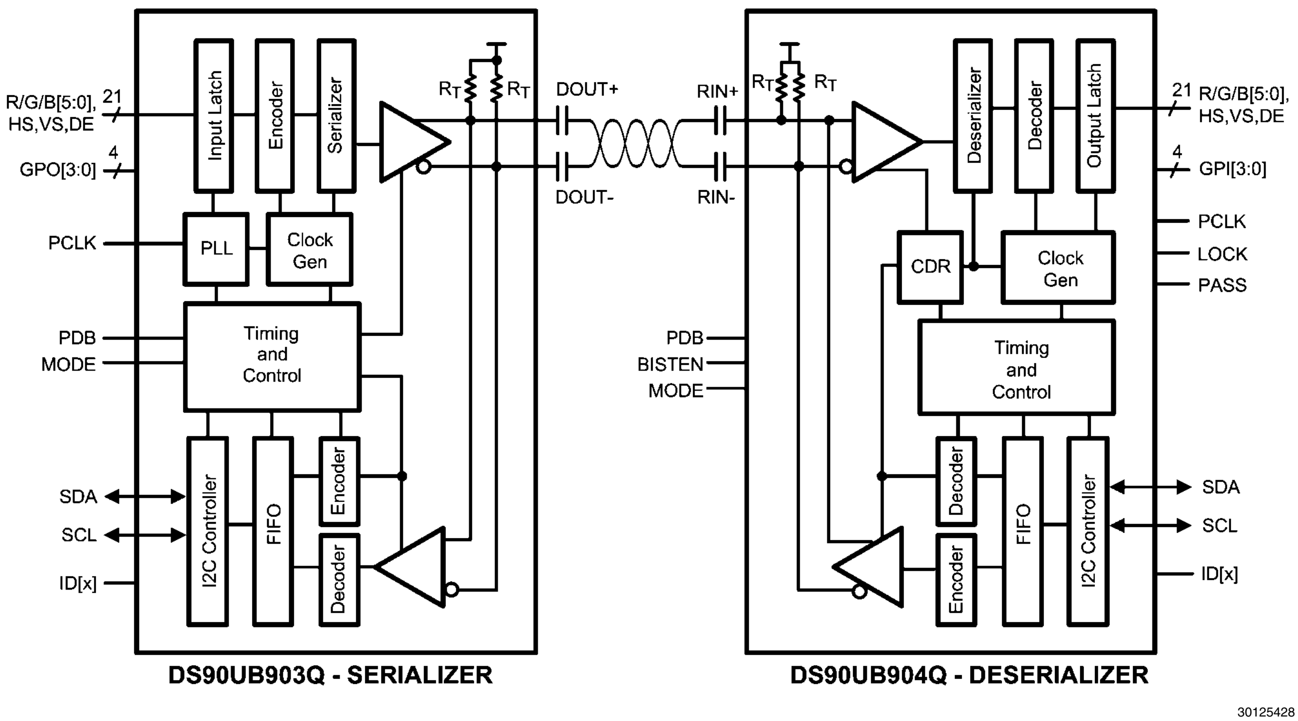


FIGURE 2. Block Diagram

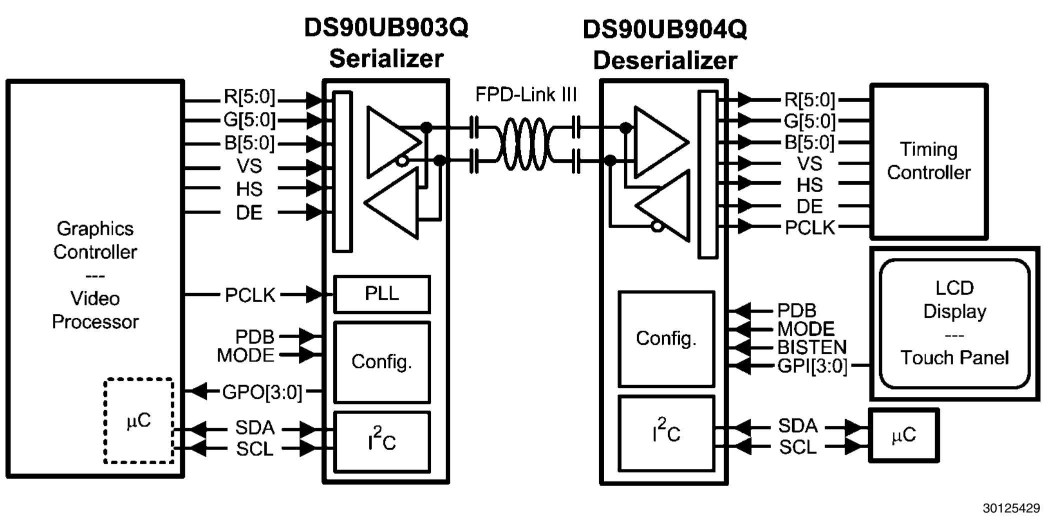


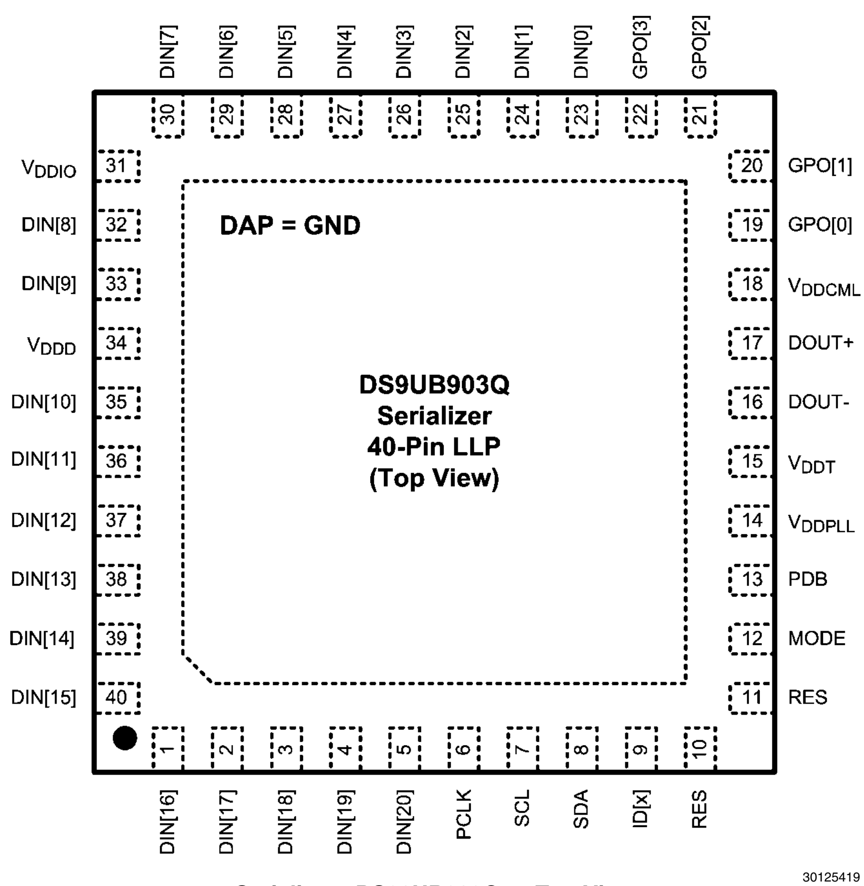
FIGURE 3. Application Block Diagram

Ordering Information

NSID	Package Description	Quantity	SPEC	Package ID
DS90UB903QSQE	40-pin LLP, 6.0 X 6.0 X 0.8 mm, 0.5 mm pitch	250	NOPB	SQA40A
DS90UB903QSQ	40-pin LLP, 6.0 X 6.0 X 0.8 mm, 0.5 mm pitch	1000	NOPB	SQA40A
DS90UB903QSQX	40-pin LLP, 6.0 X 6.0 X 0.8 mm, 0.5 mm pitch	4500	NOPB	SQA40A
DS90UB904QSQE	48-pin LLP, 7.0 X 7.0 X 0.8 mm, 0.5 mm pitch	250	NOPB	SQA48A
DS90UB904QSQ	48-pin LLP, 7.0 X 7.0 X 0.8 mm, 0.5 mm pitch	1000	NOPB	SQA48A
DS90UB904QSQX	48-pin LLP, 7.0 X 7.0 X 0.8 mm, 0.5 mm pitch	4500	NOPB	SQA48A

Note: Automotive Grade (Q) product incorporates enhanced manufacturing and support processes for the automotive market, including defect detection methodologies. Reliability qualification is compliant with the requirements and temperature grades defined in the AEC Q100 standard. Automotive Grade products are identified with the letter Q. For more information go to http://www.national.com/automotive.

DS90UB903Q Pin Diagram

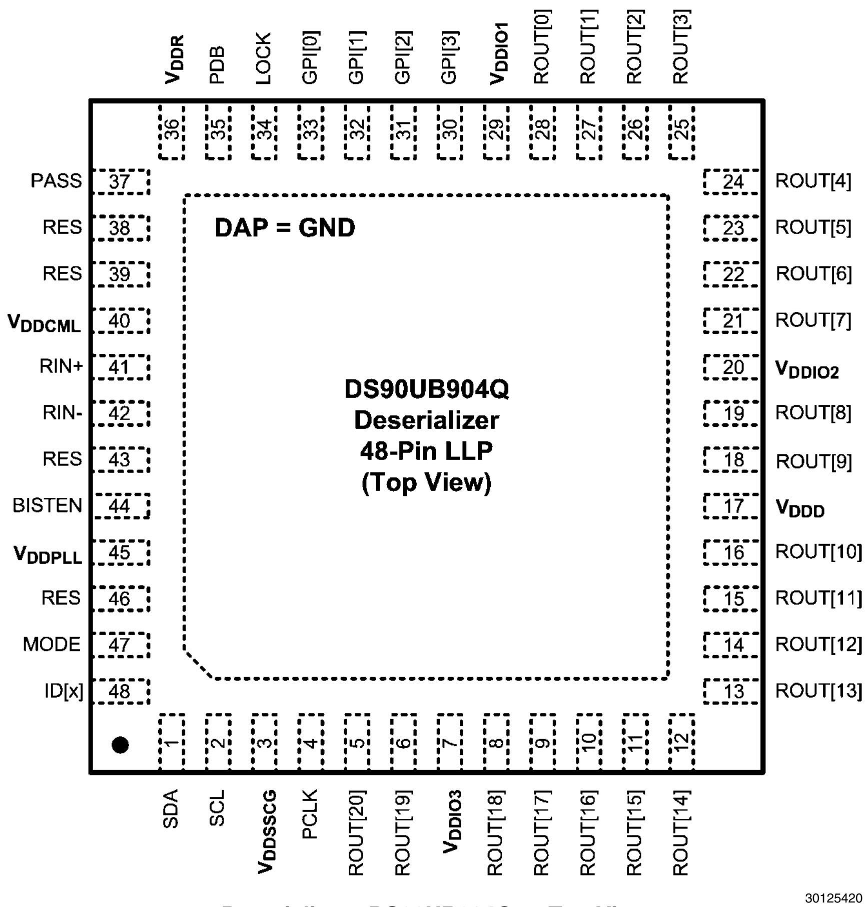


Serializer - DS90UB903Q — Top View

DS90UB903Q Serializer Pin Descriptions

Pin Name	Pin No.	I/O, Type	Description
LVCMOS PARALLEL INTERFACE			
DIN[20:0]	5, 4, 3, 2, 1, 40, 39, 38, 37, 36, 35, 33, 32, 30, 29, 28, 27, 26, 25, 24, 23	Inputs, LVCMOS w/ pull down	Parallel data inputs.
PCLK	6	Input, LVCMOS w/ pull down	Pixel Clock Input Pin. Strobe edge set by TRFB control register.
GENERAL PURPOSE OUTPUT (GPO)			
GPO[3:0]	22, 21, 20, 19	Output, LVCMOS	General-purpose output pins can be used to control and respond to various commands.
BIDIRECTIONAL CONTROL BUS - I²C COMPATIBLE			
SCL	7	Input/Output, Open Drain	Clock line for the bidirectional control bus communication SCL requires an external pull-up resistor to V_{DDIO}.
SDA	8	Input/Output, Open Drain	Data line for the bidirectional control bus communication SDA requires an external pull-up resistor to V_{DDIO}.
MODE	12	Input, LVCMOS w/ pull down	I²C Mode select MODE = L, Master mode (default); Device generates and drives the SCL clock line. Device is connected to slave peripheral on the bus. (Serializer initially starts up in Standby mode and is enabled through remote wakeup by Deserializer) MODE = H, Slave mode; Device accepts SCL clock input and attached to an I²C controller master on the bus. Slave mode does not generate the SCL clock, but uses the clock generated by the Master for the data transfers.
ID[x]	9	Input, analog	Device ID Address Select Resistor to Ground and 10 kΩ pull-up to 1.8V rail. See *Table 3*
CONTROL AND CONFIGURATION			
PDB	13	Input, LVCMOS w/ pull down	Power down Mode Input Pin. PDB = H, Serializer is enabled and is ON. PDB = L, Serailizer is in Power Down mode. When the Serializer is in Power Down, the PLL is shutdown, and IDD is minimized. Programmed control register data are NOT retained and reset to default values
RES	10, 11	Input, LVCMOS w/ pull down	Reserved. This pin MUST be tied LOW.
FPD-LINK III INTERFACE			
DOUT+	17	Input/Output, CML	Non-inverting differential output, bidirectional control channel input. The interconnect must be AC Coupled with a 100 nF capacitor.
DOUT-	16	Input/Output, CML	Inverting differential output, bidirectional control channel input. The interconnect must be AC Coupled with a 100 nF capacitor.
POWER AND GROUND			
VDDPLL	14	Power, Analog	PLL Power, 1.8V ±5%
VDDT	15	Power, Analog	Tx Analog Power, 1.8V ±5%
VDDCML	18	Power, Analog	CML & Bidirectional Channel Driver Power, 1.8V ±5%
VDDD	34	Power, Digital	Digital Power, 1.8V ±5%
VDDIO	31	Power, Digital	Power for I/O stage. The single-ended inputs and SDA, SCL are powered from V_{DDIO}. V_{DDIO} can be connected to a 1.8V ±5% or 3.3V ±10%
VSS	DAP	Ground, DAP	DAP must be grounded. DAP is the large metal contact at the bottom side, located at the center of the LLP package. Connected to the ground plane (GND) with at least 16 vias.

DS90UB904Q Pin Diagram



Deserializer - DS90UB904Q — Top View

DS90UB904Q Deserializer Pin Descriptions

Pin Name	Pin No.	I/O, Type	Description
LVCMOS PARALLEL INTERFACE			
ROUT[20:0]	5, 6, 8, 9, 10, 11, 12, 13, 14, 15, 16, 18, 19, 21, 22, 23, 24, 25, 26, 27, 28	Outputs, LVCMOS	Parallel data outputs.
PCLK	4	Output, LVCMOS	Pixel Clock Output Pin. Strobe edge set by RRFB control register.
GENERAL PURPOSE INPUT (GPI)			
GPI[3:0]	30, 31, 32, 33	Input, LVCMOS	General-purpose input pins can be used to control and respond to various commands.
BIDIRECTIONAL CONTROL BUS - I²C COMPATIBLE			
SCL	2	Input/Output, Open Drain	Clock line for the bidirectional control bus communication SCL requires an external pull-up resistor to V_{DDIO}.
SDA	1	Input/Output, Open Drain	Data line for bidirectional control bus communication SDA requires an external pull-up resistor to V_{DDIO}.
MODE	47	Input, LVCMOS w/ pull up	I²C Mode select MODE = L, Master mode; Device generates and drives the SCL clock line, where required such as Read. Device is connected to slave peripheral on the bus. MODE = H, Slave mode (default); Device accepts SCL clock input and attached to an I²C controller master on the bus. Slave mode does not generate the SCL clock, but uses the clock generated by the Master for the data transfers.
ID[x]	48	Input, analog	Device ID Address Select Resistor to Ground and 10 kΩ pull-up to 1.8V rail. See *Table 4*
CONTROL AND CONFIGURATION			
PDB	35	Input, LVCMOS w/ pull down	Power down Mode Input Pin. PDB = H, Deserializer is enabled and is ON. PDB = L, Deserializer is in Power Down mode. When the Deserializer is in Power Down. Programmed control register data are NOT retained and reset to default values.
LOCK	34	Output, LVCMOS	LOCK Status Output Pin. LOCK = H, PLL is Locked, outputs are active LOCK = L, PLL is unlocked, ROUT and PCLK output states are controlled by OSS_SEL control register. May be used as Link Status.
RES	38, 39, 43, 46	-	Reserved. Pin 46: This pin MUST be tied LOW. Pin 43: Leave pin open. Pins 38, 39: Route to test point or leave open if unused.
BIST MODE			
BISTEN	44	Input, LVCMOS w/ pull down	BIST Enable Pin. BISTEN = H, BIST Mode is enabled. BISTEN = L, BIST Mode is disabled.
PASS	37	Output, LVCOMS	PASS Output Pin for BIST mode. PASS = H, ERROR FREE Transmission PASS = L, one or more errors were detected in the received payload. Leave Open if unused. Route to test point (pad) recommended.
FPD-LINK III INTERFACE			
RIN+	41	Input/Output, CML	Noninverting differential input, bidirectional control channel output. The interconnect must be AC Coupled with a 100 nF capacitor.
RIN-	42	Input/Output, CML	Inverting differential input, bidirectional control channel output. The interconnect must be AC Coupled with a 100 nF capacitor.

Pin Name	Pin No.	I/O, Type	Description
POWER AND GROUND			
VDDSSCG	3	Power, Digital	SSCG Power, 1.8V ±5% Power supply must be connected regardless if SSCG function is in operation.
VDDIO1/2/3	29, 20, 7	Power, Digital	LVCMOS I/O Buffer Power, The single-ended outputs and control input are powered from V_{DDIO}. V_{DDIO} can be connected to a 1.8V ±5% or 3.3V ±10%
VDDD	17	Power, Digital	Digital Core Power, 1.8V ±5%
VDDR	36	Power, Analog	Rx Analog Power, 1.8V ±5%
VDDCML	40	Power, Analog	Bidirectional Channel Driver Power, 1.8V ±5%
VDDPLL	45	Power, Analog	PLL Power, 1.8V ±5%
VSS	DAP	Ground, DAP	DAP must be grounded. DAP is the large metal contact at the bottom side, located at the center of the LLP package. Connected to the ground plane (GND) with at least 16 vias.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage – V_{DDn} (1.8V)	−0.3V to +2.5V
Supply Voltage – V_{DDIO}	−0.3V to +4.0V
LVCMOS Input Voltage I/O Voltage	−0.3V to + (VDDIO + 0.3V)
CML Driver I/O Voltage (V_{DD})	−0.3V to +(V_{DD} + 0.3V)
CML Receiver I/O Voltage (V_{DD})	−0.3V to (V_{DD} + 0.3V)
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Maximum Package Power Dissipation Capacity Package	1/θ_{JA} °C/W above +25°
Package Derating:	
DS90UB903Q 40L LLP	
θ_{JA} *(based on 16 thermal vias)*	30.7 °C/W
θ_{JC} *(based on 16 thermal vias)*	6.8 °C/W
DS90UB904Q 48L LLP	
θ_{JA} *(based on 16 thermal vias)*	26.9 °C/W
θ_{JC} *(based on 16 thermal vias)*	4.4 °C/W
ESD Rating (IEC 61000-4-2)	R_D = 330Ω, C_S = 150pF
Air Discharge (DOUT+, DOUT-, RIN+, RIN-)	≥±25 kV
Contact Discharge (DOUT+, DOUT-, RIN+, RIN-)	≥±10 kV
ESD Rating (ISO10605)	R_D = 330Ω, C_S = 150/330pF
ESD Rating (ISO10605)	R_D = 2KΩ, C_S = 150/330pF
Air Discharge (DOUT+, DOUT-, RIN+, RIN-)	≥±15 kV
Contact Discharge (DOUT+, DOUT-, RIN+, RIN-)	≥±10 kV
ESD Rating (HBM)	≥±8 kV

For soldering specifications:

see product folder at www.national.com and www.national.com/ms/MS/MS-SOLDERING.pdf

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{DDn})	1.71	1.8	1.89	V
LVCMOS Supply Voltage (V_{DDIO})	1.71	1.8	1.89	V
OR				
LVCMOS Supply Voltage (V_{DDIO})	3.0	3.3	3.6	V
Supply Noise				
V_{DDn} (1.8V)			25	mVp-p
V_{DDIO} (1.8V)			25	mVp-p
V_{DDIO} (3.3V)			50	mVp-p
Operating Free Air Temperature (T_A)	-40	+25	+105	°C
PCLK Clock Frequency	10		43	MHz

Electrical Characteristics (Note 2, Note 3, Note 4)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
LVCMOS DC SPECIFICATIONS 3.3V I/O (SER INPUTS, DES OUTPUTS, GPI, GPO, CONTROL INPUTS AND OUTPUTS)							
V_{IH}	High Level Input Voltage	V_{IN} = 3.0V to 3.6V		2.0		V_{IN}	V
V_{IL}	Low Level Input Voltage	V_{IN} = 3.0V to 3.6V		GND		0.8	V
I_{IN}	Input Current	V_{IN} = 0V or 3.6V V_{IN} = 3.0V to 3.6V		-20	±1	+20	µA
V_{OH}	High Level Output Voltage	V_{DDIO} = 3.0V to 3.6V		2.4		V_{DDIO}	V
V_{OL}	Low Level Output Voltage	V_{DDIO} = 3.0V to 3.6V I_{OH} = +4 mA		GND		0.4	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V	Serializer GPO Outputs		-24		mA
			Deserializer LVCMOS Outputs		-39		
I_{OZ}	TRI-STATE® Output Current	PDB = 0V, V_{OUT} = 0V or V_{DD}	LVCMOS Outputs	-20	±1	+20	µA
LVCMOS DC SPECIFICATIONS 1.8V I/O (SER INPUTS, DES OUTPUTS, GPI, GPO, CONTROL INPUTS AND OUTPUTS)							
V_{IH}	High Level Input Voltage	V_{IN} = 1.71V to 1.89V		0.65 V_{IN}		V_{IN} +0.3	V
V_{IL}	Low Level Input Voltage	V_{IN} = 1.71V to 1.89V		GND		0.35 V_{IN}	
I_{IN}	Input Current	V_{IN} = 0V or 1.89V V_{IN} = 1.71V to 1.89V		-20	±1	+20	µA

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OH}	High Level Output Voltage	V_{DDIO} = 1.71V to 1.89V I_{OH} = –4 mA		V_{DDIO} - 0.45		V_{DDIO}	V
V_{OL}	Low Level Output Voltage	V_{DDIO} = 1.71V to 1.89V I_{OL} = +4 mA	Deserializer LVCMOS Outputs	GND		0.45	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V	Serializer GPO Outputs		-11		mA
			Deserializer LVCMOS Outputs		-20		
I_{OZ}	TRI-STATE® Output Current	PDB = 0V, V_{OUT} = 0V or V_{DD}	LVCMOS Outputs	-20	±1	+20	µA
CML DRIVER DC SPECIFICATIONS (DOUT+, DOUT-)							
$\|V_{OD}\|$	Output Differential Voltage	R_T = 100Ω (*Figure 7*)		268	340	412	mV
ΔV_{OD}	Output Differential Voltage Unbalance	R_L = 100Ω			1	50	mV
V_{OS}	Output Differential Offset Voltage	R_L = 100Ω (*Figure 7*)		$V_{DD (MIN)}$ - $V_{OD (MAX)}$	V_{DD} - V_{OD}	$V_{DD (MAX)}$ - $V_{OD (MIN)}$	V
ΔV_{OS}	Offset Voltage Unbalance	R_L = 100Ω			1	50	mV
I_{OS}	Output Short Circuit Current	DOUT+/- = 0V			-27		mA
R_T	Differential Internal Termination Resistance	Differential across DOUT+ and DOUT-		80	100	120	Ω
CML RECEIVER DC SPECIFICATIONS (RIN+, RIN-)							
V_{TH}	Differential Threshold High Voltage	(*Figure 8*)				+90	mV
V_{TL}	Differential Threshold Low Voltage			-90			
V_{IN}	Differential Input Voltage Range	RIN+ - RIN-		180			mV
I_{IN}	Input Current	V_{IN} = V_{DD} or 0V, V_{DD} = 1.89V		-20	±1	+20	µA
R_T	Differential Internal Termination Resistance	Differential across RIN+ and RIN-		80	100	120	Ω
SER/DES SUPPLY CURRENT *DIGITAL, PLL, AND ANALOG VDD							
I_{DDT}	Serializer (Tx) VDDn Supply Current (includes load current)	R_T = 100Ω WORST CASE pattern (*Figure 5*)	VDDn = 1.89V PCLK = 43 MHz Default Registers		62	90	mA
		R_T = 100Ω RANDOM PRBS-7 pattern			55		
I_{DDIOT}	Serializer (Tx) VDDIO Supply Current (includes load current)	R_T = 100Ω WORST CASE pattern (*Figure 5*)	VDDIO = 1.89V PCLK = 43 MHz Default Registers		2	5	mA
			VDDIO = 3.6V PCLK = 43 MHz Default Registers		7	15	
I_{DDTZ}	Serializer (Tx) Supply Current Power-down	PDB = 0V; All other LVCMOS Inputs = 0V	V_{DDn} = 1.89V		370	775	µA
I_{DDIOTZ}			V_{DDIO} = 1.89V		55	125	
			V_{DDIO} = 3.6V		65	135	

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{DDR}	Deserializer (Rx) VDDn Supply Current (includes load current)	V_{DDn} = 1.89V C_L = 8 pF WORST CASE Pattern (*Figure 5*)	PCLK = 43 MHz SSCG[3:0] = ON Default Registers		60	96	mA
		V_{DDn} = 1.89V C_L = 8 pF RANDOM PRBS-7 Pattern	PCLK = 43 MHz Default Registers		53		
I_{DDIOR}	Deserializer (Rx) VDDIO Supply Current (includes load current)	V_{DDIO} = 1.89V C_L = 8 pF WORST CASE Pattern (*Figure 5*)	PCLK = 43 MHz Default Registers		21	32	
		V_{DDIO} = 3.6V C_L = 8 pF WORST CASE Pattern	PCLK = 43 MHz Default Registers		49	83	
I_{DDRZ}	Deserializer (Rx) Supply Current Power-down	PDB = 0V; All other LVCMOS Inputs = 0V	V_{DDn} = 1.89V		42	400	µA
I_{DDIORZ}			V_{DDIO} = 1.89V		8	40	
			V_{DDIO} = 3.6V		350	800	

Recommended Serializer Timing for PCLK (*Note 12*)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{TCP}	Transmit Clock Period	10 MHz – 43 MHz	23.3	T	100	ns
t_{TCIH}	Transmit Clock Input High Time		0.4T	0.5T	0.6T	ns
t_{TCIL}	Transmit Clock Input Low Time		0.4T	0.5T	0.6T	ns
t_{CLKT}	PCLK Input Transition Time (*Figure 9*)		0.5		3	ns
f_{OSC}	Internal oscillator clock source			25		MHz

Serializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{LHT}	CML Low-to-High Transition Time	R_L = 100Ω (*Figure 6*)		150	330	ps
t_{HLT}	CML High-to-Low Transition Time	R_L = 100Ω (*Figure 6*)		150	330	ps
t_{DIS}	Data Input Setup to PCLK	Serializer Data Inputs (*Figure 10*)	2.0			ns
t_{DIH}	Data Input Hold from PCLK		2.0			ns
t_{PLD}	Serializer PLL Lock Time	R_L = 100Ω (*Note 5*, *Note 11*)		1	2	ms
t_{SD}	Serializer Delay	R_T = 100Ω PCLK = 10–43 MHz Register 0x03h b[0] (TRFB = 1) (*Figure 12*)	6.386T + 5	6.386T + 12	6.386T + 19.7	ns
t_{JIND}	Serializer Output Deterministic Jitter	Serializer output intrinsic deterministic jitter . Measured (cycle-cycle) with PRBS-7 test pattern PCLK = 43 MHz (*Note 4*, *Note 13*)		0.13		UI
t_{JINR}	Serializer Output Random Jitter	Serializer output intrinsic random jitter (cycle-cycle). Alternating-1,0 pattern. PCLK = 43 MHz (*Note 4*, *Note 13*)		0.04		UI
t_{JINT}	Peak-to-peak Serializer Output Jitter	Serializer output peak-to-peak jitter includes deterministic jitter, random jitter, and jitter transfer from serializer input. Measured (cycle-cycle) with PRBS-7 test pattern. PCLK = 43 MHz (*Note 4*, *Note 13*)		0.396		UI
λ_{STXBW}	Serializer Jitter Transfer Function -3 dB Bandwidth	PCLK = 43 MHz Default Registers (*Figure 18*) (*Note 4*)		1.90		MHz
δ_{STX}	Serializer Jitter Transfer Function (Peaking)	PCLK = 43 MHz Default Registers (*Figure 18*) (*Note 4*)		0.944		dB
δ_{STXf}	Serializer Jitter Transfer Function (Peaking Frequency)	PCLK = 43 MHz Default Registers (*Figure 18*) (*Note 4*)		500		kHz

Deserializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{RCP}	Receiver Output Clock Period	$t_{RCP} = t_{TCP}$	PCLK	23.3	T	100	ns
t_{PDC}	PCLK Duty Cycle	Default Registers SSCG[3:0] = OFF	PCLK	45	50	55	%
t_{CLH}	LVCMOS Low-to-High Transition Time	V_{DDIO}: 1.71V to 1.89V or 3.0 to 3.6V, C_L = 8 pF (lumped load) Default Registers (*Figure 14*) (*Note 10*)	PCLK	1.3	2.0	2.8	ns
t_{CHL}	LVCMOS High-to-Low Transition Time			1.3	2.0	2.8	
t_{CLH}	LVCMOS Low-to-High Transition Time	V_{DDIO}: 1.71V to 1.89V or 3.0 to 3.6V, C_L = 8 pF (lumped load) Default Registers (*Figure 14*) (*Note 10*)	Deserializer ROUTn Data Outputs	1.6	2.4	3.3	ns
t_{CHL}	LVCMOS High-to-Low Transition Time			1.6	2.4	3.3	
t_{ROS}	ROUT Setup Data to PCLK	V_{DDIO}: 1.71V to 1.89V or 3.0V to 3.6V, C_L = 8 pF (lumped load) Default Registers	Deserializer ROUTn Data Outputs	0.38T	0.5T		ns
t_{ROH}	ROUT Hold Data to PCLK			0.38T	0.5T		
t_{DD}	Deserializer Delay	Default Registers Register 0x03h b[0] (RRFB = 1) (*Figure 15*)	10 MHz–43 MHz	4.571T + 8	4.571T + 12	4.571T + 16	ns
t_{DDLT}	Deserializer Data Lock Time	(*Figure 13*) (*Note 5*)	10 MHz–43 MHz			10	ms
t_{RJIT}	Receiver Input Jitter Tolerance	(*Figure 17*, *Figure 19*) (*Note 13*, *Note 14*)	43 MHz		0.53		UI
t_{RCJ}	Receiver Clock Jitter	PCLK SSCG[3:0] = OFF (*Note 6*, *Note 10*)	10 MHz		300	550	ps
			43 MHz		120	250	
t_{DPJ}	Deserializer Period Jitter	PCLK SSCG[3:0] = OFF (*Note 7*, *Note 10*)	10 MHz		425	600	ps
			43 MHz		320	480	
t_{DCCJ}	Deserializer Cycle-to-Cycle Clock Jitter	PCLK SSCG[3:0] = OFF (*Note 8*, *Note 10*)	10 MHz		320	500	ps
			43 MHz		300	500	
fdev	Spread Spectrum Clocking Deviation Frequency	LVCMOS Output Bus SSC[3:0] = ON (*Figure 20*)	20 MHz–43 MHz		±0.5% to ±2.0%		%
fmod	Spread Spectrum Clocking Modulation Frequency		20 MHz–43 MHz		9 kHz to 66 kHz		kHz

Bidirectional Control Bus AC Timing Specifications (SCL, SDA) - I²C Compliant (*Figure 4*)

Over recommended supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECOMMENDED INPUT TIMING REQUIREMENTS (*Note 12*)						
f_{SCL}	SCL Clock Frequency		>0		100	kHz
t_{LOW}	SCL Low Period	f_{SCL} = 100 kHz	4.7			µs
t_{HIGH}	SCL High Period		4.0			µs
$t_{HD:STA}$	Hold time for a start or a repeated start condition		4.0			µs
$t_{SU:STA}$	Set Up time for a start or a repeated start condition		4.7			µs
$t_{HD:DAT}$	Data Hold Time		0		3.45	µs
$t_{SU:DAT}$	Data Set Up Time		250			ns
$t_{SU:STO}$	Set Up Time for STOP Condition		4.0			µs
t_r	SCL & SDA Rise Time				1000	ns
t_f	SCL & SDA Fall Time				300	ns
C_b	Capacitive load for bus				400	pF
SWITCHING CHARACTERISTICS (*Note 11*)						
f_{SCL}	SCL Clock Frequency	Serializer MODE = 0 – R/W Register 0x05 = 0x40'h		100		kHz
		Deserializer MODE = 0 – READ Register 0x06 b[6:4] = 0x00'h		100		
t_{LOW}	SCL Low Period	Serializer MODE = 0 – R/W Register 0x05 = 0x40'h	4.7			µs
		Deserializer MODE = 0 – READ Register 0x06 b[6:4] = 0x00'h				
t_{HIGH}	SCL High Period	Serializer MODE = 0 – R/W Register 0x05 = 0x40'h	4.0			µs
		Deserializer MODE = 0 – READ Register 0x06 b[6:4] = 0x00'h				
$t_{HD:STA}$	Hold time for a start or a repeated start condition	Serializer MODE = 0 Register 0x05 = 0x40'h	4.0			µs
$t_{SU:STA}$	Set Up time for a start or a repeated start condition	Serializer MODE = 0 Register 0x05 = 0x40'h	4.7			µs
$t_{HD:DAT}$	Data Hold Time		0		3.45	µs
$t_{SU:DAT}$	Data Set Up Time		250			ns
$t_{SU:STO}$	Set Up Time for STOP Condition	Serializer MODE = 0	4.0			µs
t_f	SCL & SDA Fall Time				300	ns
t_{BUF}	Bus free time between a stop and start condition	Serializer MODE = 0	4.7			µs
$t_{TIMEOUT}$	NACK Time out	Serializer MODE = 1		1		ms
		Deserializer MODE = 1 Register 0x06 b[2:0]=111'b		25		

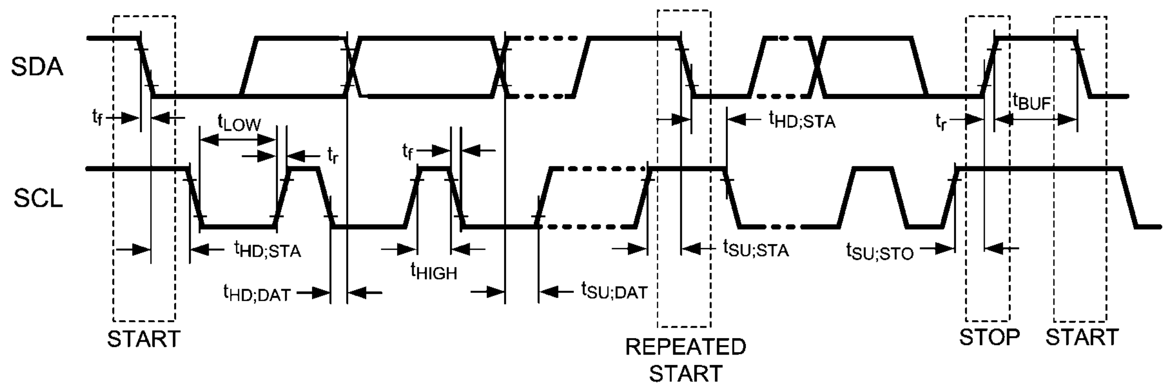


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FIGURE 4. Bidirectional Control Bus Timing

Bidirectional Control Bus DC Characteristics (SCL, SDA) - I²C Compliant

Over recommended supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Level	SDA and SCL	0.7 x V_{DDIO}		V_{DDIO}	V
V_{IL}	Input Low Level Voltage	SDA and SCL	GND		0.3 x V_{DDIO}	V
V_{HY}	Input Hysteresis	SDA and SCL		>50		mV
I_{OZ}	TRI-STATE Output Current	PDB = 0V V_{OUT} = 0V or V_{DD}	-20	±1	+20	µA
I_{IN}	Input Current	SDA or SCL, Vin = V_{DDIO} or GND	-20	±1	+20	µA
C_{IN}	Input Pin Capacitance			<5		pF
V_{OL}	Low Level Output Voltage	SCL and SDA V_{DDIO} = 3.0V I_{OL} = 1.5 mA			0.36	V
		SCL and SDA V_{DDIO} = 1.71V I_{OL} = 1 mA			0.36	V

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional; the device should not be operated beyond such conditions.

Note 2: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 3: Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except VOD, ΔVOD, VTH and VTL which are differential voltages.

Note 4: Typical values represent most likely parametric norms at 1.8V or 3.3V, T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 5: t_{PLD} and t_{DDLT} is the time required by the serializer and deserializer to obtain lock when exiting power-down state with an active PCLK

Note 6: t_{DCJ} is the maximum amount of jitter measured over 30,000 samples based on Time Interval Error (TIE).

Note 7: t_{DPJ} is the maximum amount the period is allowed to deviate measured over 30,000 samples.

Note 8: t_{DCCJ} is the maximum amount of jitter between adjacent clock cycles measured over 30,000 samples.

Note 9: Supply noise testing was done with minimum capacitors (as shown on Figures 35, 36) on the PCB. A sinusoidal signal is AC coupled to the VDDn (1.8V) supply with amplitude = 25 mVp-p measured at the device VDDn pins. Bit error rate testing of input to the Ser and output of the Des with 10 meter cable shows no error when the noise frequency on the Ser is less than 1 MHz. The Des on the other hand shows no error when the noise frequency is less than 750 kHz.

Note 10: Specification is guaranteed by characterization and is not tested in production.

Note 11: Specification is guaranteed by design.

Note 12: Recommended Input Timing Requirements are input specifications and not tested in production.

Note 13: UI – Unit Interval is equivalent to one ideal serialized data bit width. The UI scales with PCLK frequency.

Note 14: t_{RJIT} max (0.61UI) is limited by instrumentation and actual t_{RJIT} of in-band jitter at low frequency (<2 MHz) is greater 1 UI.

AC Timing Diagrams and Test Circuits

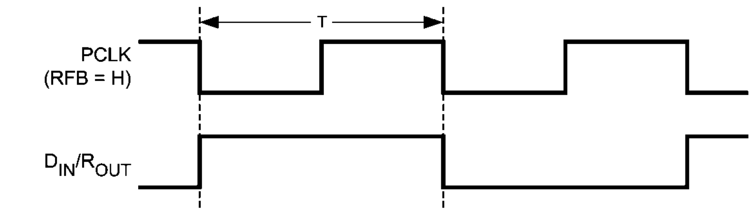

FIGURE 5. "Worst Case" Test Pattern

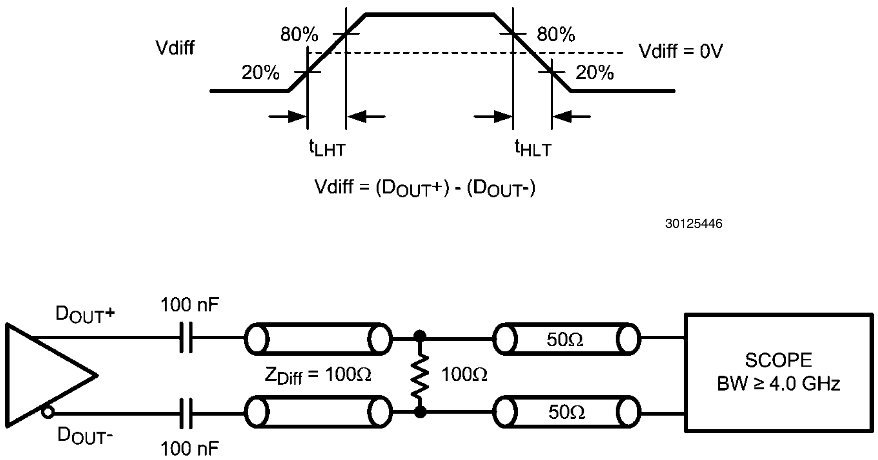

FIGURE 6. Serializer CML Output Load and Transition Times

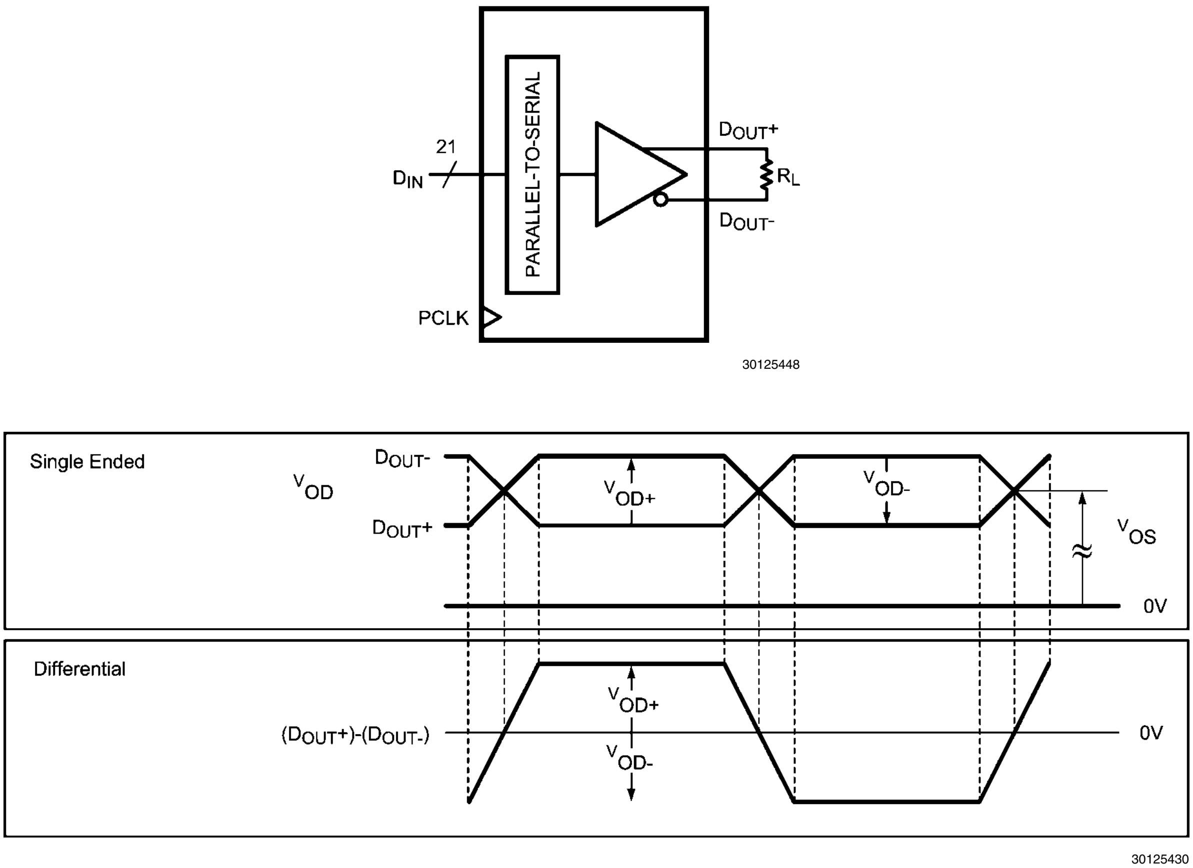

FIGURE 7. Serializer VOD DC Diagram

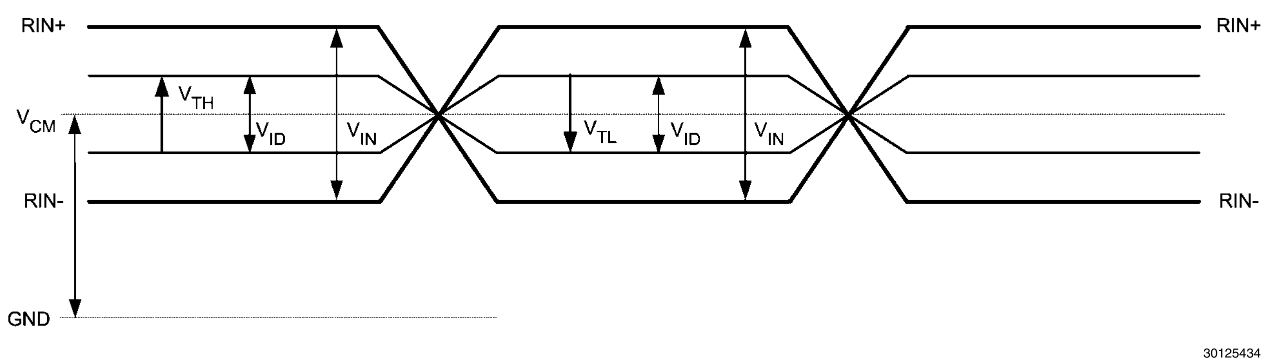

FIGURE 8. Differential VTH/VTL Definition Diagram

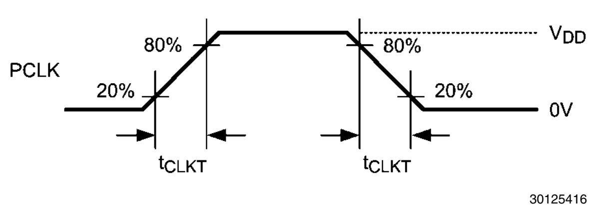

FIGURE 9. Serializer Input Clock Transition Times

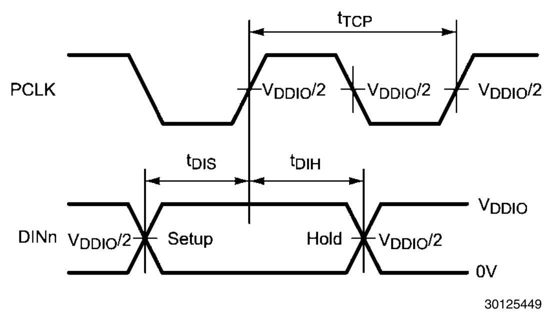

FIGURE 10. Serializer Setup/Hold Times

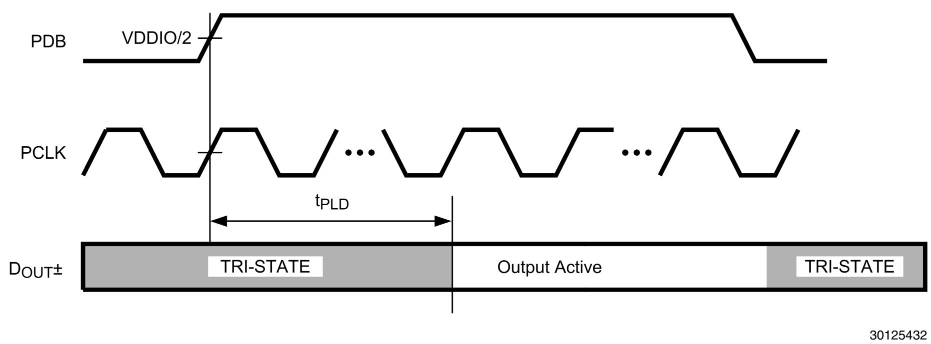

FIGURE 11. Serializer Data Lock Time

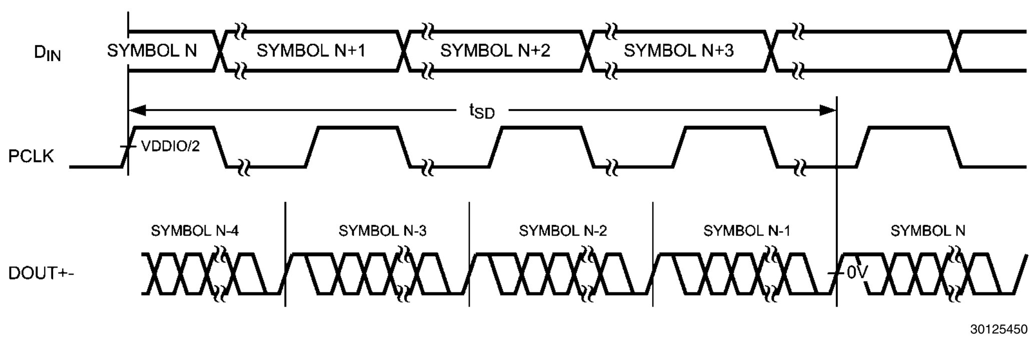

FIGURE 12. Serializer Delay

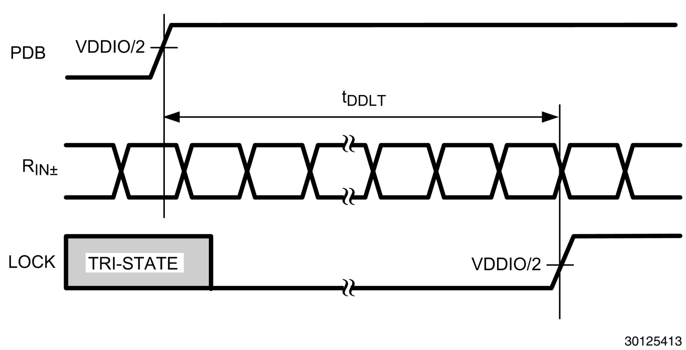

FIGURE 13. Deserializer Data Lock Time

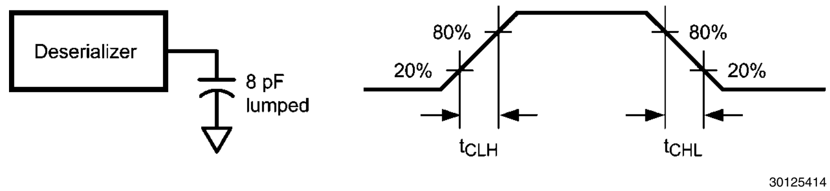

FIGURE 14. Deserializer LVCMOS Output Load and Transition Times

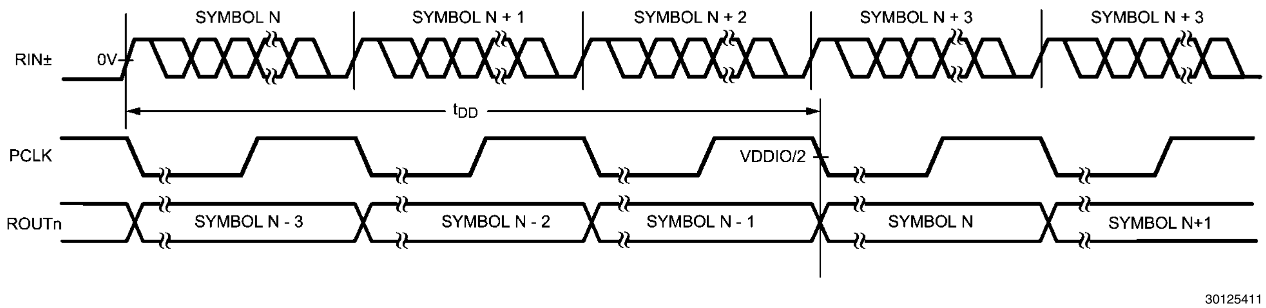

FIGURE 15. Deserializer Delay

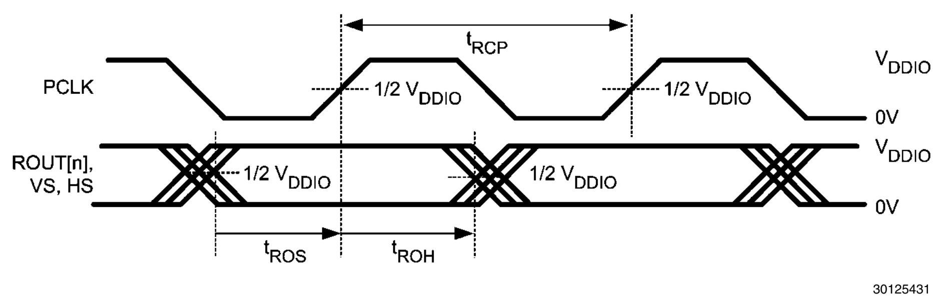

FIGURE 16. Deserializer Output Setup/Hold Times

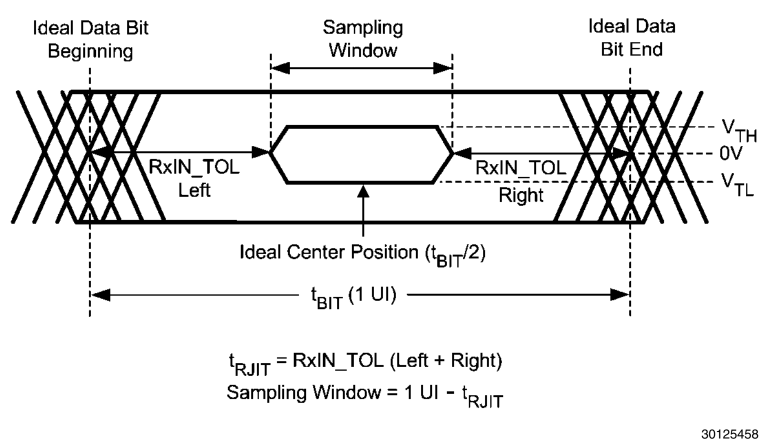

FIGURE 17. Receiver Input Jitter Tolerance

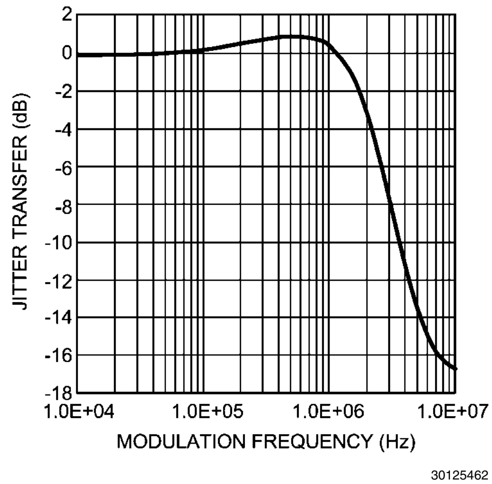

FIGURE 18. Typical Serializer Jitter Transfer Function Curve at 43 MHz

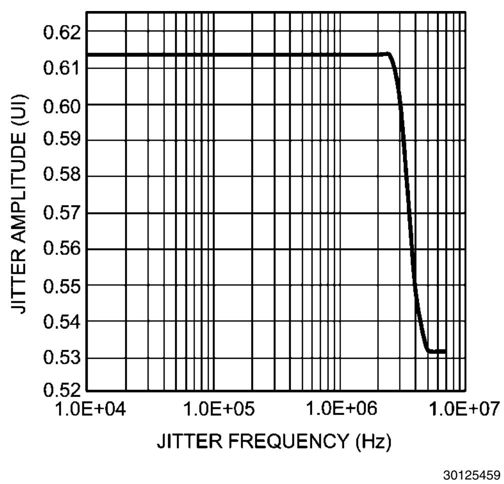

FIGURE 19. Typical Deserializer Input Jitter Tolerance Curve at 43 MHz

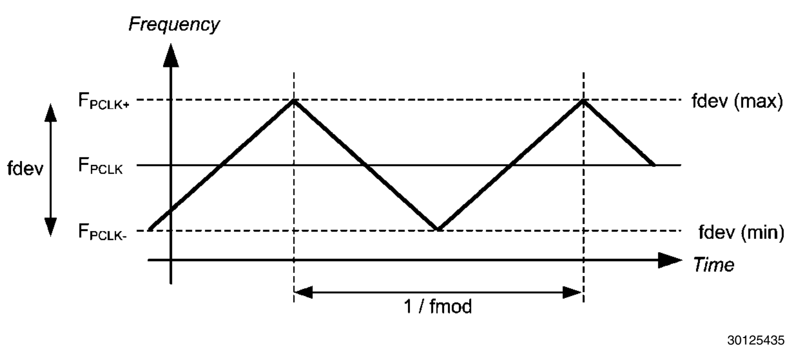

FIGURE 20. Spread Spectrum Clock Output Profile

TABLE 1. DS90UB903Q Control Registers

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
0	I2C Device ID	7:1	DEVICE ID	RW	0xB0'h	7-bit address of Serializer; 0x58'h (1011_000X'b) default
		0	SER ID SEL			0: Device ID is from ID[x] 1: Register I2C Device ID overrides ID[x]
1	Reset	7:3	RESERVED		0x00'h	Reserved
		2	$\overline{\text{STANDBY}}$	RW	0	Standby mode control. Retains control register data. Supported only when MODE = 0 0: Enabled. Low-current Standby mode with wake-up capability. Suspends all clocks and functions. 1: Disabled. Standby and wake-up disabled
		1	DIGITAL RESET0	RW	0 self clear	1: Resets the device to default register values. Does not affect device I2C Bus or Device ID
		0	DIGITAL RESET1	RW	0 self clear	1: Digital Reset, retains all register values
2	Reserved	7:0	RESERVED		0x20'h	Reserved
3	Reserved	7:6	RESERVED		11'b	Reserved
	VDDIO Control	5	VDDIO CONTOL	RW	1	Auto V_{DDIO} detect Allows manual setting of VDDIO by register. 0: Disable 1: Enable (auto detect mode)
	VDDIO Mode	4	VDDIO MODE	RW	1	VDDIO voltage set Only used when VDDIOCONTROL = 0 0: 1.8V 1: 3.3V
	I2C Pass-Through	3	I2C PASS-THROUGH	RW	1	I2C Pass-Through 0: Disabled 1: Enabled
	RESERVED	2	RESERVED		0	Reserved
	PCLK_AUTO	1	PCLK_AUTO	RW	1	Switch over to internal 25 MHz Oscillator clock in the absence of PCLK 0: Disable 1: Enable
	TRFB	0	TRFB	RW	1	Pixel Clock Edge Select: 0: Parallel Interface Data is strobed on the Falling Clock Edge. 1: Parallel Interface Data is strobed on the Rising Clock Edge.
4	RESERVED	7:0	RESERVED		0x80'h	Reserved
5	I2C Bus Rate	7:0	I2C BUS RATE	RW	0x40'h	I2C SCL frequency is determined by the following: f_{SCL} = 6.25 MHz / Register value (in decimal) 0x40'h = ~100 kHz SCL (default) Note: Register values <0x32'h are NOT supported.
6	DES ID	7:1	DES DEV ID	RW	0xC0'h	Deserializer Device ID = 0x60'h (1100_000X'b) default
		0	RESERVED			Reserved
7	Slave ID	7:1	SLAVE DEV ID	RW	0x00'h	Slave Device ID. Sets remote slave I2C address.
		0	RESERVED			Reserved
8	Reserved	7:0	RESERVED		0x00'h	Reserved
9	Reserved	7:0	RESERVED		0x01'h	Reserved
A	Reserved	7:0	RESERVED		0x00'h	Reserved

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
B	Reserved	7:0	RESERVED		0x00'h	Reserved
C	Reserved	7:3	RESERVED		0x00'h	Reserved
	PCLK Detect	2	PCLK DETECT	R	0	1: Valid PCLK detected 0: Valid PCLK not detected
	Reserved	3	RESERVED		0	Reserved
	Cable Link Detect Status	0	LINK DETECT	R	0	0: Cable link not detected 1: Cable link detected
D	Reserved	7:0	RESERVED		0x11'h	Reserved
E	Reserved	7:0	RESERVED		0x01'h	Reserved
F	Reserved	7:0	RESERVED		0x03'h	Reserved
10	Reserved	7:0	RESERVED		0x03'h	Reserved
11	Reserved	7:0	RESERVED		0x03'h	Reserved
12	Reserved	7:0	RESERVED		0x03'h	Reserved
13	General Purpose Control Reg	7:0	GPCR[7] GPCR[6] GPCR[5] GPCR[4] GPCR[3] GPCR[2] GPCR[1] GPCR[0]	RW	0x00'h	0: LOW 1: HIGH

TABLE 2. DS90UB904Q Control Registers

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
0	I2C Device ID	7:1	DEVICE ID	RW	0xC0'h	7-bit address of Deserializer; 0x60h (1100_000X) default
		0	DES ID SEL			0: Device ID is from ID[x] 1: Register I2C Device ID overrides ID[x]
1	Reset	7:3	RESERVED		0x00'h	Reserved
		2	REM_WAKEUP	RW	0	Remote Wake-up Select 1: Enable Generate remote wakeup signal automatically wake-up the Serializer in Standby mode 0: Disable Puts the Serializer in Standby mode
		1	DIGITALRESET0	RW	0 self clear	1: Resets the device to default register values. Does not affect device I2C Bus or Device ID
		0	DIGITALRESET1	RW	0 self clear	1: Digital Reset, retains all register values
2	RESERVED	7:6	RESERVED		00'b	Reserved
	Auto Clock	5	AUTO_CLOCK	RW	0	1: Output PCLK or Internal 25 MHz Oscillator clock 0: Only PCLK when valid PCLK present
	OSS Select	4	OSS_SEL	RW	0	Output Sleep State Select 0: Outputs = TRI-STATE, when LOCK = L 1: Outputs = LOW , when LOCK = L
	SSCG	3:0	SSCG		0000'b	SSCG Select 0000: Normal Operation, SSCG OFF (default) 0001: fmod (kHz) PCLK/2168, fdev ±0.50% 0010: fmod (kHz) PCLK/2168, fdev ±1.00% 0011: fmod (kHz) PCLK/2168, fdev ±1.50% 0100: fmod (kHz) PCLK/2168, fdev ±2.00% 0101: fmod (kHz) PCLK/1300, fdev ±0.50% 0110: fmod (kHz) PCLK/1300, fdev ±1.00% 0111: fmod (kHz) PCLK/1300, fdev ±1.50% 1000: fmod (kHz) PCLK/1300, fdev ±2.00% 1001: fmod (kHz) PCLK/868, fdev ±0.50% 1010: fmod (kHz) PCLK/868, fdev ±1.00% 1011: fmod (kHz) PCLK/868, fdev ±1.50% 1100: fmod (kHz) PCLK/868, fdev ±2.00% 1101: fmod (kHz) PCLK/650, fdev ±0.50% 1110: fmod (kHz) PCLK/650, fdev ±1.00% 1111: fmod (kHz) PCLK/650, fdev ±1.50%

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
3	RESERVED	7:6	RESERVED		11'b	Reserved
	VDDIO Control	5	VDDIO CONTROL	RW	1	Auto voltage control 0: Disable 1: Enable (auto detect mode)
	VDDIO Mode	4	VDDIO MODE	RW	0	VDDIO voltage set 0: 1.8V 1: 3.3V
	I2C Pass-Through	3	I2C PASS-THROUGH	RW	1	I2C Pass-Through Mode 0: Disabled 1: Enabled
	Auto ACK	2	AUTO ACK	RW	0	0: Disable 1: Enable
	RESERVED	1	RESERVED		0	Reserved
	RRFB	0	RRFB	RW	1	Pixel Clock Edge Select 0: Parallel Interface Data is strobed on the Falling Clock Edge 1: Parallel Interface Data is strobed on the Rising Clock Edge.
4	EQ Control	7:0	EQ	RW	0x00'h	EQ Gain 00'h = ~0.0 dB 01'h = ~4.5 dB 03'h = ~6.5 dB 07'h = ~7.5 dB 0F'h = ~8.0 dB 1F'h = ~11.0 dB 3F'h = ~12.5 dB FF'h = ~14.0 dB
5	RESERVED	7:0	RESERVED		0x00'h	Reserved
6	RESERVED	7	RESERVED		0	Reserved
	SCL Prescale	6:4	SCL_PRESCALE	RW	000'b	Prescales the SCL clock line when reading data byte from a slave device (MODE = 0) 000 : ~100 kHz SCL (default) 001 : ~125 kHz SCL 101 : ~11 kHz SCL 110 : ~33 kHz SCL 111 : ~50 kHz SCL Other values are NOT supported.
	Remote NACK	3	REM_NACK_TIMER	RW	1	Remote NACK Timer Enable In slave mode (MODE = 1) if bit is set the I2C core will automatically timeout when no acknowledge condition was detected. 1: Enable 0: Disable
	Remote NACK	2:0	NACK_TIMEOUT	RW	111'b	Remote NACK Timeout. 000: 2.0 ms 001: 5.2 ms 010: 8.6 ms 011: 11.8 ms 100: 14.4 ms 101: 18.4 ms 110: 21.6 ms 111: 25.0 ms

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
7	SER ID	7:1	SER DEV ID	RW	0xB0'h	Serializer Device ID = 0x58'h (1011_000X'b) default
		0	RESERVED			Reserved
8	ID[0] Index	7:1	ID[0] INDEX	RW	0x00'h	Target slave Device ID slv_id0 [7:1]
		0	RESERVED			Reserved
9	ID[1] Index	7:1	ID[1] INDEX	RW	0x00'h	Target slave Device ID slv_id1 [7:1]
		0	RESERVED			Reserved
A	ID[2] Index	7:1	ID[2] INDEX	RW	0x00'h	Target slave Device ID slv_id2 [7:1]
		0	RESERVED			Reserved
B	ID[3] Index	7:1	ID[3] INDEX	RW	0x00'h	Target slave Device ID slv_id3 [7:1]
		0	RESERVED			Reserved
C	ID[4] Index	7:1	ID[4] INDEX	RW	0x00'h	Target slave Device ID slv_id4 [7:1]
		0	RESERVED			Reserved
D	ID[5] Index	7:1	ID[5] INDEX	RW	0x00'h	Target slave Device ID slv_id5 [7:1]
		0	RESERVED			Reserved
E	ID[6] Index	7:1	ID[6] INDEX	RW	0x00'h	Target slave Device ID slv_id6 [7:1]
		0	RESERVED			Reserved
F	ID[7] Index	7:1	ID[7] INDEX	RW	0x00'h	Target slave Device ID slv_id7 [7:1]
		0	RESERVED			Reserved
10	ID[0] Match	7:1	ID[0] MATCH	RW	0x00'h	Alias to match Device ID slv_id0 [7:1]
		0	RESERVED			Reserved
11	ID[1] Match	7:1	ID[1] MATCH	RW	0x00'h	Alias to match Device ID slv_id1 [7:1]
		0	RESERVED			Reserved
12	ID[2] Match	7:1	ID[2] MATCH	RW	0x00'h	Alias to match Device ID slv_id2 [7:1]
		0	RESERVED			Reserved
13	ID[3] Match	7:1	ID[3] MATCH	RW	0x00'h	Alias to match Device ID slv_id3 [7:1]
		0	RESERVED			Reserved
14	ID[4] Match	7:1	ID[4] MATCH	RW	0x00'h	Alias to match Device ID slv_id4 [7:1]
		0	RESERVED			Reserved
15	ID[5] Match	7:1	ID[5] MATCH	RW	0x00'h	Alias to match Device ID slv_id5 [7:1]
		0	RESERVED			Reserved
16	ID[6] Match	7:1	ID[6] MATCH	RW	0x00'h	Alias to match Device ID slv_id6 [7:1]
		0	RESERVED			Reserved
17	ID[7] Match	7:1	ID[7] MATCH	RW	0x00'h	Alias to match Device ID slv_id [7:1]
		0	RESERVED			Reserved
18	RESERVED	7:0	RESERVED		0x00'h	Reserved
19	RESERVED	7:0	RESERVED		0x01'h	Reserved
1A	RESERVED	7:0	RESERVED		0x00'h	Reserved
1B	RESERVED	7:0	RESERVED		0x00'h	Reserved
1C	RESERVED	7:3	RESERVED		0x00'h	Reserved
	RESERVED	2	RESERVED		0	Reserved
	Signal Detect Status	1		R	0	0: Active signal not detected 1: Active signal detected
	LOCK Pin Status	0		R	0	0: CDR/PLL Unlocked 1: CDR/PLL Locked
1D	Reserved	7:0	RESERVED		0x17'h	Reserved
1E	Reserved	7:0	RESERVED		0x07'h	Reserved
1F	Reserved	7:0	RESERVED		0x01'h	Reserved
20	Reserved	7:0	RESERVED		0x01'h	Reserved

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
21	Reserved	7:0	RESERVED		0x01'h	Reserved
22	Reserved	7:0	RESERVED		0x01'h	Reserved
23	General Purpose Control Reg	7:0	GPCR[7] GPCR[6] GPCR[5] GPCR[4] GPCR[3] GPCR[2] GPCR[1] GPCR[0]	RW	0x00'h	0: LOW 1: HIGH
24	BIST	0	BIST_EN	RW	0	BIST Enable 0: Normal operation 1: Bist Enable
25	BIST_ERR	7:0	BIST_ERR	R	0x00'h	Bist Error Counter
26	Remote Wake Enable	7:6	REM_WAKEUP_EN	RW	00'b	11: Enable remote wake up mode 00: Normal operation mode Other values are NOT supported
		5:0	RESERVED	RW	0	Reserved

Functional Description

The DS90UB903Q/904Q FPD-Link III chipset is intended for video display applications. The Serializer/ Deserializer chipset operates from a 10 MHz to 43 MHz pixel clock frequency. The DS90UB903Q transforms a 21-bit wide parallel LVCMOS data bus along with a bidirectional control bus into a single high-speed differential pair. The high-speed serial bit stream contains an embedded clock and DC-balance information which enhances signal quality to support AC coupling. The DS90UB904Q receives the single serial data stream and converts it back into a 21-bit wide parallel data bus together with the bidirectional control channel data bus.

The control channel function of the DS90UB903Q/904Q provides bidirectional communication between the host processor and display. The integrated control channel transfers data simultaneously over the same differential pair used for video data interface. This interface offers advantages over other chipsets by eliminating the need for additional wires for programming and control. The control supports I²C port. The bidirectional control channel offers asymmetrical communication and is not dependent on video blanking intervals.

DISPLAY APPLICATION

The DS90UB903Q/904Q chipset is intended for interface between a host (graphics processor) and a Display. It supports a 21 bit parallel video bus for 18-bit color depth (RGB666) display format. In a RGB666 configuration, 18 color bits (R[5:0], G[5:0], B[5:0]), Pixel Clock (PCLK) and three control bits (VS, HS and DE) are supported across the serial link.

The DS90UB903Q Serializer accepts a 21-bit parallel data bus along with a bidirectional control bus. The parallel data and bidirectional control channel information is converted into a single differential link. The integrated bidirectional control channel bus supports I2C compatible operation for controlling auxiliary data transport to and from host processor and display module. The DS90UB904Q Deserializer extracts the clock/control information from the incoming data stream and reconstructs the 21-bit data with control channel data.

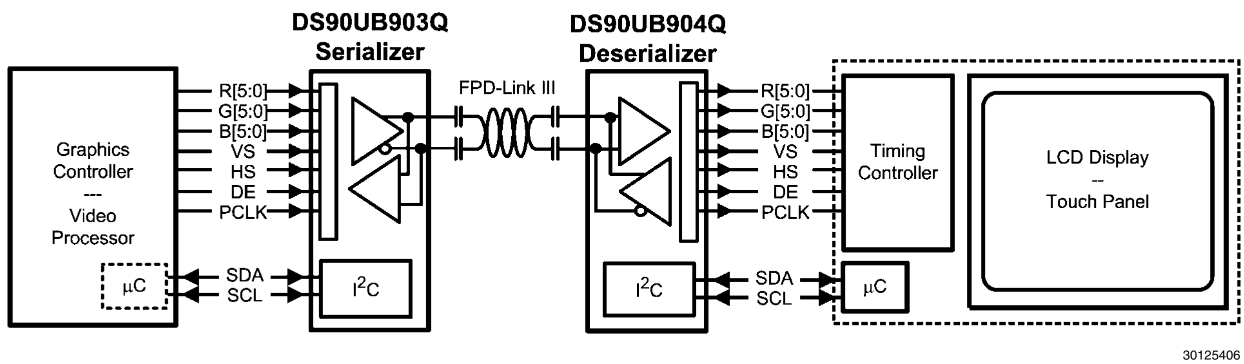

FIGURE 21. Typical Display System Diagram

SERIAL FRAME FORMAT

The DS90UB903Q/904Q chipset will transmit and receive a pixel of data in the following format:

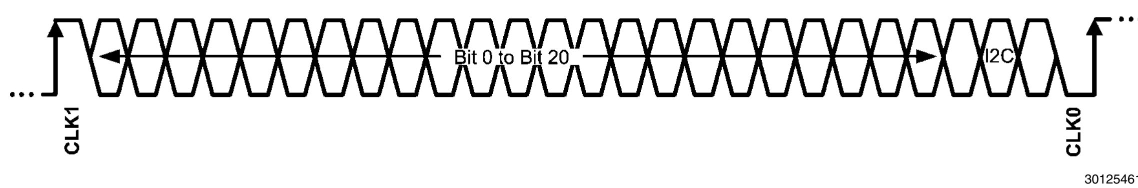

FIGURE 22. Serial Bitstream for 28-bit Symbol

The High Speed Forward Channel is a 28-bit symbol composed of 21 bits of data containing video data & control information transmitted from Serializer to Deserializer. CLK1 and CLK0 represent the embedded clock in the serial stream. CLK1 is always HIGH and CLK0 is always LOW. This data payload is optimized for signal transmission over an AC coupled link. Data is randomized, balanced and scrambled.

The bidirectional control channel data is transferred along with the high-speed forward data over the same serial link. This architecture provides a full duplex low speed forward channel across the serial link together with a high speed forward channel without the dependence of the video blanking phase.

DESCRIPTION OF BIDIRECTIONAL CONTROL BUS AND I2C MODES

The I²C compatible interface allows programming of the DS90UB903Q, DS90UB904Q, or an external remote device (such as a display) through the bidirectional control channel. Register programming transactions to/from the DS90UB903Q/904Q chipset are employed through the clock (SCL) and data (SDA) lines. These two signals have open-drain I/Os and both lines must be pulled-up to VDDIO by external resistor. *Figure 4* shows the timing relationships of the clock (SCL) and data (SDA) signals. Pull-up resistors or current sources are required on the SCL and SDA busses to pull them high when they are not being driven low. A logic zero is transmitted by driving the output low. A logic high is transmitted by releasing the output and allowing it to be pulled-up externally. The appropriate pull-up resistor values will depend upon the total bus capacitance and operating speed. The DS90UB903Q/904Q I2C bus data rate supports up to 100 kbps according to I2C specification.

To start any data transfer, the DS90UB903Q/904Q must be configured in the proper I2C mode. Each device can function as an I2C slave proxy or master proxy depending on the mode determined by MODE pin. The Ser/Des interface acts as a virtual bridge between Master Controller Unit (MCU) and the remote device. When the MODE pin is set to High, the device is treated as a slave proxy; acts as a slave on behalf of the remote slave. When addressing a remote peripheral or Serializer/Deserializer (not wired directly to the MCU), the slave proxy will forward any byte transactions sent by the Master controller to the target device. When MODE pin is set to Low, the device will function as a master proxy device; acts as a master on behalf of the I2C master controller. Note that the devices must have complementary settings for the MODE configuration. For example, if the Serializer MODE pin is set to High then the Deserializer MODE pin must be set to Low and vice-versa.

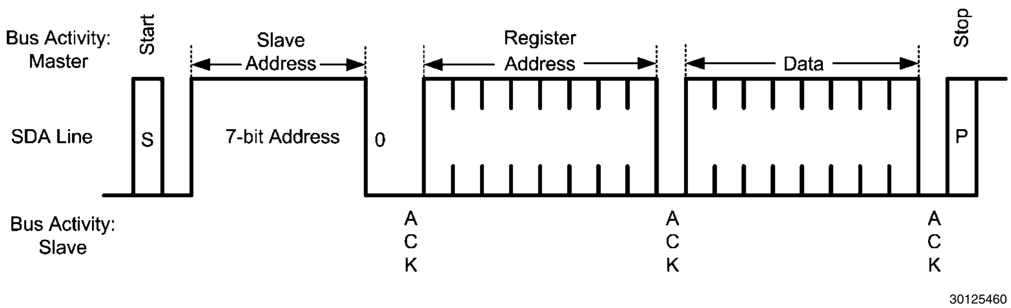

FIGURE 23. Write Byte

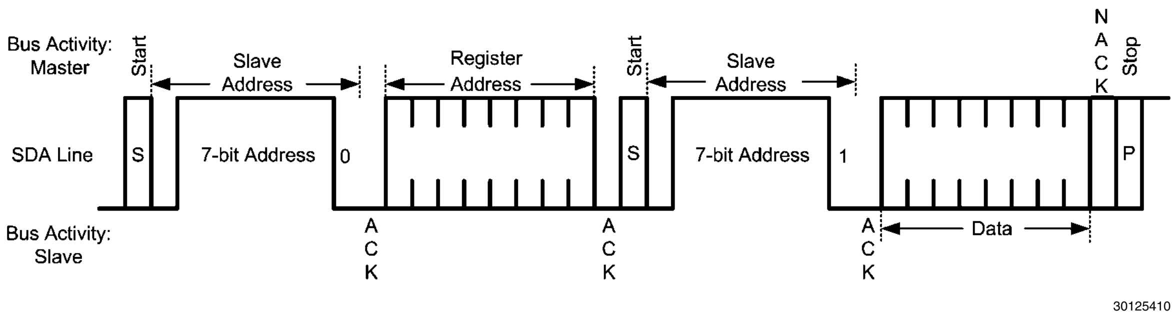

FIGURE 24. Read Byte

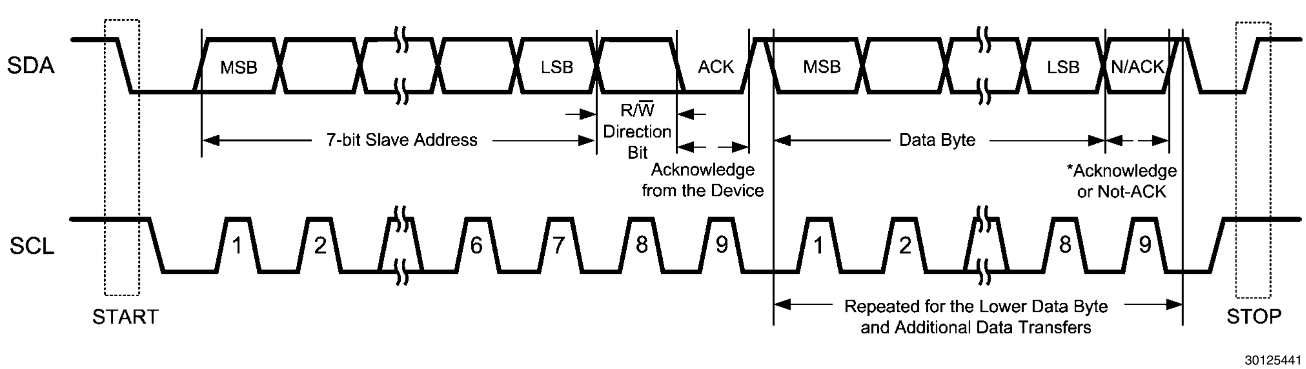

FIGURE 25. Basic Operation

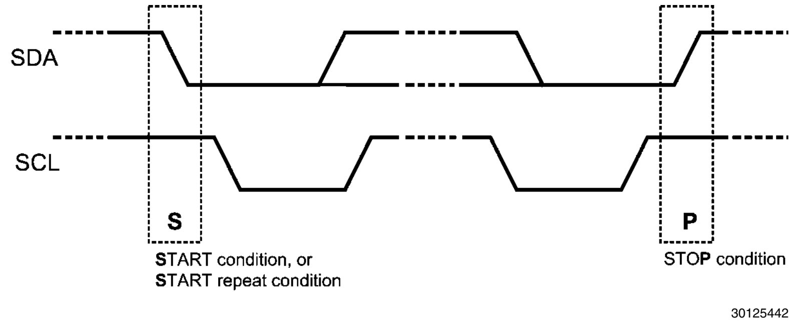

FIGURE 26. START and STOP Conditions

SLAVE CLOCK STRETCHING

In order to communicate and synchronize with remote devices on the I2C bus through the bidirectional control channel, slave clock stretching must be supported by the I2C master controller/MCU. The chipset utilizes bus clock stretching (holding the SCL line low) during data transmission; where the I2C slave pulls the SCL line low on the 9th clock of every I2C data transfer (before the ACK signal). The slave device will not control the clock and only stretches it until the remote peripheral has responded; which is typically in the order of 12 us (typical).

ID[X] ADDRESS DECODER

The ID[x] pin is used to decode and set the physical slave address of the Serializer/Deserializer (I2C only) to allow up to six devices on the bus using only a single pin. The pin sets one of six possible addresses for each Serializer/Deserializer device. The pin must be pulled to VDD (1.8V, NOT VDDIO)) with a 10 kΩ resistor and a pull down resistor (RID) of the recommended value to set the physical device address. The recommended maximum resistor tolerance is 0.1% worst case (0.2% total tolerance).

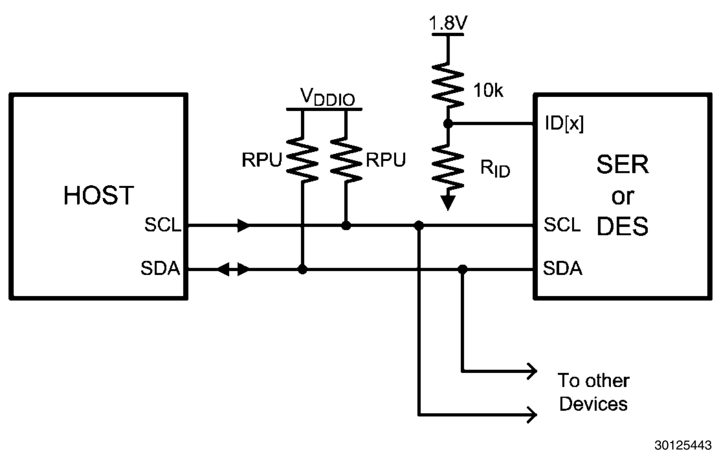

FIGURE 27. Bidirectional Control Bus Connection

TABLE 3. ID[x] Resistor Value – DS90UB903Q

ID[x] Resistor Value - DS90UB903Q Ser		
Resistor RID Ω (±0.1%)	Address 7'b (*Note 11*)	Address 8'b 0 appended (WRITE)
0 GND	7b' 101 1000 (h'58)	8b' 1011 0000 (h'B0)
2.0k	7b' 101 1001 (h'59)	8b' 1011 0010 (h'B2)
4.7k	7b' 101 1010 (h'5A)	8b' 1011 0100 (h'B4)
8.2k	7b' 101 1011 (h'5B)	8b' 1011 0110 (h'B6)
12.1k	7b' 101 1100 (h'5C)	8b' 1011 1000 (h'B8)
39.0k	7b' 101 1110 (h'5E)	8b' 1011 1100 (h'BC)

TABLE 4. ID[x] Resistor Value – DS90UB904Q

ID[x] Resistor Value - DS90UB904Q Des		
Resistor RID Ω (±0.1%)	Address 7'b (*Note 11*)	Address 8'b 0 appended (WRITE)
0 GND	7b' 110 0000 (h'60)	8b' 1100 0000 (h'C0)
2.0k	7b' 110 0001 (h'61)	8b' 1100 0010 (h'C2)
4.7k	7b' 110 0010 (h'62)	8b' 1100 0100 (h'C4)
8.2k	7b' 110 0011 (h'63)	8b' 1101 0110 (h'C6)
12.1k	7b' 110 0100 (h'64)	8b' 1101 1000 (h'C8)
39.0k	7b' 110 0110 (h'66)	8b' 1100 1100 (h'CC)

CAMERA MODE OPERATION

In Camera mode, I^{2}C transactions originate from the Deserializer from the Master controller (*Figure 28*). The I^{2}C slave core in the Deserializer will detect if a transaction is intended for the Serializer or a slave at the Serializer. Commands are sent over the bidirectional control channel to initiate the transactions. The Serializer will receive the command and generate an I^{2}C transaction on its local I^{2}C bus. At the same time, the Serializer will capture the response on the I^{2}C bus and return the response as a command on the forward channel link. The Deserializer parses the response and passes the appropriate response to the Deserializer I^{2}C bus.

To configure the devices for camera mode operation, set the Serializer MODE pin to Low and the Deserializer MODE pin to High. Before initiating any I^{2}C commands, the Deserializer needs to be programmed with the target slave device addresses and Serializer device address. SER_DEV_ID Register 0x07h sets the Serializer device address and SLAVE_x_MATCH/SLAVE_x_INDEX registers 0x08h~0x17h set the remote target slave addresses. The slave address match registers must also be set. In slave mode the address register is compared with the address byte sent by the I^{2}C master. If the addresses are equal to any of registers values, the I^{2}C slave will acknowledge the transaction to the I^{2}C master allowing reads or writes to target device.

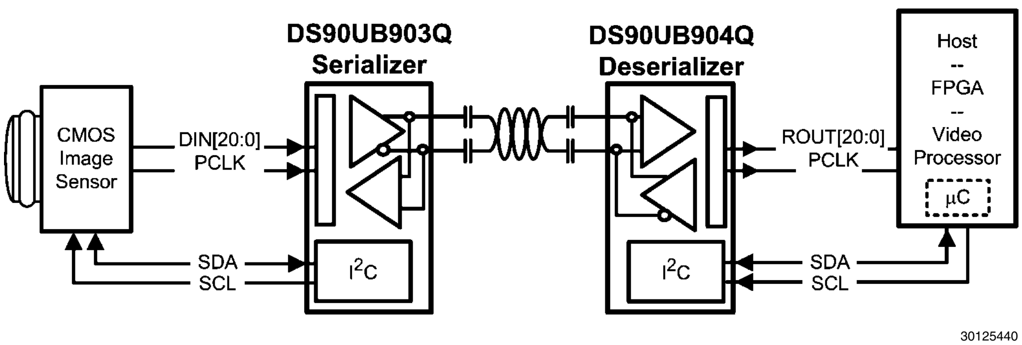

FIGURE 28. Typical Camera System Diagram

DISPLAY MODE OPERATION

In Display mode, I^{2}C transactions originate from the controller attached to the Serializer. The I^{2}C slave core in the Serializer will detect if a transaction targets (local) registers within the Serialier or the (remote) registers within the Deserializer or a remote slave connected to the I^{2}C master interface of the Deserializer. Commands are sent over the forward channel link to initiate the transactions. The Deserializer will receive the command and generate an I^{2}C transaction on its local I^{2}C bus. At the same time, the Deserializer will capture the response on the I^{2}C bus and return the response as a command on the bidirectional control channel. The Serializer parses the response and passes the appropriate response to the Serializer I^{2}C bus.

The physical device ID of the I^{2}C slave in the Serializer is determined by the analog voltage on the ID[x] input. It can be reprogrammed by using the SER_DEV_ID register and setting the bit . The device ID of the logical I^{2}C slave in the Deserializer is determined by programming the DES ID in the Serializer. The state of the ID[x] input on the Deserializer is used to set the device ID. The I^{2}C transactions between Ser/Des will be bridged between the host to the remote slave.

To configure the devices for display mode operation, set the Serializer MODE pin to High and the Deserializer MODE pin to Low. Before initiating any I^{2}C commands, the Serializer needs to be programmed with the target slave device address and Serializer device address. DES_DEV_ID Register 0x06h sets the Deserializer device address and SLAVE_DEV_ID register 0x7h sets the remote target slave address. If the I^{2}C slave address matches any of registers values, the I^{2}C slave will acknowledge the transaction allowing read or write to target device. Note: In Display mode operation, registers 0x08h~0x17h on Deserializer must be reset to 0x00.

PROGRAMMABLE CONTROLLER

An integrated I^{2}C slave controller is embedded in each of the DS90UB903Q Serializer and DS90UB904Q Deserializer. It must be used to access and program the extra features embedded within the configuration registers. Refer to *Table 1* and *Table 2* for details of control registers.

I^{2}C PASS THROUGH

I^{2}C pass-through provides an alternative means to independently address slave devices. The mode enables or disables I^{2}C bidirectional control channel communication to the remote I^{2}C bus. This option is used to determine whether or not an I^{2}C instruction is to be transferred over to the remote I^{2}C device. When enabled, the I^{2}C bus traffic will continue to pass through and will be received by I^{2}C devices downstream. If disabled, I^{2}C commands will be excluded to the remote I^{2}C device. The pass through function also provides access and communication to only specific devices on the remote bus. The feature is effective for both Camera mode and Display mode.

SYNCHRONIZING MULTIPLE LINKS

For applications requiring synchronization across multiple links, it is recommended to utilize the General Purpose Input/Output (GPI/GPO) pins to transmit control signals to synchronize slave peripherals together. To synchronize the peripherals properly, the system controller needs to provide a sync signal output. Note this form of synchronization timing relationship has a non-deterministic latency. After the control data is reconstructed from the birectional control channel, there will be a time variation of the GPI/GPO signals arriving at the different target devices (between the parallel links). The maximum latency delta (t1) of the GPI/GPO data transmitted across multiple links is 25 us.

Note: The user must verify that the timing variations between the different links are within their system and timing specifications.

The maximum time (t1) between the rising edge of GPI/GPO (i.e. sync signal) arriving at SER A and SER B is 25 us.

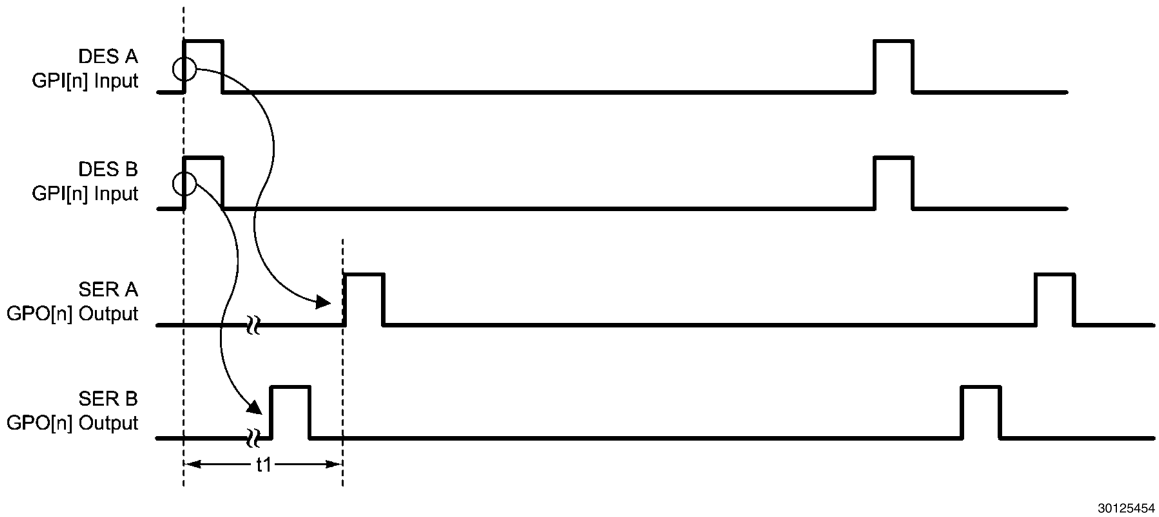

FIGURE 29. GPI/GPO Delta Latency

GENERAL PURPOSE I/O (GPI/GPO)

The DS90UB903Q/904Q has up to 4 GPO and 4 GPI on the Serializer and Deserializer respectively. The GPI/GPO maximum switching rate is up to 66 kHz for communication between Deserializer GPI to Serializer GPO.

AT-SPEED BIST (BISTEN, PASS)

An optional AT SPEED Built in Self Test (BIST) feature supports at speed testing of the high-speed serial and the bidirectional control channel link. Control pins at the Deserializer are used to enable the BIST test mode and allow the system to initiate the test and set the duration. A HIGH on PASS pin indicates that all payloads received during the test were error free during the BIST duration test. A LOW on this pin at the conclusion of the test indicates that one or more payloads were detected with errors.

The BIST duration is defined by the width of BISTEN. BIST starts when Deserializer LOCK goes HIGH and BISTEN is set HIGH. BIST ends when BISTEN goes LOW. Any errors detected after the BIST Duration are not included in PASS logic.

Note: AT-SPEED BIST is only available in the Camera mode and not the Display mode

The following diagram shows how to perform system AT SPEED BIST:

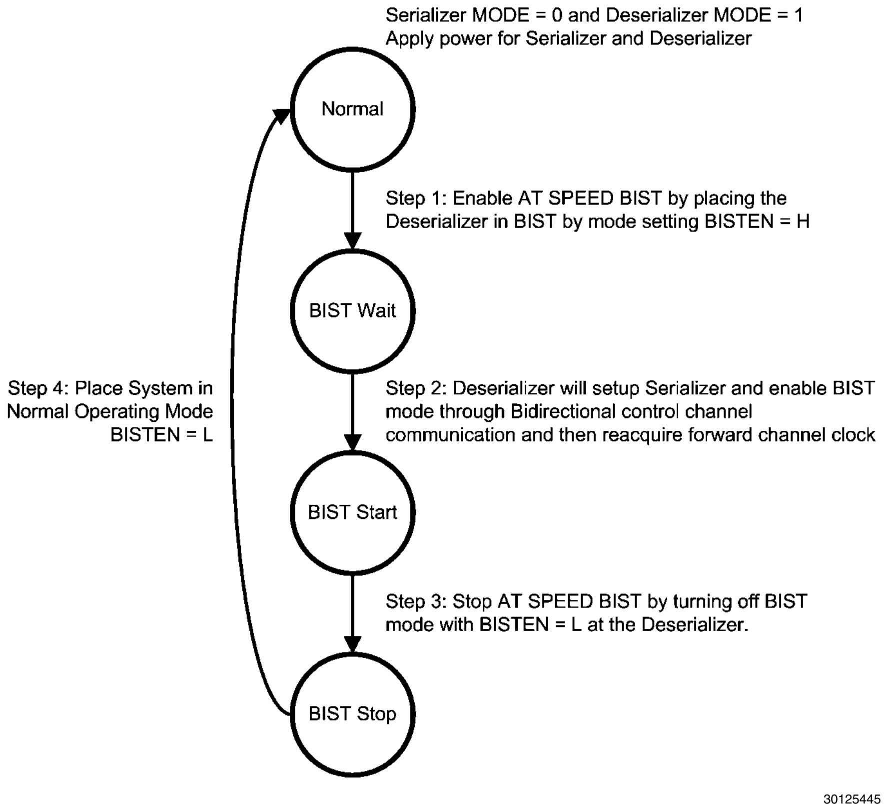

FIGURE 30. AT-SPEED BIST System Flow Diagram

Step 1: Place the Deserializer in BIST Mode.

Serializer and Deserializer power supply must be supplied. Enable the AT SPEED BIST mode on the Deserializer by setting the BISTEN pin High. The 904 GPI[1:0] pins are used to select the PCLK frequency of the on-chip oscillator for the BIST test on high speed data path.

TABLE 5. BIST Oscillator Frequency Select

Des GPI [1:0]	Oscillator Source	min (MHz)	typ (MHz)	max (MHz)
00	External PCLK	10		43
01	Internal		50	
10	Internal		25	
11	Internal		12.5	

The Deserializer GPI[1:0] set to 00 will bypass the on-chip oscillator and an external oscillator to Serializer PCLK input is required. This allows the user to operate BIST under different frequencies other than the predefined ranges.

Step 2: Enable AT SPEED BIST by placing the Serializer into BIST mode.

Deserializer will communicate through the bidirectional control channel to configure Serializer into BIST mode. Once the BIST mode is set, the Serializer will initiate BIST transmission to the Deserializer.

Wait 10 ms for Deserializer to acquire lock and then monitor the LOCK pin transition from LOW to HIGH. At this point, AT SPEED BIST is operational and the BIST process has begun. The Serializer will start transfer of an internally generated PRBS data pattern through the high speed serial link. This pattern traverses across the interconnecting link to the Deserializer. Check the status of the PASS pin; a HIGH indicates a pass, a LOW indicates a fail. A fail will stay LOW for ½ a clock cycle. If two or more bits in the serial frame fail, the PASS pin will toggle ½ clock cycle HIGH and ½ clock cycle low. The user can use the PASS pin to count the number of fails on the high speed link. In addition, there is a defined SER and DES register that will keep track of the accumulated error count. The Serializer 903 GPO[0] pin will be assigned as a PASS flag error indicator for the bidirectional control channel link.

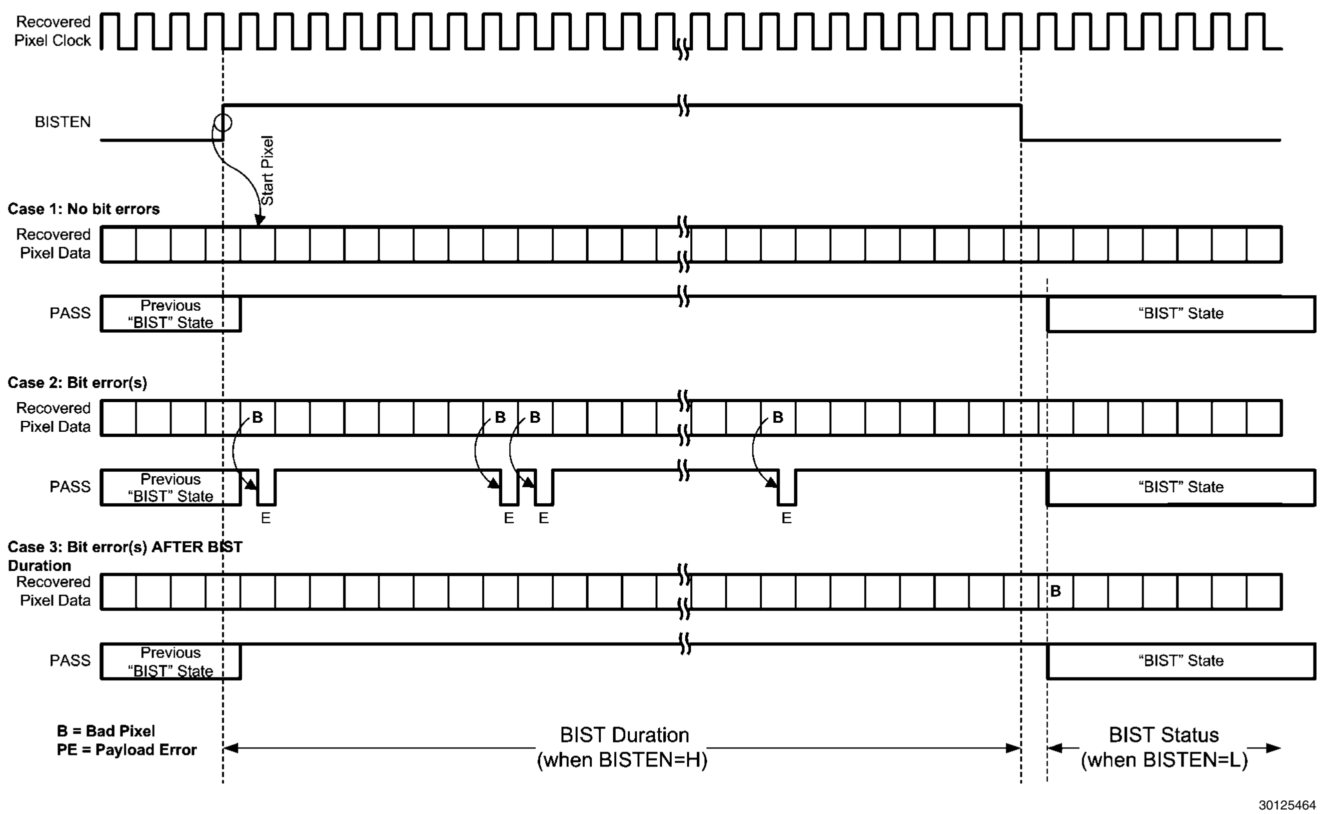

FIGURE 31. BIST Timing Diagram

Step 3: Stop at SPEED BIST by turning off BIST mode in the Deserializer to determine Pass/Fail.

To end BIST, the system must pull BISTEN pin of the Deserializer LOW. The BIST duration is fully defined by the BISTEN width and Deserializer LOCK is HIGH; thus the Bit Error Rate is determined by how long the system holds BISTEN HIGH.

$$\frac{\text{BIST Duration (s)}}{\text{1 Pixel period (ns) x Total Bits}} = \text{BIST Duration (s)} \times \frac{f_{pixel}\text{ (MHz)}}{\text{Pixel}} \times \text{Total Pixels Transmitted} = \text{Total Bits Transmitted}$$

$$\therefore \begin{array}{c}\text{Bit (Pixel) Error Rate}\\ \text{(for passing BIST)}\end{array} = [\text{Total Bits Transmitted}]^{-1}$$

$$= [\text{Total Bits Transmitted x Bits/Pixel}]^{-1}$$

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FIGURE 32. BIST BER Calculation

Step 4: Place system in Normal Operating Mode by disabling BIST at the Serializer.

Once Step 3 is complete, AT SPEED BIST is over and the Deserializer is out of BIST mode. To fully return to Normal mode, apply Normal input data into the Serializer.

Any PASS result will remain unless it is changed by a new BIST session or cleared by asserting and releasing PDB. The default state of PASS after a PDB toggle is HIGH.

It is important to note that AT SPEED BIST will only determine if there is an issue on the link that is not related to the clock and data recovery of the link (whose status is flagged with LOCK pin).

LVCMOS VDDIO OPTION

1.8V or 3.3V SER Inputs and DES Outputs are user seletable to provide compatibility with 1.8V and 3.3V system interfaces.

REMOTE WAKE UP (Camera Mode)

After initial power up, the Serializer is in a low-power Standby mode. The Deserializer (controlled by ECU/MCU) 'Remote Wake-up' register allows the Deserializer side to generate a signal across the link to remotely wake-up the Serializer. Once the Serializer detects the wake-up signal Serializer switches from Standby mode to active mode. In active mode, the Serializer locks onto PCLK input (if present), otherwise the on-chip oscillator is used as the input clock source. Note the MCU controller should monitor the Deserializer LOCK pin and confirm LOCK = H before performing any I²C communication across the link.

For Remote Wake-up to function properly:

- The chipset needs to be configured in Camera mode: Serializer MODE = 0 and Deserializer MODE = 1
- Serializer expects remote wake-up by default at power on.
- Configure the control channel driver of the Deserializer to be in remote wake-up mode by setting Deserializer Register 0x26h = 0xC0h.
- Perform remote wake-up on Serializer by setting Deserializer Register 0x01 b[2] = 1
- Return the control channel driver of the Deserializer to the normal operation mode by setting Deserializer Register 0x26h = 0x00h

Serializer can also be put into standby mode by programming the Deserializer remote wake-up control register 0x01 b[2] REM_WAKEUP to 0.

POWERDOWN

The SER has a PDB input pin to ENABLE or Powerdown the device. The modes can be controlled by the host and is used to disable the Link to save power when the remote device is not operational. An auto mode is also available. In this mode, the PDB pin is tied High and the SER switches over to an internal oscillator when the PCLK stops or not present. When a PCLK starts again, the SER will then lock to the valid input PCLK and transmits the data to the DES. In powerdown mode, the high-speed driver outputs are static (High).

The DES has a PDB input pin to ENABLE or Powerdown the device. This pin can be controlled by the system and is used to disable the DES to save power. An auto mode is also available. In this mode, the PDB pin is tied High and the DES will enter powerdown when the serial stream stops. When the serial stream starts up again, the DES will lock to the input stream and assert the LOCK pin and output valid data. In powerdown mode, the Data and PCLK outputs are set by the OSS_SEL control register.

POWER UP REQUIREMENTS AND PDB PIN

It is required to delay and release the PDB input signal after VDD (VDDn and VDDIO) power supplies have settled to the recommended operating voltages. A external RC network can be connected to the PDB pin to ensure PDB arrives after all the VDD have stabilized.

SIGNAL QUALITY ENHANCERS

Des - Receiver Input Equalization (EQ)

The receiver inputs provided input equalization filter in order to compensate for loss from the media. The level of equalization is controlled via register setting.

EMI REDUCTION

Des - Receiver Staggered Output

The Receiver staggered outputs allows for outputs to switch in a random distribution of transitions within a defined window. Outputs transitions are distributed randomly. This minimizes the number of outputs switching simultaneously and helps to reduce supply noise. In addition it spreads the noise spectrum out reducing overall EMI.

Des Spread Spectrum Clocking

The DS90UB904Q parallel data and clock outputs have programmable SSCG ranges from 9 kHz–66 kHz and ±0.5%–±2% from 20 MHz to 43 MHz. The modulation rate and modulation frequency variation of output spread is controlled through the SSC control registers.

PIXEL CLOCK EDGE SELECT (TRFB/RRFB)

The TRFB/RRFB selects which edge of the Pixel Clock is used. For the SER, this register determines the edge that the data is latched on. If TRFB register is 1, data is latched on the Rising edge of the PCLK. If TRFB register is 0, data is latched on the Falling edge of the PCLK. For the DES, this register determines the edge that the data is strobed on. If RRFB register is 1, data is strobed on the Rising edge of the PCLK. If RRFB register is 0, data is strobed on the Falling edge of the PCLK.

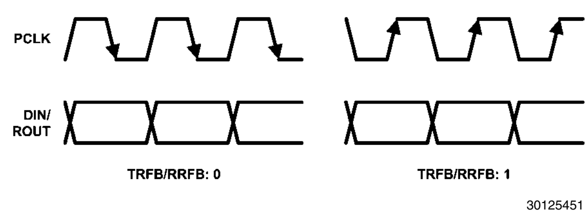


FIGURE 33. Programmable PCLK Strobe Select

Applications Information

AC COUPLING

The SER/DES supports only AC-coupled interconnects through an integrated DC balanced decoding scheme. External AC coupling capacitors must be placed in series in the FPD-Link III signal path as illustrated in *Figure 34*.

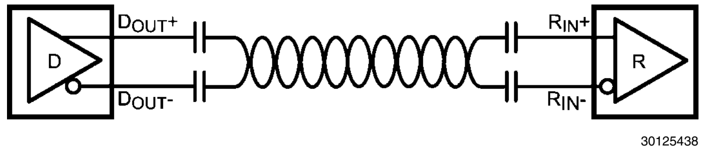


FIGURE 34. AC-Coupled Connection

For high-speed FPD-Link III transmissions, the smallest available package should be used for the AC coupling capacitor. This will help minimize degradation of signal quality due to package parasitics. The I/O's require a 100 nF AC coupling capacitors to the line.

TYPICAL APPLICATION CONNECTION

Figure 35 shows a typical connection of the DS90UB903Q Serializer.

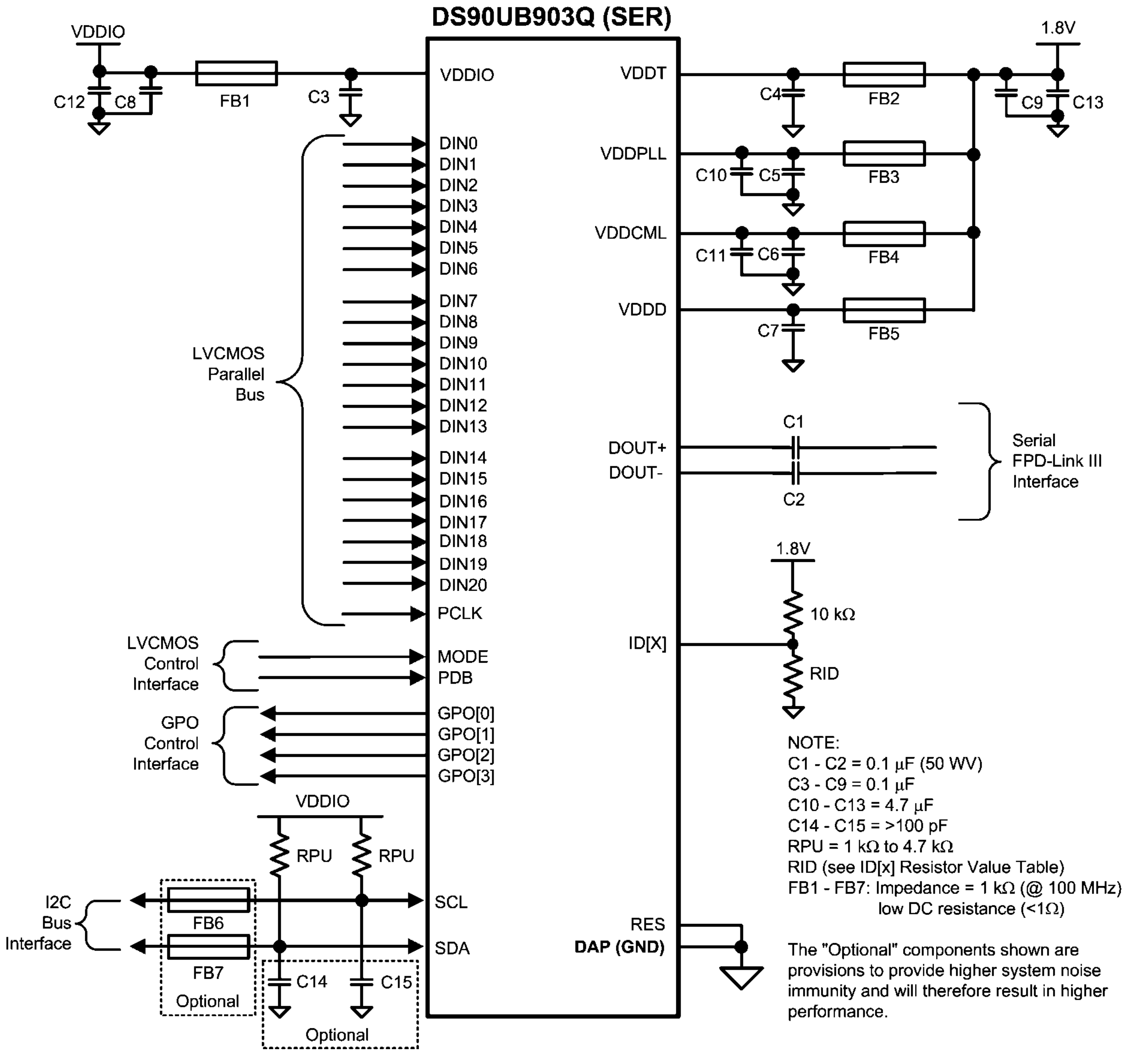


FIGURE 35. DS90UB903Q Typical Connection Diagram — Pin Control

Figure 36 shows a typical connection of the DS90UB904Q Deserializer.

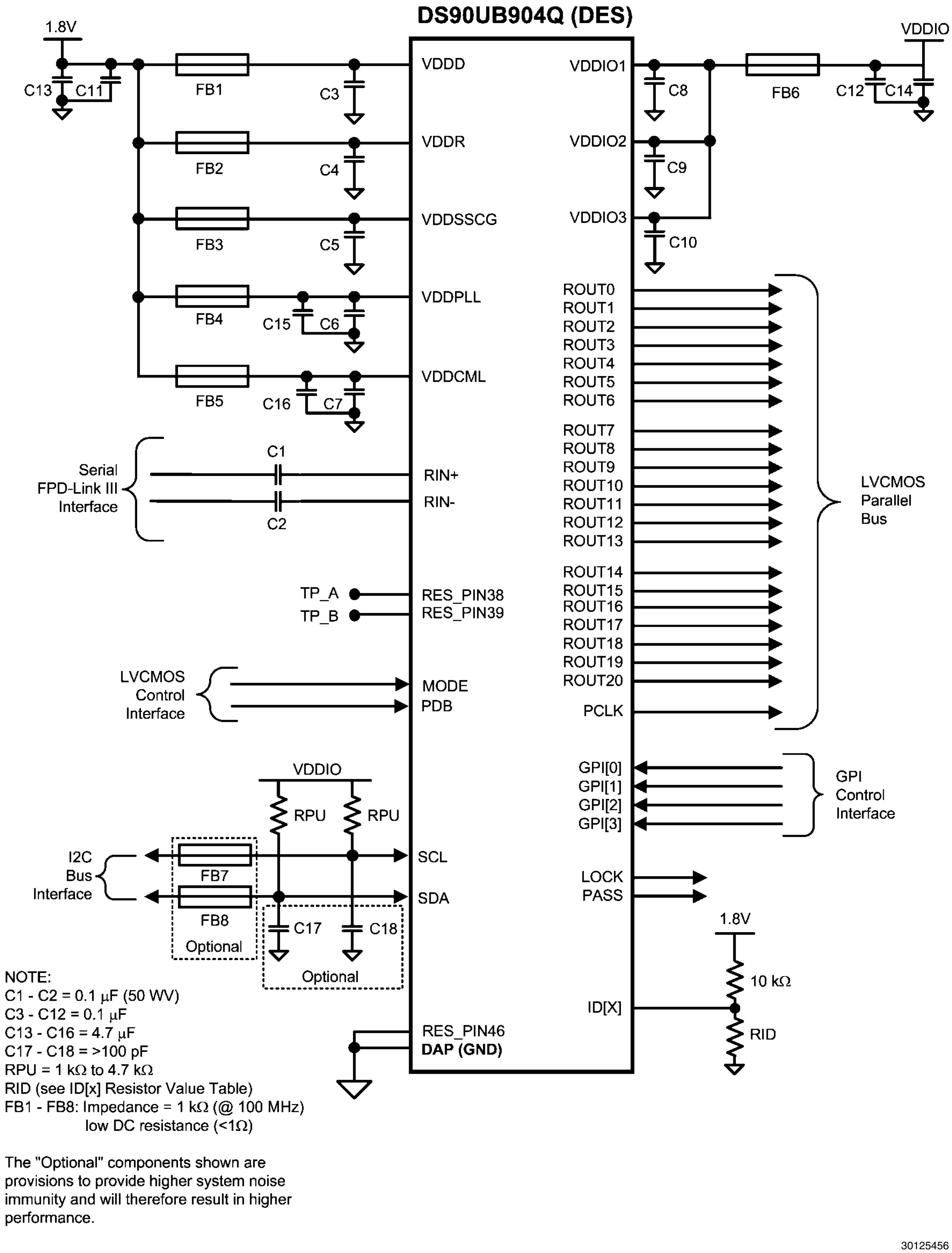


FIGURE 36. DS90UB904Q Typical Connection Diagram — Pin Control

TRANSMISSION MEDIA

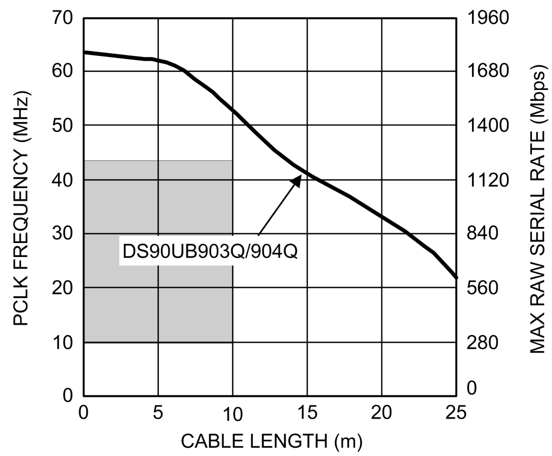
The Ser/Des chipset is intended to be used over a wide variety of balanced cables depending on distance and signal quality requirements. The Ser/Des employ internal termination providing a clean signaling environment. The interconnect for FPD-Link III interface should present a differential impedance of 100 Ohms. Use of cables and connectors that have matched differential impedance will minimize impedance discontinuities. Shielded or un-shielded cables may be used depending upon the noise environment and application requirements. The chipset's optimum cable drive performance is achieved at 43 MHz at 10 meters length. The maximum signaling rate increases as the cable length decreases. Therefore, the chipset supports 50 MHz at shorter distances.

Other cable parameters that may limit the cable's performance boundaries are: cable attenuation, near-end crosstalk and pair-to-pair skew.

For obtaining optimal performance, we recommend:

- Use Shielded Twisted Pair (STP) cable
- 100Ω differential impedance and 24 AWG (or lower AWG) cable
- Low skew, impedance matched
- Ground and/or terminate unused conductors

Figure 37 shows the Typical Performance Characteristics demonstrating various lengths and data rates using Rosenberger HSD and Leoni DACAR 538 Cable.



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*Note: Equalization is enabled for cable lengths greater than 7 meters

FIGURE 37. Rosenberger HSD & Leoni DACAR 538 Cable Performance

PCB LAYOUT AND POWER SYSTEM CONSIDERATIONS

Circuit board layout and stack-up for the Ser/Des devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50uF to 100uF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines. Closely-coupled differential lines of 100 Ohms are typically recommended for differential interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Information on the LLP style package is provided in National Application Note: AN-1187.

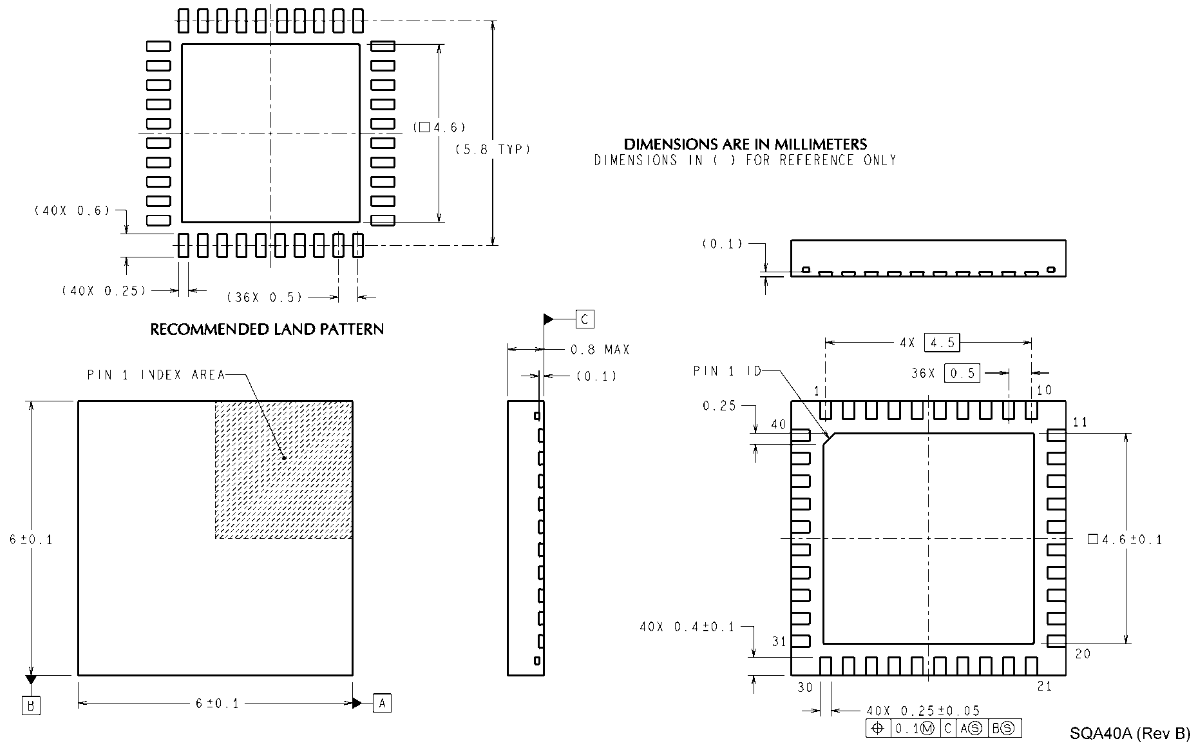
INTERCONNECT GUIDELINES

See AN-1108 and AN-905 for full details.

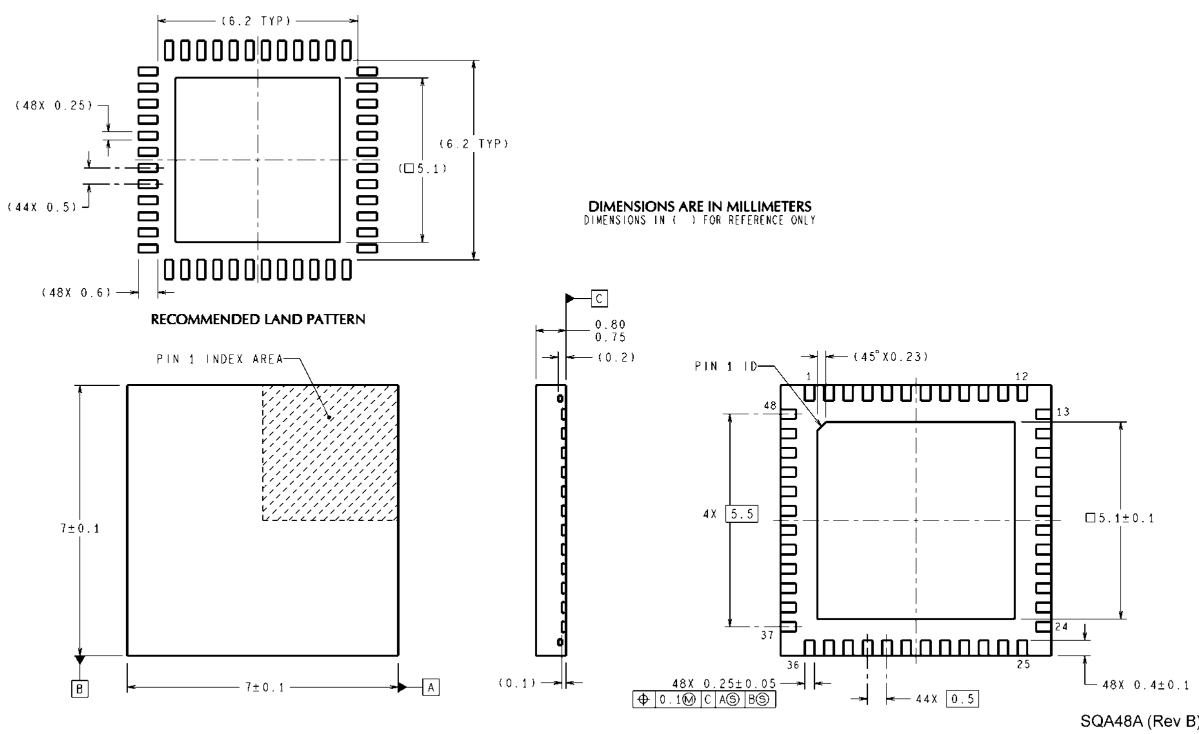
- Use 100Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  – S = space between the pair
  – 2S = space between pairs
  – 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the National web site at: **www.national.com/lvds**

Physical Dimensions inches (millimeters) unless otherwise noted



DS90UB903Q Serializer
NS Package Number SQA40A



DS90UB904Q Deserializer
NS Package Number SQA48A

Notes

Notes

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