National Semiconductor

October 20, 2010

DS90UR908Q

5 - 65 MHz 24-bit Color FPD-Link II to FPD-Link Converter

General Description

The DS90UR908Q converts FPD-Link II to FPD Link. It translates a high-speed serialized interface with an embedded clock over a single pair (FPD-Link II) to four LVDS data/control streams and one LVDS clock pair (FPD-Link). This serial bus scheme greatly eases system design by eliminating skew problems between clock and data, reduces the number of connector pins, reduces the interconnect size, weight, and cost, and overall eases PCB layout. In addition, internal DC balanced decoding is used to support AC-coupled interconnects.

The DS90UR908Q converter recovers the data (RGB) and control signals and extracts the clock from a serial stream (FPD-Link II). It is able to lock to the incoming data stream without the use of a training sequence or special SYNC patterns and does not require a reference clock. A link status (LOCK) output signal is provided.

Adjustable input equalization of the serial input stream provides compensation for transmission medium losses of the cable and reduces the medium-induced deterministic jitter. EMI is minimized by the use of low voltage differential signaling, output voltage level select feature, and additional output spread spectrum generation.

With fewer wires to the physical interface of the display, FPD-Link output with LVDS technology is ideal for high speed, low power and low EMI data transfer.

The DS90UR908Q is offered in a 48-pin LLP package and is specified over the automotive AEC-Q100 grade 2 temperature range of -40˚C to +105˚C.

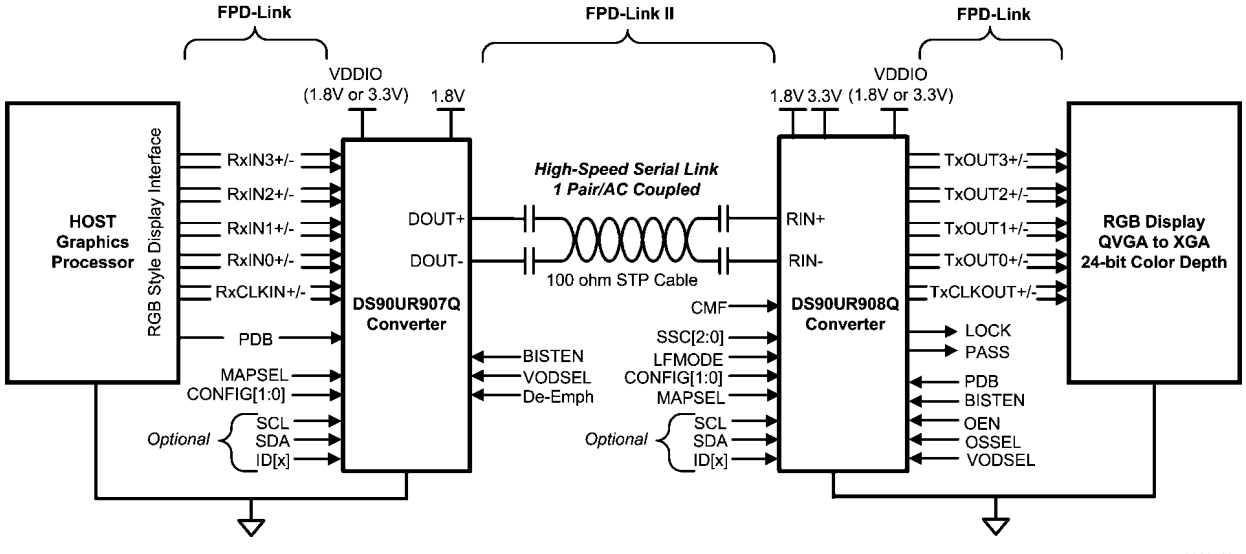
Features

- 5 – 65 MHz support (140 Mbps to 1.82 Gbps Serial Link)
- 5-channel (4 data + 1 clock) FPD-Link driver outputs
- AC Coupled STP Interconnect up to 10 meters in length
- Integrated input termination
- @ Speed link BIST Mode and reporting pin
- Optional I2C compatible Serial Control Bus
- RGB888 + VS, HS, DE support
- Power down mode minimizes power dissipation
- FAST random data lock; no reference clock required
- Adjustable input receive equalization
- LOCK (real time link status) reporting pin
- Low EMI FPD-Link output
- SSCG option for lower EMI
- 1.8V or 3.3V compatible I/O interface
- Automotive grade product: AEC-Q100 Grade 2 qualified
- >8kV HBM ESD tolerance
- Backward compatible mode for operation with older generation devices

Applications

- Automotive Display for Navigation
- Automotive Display for Entertainment

Applications Diagram



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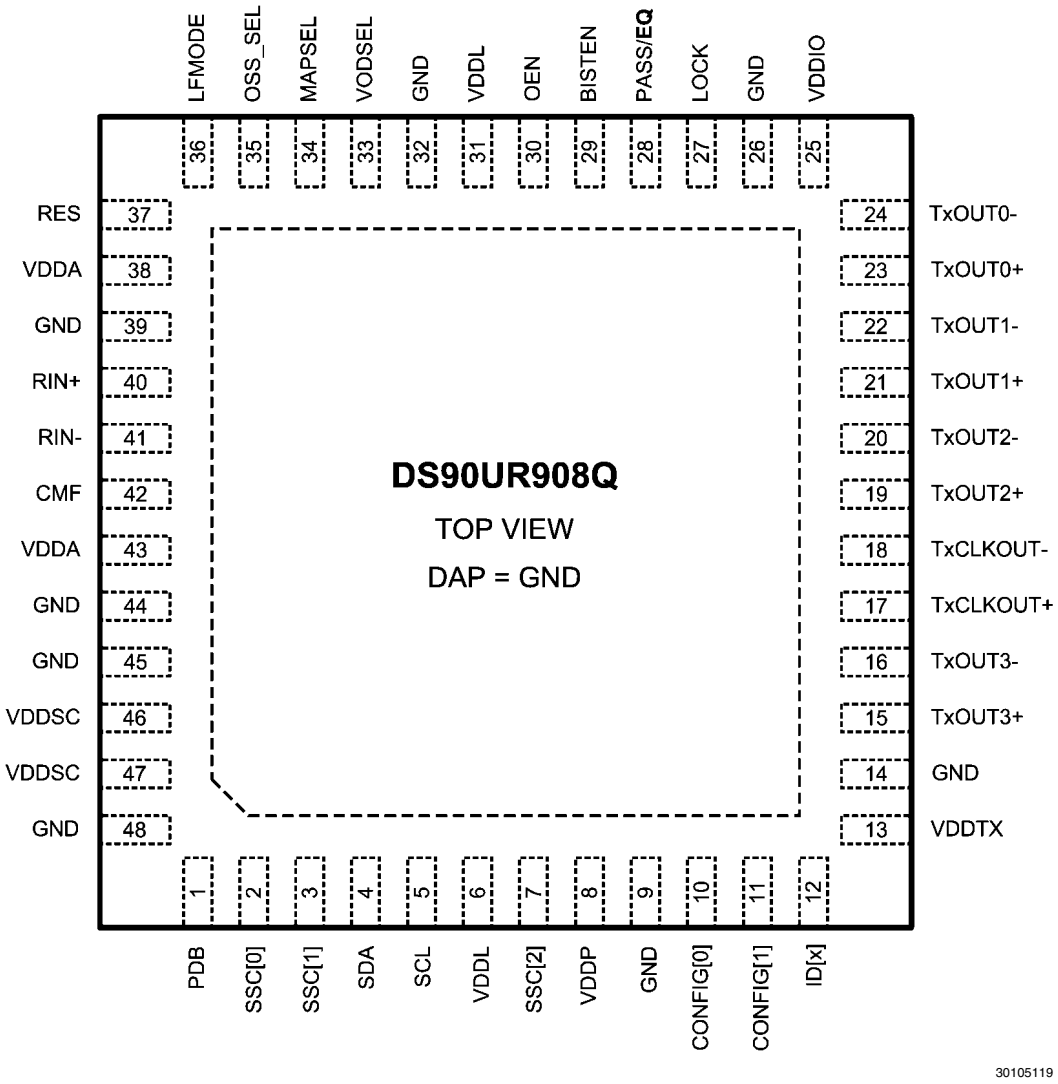
DS90UR908Q Pin Diagram



Pin Descriptions

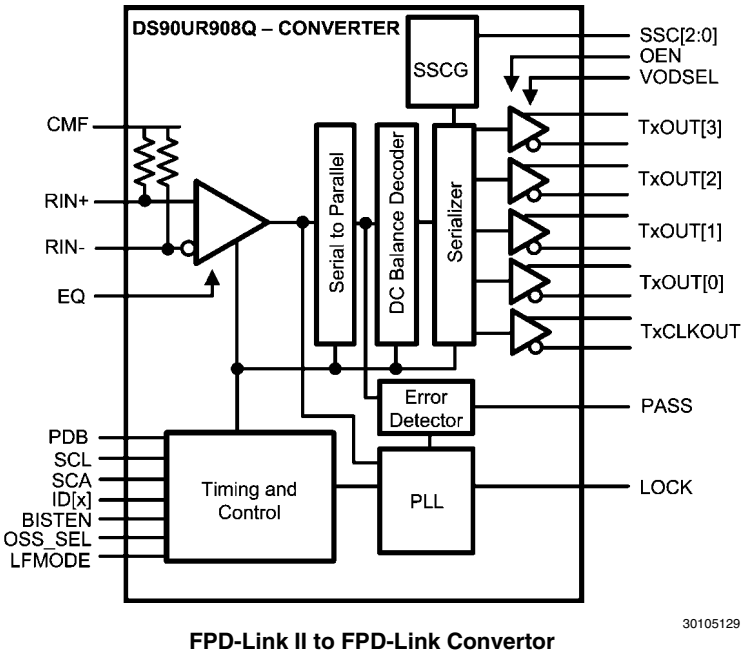
Pin Name	Pin #	I/O, Type	Description
FPD-Link II Input Interface			
RIN+	40	I, LVDS	True input The input must be AC coupled with a 100 nF capacitor. Internal termination.
RIN-	41	I, LVDS	Inverting input The input must be AC coupled with a 100 nF capacitor. Internal termination.
CMF	42	I, Analog	Common-Mode Filter VCM center-tap is a virtual ground which maybe ac-coupled to ground to increase receiver common mode noise immunity. Recommended value is 4.7 µF or higher.
FPD-Link Output Interface			
TxOUT[3:0]+	15,19, 21, 23	O, LVDS	True LVDS Data Output
TxOUT[3:0]-	16,20, 22, 24	O, LVDS	Inverting LVDS Data Output
TxCLKOUT+	17	O, LVDS	True LVDS Clock Output
TxCLKOUT-	18	O, LVDS	Inverting LVDS Clock Output

Pin Name	Pin #	I/O, Type	Description
LVCMOS Outputs			
LOCK	27	O, LVMOS	LOCK Status Output LOCK = 1, PLL is locked, output states determined by OEN. LOCK = 0, PLL is unlocked, output states determined by OSS_SEL and OEN. *Table 3* May be used as a Link Status or to flag when the Video Data is active (ON/OFF).
Control and Configuration			
PDB	1	I, LVCMOS w/ pull-down	Power Down Mode Input PDB = 1, Device is enabled (normal operation) PDB = 0, Device is in power-down, the outputs are TRI-STATE. Control registers are **RESET**.
VODSEL	33	I, LVCMOS w/ pull-down	FPD-Link Output Voltage Select. *Table 4* VODSEL = 1, LVDS VOD is ±400 mV, 800 mVp-p (typ) VODSEL = 0, LVDS VOD is ±250 mV, 500 mVp-p (typ)
OEN	30	I, LVCMOS w/ pull-down	Output Enable Input *Table 3*
OSS_SEL	35	I, LVCMOS w/ pull-down	Output Sleep State Select Input See *Table 3*.
LFMODE	36	I, LVCMOS w/ pull-down	Low Frequency Mode — Pin or Register Control LF_MODE = 1, low frequency mode (TxCLKOUT = 5-20 MHz) LF_MODE = 0, high frequency mode (TxCLKOUT = 20-65 MHz)
MAPSEL	34	I, LVCMOS w/ pull-down	FPD-Link Map Select — Pin or Register Control MAPSEL = 1, MSB on TxOUT3+/-, *Figure 15* MAPSEL = 0, LSB on TxOUT3+/-, *Figure 14*
CONFIG[1:0]	11,10	I, LVCMOS w/ pull-down	Operating Modes — Pin or Register Control Determine the device operating mode and interfacing device. *Table 1* CONFIG[1:0] = 00: Interfacing to DS90UR905Q or DS90UR907Q, Control Signal Filter DISABLED CONFIG[1:0] = 01: Interfacing to DS90UR905Q or DS90UR907Q, Control Signal Filter ENABLED CONFIG[1:0] = 01: Interfacing to DS90UR241 or DS99R421 CONFIG[1:0] = 11: Interfacing to DS90C241
SSC[2:0]	7, 2, 3	I, LVCMOS w/ pull-down	Spread Spectrum Clock Generation (SSCG) Range Select See Tables 5, 6
RES	37	I, LVCMOS w/ pull-down	***Reserved*** Tie Low
Control and Configuration — STRAP PIN For a High State, use a 10 kΩ pull up to VDDIO; for a Low State, the IO includes an internal pull down. The STRAP pin is read upon power-up and set device configuration. Pin number listed along with shared LVCMOS Output name in square bracket.			
EQ	28 [PASS]	STRAP I, LVCMOS w/ pull-down	EQ Gain Control of FPD-Link II Input EQ = 1, EQ gain is enabled (~13 dB) EQ = 0, EQ gain is disabled (~1.625 dB)
Optional BIST Mode			
BISTEN	29	I, LVCMOS w/ pull-down	BIST Enable Input – Optional BISTEN = 1, BIST Mode is enabled. BISTEN = 0, normal mode.
PASS	28	O, LVCMOS	PASS Output (BIST Mode) – Optional PASS = 1, no errors detected PASS = 0, errors detected Leave open if unused. Route to a test point (pad) recommended.

Pin Name	Pin #	I/O, Type	Description
Optional Serial Bus Control Interface			
SCL	5	I, LVCMOS	Serial Control Bus Clock Input - Optional SCL requires an external pull-up resistor to V_{DDIO}.
SDA	4	I/O, LVCMOS Open Drain	Serial Control Bus Data Input / Output - Optional SDA requires an external pull-up resistor to V_{DDIO}.
ID[x]	12	I, Analog	Serial Control Bus Device ID Address Select — Optional Resistor to Ground and 10 kΩ pull-up to 1.8V rail. See *Table 7*.
Power and Ground			
VDDL	6, 31	Power	Logic Power, 1.8 V ±5%
VDDA	38, 43	Power	Analog Power, 1.8 V ±5%
VDDP	8	Power	PLL Power, 1.8 V ±5%
VDDSC	46, 47	Power	SSC Generator Power, 1.8 V ±5%
VDDTX	13	Power	FPD-Link Power, 3.3 V ±10%
V_{DDIO}	25	Power	LVCMOS I/O Power, 1.8 V ±5% OR 3.3 V ±10%
GND	9, 14, 26, 32, 39, 44, 45, 48	Ground	Ground
DAP	DAP	Ground	DAP is the large metal contact at the bottom side, located at the center of the LLP package. **Connect to the ground plane** (GND) with at least 9 vias.

NOTE: 1 = HIGH, 0 = LOW

Block Diagram



FPD-Link II to FPD-Link Convertor

Ordering Information

NSID	Package Description	Quantity	SPEC	Package ID
DS90UR908QSQE	48–pin LLP, 7.0 X 7.0 X 0.8 mm, 0.5 mm pitch	250	NOPB	SQA48A
DS90UR908QSQ	48–pin LLP, 7.0 X 7.0 X 0.8 mm, 0.5 mm pitch	1000	NOPB	SQA48A
DS90UR908QSQX	48–pin LLP, 7.0 X 7.0 X 0.8 mm, 0.5 mm pitch	2500	NOPB	SQA48A

Note: Automotive Grade (Q) product incorporates enhanced manufacturing and support processes for the automotive market, including defect detection methodologies. Reliability qualification is compliant with the requirements and temperature grades defined in the AEC Q100 standard. Automotive Grade products are identified with the letter Q. For more information go to http://www.national.com/automotive.

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage – V_{DDn} (1.8V)	−0.3V to +2.5V
Supply Voltage – V_{DDTX} (3.3V)	−0.3V to +4.0V
Supply Voltage – V_{DDIO}	−0.3V to +4.0V
LVCMOS I/O Voltage	−0.3V to +(VDDIO + 0.3V)
Receiver Input Voltage	−0.3V to (VDD + 0.3V)
LVDS Output Voltage	−0.3V to (VDDTX + 0.3V)
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
48L LLP Package	
Maximum Power Dissipation Capacity at 25°C	
Derate above 25°C	1/ θ_{JA}°C/W
θ_{JA}	27.7 °C/W
θ_{JC}	3.0 °C/W
ESD Rating (IEC, powered-up only), R_D = 330Ω, C_S = 150pF	
Air Discharge (R_{IN+}, R_{IN-})	≥±15 kV
Contact Discharge (R_{IN+}, R_{IN-})	≥±8 kV
ESD Rating (ISO10605), R_D = 330Ω, C_S = 150/330pF	
ESD Rating (ISO10605), R_D = 2kΩ, C_S = 150/330pF	
Air Discharge (R_{IN+}, R_{IN-})	≥±15 kV
Contact Discharge (R_{IN+}, R_{IN-})	≥±8 kV
ESD Rating (HBM)	≥±8 kV
ESD Rating (HBM)	≥±8 kV
ESD Rating (CDM)	≥±1.25 kV

For soldering specifications:
see product folder at www.national.com and www.national.com/ms/MS/MS-SOLDERING.pdf

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{DDn})	1.71	1.8	1.89	V
LVCMOS Supply Voltage (V_{DDIO})	1.71	1.8	1.89	V
OR				
LVCMOS Supply Voltage (V_{DDIO})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−40	+25	+105	°C
TxCLKOUT Frequency	5		65	MHz
Supply Noise (*Note 8*)			100	mV_{P-P}

DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Pin/Freq.	Min	Typ	Max	Units
FPD-Link LVDS Output								
$\|V_{OD}\|$	Differential Output Voltage	R_L = 100Ω *Figure 7*	VODSEL = L	TxCLKOUT+, TxCLKOUT-, TxOUT[3:0]+, TxOUT[3:0]-	100	250	400	mV
			VODSEL = H		200	400	600	mV
V_{ODp-p}	Differential Output Voltage A-B		VODSEL = L			500		mVp-p
			VODSEL = H			800		mVp-p
ΔV_{OD}	Output Voltage Unbalance		VODSEL = H			4	50	mV
V_{OS}	Offset Voltage		VODSEL = L		1.0	1.2	1.5	V
			VODSEL = H			1.2		V
ΔV_{OS}	Offset Voltage Unbalance					1	50	mV
I_{OS}	Output Short Circuit Current	Vout = GND				-5		mA
I_{OZ}	Output TRI-STATE® Current	OEN = GND, Vout = V_{DDTX}, or GND			-10		+10	µA
3.3 V I/O LVCMOS DC SPECIFICATIONS – V_{DDIO} = 3.0 to 3.6V								
V_{IH}	High Level Input Voltage			PDB, VODSEL, OEN, OSS_SEL, MAPSEL, LFMODE, SSC[2:0], BISTEN	2.2		V_{DDIO}	V
V_{IL}	Low Level Input Voltage				GND		0.8	V
I_{IN}	Input Current	V_{IN} = 0V or V_{DDIO}			-15	±1	+15	µA

Symbol	Parameter	Conditions		Pin/Freq.	Min	Typ	Max	Units
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA		LOCK, PASS	V_{DDIO}- 0.25	V_{DDIO}		V
V_{OL}	Low Level Output Voltage	I_{OL} = +2 mA				GND	0.2	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V				-45		mA
I_{OZ}	TRI-STATE® Output Current	PDB = 0V, OSS_SEL = 0V, V_{OUT} = 0V or V_{DDIO}			-10		+10	µA
1.8 V I/O LVCMOS DC SPECIFICATIONS – V_{DDIO} = 1.71 to 1.89V								
V_{IH}	High Level Input Voltage			PDB, VODSEL, OEN, OSS_SEL, MAPSEL, LFMODE, SSC[2:0], BISTEN	0.7* V_{DDIO}		V_{DDIO}	V
V_{IL}	Low Level Input Voltage				GND		0.3* V_{DDIO}	V
I_{IN}	Input Current	V_{IN} = 0V or V_{DDIO}			-10	±1	+10	µA
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA		LOCK, PASS	V_{DDIO} - 0.2	V_{DDIO}		V
V_{OL}	Low Level Output Voltage	I_{OL} = +2 mA			GND		0.2	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V				-13		mA
I_{OZ}	TRI-STATE Output Current	V_{OUT} = 0V or V_{DDIO}			-15		+15	µA
FPD-Link II LVDS RECEIVER DC SPECIFICATIONS								
V_{TH}	Differential Input Threshold High Voltage	V_{CM} = +1.2V (Internal V_{BIAS})		RIN+, RIN-			+50	mV
V_{TL}	Differential Input Threshold Low Voltage				-50			mV
V_{CM}	Common Mode Voltage, Internal V_{BIAS}					1.2		V
R_T	Input Termination				80	100	120	Ω
SUPPLY CURRENT								
I_{DD1}	Supply Current (includes load current) 65 MHz Clock	Checker Board Pattern, VODSEL = H SSC{2:0] = 000 *Figure 1*	V_{DDn}= 1.89V	All $V_{DD(1.8)}$ pins		85	95	mA
I_{DDTX1}			V_{DDTX} = 3.6V	V_{DDTX}		40	50	mA
I_{DDIO1}			V_{DDIO}=1.89V	V_{DDIO}		0.3	0.8	mA
			V_{DDIO} = 3.6V			0.8	1.5	mA
I_{DD2}	Supply Current (includes load current) 65 MHz Clock	Checker Board Pattern, VODSEL = H SSC[2:0] = 111 *Figure 1*	V_{DDn}= 1.89V	All $V_{DD(1.8)}$ pins		95		mA
I_{DDTX2}			V_{DDTX} = 3.6V	V_{DDTX}		40		mA
I_{DDIO2}			V_{DDIO}=1.89V	V_{DDIO}		0.3		mA
			V_{DDIO} = 3.6V			0.8		mA
I_{DDZ}	Supply Current Power Down	PDB = 0V, All other LVCMOS Inputs = 0V	V_{DD}= 1.89V	All $V_{DD(1.8)}$ pins		0.15	2.00	mA
I_{DDTXZ}			V_{DDTX} = 3.6V	V_{DDTX}		0.01	0.10	mA
I_{DDIOZ}			V_{DDIO}=1.89V	V_{DDIO}		0.01	0.08	mA
			V_{DDIO} = 3.6V			0.01	0.08	mA

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
FPD-Link II							
t_{DDLT}	Lock Time *Figure 6*	SSC[2:0] = 000	5 MHz		7		ms
		SSC[2:0] = 111	5 MHz		14		ms
		SSC[2:0] = 000	65 MHz		6		ms
		SSC[2:0] = 111	65 MHz		8		ms
t_{IJIT}	Input Jitter Tolerance *Figure 9*	EQ = Off SSC[2:0] = 000 TxCLKOUT± = 65 MHz	Input Jitter Frequency < 2 MHz		>0.9		UI
			Input Jitter Frequency > 6 MHz		> 0.5		UI
FPD-Link Output							
t_{TLHT}	Low to High Transition Time	R_L = 100Ω	TxCLKOUT±, TxOUT[3:0]±		0.3	0.6	ns
t_{THLT}	High to Low Transition Time				0.3	0.6	ns
t_{DCCJ}	Cycle-to-Cycle Output Jitter (*Note 7*, *Note 9*, *Note 10*)	5 MHz	TxCLKOUT±		900	2100	ps
		65 MHz			75	125	ps
t_{TTP1}	Transmitter Pulse Position for bit 1	5 - 65 MHz *Figure 8*	TxOUT[3:0]±		1		UI
t_{TTP0}	Transmitter Pulse Position for bit 0				2		UI
t_{TPP6}	Transmitter Pulse Position for bit 6				3		UI
t_{TTP5}	Transmitter Pulse Position for bit 5				4		UI
t_{TTP4}	Transmitter Pulse Position for bit 4				5		UI
t_{TTP3}	Transmitter Pulse Position for bit 3				6		UI
t_{TTP2}	Transmitter Pulse Position for bit 2				7		UI
Δt_{TTP}	Offset Transmitter Pulse Position (bit 6— bit 0)	65 MHz *Figure 8*			< +0.1		UI
t_{DD}	Delay-Latency	*Figure 3*			10*T		T
t_{TPDD}	Power Down Delay active to OFF	65 MHz *Figure 4*			7	12	ns
t_{TXZR}	Enable Delay OFF to active	65 MHz *Figure 5*			40	55	ns
LVCMOS Outputs							
t_{CLH}	Low to High Transition Time	C_L = 8 pF *Figure 2*	LOCK, PASS		5	15	ns
t_{CHL}	High to Low Transition Time				5	15	ns
t_{PASS}	BIST PASS Valid Time, BISTEN = 1, *Figure 10*	5 MHz	PASS		570	580	ns
		65 MHz			50	65	ns
SSCG Mode							
f_{DEV}	Spread Spectrum Clocking Deviation Frequency	(*Note 10*)	TxCLKOUT = 5 to 65 MHz, SSC[2:0] = ON	±0.5		±2	%
f_{MOD}	Spread Spectrum Clocking Modulation Frequency	(*Note 10*)	TxCLKOUT = 5 to 65 MHz, SSC[2:0] = ON	8		100	kHz

Recommended Timing for the Serial Control Bus

Over 3.3V operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{SCL}	SCL Clock Frequency	Standard Mode	0		100	kHz
		Fast Mode	0		400	kHz
t_{LOW}	SCL Low Period	Standard Mode	4.7			us
		Fast Mode	1.3			us
t_{HIGH}	SCL High Period	Standard Mode	4.0			us
		Fast Mode	0.6			us
$t_{HD;STA}$	Hold time for a start or a repeated start condition, *Figure 11*	Standard Mode	4.0			us
		Fast Mode	0.6			us
$t_{SU:STA}$	Set Up time for a start or a repeated start condition, *Figure 11*	Standard Mode	4.7			us
		Fast Mode	0.6			us
$t_{HD;DAT}$	Data Hold Time, *Figure 11*	Standard Mode	0		3.45	us
		Fast Mode	0		0.9	us
$t_{SU;DAT}$	Data Set Up Time, *Figure 11*	Standard Mode	250			ns
		Fast Mode	100			ns
$t_{SU;STO}$	Set Up Time for STOP Condition, *Figure 11*	Standard Mode	4.0			us
		Fast Mode	0.6			us
t_{BUF}	Bus Free Time Between STOP and START, *Figure 11*	Standard Mode	4.7			us
		Fast Mode	1.3			us
t_r	SCL & SDA Rise Time, *Figure 11*	Standard Mode			1000	ns
		Fast Mode			300	ns
t_f	SCL & SDA Fall Time, *Figure 11*	Standard Mode			300	ns
		Fast mode			300	ns

DC and AC Serial Control Bus Characteristics

Over 3.3V supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Level	SDA and SCL	0.7* V_{DDIO}		V_{DDIO}	V
V_{IL}	Input Low Level Voltage	SDA and SCL	GND		0.3* V_{DDIO}	V
V_{HY}	Input Hysteresis			>50		mV
V_{OL}		SDA, IOL = 0.5mA	0		0.36	V
I_{in}		SDA or SCL, Vin = V_{DDIO} or GND	-10		+10	µA
t_R	SDA RiseTime – READ	SDA, RPU = X, Cb ≤ 400pF *Figure 11*		800		ns
t_F	SDA Fall Time – READ			50		ns
$t_{SU;DAT}$	Set Up Time — READ	*Figure 11*		540		ns
$t_{HD;DAT}$	Hold Up Time — READ			600		ns
t_{SP}	Input Filter			50		ns
C_{in}	Input Capacitance	SDA or SCL		<5		pF

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 2: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 3: Typical values represent most likely parametric norms at V_{DD} = 3.3V, Ta = +25 degC, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 4: Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except VOD, ΔVOD, VTH and VTL which are differential voltages.

Note 5: When the Serializer output is at TRI-STATE the Deserializer will lose PLL lock. Resynchronization / Relock must occur before data transfer require t_{PLD}

Note 6: t_{PLD} and t_{DDLT} is the time required by the serializer and deserializer to obtain lock when exiting power-down state with an active PCLK.

Note 7: t_{DCCJ} is the maximum amount of jitter between adjacent clock cycles.

Note 8: Supply noise testing was done with minimum capacitors on the PCB. A sinusoidal signal is AC coupled to the V_{DDn} (1.8V) supply with amplitude = 100 mVp-p measured at the device V_{DDn} pins. Bit error rate testing of input to the Ser and output of the Des with 10 meter cable shows no error when the noise frequency on the Ser is less than 750 kHz. The Des on the other hand shows no error when the noise frequency is less than 400 kHz.

Note 9: Specification is guaranteed by characterization and is not tested in production.

Note 10: Specification is guaranteed by design and is not tested in production.

AC Timing Diagrams and Test Circuits

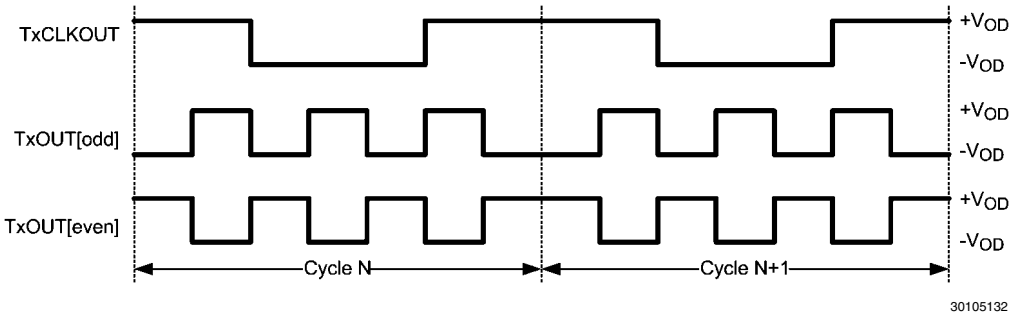


FIGURE 1. Checkerboard Data Pattern

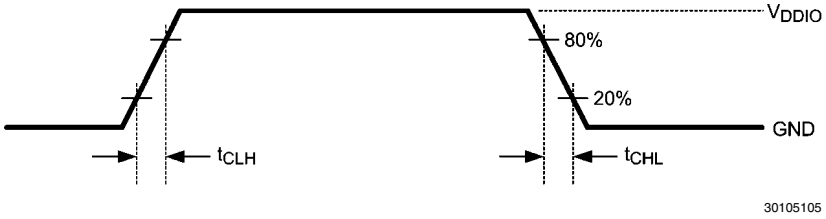


FIGURE 2. LVCMOS Transition Times

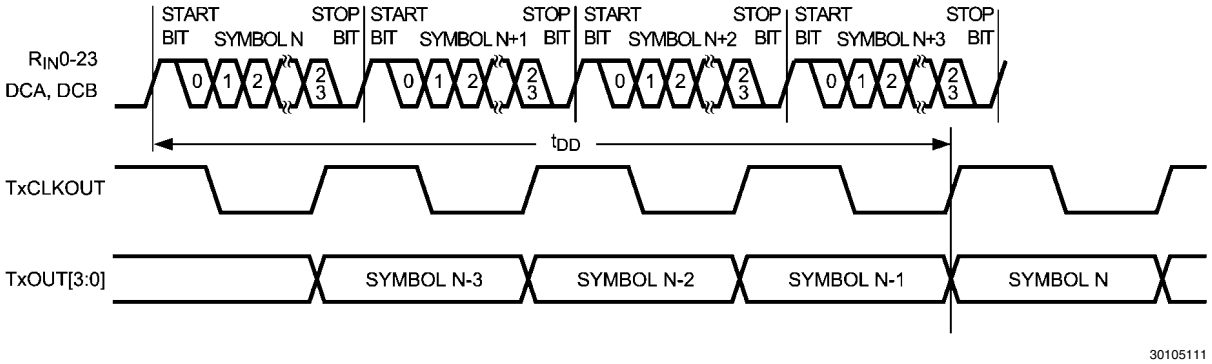


FIGURE 3. Delay – Latency

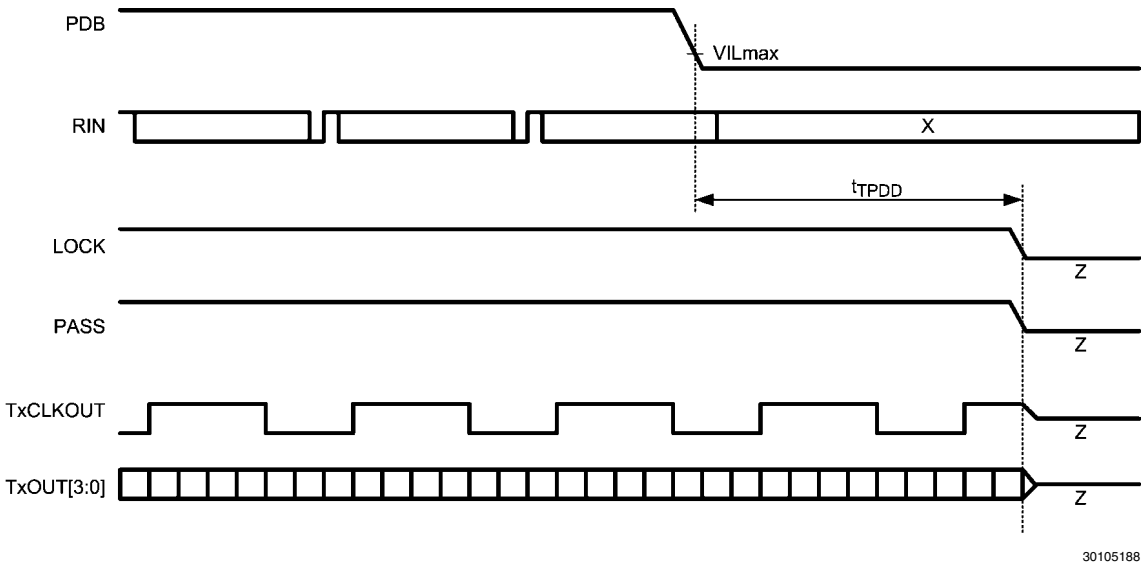


FIGURE 4. FPD-Link & LVCMOS Powerdown Delay

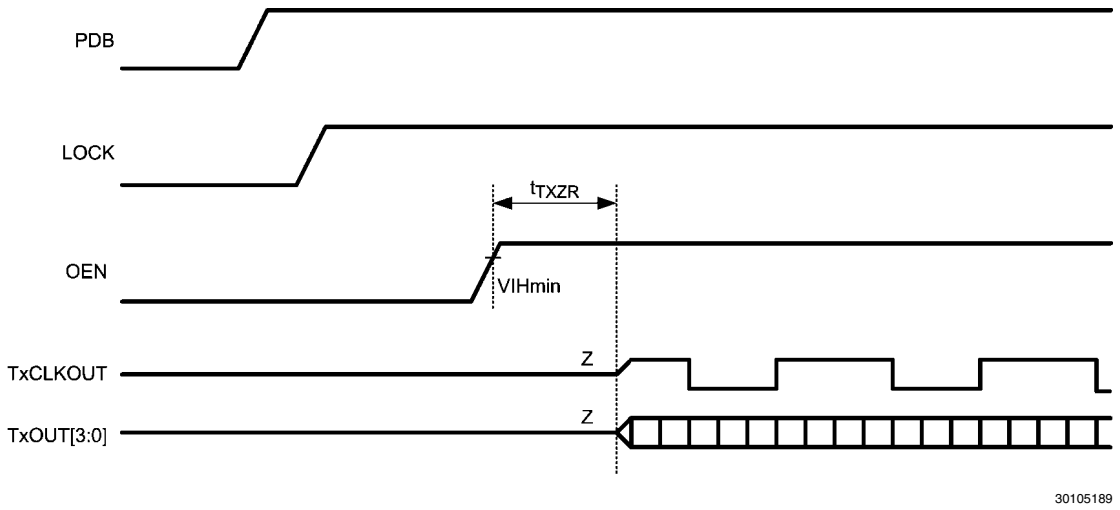


FIGURE 5. FPD-Link Outputs Enable Delay

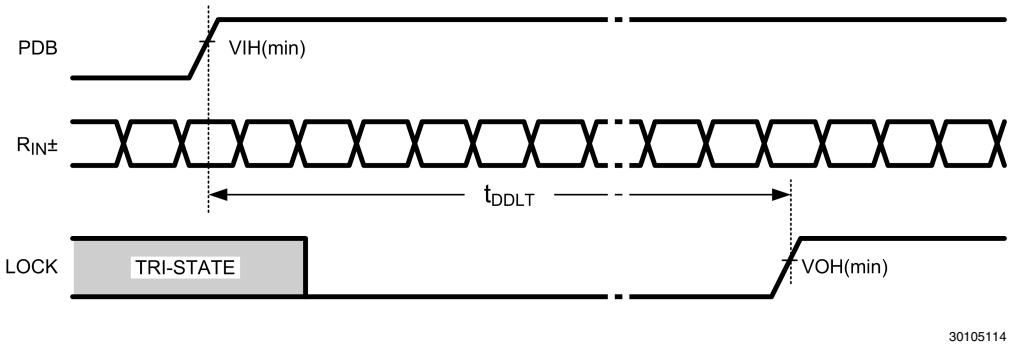


FIGURE 6. PLL Lock Times

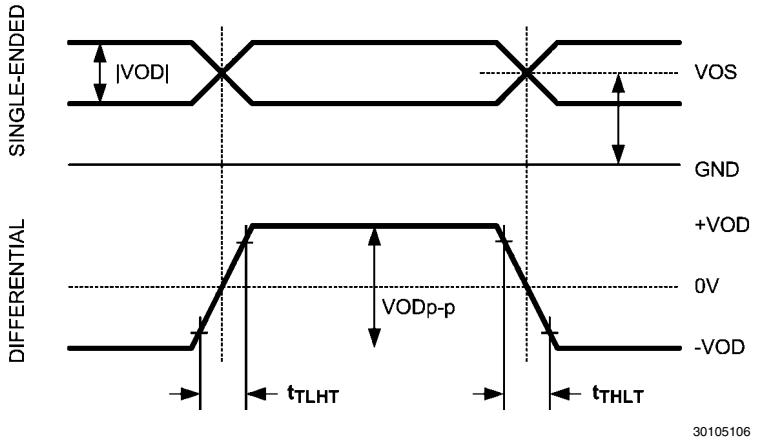


FIGURE 7. FPD-Link (LVDS) Single-ended and Differential Waveforms

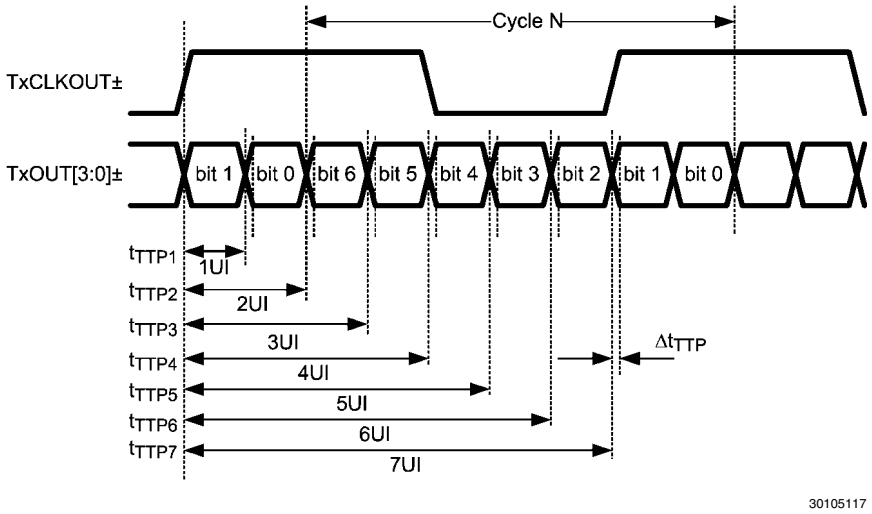


FIGURE 8. FPD-Link Transmitter Pulse Positions

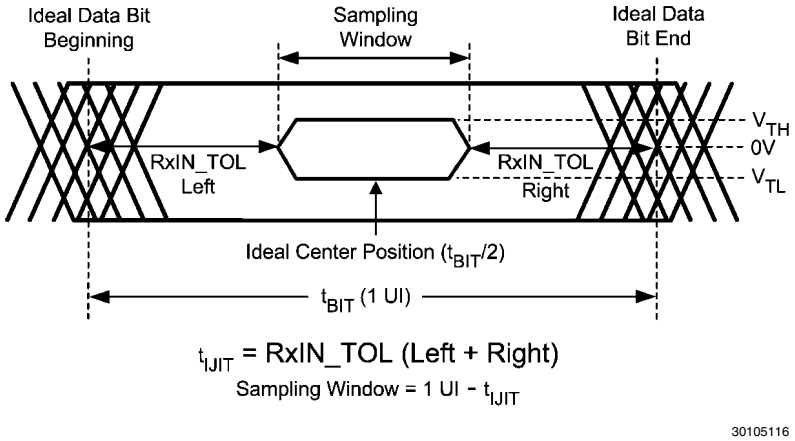


FIGURE 9. Receiver Input Jitter Tolerance

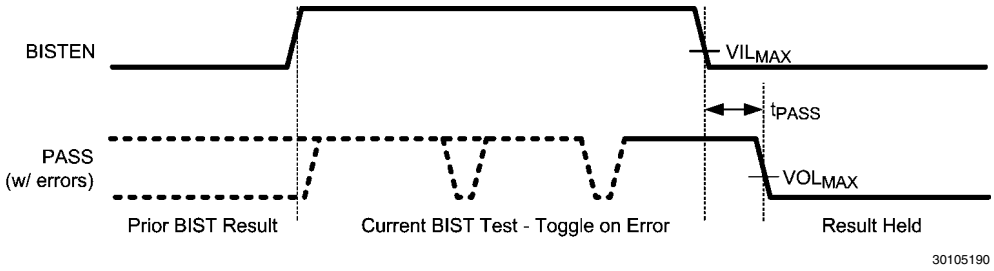


FIGURE 10. BIST PASS Waveform

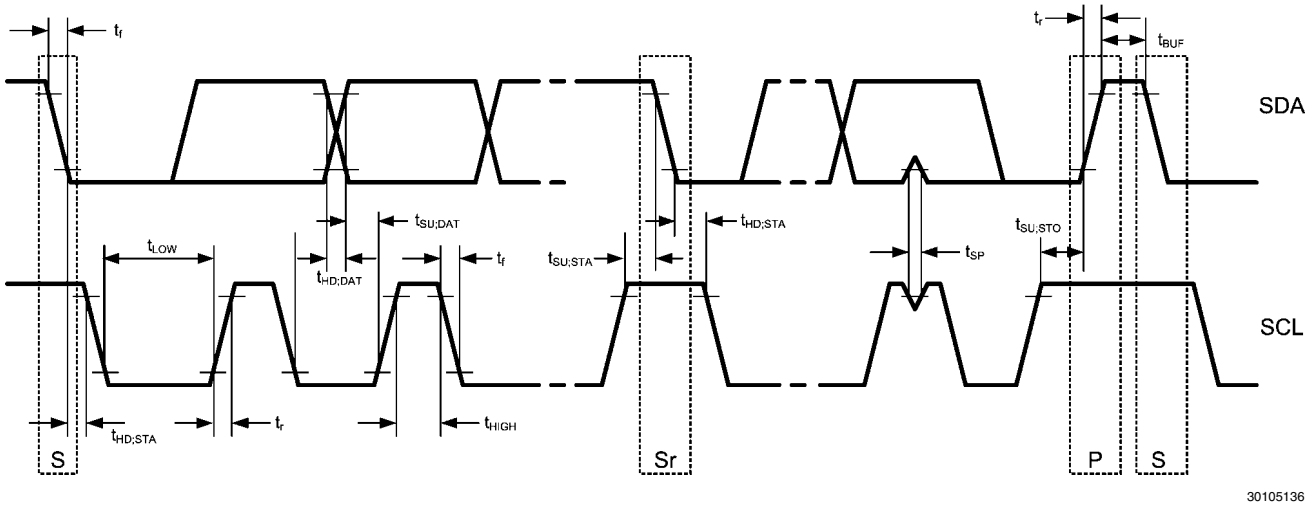


FIGURE 11. Serial Control Bus Timing Diagram

Functional Description

The DS90UR908Q receives 27-bits of data (24-high speed bits and 3 low speed bits) over a single serial FPD-Link II pair operating at 140Mbps to 1.82Gbps. The serial stream contains an embedded clock, video control signals and the DC-balance information which enhances signal quality and supports AC coupling. The receiver converts the serial stream into a 5-channel (4 data and 1 clock) FPD-Link LVDS Interface. The device is intended to be used with the DS90UR907Q or the DS90UR905Q FPD-Link II serializers, but is backward compatible with previous generation of FPD-Link II as well.

The device converts a single input serial data stream to a FPD-Link output bus, and also provides a signal check for the chipset Built In Self Test (BIST) mode. The device can be configured via external pins or through the optional serial control bus. It features enhance signal quality on the link by supporting the FPD-Link II data coding that provides randomization, scrambling, and DC balancing of the data. It also includes multiple features to reduce EMI associated with display data transmission. This includes the randomization and scrambling of the data, FPD-Link LVDS Output interface, and also the output spread spectrum clock generation (SSCG) support. The power saving features include a power down mode, and optional LVCMOS (1.8 V) interface compatibility.

The DS90UR908Q can lock to a data stream without the use of a separate reference clock source, which greatly simplifies system complexity and overall cost. It also synchronizes to the serializer regardless of the data pattern, delivering true automatic “plug and lock” performance. It can lock to the incoming serial stream without the need of special training patterns or sync characters. The DS90UR908Q recovers the clock and data by extracting the embedded clock information, validating and then deserializing the incoming data stream.

The DS90UR907Q / DS90UR908Q chipset supports 24-bit color depth, HS, VS and DE video control signals and up to three over-sampled low-speed (general purpose) data bits.

DATA TRANSFER

The DS90UR908Q will receive a pixel of data in the following format: C1 and C0 represent the embedded clock in the serial stream. C1 is always HIGH and C0 is always LOW. b[23:0] contain the scrambled data. DCB is the DC-Balanced control bit. DCB is used to minimize the short and long-term DC bias on the signal lines. This bit determines if the data is unmodified or inverted. DCA is used to validate data integrity in the embedded data stream. Both DCA and DCB coding schemes are generated by the Ser and decoded by the Des automatically. *Figure 12* illustrates the serial stream per PCLK cycle.

Note: The figure only illustrates the bits but does not actually represent the bit location as the bits are scrambled and balanced continuously.

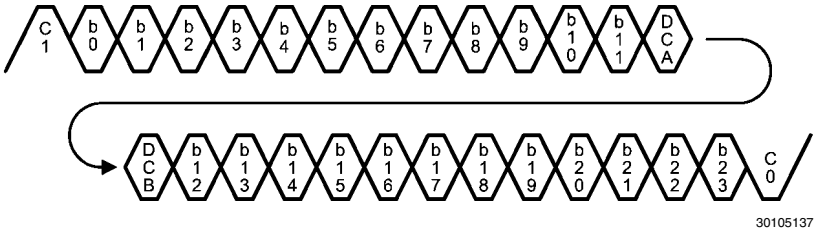


FIGURE 12. FPD-Link II Serial Stream

The device supports clocks in the range of 5 MHz to 65 MHz. With every clock cycle 24 bits of payload are received along with the four overhead bits. Thus, the line rate is 1.82 Gbps maximum (140 Mbps minimum) with an effective data rate of 1.56 Gbps maximum. The link is extremely efficient at 86% (24/28).

OPERATING MODES AND BACKWARD COMPATIBILITY (CONFIG[1:0])

The DS90UR908Q is backward compatible with previous generations of FPD-Link II serializers. Configuration modes are provided for backwards compatibility with the DS90C241 FPD-Link II Generation 1, and also the DS90UR241 or DS99R421 FPD-Link II Generation 2 serializer by setting the respective mode with the CONFIG[1:0] pins as shown in . The selection also determine whether the Video Control Signal filter feature is enabled or disabled in Normal mode. This feature may be controlled by pin or by Register.

TABLE 1. DS90UR908Q Configuration Modes

CONFIG1	CONFIG0	Mode	Des Device
L	L	Normal Mode, Control Signal Filter disabled	DS90UR907Q, DS90UR905Q
L	H	Normal Mode, Control Signal Filter enabled	DS90UR907Q, DS90UR905Q
H	L	Backwards Compatible GEN2	DS90UR241 DS99R421
H	H	Backwards Compatible GEN1	DS90C241

VIDEO CONTROL SIGNAL FILTER

When operating the devices in Normal Mode, the Video Control Signals (DE, HS, VS) have the following restrictions:

- Normal Mode with Control Signal Filter Enabled:
  DE and HS — Only 2 transitions per 130 clock cycles are transmitted, the transition pulse must be 3 PCLK or longer.
- Normal Mode with Control Signal Filter Disabled:
  DE and HS — Only 2 transitions per 130 clock cycles are transmitted, no restriction on minimum transition pulse.
- VS — Only 1 transition per 130 clock cycles are transmitted, minimum pulse width is 130 clock cycles.

Video Control Signals are defined as low frequency signals with limited transitions. Glitches of a control signal can cause a visual display error. This feature allows for the chipset to validate and filter out any high frequency noise on the control signals. See *Figure 13*.

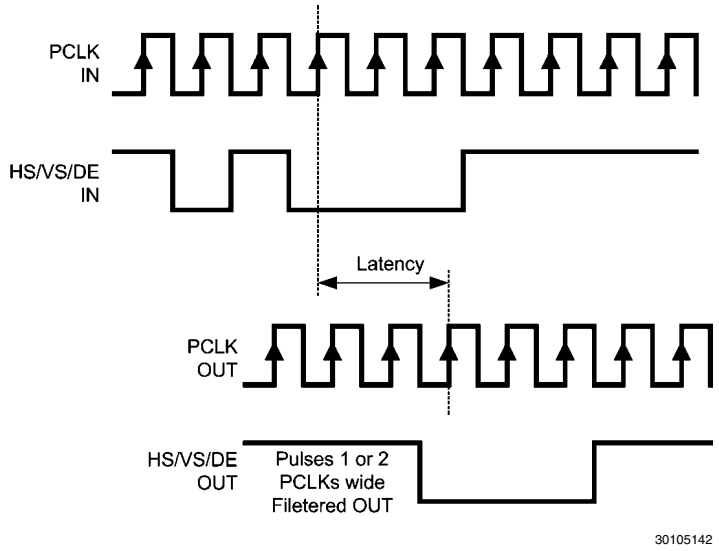


FIGURE 13. Video Control Signal Filter Wavefrom

COLOR BIT MAPPING SELECT

The DS90UR908Q can be configured to accept 24-bit color (8-bit RGB) with 2 different mapping schemes: LSBs on TxOUT[3] shown in *Figure 14* or MSBs on TxOUT[3] shown in *Figure 15*. The user selects which mapping scheme is controlled by MAPSEL pin or by Register.

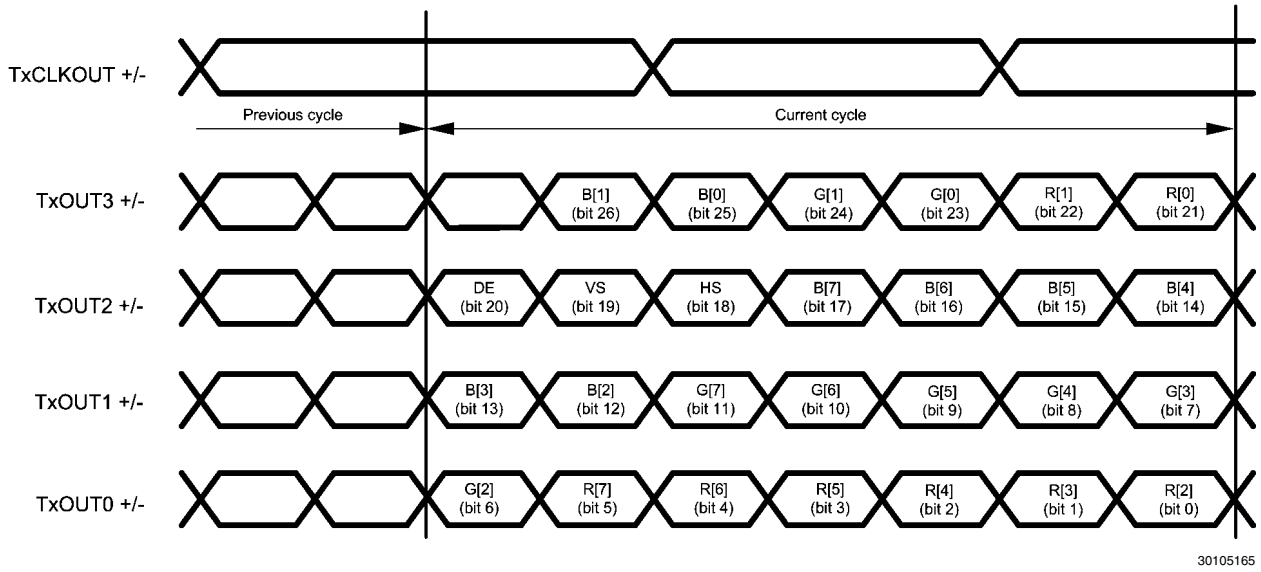


FIGURE 14. 8–bit FPD-LInk Mapping: LSB's on TxOUT3

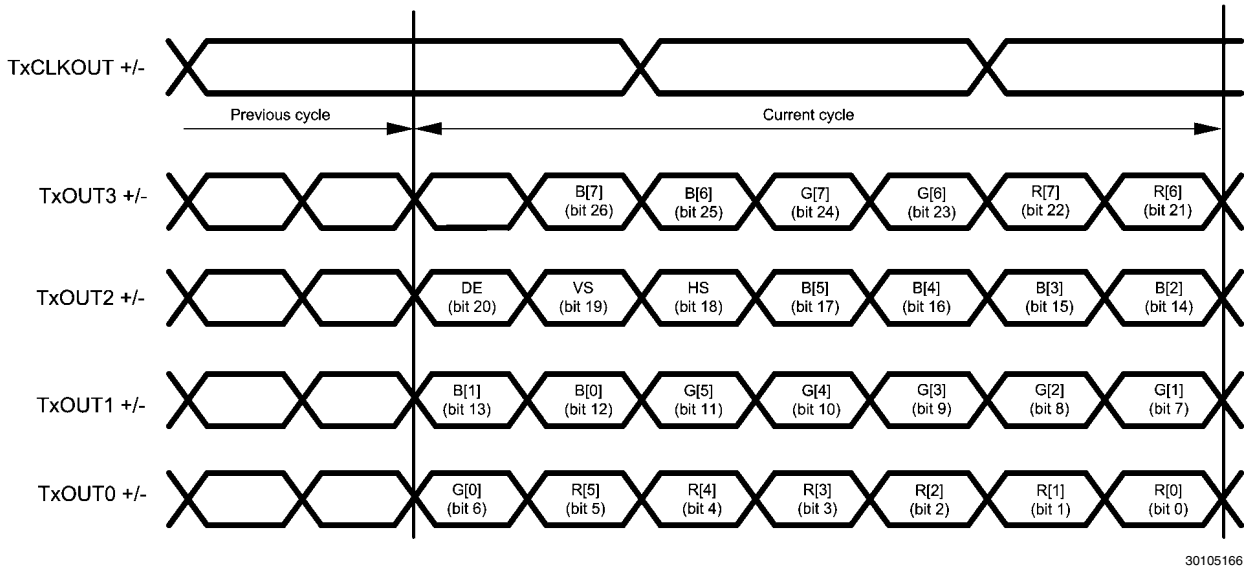


FIGURE 15. 8–bit FPD-LInk Mapping: MSB's on TxOUT3

FPD-LINK II INPUT

Common Mode Filter Pin (CMF) — Optional

The DS90UR908Q provides access to the center tap of the internal termination. A capacitor may be placed on this pin for additional common-mode filtering of the differential pair. This can be useful in high noise environments for additional noise rejection capability. A 4.7 µF capacitor may be connected to this pin to Ground.

Input Equalizer Gain (EQ)

The DS90UR908Q can enable receiver input equalization of the serial stream to compensate the cable loss and increase the eye opening to the input. The equalization feature may be controlled by the EQ pin (strap option) *Table 4* or by register *Table 8*.

TABLE 2. EQ Pin Configuration Table

EQ (Strap Option)	Effect
L	EQ = Off
H	~12 dB

POWER SAVING FEATURES

PowerDown Feature (PDB)

The DS90UR908Q has a PDB input pin to ENABLE or POWER DOWN the device. This pin can be controlled by the system to save power, disabling the Des when the display is not needed. An auto detect mode is also available. In this mode, the PDB pin is tied High and the Des will enter POWER DOWN when the serial stream stops. When the serial stream starts up again, the Des will lock to the input stream and assert the LOCK pin and output valid data. In POWER DOWN mode, the Data and PCLK output states are determined by the OSS_SEL status. Note – in POWER DOWN, the optional Serial Bus Control Registers are **RESET**.

Stop Stream SLEEP Feature

The DS90UR908Q will enter a low power SLEEP state when the input serial stream is stopped. A STOP condition is detected when the embedded clock bits are not present. When the serial stream starts again, the Des will then lock to the incoming signal and recover the data. Note – in STOP STREAM SLEEP, the optional Serial Bus Control Registers values are **RETAINED**.

OUTPUT INTERFACES (LVCMOS & FPD-LINK)

CLOCK-DATA RECOVERY STATUS FLAG (LOCK), OUTPUT ENABLE (OEN) and OUTPUT STATE SELECT (OSS_SEL)

When PDB is driven HIGH, the CDR PLL begins locking to the serial input, LOCK is Low and the FPD-Link interface state is determined by the state of the OSS_SEL pin.

After the DS90UR908Q completes its lock sequence to the input serial data, the LOCK output is driven HIGH, indicating valid data and clock recovered from the serial input is available on the FPD-Link outputs. The TxCLK output is held at its current state at the change from OSC_CLK (if this is enabled via OSC_SEL) to the recovered clock (or vice versa). Note that the FPD-Link outputs may be held in an inactive state (TRI-STATE) through the use of the Output Enable pin (OEN).

If there is a loss of clock from the input serial stream, LOCK is driven Low and the state of the outputs are based on the OSS_SEL setting (configuration pin or register).

TABLE 3. Output State Table

INPUTS			OUTPUTS	
PDB	**OEN**	**OSS_SEL**	**LOCK**	**OTHER OUTPUTS**
L	X	X	X	TxCLKOUT is TRI-STATE TxOUT[3:0] areTRI-STATE PASS is TRI-STATE
L	X	L	L	TxCLKOUT is TRI-STATE TxOUT[3:0] areTRI-STATE PASS is HIGH
H	L	H	L	TxCLKOUT is TRI-STATE TxOUT[3:0] areTRI-STATE PASS is TRI-STATE
H	H	H	L	TxCLKOUT is TRI-STATE or OSC Output through Register bit TxOUT[3:0] areTRI-STATE PASS is TRI-STATE
H	L	X	H	TxCLKOUT is TRI-STATE TxOUT[3:0] areTRI-STATE PASS is HIGH
H	H	X	H	TxCLKOUT is Active TxOUT[3:0] are Active PASS is Active *(Normal operating mode)*

LVCMOS 1.8V / 3.3V VDDIO Operation

The LVCMOS outputs can operate with 1.8 V or 3.3 V levels (V_{DDIO}) for target (Display) compatibility. The 1.8 V levels will offer a system power savings. This applies to the following pins: PASS and LOCK.

FPD-LINK OUTPUT

VODSEL

The differential output voltage of the FPD-Link interface is controlled by the VODSEL input.

TABLE 4. VODSEL Configuration Table

VODSEL	Result
L	VOD is 250mV TYP (500mVp-p)
H	VOD is 400mV TYP (800mVp-p)

SSCG GENERATION — OPTIONAI

The Des provides an internally generated spread spectrum clock (SSCG) to modulate its outputs. Both clock and data outputs are modulated. This will aid to lower system EMI. Output SSCG deviations to ±2.0% (4% total) at up to 35kHz modulations nominally are available. See *Table 5* and *Table 6*. This feature may be controlled by pins or by register. The LFMODE should be set appropriately if the SSCG is being used. Set LFMODE High if the clock frequency is between 5 MHz and 20 MHz, set LFMODE Low if the clock frequency is between 20 MHz and 65 MHz.

TABLE 5. SSCG Configuration (LFMODE = L) — Des Output

SSC[2:0] Inputs LFMODE = L (20 - 65 MHz)			Result	
SSC2	**SSC1**	**SSC0**	**fdev (%)**	**fmod (kHz)**
L	L	L	OFF	OFF
L	L	H	±0.9	CLK/2168
L	H	L	±1.2	
L	H	H	±1.9	
H	L	L	±2.3	
H	L	H	±0.7	CLK/1300
H	H	L	±1.3	
H	H	H	±1.7	

TABLE 6. SSCG Configuration (LFMODE = H) — Des Output

SSC[2:0] Inputs LFMODE = H (5 - 20 MHz)			Result	
SSC2	SSC1	SSC0	fdev (%)	fmod (kHz)
L	L	L	OFF	OFF
L	L	H	±0.7	CLK/625
L	H	L	±1.3	
L	H	H	±1.8	
H	L	L	±2.2	
H	L	H	±0.7	CLK/385
H	H	L	±1.2	
H	H	H	±1.7	

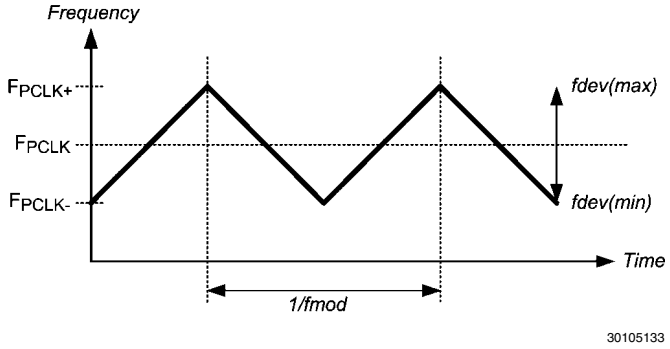
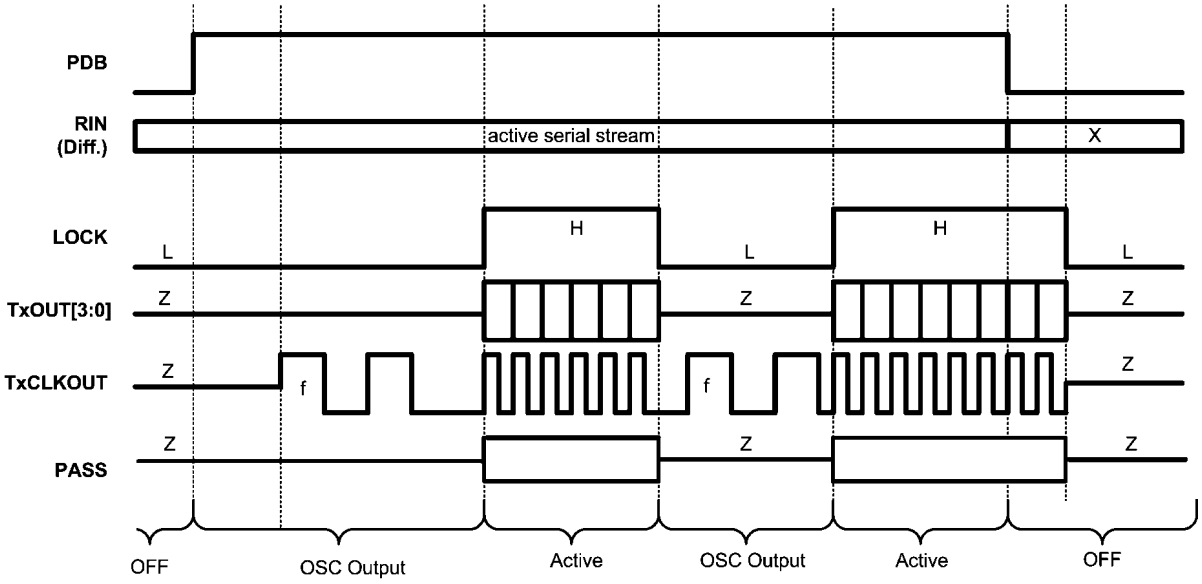


FIGURE 16. SSCG Waveform

OSCILLATOR OUTPUT — OPTIONAL

The DS90UR908Q provides an optional TxCLKOUT when the input clock (serial stream) has been lost. This is based on an internal oscillator. The frequency of the oscillator may be selected. This feature may be controlled by the external pin and the register. See Tables 3, 8.*Figure 17*



CONDITIONS: OEN = H, OSS_SEL = H, and OSC_SEL not equal to 000.

30105154

FIGURE 17. TxCLKOUT Output Oscillator Option Enabled

Built In Self Test (BIST) — Optional

An optional At-Speed Built In Self Test (BIST) feature supports the testing of the high-speed serial link. This is useful in the prototype stage, equipment production, in-system test and also for system diagnostics. In the BIST mode only an input clock is required along with control to the Ser and Des BISTEN input pins. The Ser outputs a test pattern (PRBS7) and drives the link at speed. The Des detects the PRBS7 pattern and monitors it for errors. The PASS output pin toggles to flag any payloads that are received with 1 to 24 bit errors. The BISTM pin selects the operational mode of the PASS pin. If BISTM = L, the PASS pins reports the final result only. If BISTM = H, the PASS pins counts payload errors and also results the result. The result of the test is held on the PASS output until reset (new BIST test or Power Down). A high on PASS indicates NO ERRORS were detected. A Low on PASS indicates one or more errors were detected. The duration of the test is controlled by the pulse width applied to the Des BISTEN pin.

Sample BIST Sequence

See *Figure 18* for the BIST mode flow diagram.

Step 1: Place the DS90UR907Q or DS90UR905Q in BIST Mode by setting BISTEN = H. The BIST Mode is enabled via the BISTEN pin. An RxCLKIN or PCLK is required for all the Ser options. When the DS90UR908Q detects the BIST mode pattern and command (DCA and DCB code) the RGB and control signal outputs are shut off.

Step 2: Place the DS90UR908Q in BIST mode by setting the BISTEN = H. The Device is now in the BIST mode and checks the incoming serial payloads for errors. If an error in the payload (1 to 24) is detected, the PASS pin will switch low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.

Step 3: To Stop the BIST mode, the DS90UR908Q BISTEN pin is set Low. It stops checking the data and the final test result is held on the PASS pin. If the test ran error free, the PASS output will be High. If there was one or more errors detected, the PASS output will be Low. The PASS output state is held until a new BIST is run, the device is RESET, or Powered Down. The BIST duration is user controlled by the duration of the BISTEN signal.

Step 4: To return the link to normal operation, the serializer BISTEN input is set Low. The Link returns to normal operation.

Figure 19 shows the waveform diagram of a typical BIST test for two cases. Case 1 is error free, and Case 2 shows one with multiple errors. In most cases it is difficult to generate errors due to the robustness of the link (differential data transmission etc.), thus they may be introduced by greatly extending the cable length, faulting the interconnect, reducing signal condition enhancements (De-Emphasis, VODSEL, or Rx Equalization).

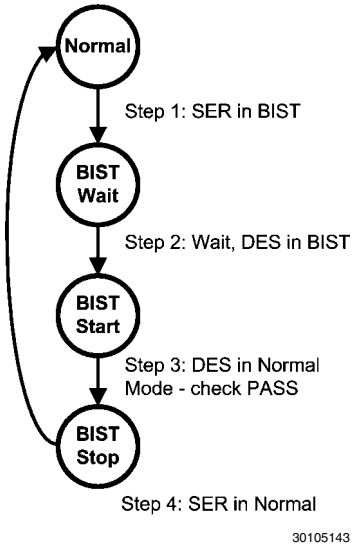


FIGURE 18. BIST Mode Flow Diagram

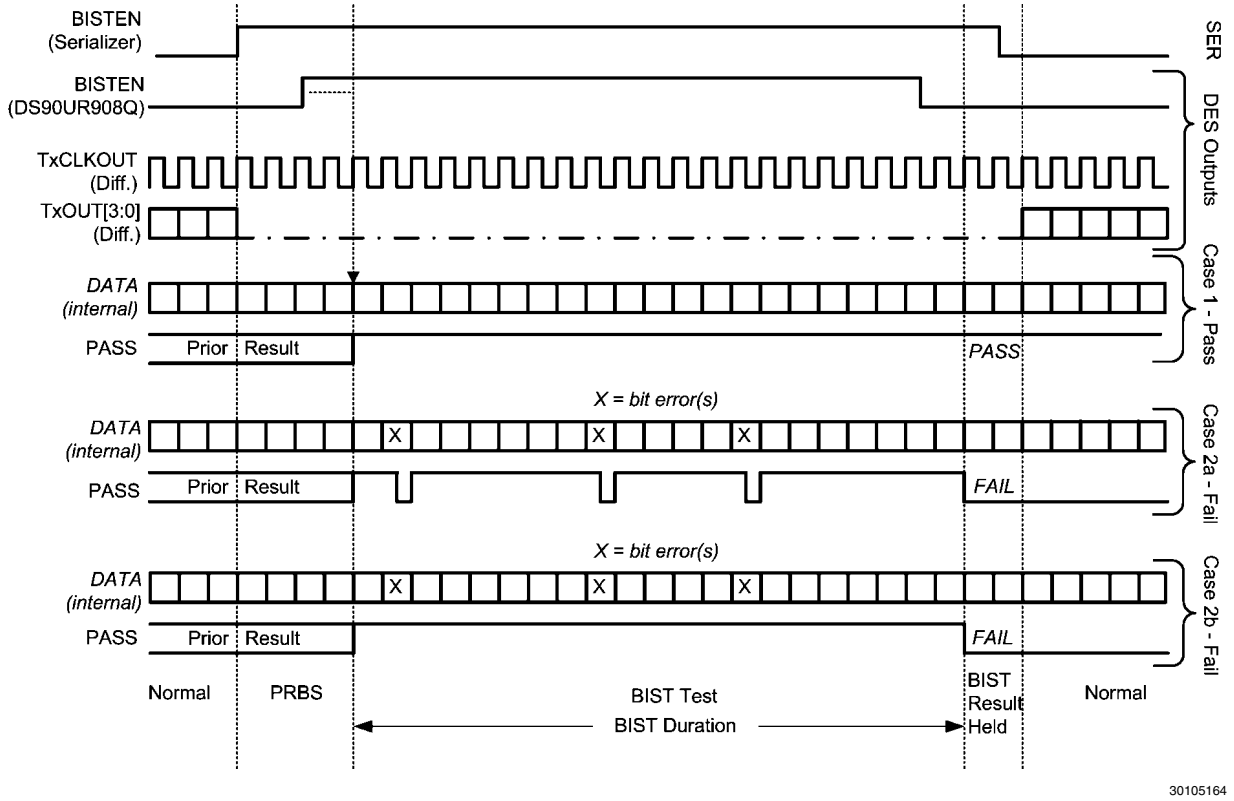


FIGURE 19. BIST Waveforms

Serial Bus Control — Optional

The DS90UR908Q may also be configured by the use of a serial control bus that is I2C protocol compatible. By default, the I2C reg_0x00'h is set to 00'h and all configuration is set by control/strap pins. A write of 01'h to reg_0x00'h will enable/allow configuration by registers; this will override the control/strap pins. Multiple devices may share the serial control bus since multiple addresses are supported. See *Figure 20*.

The serial bus is comprised of three pins. The SCL is a Serial Bus Clock Input. The SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pull up resistor to V_{DDIO}. For most applications a 4.7 k pull up resistor to V_{DDIO} may be used. The resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled High, or driven Low.

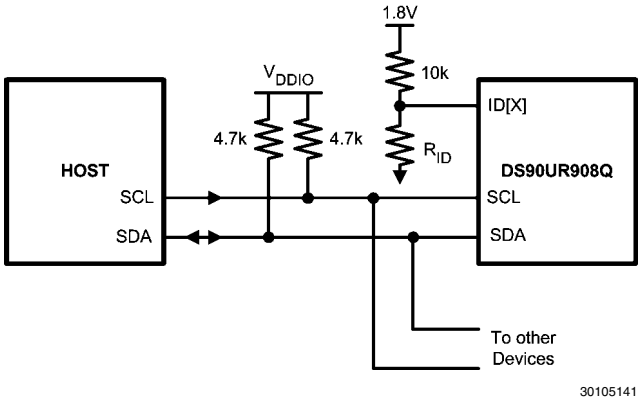


FIGURE 20. Serial Control Bus Connection

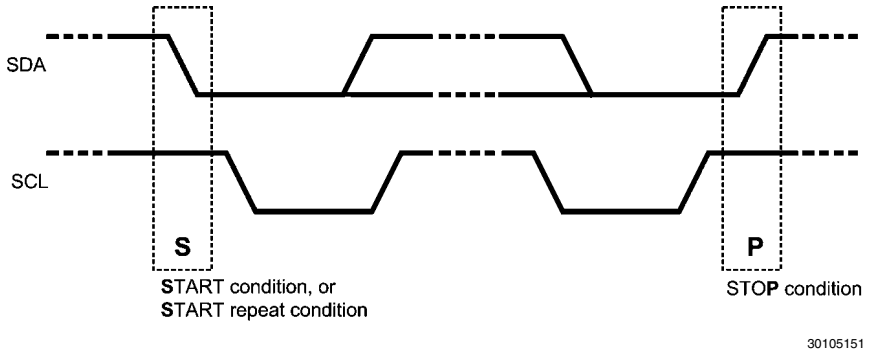


FIGURE 21. START and STOP Conditions

The third pin is the ID[X] pin. This pin sets one of five possible device addresses. Two different connections are possible. The pin may be pulled to V_{DD} (**1.8V, NOT V_{DDIO}**)) with a 10 kΩ resistor. Or a 10 kΩ pull up resistor (to V_{DD} **1.8V, NOT V_{DDIO}**)) and a pull down resistor of the recommended value to set other three possible addresses may be used. See *Table 7* for the Des. Do not tie ID[x] directly to ground.

The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SCL transitions Low while SDA is High. A STOP occurs when SDA transition High while SCL is also HIGH. See *Figure 21*

To communicate with a remote device, the host controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit (ACK). If a slave on the bus is addressed correctly, it Acknowledges (ACKs) the master by driving the SDA bus low. If the address doesn't match a device's slave address, it Not-acknowledges (NACKs) the master by letting SDA be pulled High. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a Start condition or a Repeated Start condition. All communication on the bus ends with a Stop condition. A READ is shown in *Figure 22* and a WRITE is shown in *Figure 23*.

If the Serial Bus is not required, the three pins may be left open (NC).

TABLE 7. ID[x] Resistor Value

Resistor RID kΩ (5%tol)	Address 7'b	Address 8'b 0 appended (WRITE)
0.47	7b' 111 0001 (h'71)	8b' 1110 0010 (h'E2)
2.7	7b' 111 0010 (h'72)	8b' 1110 0100 (h'E4)
8.2	7b' 111 0011 (h'73)	8b' 1110 0110 (h'E6)
Open	7b' 111 0110 (h'76)	8b' 1110 1100 (h'EC)

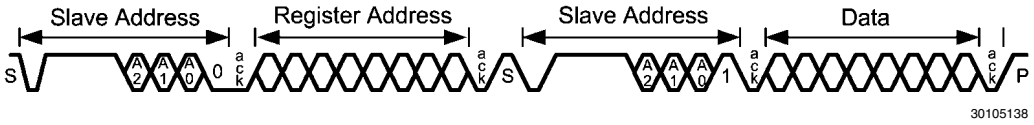


FIGURE 22. Serial Control Bus — READ

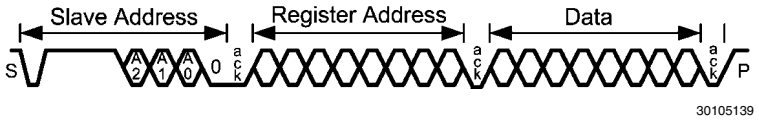


FIGURE 23. Serial Control Bus — WRITE

TABLE 8. Serial Bus Control Registers

ADD (dec)	ADD (hex)	Register Name	Bit(s)	R/W	Default (bin)	Function	Description
0	0	Des Config 1	7	R/W	0	LFMODE	0: 20 to 65 MHz Operation 1: 5 to 20 MHz Operation
			6	R/W	0	MAPSEL	FPD-Link Map Select 0: LSB on TxOUT3+/- 1: MSB on TxOUT3+/-
			5	R/W	0	***Reserved***	***Reserved***
			4	R/W	0	***Reserved***	***Reserved***
			3:2	R/W	00	CONFIG	00: Normal Mode, Control Signal Filter Disabled 01: Normal Mode, Control Signal Filter Enabled 10: Backwards Compatible (DS90UR241) 11: Backwards Compatible (DS90C241)
			1	R/W	0	SLEEP	Note – not the same function as $\overline{\text{PowerDown}}$ (PDB) 0: normal mode 1: Sleep Mode – **Register settings retained.**
			0	R/W	0	REG Control	0: Configurations set from control pins / STRAP pin 1: Configurations set from registers (except I2C_ID)
1	1	Slave ID	7	R/W	0		0: Address from ID[X] Pin 1: Address from Register
			6:0	R/W	1110 000	ID[X]	Serial Bus Device ID, Four IDs are: 7b '1110 001 (h'71); 8b ' 1110 0010 (h'E2) 7b '1110 010 (h'72); 8b ' 1110 0100 (h'E4) 7b '1110 011 (h'73); 8b ' 1110 0110 (h'E6) 7b '1110 110 (h'76); 8b ' 1110 1100 (h'EC) All other addresses are ***Reserved***.

ADD (dec)	ADD (hex)	Register Name	Bit(s)	R/W	Default (bin)	Function	Description
2	2	Des Features 1	7	R/W	0	OEN	Output Enable Input *Table 3*
			6	R/W	0	OSS_SEL	Output Sleep State Select *Table 3*
			5:4	R/W	00	***Reserved***	***Reserved***
			3	R/W	0	VODSEL	Differential Driver Output Voltage Select 0: LVDS VOD is ±250 mV, 500 mVp-p (typ) 1: LVDS VOD is ±400 mV, 800 mVp-p (typ)
			2:0	R/W	00	OSC_SEL	000: OFF 001: ***Reserved*** 010: 25 MHz ±40% 011: 16.7 MHz ±40% 100: 12.5 MHz ±40% 101: 10 MHz ±40% 110: 8.3 MHz ±40% 111: 6.3 MHz ±40%
3	3	Des Features 2	7:5	R/W	000	EQ Gain	000: ~1.625 dB 001: ~3.25 dB 010: ~4.87 dB 011: ~6.5 dB 100: ~8.125 dB 101: ~9.75 dB 110: ~11.375 dB 111: ~13 dB
			4	R/W	0	EQ Enable	0: EQ = disabled 1: EQ = enabled
			3	R/W	0	***Reserved***	***Reserved***
			2:0	R/W	000	SSC	**IF LFMODE = 0, then**: 000: SSCG OFF 001: fdev = ±0.9%, fmod = CLK/2168 010: fdev = ±1.2%, fmod = CLK/2168 011: fdev = ±1.9%, fmod = CLK/2168 100: fdev = ±2.3%, fmod = CLK/2168 101: fdev = ±0.7%, fmod = CLK/1300 110: fdev = ±1.3%, fmod = CLK/1300 111: fdev = ±1.57%, fmod = CLK/1300 **IF LFMODE = 1, then**: 000: SSCG OFF 001: fdev = ±0.7%, fmod = CLK/625 010: fdev = ±1.3%, fmod = CLK/625 011: fdev = ±1.8%, fmod = CLK/625 100: fdev = ±2.2%, fmod = CLK/625 101: fdev = ±0.7%, fmod = CLK/385 110: fdev = ±1.2%, fmod = CLK/385 111: fdev = ±1.7%, fmod = CLK/385

Applications Information

DISPLAY APPLICATION

The DS90UR908Q, in conjunction with the DS90UR907Q or DS90UR905Q, is intended for interfacing between a host (graphics processor) and a Display. It supports an 24-bit color depth (RGB888) and up to 1024 X 768 display formats. In a RGB888 application, 24 color bits (R[7:0], G[7:0], B[7:0]), Pixel Clock (PCLK) and three control bits (VS, HS and DE) are supported across the serial link with PCLK rates from 5 to 65 MHz. The device may also be used in 18-bit color applications. In this application three to six general purpose signals may also be send from host to display.

TYPICAL APPLICATION CONNECTION

Figure 24 shows a typical application of the DS90UR908Q for a 65 MHz XGA Display. The LVDS inputs utilize 100 nF coupling capacitors to the line and the Receiver provides internal termination. Bypass capacitors are placed near the power supply pins. Ferrite beads are placed on the power lines for effective noise suppression.

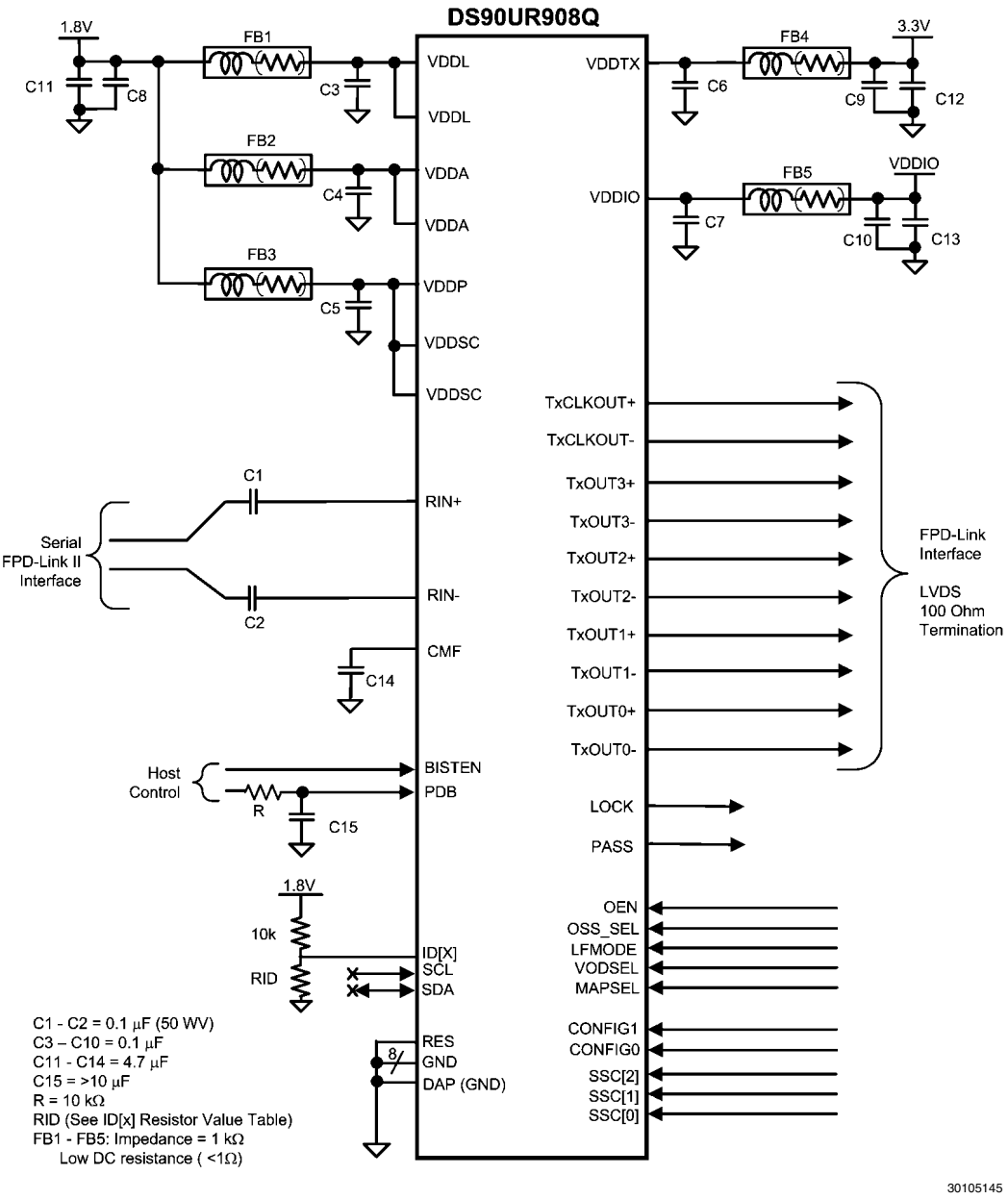


FIGURE 24. DS90UR908Q Typical Connection Diagram

POWER UP REQUIREMENTS AND PDB PIN

The VDD (V_{DDn}), V_{DDTX} and V_{DDIO} supply ramps should be faster than 1.5 ms with a monotonic rise. Supplies may power up in any order, however device operation should be initiated only after all supplies are in their valid operating ranges. The optional serial bus address selection is done upon power up also. Thus, if using this optional feature, the PDB signal must be delayed to allow time for the ID setting to occur. The delay maybe done by simply holding the PDB pin at a Low, or with an external RC delay based off the V_{DDIO} rail which would then need to lag the others in time. If the PDB pin is pulled to V_{DDIO}, it is recommended to use a 10 kΩ pull-up and a 10 uF cap to GND to delay the PDB input signal.

TRANSMISSION MEDIA

The FPD-Link II chipset is intended to be used in a point-to-point configuration, through a PCB trace, or through twisted pair cable. The serializer and deserializer provide internal terminations providing a clean signaling environment. The interconnect for LVDS should present a differential impedance of 100 Ohms. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Shielded or un-shielded cables may be used depending upon the noise environment and application requirements.

LIVE LINK INSERTION

The serializer and deserializer devices support live pluggable applications. The automatic receiver lock to random data "plug & go" hot insertion capability allows the DS90UR908Q to attain lock to the active data stream during a live insertion event.

ALTERNATE COLOR / DATA MAPPING

Color Mapped data Pin names are provided to specify a recommended mapping for 24-bit and 18-bit Applications. When connecting to earlier generations of FPD-Link II serializer devices, a color mapping review is recommended to ensure the correct connectivity is obtained. *Table 9* provides examples for interfacing between DS90UR908Q and different deserializers.

TABLE 9. Alternate Color / Data Mapping

FPD-Link	Bit Number	RGB (LSB Example)	DS90UR905Q	DS90UR241	DS99R421	DS90C241
TxOUT3	Bit 26	B1	B1	N/A		
	Bit 25	B0	B0			
	Bit 24	G1	G1			
	Bit 23	G0	G0			
	Bit 22	R1	R1			
	Bit 21	R0	R0			
TxOUT2	Bit 20	DE	DE	DIN20	RxIN2	DIN20
	Bit 19	VS	VS	DIN19		DIN19
	Bit 18	HS	HS	DIN18		DIN18
	Bit 17	B7	B7	DIN17		DIN17
	Bit 16	B6	B6	DIN16		DIN16
	Bit 15	B5	B5	DIN15		DIN15
	Bit 14	B4	B4	DIN14		DIN14
TxOUT1	Bit 13	B3	B3	DIN13	RxIN1	DIN13
	Bit 12	B2	B2	DIN12		DIN12
	Bit 11	G7	G7	DIN11		DIN11
	Bit 10	G6	G6	DIN10		DIN10
	Bit 9	G5	G5	DIN9		DIN9
	Bit 8	G4	G4	DIN8		DIN8
	Bit 7	G3	G3	DIN7		DIN7
TxOUT0	Bit 6	G2	G2	DIN6	RxIN0	DIN6
	Bit 5	R7	R7	DIN5		DIN5
	Bit 4	R6	R6	DIN4		DIN4
	Bit 3	R5	R5	DIN3		DIN3
	Bit 2	R4	R4	DIN2		DIN2
	Bit 1	R3	R3	DIN1		DIN1
	Bit 0	R2	R2	DIN0		DIN0
N/A			N/ADIN12	DIN23	OS2	DIN23
				DIN22	OS1	DIN22
				DIN21	OS0	DIN21
DS90UR908Q Settings	**MAPSEL = 0**		**CONFIG [1:0] = 00**	**CONFIG [1:0] = 10**		**CONFIG [1:0] = 11**

PCB LAYOUT AND POWER SYSTEM CONSIDERATIONS

Circuit board layout and stack-up for the LVDS devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50uF to 100uF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely-coupled differential lines of 100 Ohms are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Information on the LLP style package is provided in National Application Note: AN-1187.

LVDS INTERCONNECT GUIDELINES

See AN-1108 and AN-905 for full details.

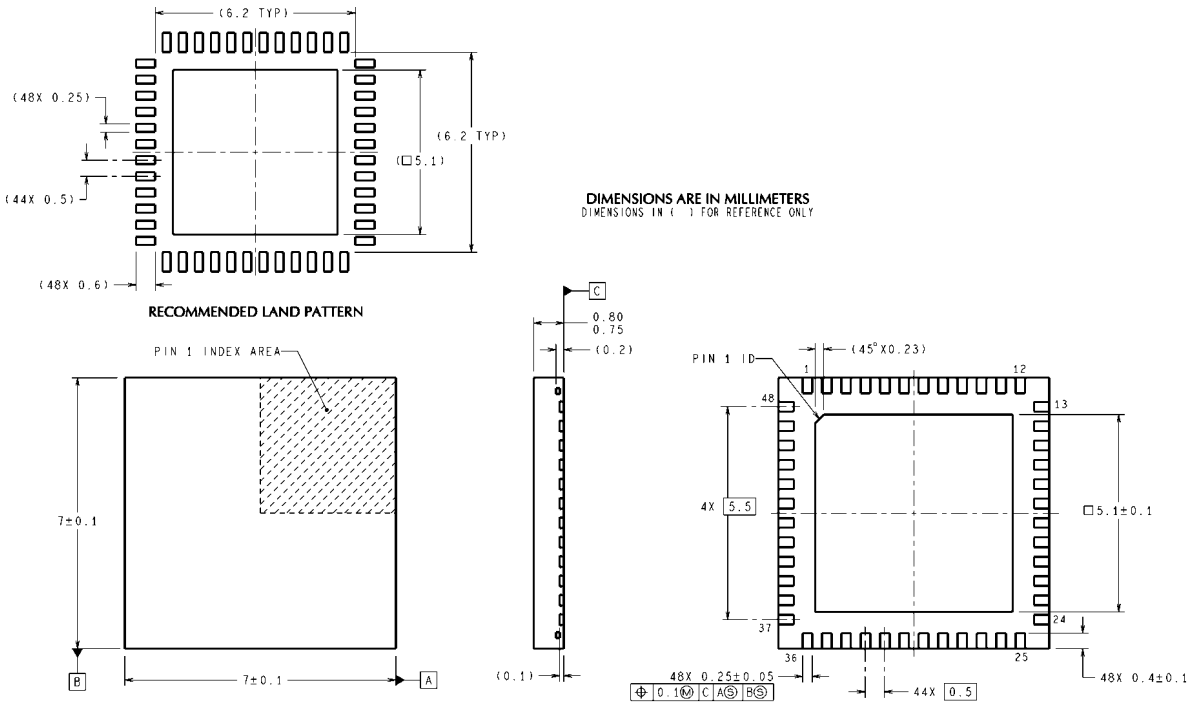
- Use 100Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  – S = space between the pair
  – 2S = space between pairs
  – 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Terminate as close to the TX outputs and RX inputs as possible

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the National web site at: **www.national.com/lvds**

Revision History

- 03/30/2010 — Initial Release
- 07/26/2010 — Update all final AC and DC parameter limits
- 08/09/2010 — Update Pin Description of VODSEL

Physical Dimensions inches (millimeters) unless otherwise noted



48–pin LLP Package (7.0 mm x 7.0 mm x 0.8 mm, 0.5 mm pitch)
NS Package Number SQA48A

Notes

Notes

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LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
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PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions
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