National Semiconductor

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DS90UR905Q/DS90UR906Q

5 - 65 MHz 24-bit Color FPD-Link II Serializer and Deserializer

General Description

The DS90UR905Q/906Q chipset translates a parallel RGB Video Interface into a high-speed serialized interface over a single pair. This serial bus scheme greatly eases system design by eliminating skew problems between clock and data, reduces the number of connector pins, reduces the interconnect size, weight, and cost, and overall eases PCB layout. In addition, internal DC balanced decoding is used to support AC-coupled interconnects.

The DS90UR905Q Ser (serializer) embeds the clock, balances the data payload, and level shifts the signals to high-speed low voltage differential signaling. Up to 24 inputs are serialized along with the three video control signals. This supports full 24-bit color or 18-bit color and 6 general purpose signals (e.g. Audio I2S) applications.

The DS90UR906Q Des (deserializer) recovers the data (RGB) and control signals and extracts the clock from the serial stream. It is able to lock to the incoming data stream without the use of a training sequence or special SYNC patterns, and does not require a reference clock. A link status (LOCK) output signal is provided.

Serial transmission is optimized by a user selectable de-emphasis, differential output level select features, and receiver equalization. EMI is minimized by the use of low voltage differential signaling, receiver drive strength control, and spread spectrum clocking compatibility. The Des may be configured to generate Spread Spectrum Clock and Data on its parallel outputs.

The DS90UR905Q (Ser) is offered in a 48-pin LLP and the DS90UR906Q (Des) is offered in a 60-pin LLP package. They are specified over the automotive AEC-Q100 grade 2 temperature range of -40°C to +105°C.

Features

- 5 – 65 MHz PCLK support (140 Mbps – 1.82 Gbps)
- AC coupled STP interconnect cable up to 10 meters
- Integrated terminations on Ser and Des
- @ Speed link BIST mode and reporting pin
- Optional I2C compatible Serial Control Bus
- RGB888 + VS, HS, DE support
- Power down mode minimizes power dissipation
- 1.8V or 3.3V compatible LVCMOS I/O interface
- Automotive grade product: AEC-Q100 Grade 2 qualified
- >8 kV HBM and ISO 10605 ESD Rating
- Backward compatible mode for operation with older generation devices

SERIALIZER — DS90UR905Q

- RGB888 + VS/HS/DE serialized to 1 pair FPD-Link II
- Randomizer/Scrambler — DC-balanced data stream
- Selectable output VOD and adjustable de-emphasis

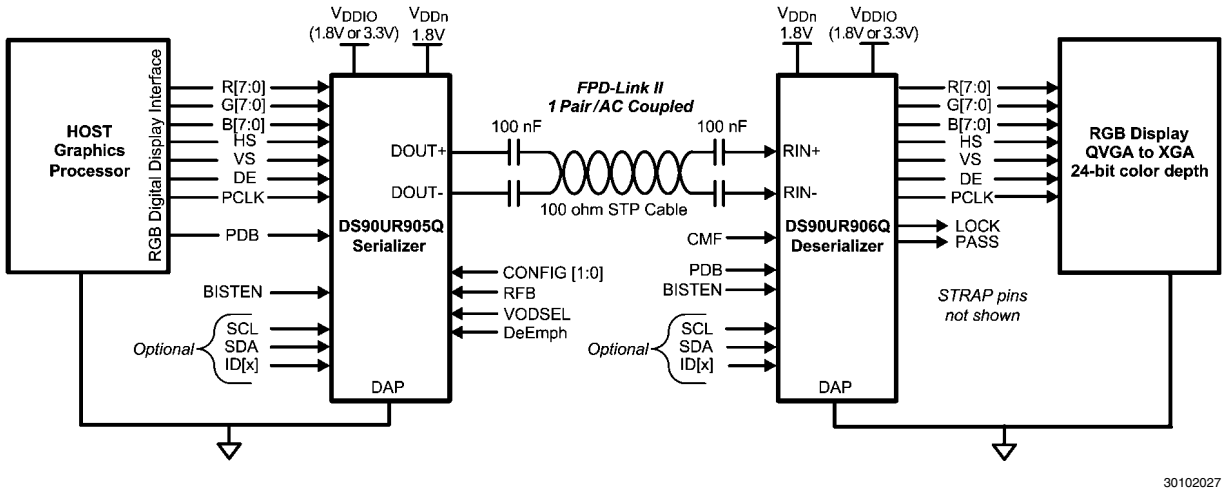
DESERIALIZER — DS90UR906Q

- FAST random data lock; no reference clock required
- Adjustable input receiver equalization
- LOCK (real time link status) reporting pin
- EMI minimization on output parallel bus (SSCG)
- Output Slew control (OS)

Applications

- Automotive Display for Navigation
- Automotive Display for Entertainment

Applications Diagram



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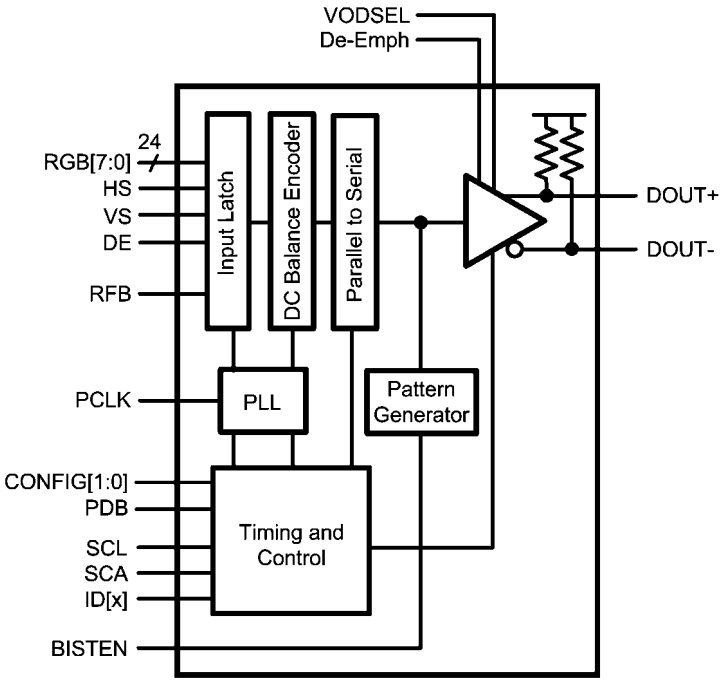
Block Diagrams



DS90UR905Q – SERIALIZER

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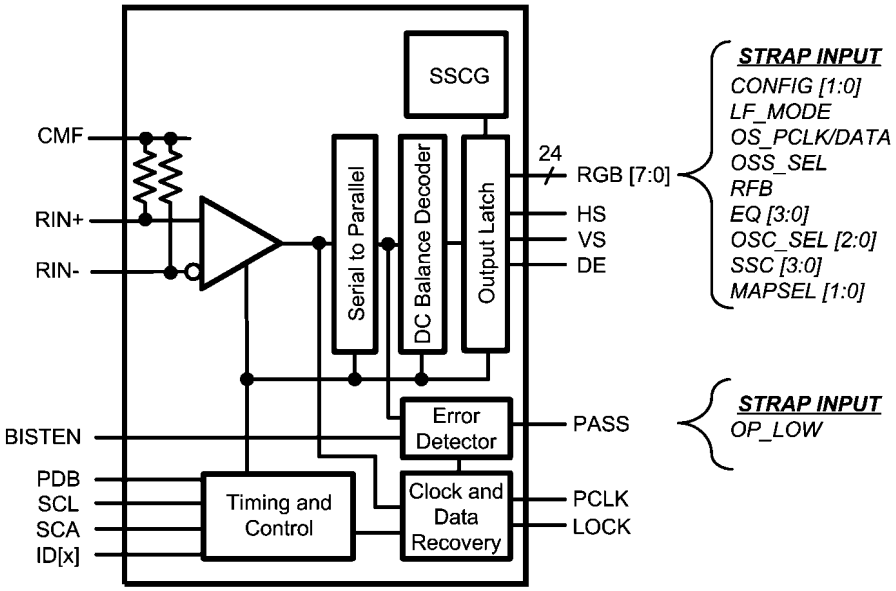

DS90UR906Q – DESERIALIZER

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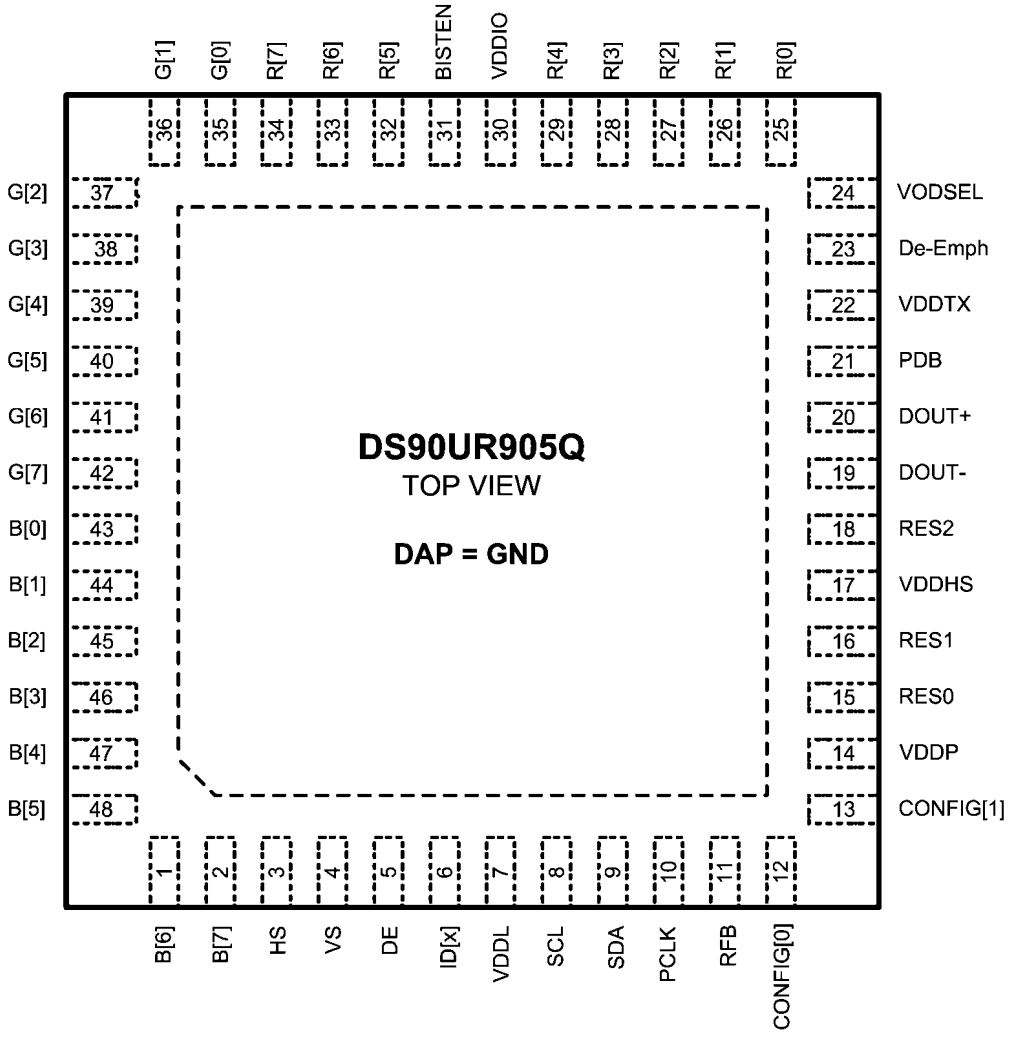
Ordering Information

NSPN	Package Description	Quantity	Package ID
DS90UR905QSQE NOPB	48–pin LLP, 7.0 X 7.0 X 0.8 mm, 0.5 mm pitch	250	SQA48A
DS90UR905QSQ NOPB	48–pin LLP, 7.0 X 7.0 X 0.8 mm, 0.5 mm pitch	1000	SQA48A
DS90UR905QSQX NOPB	48–pin LLP, 7.0 X 7.0 X 0.8 mm, 0.5 mm pitch	2500	SQA48A
DS90UR906QSQE NOPB	60–pin LLP, 9.0 X 9.0 X 0.8 mm, 0.5 mm pitch	250	SQA60B
DS90UR906QSQ NOPB	60–pin LLP, 9.0 X 9.0 X 0.8 mm, 0.5 mm pitch	1000	SQA60B
DS90UR906QSQX NOPB	60–pin LLP, 9.0 X 9.0 X 0.8 mm, 0.5 mm pitch	2000	SQA60B

Note: Automotive Grade (Q) product incorporates enhanced manufacturing and support processes for the automotive market, including defect detection methodologies. Reliability qualification is compliant with the requirements and temperature grades defined in the AEC Q100 standard. Automotive Grade products are identified with the letter Q. For more information go to http://www.national.com/automotive.

DS90UR905Q Pin Diagram



Serializer - DS90UR905Q — Top View

DS90UR905Q Serializer Pin Descriptions

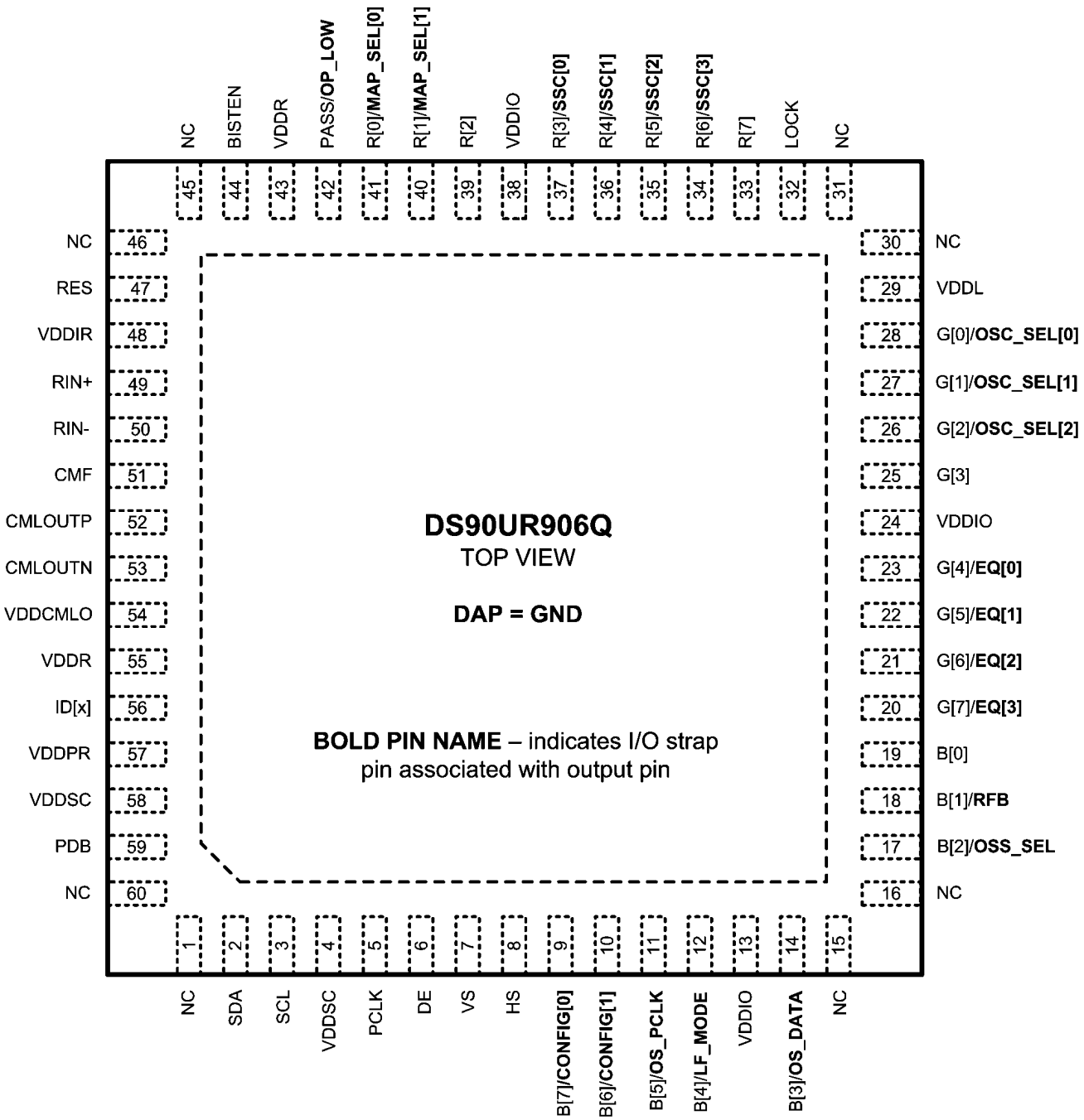
Pin Name	Pin #	I/O, Type	Description
LVCMOS Parallel Interface			
R[7:0]	34, 33, 32, 29, 28, 27, 26, 25	I, LVCMOS w/ pull-down	RED Parallel Interface Data Input Pins (MSB = 7, LSB = 0)
G[7:0]	42, 41, 40, 39, 38, 37, 36, 35	I, LVCMOS w/ pull-down	GREEN Parallel Interface Data Input Pins (MSB = 7, LSB = 0)
B[7:0]	2, 1, 48, 47, 46, 45, 44, 43	I, LVCMOS w/ pull-down	BLUE Parallel Interface Data Input Pins (MSB = 7, LSB = 0)
HS	3	I, LVCMOS w/ pull-down	Horizontal Sync Input Video control signal pulse width must be 3 PCLKs or longer to be transmitted when the Control Signal Filter is enabled (CONFIG[1:0] = 01). There is no restriction on the minimum transition pulse when the Control Signal Filter is disabled (CONFIG[1:0] = 00). The signal is limited to 2 transitions per 130 PCLKs.
VS	4	I, LVCMOS w/ pull-down	Vertical Sync Input Video control signal is limited to 1 transition per 130 PCLKs. Thus, the minimum pulse width is 130 PCLKs.
DE	5	I, LVCMOS w/ pull-down	Data Enable Input Video control signal pulse width must be 3 PCLKs or longer to be transmitted when the Control Signal Filter is enabled (CONFIG[1:0] = 01). There is no restriction on the minimum transition pulse when the Control Signal Filter is disabled (CONFIG[1:0] = 00). The signal is limited to 2 transitions per 130 PCLKs.
PCLK	10	I, LVCMOS w/ pull-down	Pixel Clock Input Latch edge set by RFB function.
Control and Configuration			
PDB	21	I, LVCMOS w/ pull-down	Power-down Mode Input PDB = 1, Ser is enabled (normal operation). Refer to ”Power Up Requirements and PDB Pin” in the Applications Information Section. PDB = 0, Ser is powered down When the Ser is in the power-down state, the driver outputs (DOUT+/-) are both logic high, the PLL is shutdown, IDD is minimized. Control Registers are **RESET**.
VODSEL	24	I, LVCMOS w/ pull-down	Differential Driver Output Voltage Select — Pin or Register Control VODSEL = 1, LVDS VOD is ±420 mV, 840 mVp-p (typ) — Long Cable / De-E Applications VODSEL = 0, LVDS VOD is 280 mV, 560 mVp-p (typ)
De-Emph	23	I, Analog w/ pull-up	De-Emphasis Control — Pin or Register Control De-Emph = open (float) - disabled To enable De-emphasis, tie a resistor from this pin to GND or control via register. See *Table 4*.
RFB	11	I, LVCMOS w/ pull-down	Pixel Clock Input Latch Edge Select — Pin or Register Control RFB = 1, parallel interface data and control signals are latched on the rising clock edge. RFB = 0, parallel interface data and control signals are latched on the falling clock edge.
CONFIG [1:0]	13, 12	I, LVCMOS w/ pull-down	Operating Modes — Pin or Register Control Determine the DS90UR905’s operating mode and interfacing device. CONFIG[1:0] = 00: Interfacing to DS90UR906, Control Signal Filter DISABLED CONFIG[1:0] = 01: Interfacing to DS90UR906, Control Signal Filter ENABLED CONFIG [1:0] = 10: Interfacing to DS90UR124, DS99R124 CONFIG [1:0] = 11: Interfacing to DS90C124
ID[x]	6	I, Analog	Serial Control Bus Device ID Address Select — Optional Resistor to Ground and 10 kΩ pull-up to 1.8V rail. See *Table 13*.
SCL	8	I, LVCMOS	Serial Control Bus Clock Input - Optional SCL requires an external pull-up resistor to V_{DDIO}.
SDA	9	I/O, LVCMOS Open Drain	Serial Control Bus Data Input / Output - Optional SDA requires an external pull-up resistor V_{DDIO}.

Pin Name	Pin #	I/O, Type	Description
BISTEN	31	I, LVCMOS w/ pull-down	BIST Mode — Optional BISTEN = 1, BIST is enabled BISTEN = 0, BIST is disabled
RES[2:0]	18, 16, 15	I, LVCMOS w/ pull-down	***Reserved*** - tie LOW
FPD-Link II Serial Interface			
DOUT+	20	O, LVDS	True Output. The output must be AC Coupled with a 100 nF capacitor.
DOUT-	19	O, LVDS	Inverting Output. The output must be AC Coupled with a 100 nF capacitor.
Power and Ground			
VDDL	7	Power	Logic Power, 1.8 V ±5%
VDDP	14	Power	PLL Power, 1.8 V ±5%
VDDHS	17	Power	TX High Speed Logic Power, 1.8 V ±5%
VDDTX	22	Power	Output Driver Power, 1.8 V ±5%
VDDIO	30	Power	LVCMOS I/O Power, **1.8 V ±5% OR 3.3 V ±10%**
GND	DAP	Ground	DAP is the large metal contact at the bottom side, located at the center of the LLP package. **Connect to the ground plane** (GND) with at least 9 vias.

NOTE: 1 = HIGH, 0 = LOW

The VDD (V_{DDn} and V_{DDIO}) supply ramp should be faster than 1.5 ms with a monotonic rise. If slower then 1.5 ms then a capacitor on the PDB pin is needed to ensure PDB arrives after all the VDD have settled to the recommended operating voltage.

DS90UR906Q Pin Diagram



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Deserializer - DS90UR906Q — Top View

DS90UR906Q Deserializer Pin Descriptions

Pin Name	Pin #	I/O, Type	Description
LVCMOS Parallel Interface			
R[7:0]	33, 34, 35, 36, 37, 39, 40, 41	I, STRAP, O, LVCMOS	RED Parallel Interface Data Output Pins (MSB = 7, LSB = 0) In power-down (PDB = 0), outputs are controlled by the OSS_SEL (See *Table 8*). These pins are inputs during power-up (See STRAP Inputs).
G[7:0]	20, 21, 22, 23, 25, 26, 27, 28	I, STRAP, O, LVCMOS	GREEN Parallel Interface Data Output Pins (MSB = 7, LSB = 0) In power-down (PDB = 0), outputs are controlled by the OSS_SEL (See *Table 8*). These pins are inputs during power-up (See STRAP Inputs).
B[7:0]	9, 10, 11, 12, 14, 17, 18, 19	I, STRAP, O, LVCMOS	BLUE Parallel Interface Data Output Pins (MSB = 7, LSB = 0) In power-down (PDB = 0), outputs are controlled by the OSS_SEL (See *Table 8*). These pins are inputs during power-up (See STRAP Inputs).
HS	8	O, LVCMOS	Horizontal Sync Output In power-down (PDB = 0), output is controlled by the OSS_SEL pin (See *Table 8*). Video control signal pulse width must be 3 PCLKs or longer to be transmitted when the Control Signal Filter is enabled (CONFIG[1:0] = 01). There is no restriction on the minimum transition pulse when the Control Signal Filter is disabled (CONFIG[1:0] = 00). The signal is limited to 2 transitions per 130 PCLKs.
VS	7	O, LVCMOS	Vertical Sync Output In power-down (PDB = 0), output is controlled by the OSS_SEL pin (See *Table 8*). Video control signal is limited to 1 transition per 130 PCLKs. Thus, the minimum pulse width is 130 PCLKs.
DE	6	O, LVCMOS	Data Enable Output In power-down (PDB = 0), output is controlled by the OSS_SEL pin (See *Table 8*). Video control signal pulse width must be 3 PCLKs or longer to be transmitted when the Control Signal Filter is enabled (CONFIG[1:0] = 01). There is no restriction on the minimum transition pulse when the Control Signal Filter is disabled (CONFIG[1:0] = 00). The signal is limited to 2 transitions per 130 PCLKs.
PCLK	5	O, LVCMOS	Pixel Clock Output In power-down (PDB = 0), output is controlled by the OSS_SEL pin (See *Table 8*). Strobe edge set by RFB function.
LOCK	32	O, LVCMOS	LOCK Status Output LOCK = 1, PLL is Locked, outputs are active LOCK = 0, PLL is unlocked, RGB[7:0], HS, VS, DE and PCLK output states are controlled by OSS_SEL (See *Table 8*). May be used as Link Status or to flag when Video Data is active (ON/OFF).
PASS	42	O, LVCMOS	PASS Output (BIST Mode) PASS = 1, error free transmission PASS = 0, one or more errors were detected in the received payload Route to test point for monitoring, or leave open if unused.
Control and Configuration — STRAP PINS For a High State, use a 10 kΩ pull up to V_{DDIO}; for a Low State, the IO includes an internal pull down. The STRAP pins are read upon power-up and set device configuration. Pin Number listed along with shared RGB Output name in square brackets.			
CONFIG[1:0]	10 [B6], 9 [B7]	STRAP I, LVCMOS w/ pull-down	Operating Modes — Pin or Register Control These pins determine the DS90UR906's operating mode and interfacing device. CONFIG[1:0] = 00: Interfacing to DS90UR905, Control Signal Filter DISABLED CONFIG[1:0] = 01: Interfacing to DS90UR905, Control Signal Filter ENABLED CONFIG[1:0] = 10: Interfacing to DS90UR241 CONFIG[1:0] = 11: Interfacing to DS90C241
LF_MODE	12 [B4]	STRAP I, LVCMOS w/ pull-down	SSCG Low Frequency Mode — Pin or Register Control Only required when SSCG is enabled, otherwise LF_MODE condition is a DON'T CARE (X). LF_MODE = 1, SSCG in low frequency mode (PCLK = 5-20 MHz) LF_MODE = 0, SSCG in high frequency mode (PCLK = 20-65 MHz)

Pin Name	Pin #	I/O, Type	Description
OS_PCLK	11 [B5]	STRAP I, LVCMOS w/ pull-down	PCLK Output Slew Select — Pin or Register Control OS_PCLK = 1, increased PCLK slew OS_PCLK = 0, normal (default)
OS_DATA	14 [B3]	STRAP I, LVCMOS w/ pull-down	Data Output Slew Select — Pin or Register Control OS_DATA = 1, increased DATA slew OS_DATA = 0, normal (default)
OP_LOW	42 PASS	STRAP I, LVCMOS w/ pull-down	Outputs held Low when LOCK = 1 — Pin or Register Control NOTE: IT IS NOT RECOMMENDED TO USE ANY OTHER STRAP OPTIONS WITH THIS STRAP FUNCTION OP_LOW = 1: all outputs are held LOW during power up until released by programming OP_LOW release/set register HIGH NOTE: Before the device is powered up, the outputs are in tri-state. See *Figure 26* and *Figure 27*. OP_LOW = 0: all outputs toggle normally as soon as LOCK goes HIGH (default).
OSS_SEL	17 [B2]	STRAP I, LVCMOS w/ pull-down	Output Sleep State Select — Pin or Register Control NOTE: OSS_SEL STRAP CANNOT BE USED IF OP_LOW =1 OSS_SEL is used in conjunction with PDB to determine the state of the outputs in Power Down (Sleep). (See *Table 8*).
RFB	18 [B1]	STRAP I, LVCMOS w/ pull-down	Pixel Clock Output Strobe Edge Select — Pin or Register Control RFB = 1, parallel interface data and control signals are strobed on the rising clock edge. RFB = 0, parallel interface data and control signals are strobed on the falling clock edge.
EQ[3:0]	20 [G7], 21 [G6], 22 [G5], 23 [G4]	STRAP I, LVCMOS w/ pull-down	Receiver Input Equalization — Pin or Register Control (See *Table 5*).
OSC_SEL[2:0]	26 [G2], 27 [G1], 28 [G0]	STRAP I, LVCMOS w/ pull-down	Oscillator Select — Pin or Register Control (See *Table 9* and *Table 10*).
SSC[3:0]	34 [R6], 35 [R5], 36 [R4], 37 R[3]	STRAP I, LVCMOS w/ pull-down	Spread Spectrum Clock Generation (SSCG) Range Select — Pin or Register Control (See *Table 6* and *Table 7*).
MAP_SEL[1:0]	40 [R1], 41 [R0]	STRAP I, LVCMOS w/ pull-down	Bit Mapping Backward Compatibility / DS90UR241 Options — Pin or Register Control Normal setting to b'00. See (*Table 11*).
Control and Configuration			
PDB	59	I, LVCMOS w/ pull-down	Power Down Mode Input PDB = 1, Des is enabled (normal operation). Refer to “Power Up Requirements and PDB Pin” in the Applications Information Section. PDB = 0, Des is in power-down. When the Des is in the power-down state, the LVCMOS output state is determined by *Table 8*. Control Registers are **RESET**.
ID[x]	56	I, Analog	Serial Control Bus Device ID Address Select — Optional Resistor to Ground and 10 kΩ pull-up to 1.8V rail. (See *Table 12*).
SCL	3	I, LVCMOS	Serial Control Bus Clock Input - Optional SCL requires an external pull-up resistor to V_{DDIO}.
SDA	2	I/O, LVCMOS Open Drain	Serial Control Bus Data Input / Output - Optional SDA requires an external pull-up resistor to V_{DDIO}.
BISTEN	44	I, LVCMOS w/ pull-down	BIST Enable Input — Optional BISTEN = 1, BIST is enabled BISTEN = 0, BIST is disabled
RES	47	I, LVCMOS w/ pull-down	***Reserved*** - tie LOW

Pin Name	Pin #	I/O, Type	Description
NC	1, 15, 16, 30, 31, 45, 46, 60		Not Connected Leave pin open (float)
FPD-Link II Serial Interface			
RIN+	49	I, LVDS	True Input. The input must be AC Coupled with a 100 nF capacitor.
RIN-	50	I, LVDS	Inverting Input. The input must be AC Coupled with a 100 nF capacitor.
CMF	51	I, Analog	Common-Mode Filter VCM center-tap is a virtual ground which may be ac-coupled to ground to increase receiver common mode noise immunity. Recommended value is 0.1µF or higher.
CMLOUTP	52	O, LVDS	Test Monitor Pin — EQ Waveform NC or connect to test point. Requires Serial Bus Control to enable.
CMLOUTN	53	O, LVDS	Test Monitor Pin — EQ Waveform NC or connect to test point. Requires Serial Bus Control to enable.
Power and Ground			
VDDL	29	Power	Logic Power, 1.8 V ±5%
VDDIR	48	Power	Input Power, 1.8 V ±5%
VDDR	43, 55	Power	RX High Speed Logic Power, 1.8 V ±5%
VDDSC	4, 58	Power	SSCG Power, 1.8 V ±5%
VDDPR	57	Power	PLL Power, 1.8 V ±5%
VDDCMLO	54	Power	RX High Speed Logic Power, 1.8 V ±5%
VDDIO	13, 24, 38	Power	LVCMOS I/O Power, **1.8 V ±5% OR 3.3 V ±10%** (V_{DDIO})
GND	DAP	Ground	DAP is the large metal contact at the bottom side, located at the center of the LLP package. **Connected to the ground plane** (GND) with at least 9 vias.

NOTE: 1 = HIGH, 0 = LOW

The VDD (V_{DDn} and V_{DDIO}) supply ramp should be faster than 1.5 ms with a monotonic rise. If slower then 1.5 ms then a capacitor on the PDB pin is needed to ensure PDB arrives after all the VDD have settled to the recommended operating voltage.

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage – V_{DDn} (1.8V)	−0.3V to +2.5V
Supply Voltage – V_{DDIO}	−0.3V to +4.0V
LVCMOS I/O Voltage	−0.3V to +(VDDIO + 0.3V)
Receiver Input Voltage	−0.3V to (VDD + 0.3V)
Driver Output Voltage	−0.3V to (VDD + 0.3V)
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
48L LLP Package	
Maximum Power Dissipation Capacity at 25°C	215mW
Derate above 25°C	$1/\theta_{JA}$ mW / °C
θ_{JA} *(based on 9 thermal vias)*	27.1 °C/W
θ_{JC} *(based on 9 thermal vias)*	4.5 °C/W
60L LLP Package	
Maximum Power Dissipation Capacity at 25°C	470mW
Derate above 25C	$1/\theta_{JA}$ mW / °C
θ_{JA} *(based on 9 thermal vias)*	24.6 °C/W
θ_{JC} *(based on 9 thermal vias)*	2.8 °C/W
ESD Rating (HBM)	≥±8 kV
ESD Rating (CDM)	≥±1 kV
ESD Rating (MM)	≥±250 V
ESD Rating (ISO10605), R_D = 2kΩ, C_S = 150pF or R_D = 2kΩ, C_S = 330pF or R_D = 330Ω, C_S = 150pF	
Air Discharge (D_{OUT+}, D_{OUT-})	≥±30 kV
Contact Discharge (D_{OUT+}, D_{OUT-})	≥±10 kV
Air Discharge (R_{IN+}, R_{IN-})	≥±30 kV
Contact Discharge (R_{IN+}, R_{IN-})	≥±10 kV
ESD Rating (ISO10605), R_D = 330Ω, C_S = 330pF	
Air Discharge (D_{OUT+}, D_{OUT-})	≥±15 kV
Contact Discharge (D_{OUT+}, D_{OUT-})	≥±10 kV
Air Discharge (R_{IN+}, R_{IN-})	≥±15 kV
Contact Discharge (R_{IN+}, R_{IN-})	≥±10 kV
ESD Rating (IEC 61000-4-2), R_D = 330Ω, C_S = 150pF	
Air Discharge (D_{OUT+}, D_{OUT-})	≥±25 kV
Contact Discharge (D_{OUT+}, D_{OUT-})	≥±8 kV
Air Discharge (R_{IN+}, R_{IN-})	≥±25 kV
Contact Discharge (R_{IN+}, R_{IN-})	≥±8 kV

For soldering specifications:
see product folder at www.national.com and
www.national.com/ms/MS/MS-SOLDERING.pdf

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{DDn})	1.71	1.8	1.89	V
LVCMOS Supply Voltage (V_{DDIO})	1.71	1.8	1.89	V
OR				
LVCMOS Supply Voltage (V_{DDIO})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−40	+25	+105	°C
PCLK Clock Frequency	5		65	MHz
Supply Noise (*Note 10*)			50	mV_{P-P}

Serializer DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (*Note 2*, *Note 3*, *Note 4*)

Symbol	Parameter	Conditions		Pin/Freq.	Min	Typ	Max	Units
LVCMOS INPUT DC SPECIFICATIONS								
V_{IH}	High Level Input Voltage	V_{DDIO} = 3.0 to 3.6V		R[7:0], G[7:0], B[7:0], HS, VS, DE, PCLK, PDB, VODSEL, RFB, CONFIG[1:0], BISTEN	2.2		V_{DDIO}	V
		V_{DDIO} = 1.71 to 1.89V			0.65* V_{DDIO}		V_{DDIO}	V
V_{IL}	Low Level Input Voltage	V_{DDIO} = 3.0 to 3.6V			GND		0.8	V
		V_{DDIO} = 1.71 to 1.89V			GND		0.35* V_{DDIO}	V
I_{IN}	Input Current	V_{IN} = 0V or V_{DDIO}	V_{DDIO} = 3.0 to 3.6V		−15	±1	+15	µA
			V_{DDIO} = 1.7 to 1.89V		−15	±1	+15	µA
LVDS DRIVER DC SPECIFICATIONS								
V_{OD}	Differential Output Voltage	R_L = 100Ω, De-emph = disabled, *Figure 2*	VODSEL = 0	DOUT+, DOUT-	±205	±280	±355	mV
			VODSEL = 1		±320	±420	±520	
V_{ODp-p}	Differential Output Voltage (DOUT+) – (DOUT-)		VODSEL = 0			560		mVp-p
			VODSEL = 1			840		mVp-p
ΔV_{OD}	Output Voltage Unbalance	R_L = 100Ω, De-emph = disabled, VODSEL = L				1	50	mV
V_{OS}	Offset Voltage – Single-ended At TP A & B, *Figure 1*	R_L = 100Ω, De-emph = disabled	VODSEL = 0			1.65		V
			VODSEL = 1			1.575		V
ΔV_{OS}	Offset Voltage Unbalance Single-ended At TP A & B, *Figure 1*	R_L = 100Ω, De-emph = disabled				1		mV
I_{OS}	Output Short Circuit Current	DOUT+/- = 0V, De-emph = disabled	VODSEL = 0			−36		mA
R_T	Internal Termination Resistor			DOUT+, DOUT-	80	100	120	Ω
SUPPLY CURRENT								
I_{DDT1}	Serializer Supply Current (includes load current) R_L = 100Ω, f = 65MHz	Checker Board Pattern, De-emph = 3KΩ VODSEL = H, *Figure 9*	V_{DD}= 1.89V	All V_{DD} pins		75	85	mA
I_{DDIOT1}			V_{DDIO}= 1.89V	V_{DDIO}		3	5	mA
			V_{DDIO} = 3.6V			11	15	mA
I_{DDT2}		Checker Board Pattern, De-emph = 6KΩ, VODSEL = L, *Figure 9*	V_{DD}= 1.89V	All V_{DD} pins		65	75	mA
I_{DDIOT2}			V_{DDIO}= 1.89V	V_{DDIO}		3	5	mA
			V_{DDIO} = 3.6V			11	15	mA
I_{DDZ}	Serializer Supply Current Power-down	PDB = 0V , (All other LVCMOS Inputs = 0V)	V_{DD}= 1.89V	All V_{DD} pins		40	1000	µA
I_{DDIOZ}			V_{DDIO}= 1.89V	V_{DDIO}		5	10	µA
			V_{DDIO} = 3.6V			10	20	µA

Deserializer DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
3.3 V I/O LVCMOS DC SPECIFICATIONS – V_{DDIO} = 3.0 to 3.6V							
V_{IH}	High Level Input Voltage		PDB, BISTEN	2.2		V_{DDIO}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
I_{IN}	Input Current	V_{IN} = 0V or V_{DDIO}		–15	±1	+15	µA
V_{OH}	High Level Output Voltage	I_{OH} = –2 mA, OS_PCLK/ DATA = L	R[7:0], G[7:0], B[7:0], HS,VS, DE, PCLK, LOCK, PASS	2.4	V_{DDIO}		V
V_{OL}	Low Level Output Voltage	I_{OL} = +2 mA, OS_PCLK/ DATA = L	R[7:0], G[7:0], B[7:0], HS, VS, DE,PCLK, LOCK, PASS		GND	0.4	V
I_{OS}	Output Short Circuit Current	V_{DDIO} = 3.3V V_{OUT} = 0V, OS_PCLK/ DATA = L/H	PCLK		36		mA
	Output Short Circuit Current	V_{DDIO} = 3.3V V_{OUT} = 0V, OS_PCLK/ DATA = L/H	Des Outputs		37		mA
I_{OZ}	TRI-STATE® Output Current	PDB = 0V, OSS_SEL = 0V, V_{OUT} = H	Outputs	–15		+15	uA
1.8 V I/O LVCMOS DC SPECIFICATIONS – V_{DDIO} = 1.71 to 1.89V							
V_{IH}	High Level Input Voltage		PDB, BISTEN	1.235		V_{DDIO}	V
V_{IL}	Low Level Input Voltage			GND		0.595	V
I_{IN}	Input Current	V_{IN} = 0V or V_{DDIO}		–15	±1	+15	µA
V_{OH}	High Level Output Voltage	I_{OH} = –2 mA, OS_PCLK/ DATA = L/H	R[7:0], G[7:0], B[7:0], HS, VS, DE, PCLK, LOCK, PASS	V_{DDIO} –0.45	V_{DDIO}		V
V_{OL}	Low Level Output Voltage	I_{OL} = +2 mA, OS_PCLK/ DATA = L/H		GND		0.45	V
I_{OS}	Output Short Circuit Current	VDDIO = 1.8V V_{OUT} = 0V, OS_PCLK/ DATA = L/H	PCLK		18		mA
		VDDIO = 1.8V V_{OUT} = 0V, OS_PCLK/ DATA = L/H	DATA		18		mA
I_{OZ}	TRI-STATE Output Current	PDB = 0V, OSS_SEL = 0V, V_{OUT} = 0V or V_{DDIO}	Outputs	-15		+15	µA

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
LVDS RECEIVER DC SPECIFICATIONS							
V_{TH}	Differential Input Threshold High Voltage	V_{CM} = +1.2V (Internal V_{BIAS})	RIN+, RIN-	+50			mV
V_{TL}	Differential Input Threshold Low Voltage			–50			mV
V_{CM}	Common Mode Voltage, Internal V_{BIAS}				1.2		V
I_{IN}	Input Current	V_{IN} = 0V or V_{DDIO}		-15		+15	µA
R_T	Internal Termination Resistor		RIN+, RIN-	80	100	120	Ω
CMLOUTP/N DRIVER OUTPUT DC SPECIFICATIONS – EQ TEST PORT							
V_{OD}	Differential Output Voltage	R_L = 100Ω,	CMLOUTP, CMLOUTN		542		mV
V_{OS}	Offset Voltage Single-ended	R_L = 100Ω			1.4		V
R_T	Internal Termination Resistor		CMLOUTP, CMLOUTN	80	100	120	Ω
SUPPLY CURRENT							
I_{DD1}	Deserializer Supply Current (includes load current)	Checker Board Pattern, OS_PCLK/DATA = H, EQ = 001, SSCG=ON CMLOUTP/N = enabled C_L = 4pF, *Figure 9*	All V_{DD} pins		93	110	mA
I_{DDIO1}			V_{DDIO}		33	45	mA
					62	75	mA
I_{DDZ}	Deserializer Supply Current Power Down	PDB = 0V, All other LVCMOS Inputs = 0V	All V_{DD} pins		40	3000	µA
I_{DDIOZ}			V_{DDIO}		5	50	µA
					10	100	µA

Recommended Serializer Timing for PCLK

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{TCP}	Transmit Input PCLK Period	5 MHz to 65 MHz, *Figure 4*	15.38	T	200	ns
t_{TCIH}	Transmit Input PCLK High Time		0.4T	0.5T	0.6T	ns
t_{TCIL}	Transmit Input PCLK Low Time		0.4T	0.5T	0.6T	ns
t_{CLKT}	PCLK Input Transition Time		0.5		2.4	ns
SSC_{IN}	PCLK Input – Spread Spectrum at PCLK = 65 MHz	fmod			35	kHz
		fdev			±2	%

Serializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{LHT}	Ser Output Low-to-High Transition Time, *Figure 3*	R_L = 100Ω, De-emphasis = disabled, VODSEL = 0		200		ps
		R_L = 100Ω, De-emphasis = disabled, VODSEL = 1		200		ps
t_{HLT}	Ser Output High-to-Low Transition Time, *Figure 3*	R_L = 100Ω, De-emphasis = disabled, VODSEL = 0		200		ps
		R_L = 100Ω, De-emphasis = disabled, VODSEL = 1		200		ps
t_{DIS}	Input Data - Setup Time, *Figure 4*	RGB[7:0], HS, VS, DE to PCLK	2			ns
t_{DIH}	Input Data - Hold Time, *Figure 4*	PCLK to RGB[7:0], HS, VS, DE	2			ns
t_{XZD}	Ser Ouput Active to OFF Delay, *Figure 6* (*Note 11*)			8	15	ns
t_{PLD}	Serializer PLL Lock Time, *Figure 5* (*Note 11*)	R_L = 100Ω		1.4	10	ms
t_{SD}	Serializer Delay - Latency, *Figure 7* (*Note 11*)	R_L = 100Ω		144*T	145 * T	ns
t_{DJIT}	Ser Output Total Jitter, *Figure 8*	R_L = 100Ω, De-Emph = disabled, RANDOM pattern PCLK = 65 MHz		0.28		UI
		R_L = 100Ω, De-Emph = disabled, RANDOM pattern PCLK = 43 MHz		0.27		UI
		R_L = 100Ω, De-Emph = disabled, RANDOM pattern PCLK = 5 MHz		0.35		UI
λ_{STXBW}	Serializer Jitter Transfer Function -3 dB Bandwidth	PCLK = 65 MHz		3		MHz
		PCLK = 43 MHz		2.3		MHz
		PCLK = 20 MHz		1.3		MHz
		PCLK = 5 MHz		650		kHz
δ_{STX}	Serializer Jitter Transfer Function Peaking	PCLK = 65 MHz		0.838		dB
		PCLK = 43 MHz		0.825		dB
		PCLK = 20 MHz		0.826		dB
		PCLK = 5 MHz		0.278		dB

Deserializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{RCP}	PCLK Output Period	$t_{RCP} = t_{TCP}$	PCLK	15.38	T	200	ns
t_{RDC}	PCLK Output Duty Cycle	SSCG=OFF, 5–65MHz	PCLK	43	50	57	%
		SSCG=ON, 5–20MHz		35	59	65	%
		SSCG=ON, 20–65MHz		40	53	60	%
t_{CLH}	LVCMOS Low-to-High Transition Time, *Figure 10*	V_{DDIO} = 1.8V, C_L = 4 pF	PCLK/RGB[7:0], HS, VS, DE		2.1		ns
		V_{DDIO} = 3.3V C_L = 4 pF			2.0		ns
t_{CHL}	LVCMOS High-to-Low Transition Time, *Figure 10*	V_{DDIO} = 1.8V C_L = 4 pF, OS_PCLK/DATA = L	PCLK/RGB[7:0], HS, VS, DE		1.6		ns
		V_{DDIO} = 3.3V C_L = 4 pF, OS_PCLK/DATA = H			1.5		ns
t_{ROS}	Data Valid before PCLK – Set Up Time, *Figure 14*	V_{DDIO} = 1.71 to 1.89V or 3.0 to 3.6V C_L = 4pF (lumped load)	RGB[7:0], HS, VS, DE	0.27	0.45		T
t_{ROH}	Data Valid after PCLK – Hold Time, *Figure 14*	V_{DDIO} = 1.71 to 1.89V or 3.0 to 3.6V C_L = 4pF (lumped load)	RGB[7:0], HS, VS, DE	0.40	0.55		T
t_{DDLT}	Deserializer Lock Time, *Figure 13*	SSC[3:0] = 0000 (OFF), (*Note 6*)	PCLK = 5MHz		3		ms
		SSC[3:0] = 0000 (OFF), (*Note 6*)	PCLK = 65 MHz		4		ms
		SSC[3:0] = ON, (*Note 6*)	PCLK = 5MHz		30		ms
		SSC[3:0] = ON, (*Note 6*)	PCLK = 65 MHz		6		ms
t_{DD}	Des Delay - Latency, *Figure 11*	SSC[3:0] = 0000 (OFF), (*Note 6*)			139*T	140*T	ns
t_{DPJ}	Des Period Jitter	SSC[3:0] = OFF, (*Note 8*), (*Note 11*)	PCLK = 5MHz		975	1700	ps
			PCLK = 10MHz		500	1000	ps
			PCLK = 65 MHz		550	1250	ps
t_{DCCJ}	Des Cycle-to-Cycle Jitter	SSC[3:0] = OFF, (*Note 9*), (*Note 11*)	PCLK = 5MHz		675	1150	ps
			PCLK = 10MHz		375	900	ps
			PCLK = 65 MHz		500	1150	ps
t_{IJT}	Des Input Jitter Tolerance, *Figure 16*	EQ = OFF, SSCG = OFF, PCLK = 65MHz	for jitter freq < 2MHz		0.9		UI
			for jitter freq > 6MHz		0.5		UI

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
BIST Mode							
t_{PASS}	BIST PASS Valid Time, BISTEN = 1, *Figure 17*				1	10	us
SSCG Mode							
f_{DEV}	Spread Spectrum Clocking Deviation Frequency	Under typical conditions	PCLK = 5 to 65 MHz, SSC[3:0] = ON	±0.5		±2	%
f_{MOD}	Spread Spectrum Clocking Modulation Frequency	Under typical conditions	PCLK = 5 to 65 MHz, SSC[3:0] = ON	8		100	kHz

Recommended Timing for the Serial Control Bus

Over 3.3V supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{SCL}	SCL Clock Frequency	Standard Mode	>0		100	kHz
		Fast Mode	>0		400	kHz
t_{LOW}	SCL Low Period	Standard Mode	4.7			us
		Fast Mode	1.3			us
t_{HIGH}	SCL High Period	Standard Mode	4.0			us
		Fast Mode	0.6			us
$t_{HD;STA}$	Hold time for a start or a repeated start condition, *Figure 18*	Standard Mode	4.0			us
		Fast Mode	0.6			us
$t_{SU:STA}$	Set Up time for a start or a repeated start condition, *Figure 18*	Standard Mode	4.7			us
		Fast Mode	0.6			us
$t_{HD;DAT}$	Data Hold Time, *Figure 18*	Standard Mode	0		3.45	us
		Fast Mode	0		0.9	us
$t_{SU;DAT}$	Data Set Up Time, *Figure 18*	Standard Mode	250			ns
		Fast Mode	100			ns
$t_{SU;STO}$	Set Up Time for STOP Condition, *Figure 18*	Standard Mode	4.0			us
		Fast Mode	0.6			us
t_{BUF}	Bus Free Time Between STOP and START, *Figure 18*	Standard Mode	4.7			us
		Fast Mode	1.3			us
t_r	SCL & SDA Rise Time, *Figure 18*	Standard Mode			1000	ns
		Fast Mode			300	ns
t_f	SCL & SDA Fall Time, *Figure 18*	Standard Mode			300	ns
		Fast mode			300	ns

DC and AC Serial Control Bus Characteristics

Over 3.3V supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Level	SDA and SCL	2.2		V_{DDIO}	V
V_{IL}	Input Low Level Voltage	SDA and SCL	GND		0.8	V
V_{HY}	Input Hysteresis			>50		mV
V_{OL}	Output Low Level Voltage, (*Note 11*)	SDA, IOL = 1.25mA	0		0.4	V
I_{in}		SDA or SCL, Vin = V_{DDIO} or GND	-15		+15	µA
t_R	SDA RiseTime – READ	SDA, RPU = 10kΩ, Cb ≤ 400pF		40		ns
t_F	SDA Fall Time – READ			25		ns
$t_{SU;DAT}$	Set Up Time — READ			520		ns
$t_{HD;DAT}$	Hold Up Time — READ			55		ns
t_{SP}	Input Filter			50		ns
C_{in}	Input Capacitance	SDA or SCL		<5		pF

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 2: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 3: Typical values represent most likely parametric norms at V_{DD} = 3.3V, Ta = +25 degC, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 4: Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except VOD, ΔVOD, VTH and VTL which are differential voltages.

Note 5: When the Serializer output is at TRI-STATE the Deserializer will lose PLL lock. Resynchronization / Relock must occur before data transfer require t_{PLD}

Note 6: t_{PLD} and t_{DDLT} is the time required by the serializer and deserializer to obtain lock when exiting power-down state with an active PCLK.

Note 7: UI – Unit Interval is equivalent to one serialized data bit width (1UI = 1 / 28*PCLK). The UI scales with PCLK frequency.

Note 8: t_{DPJ} is the maximum amount the period is allowed to deviate over many samples.

Note 9: t_{DCCJ} is the maximum amount of jitter between adjacent clock cycles.

Note 10: Supply noise testing was done with minimum capacitors on the PCB. A sinusoidal signal is AC coupled to the V_{DDn} (1.8V) supply with amplitude = 100 mVp-p measured at the device V_{DDn} pins. Bit error rate testing of input to the Ser and output of the Des with 10 meter cable shows no error when the noise frequency on the Ser is less than 750 kHz. The Des on the other hand shows no error when the noise frequency is less than 400 kHz.

Note 11: Specification is guaranteed by characterization and is not tested in production.

Note 12: Specification is guaranteed by design and is not tested in production.

AC Timing Diagrams and Test Circuits

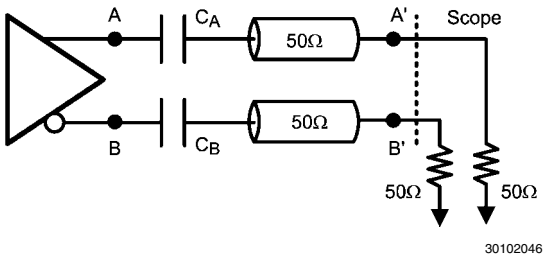


FIGURE 1. Serializer Test Circuit

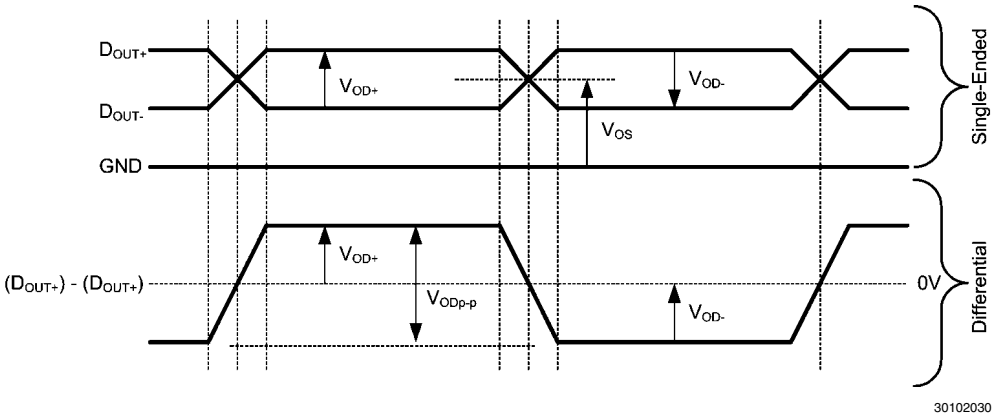


FIGURE 2. Serializer Output Waveforms

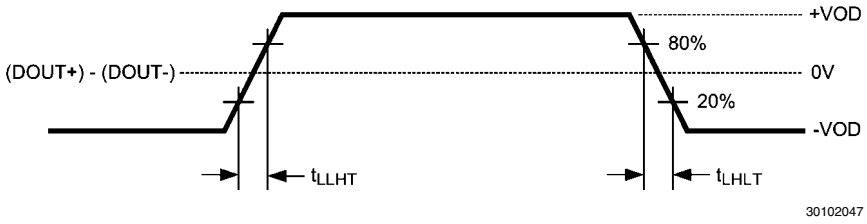


FIGURE 3. Serializer Output Transition Times

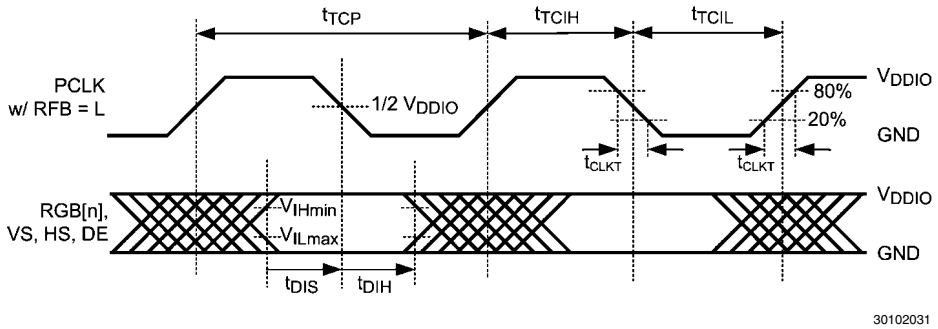


FIGURE 4. Serializer Input PCLK Waveform and Set and Hold Times

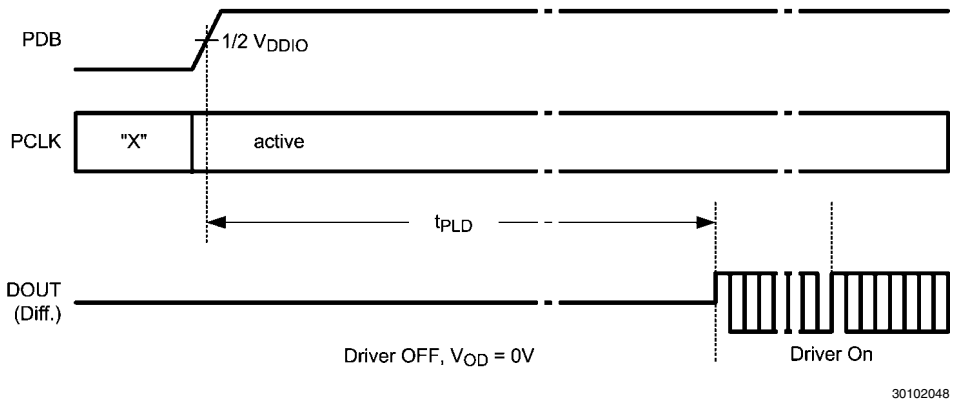


FIGURE 5. Serializer Lock Time

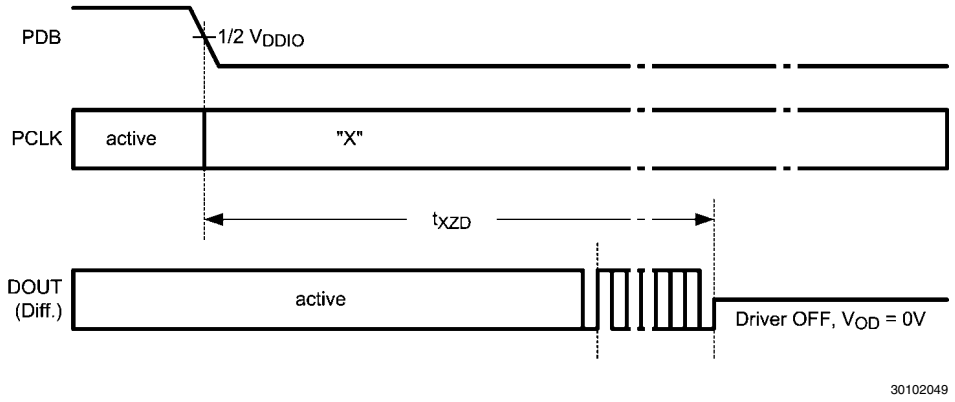


FIGURE 6. Serializer Disable Time

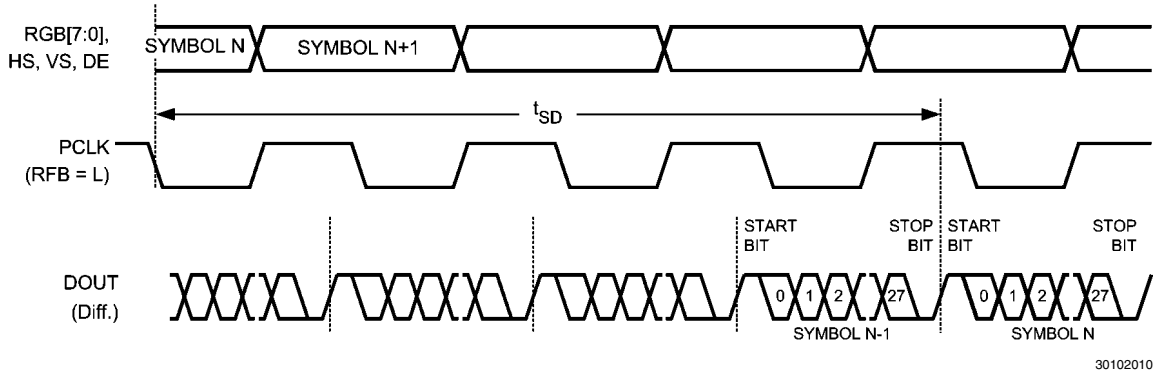


FIGURE 7. Serializer Latency Delay

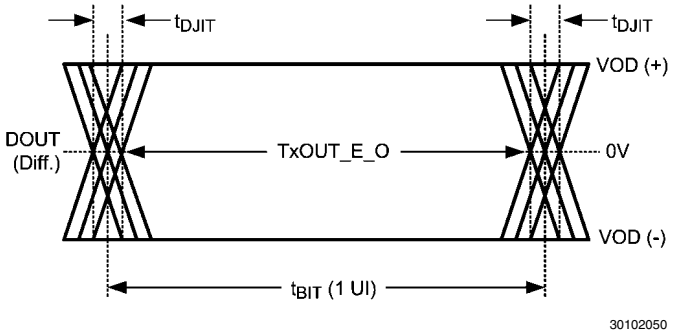


FIGURE 8. Serializer Output Jitter

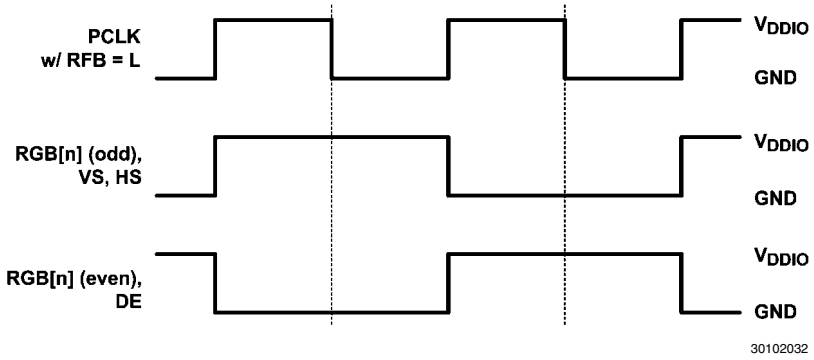


FIGURE 9. Checkerboard Data Pattern

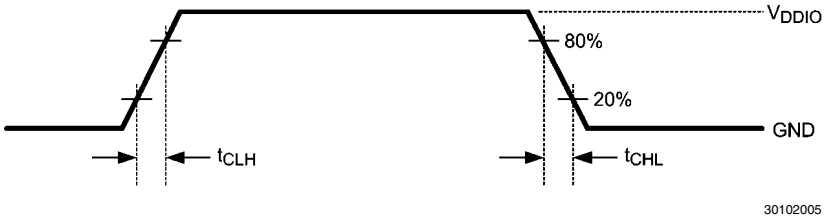


FIGURE 10. Deserializer LVCMOS Transition Times

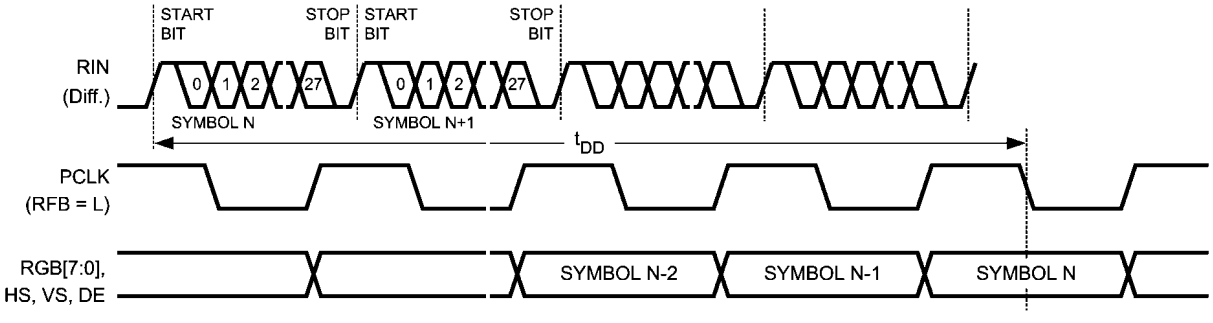


FIGURE 11. Deserializer Delay – Latency

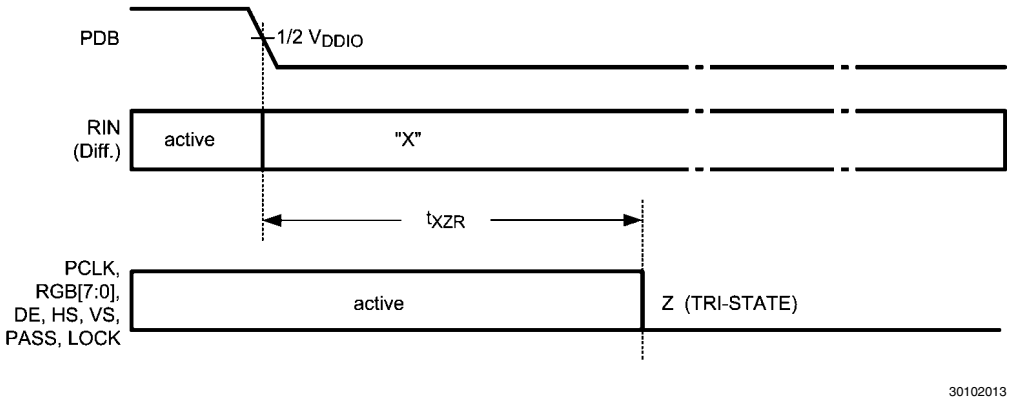


FIGURE 12. Deserializer Disable Time (OSS_SEL = 0)

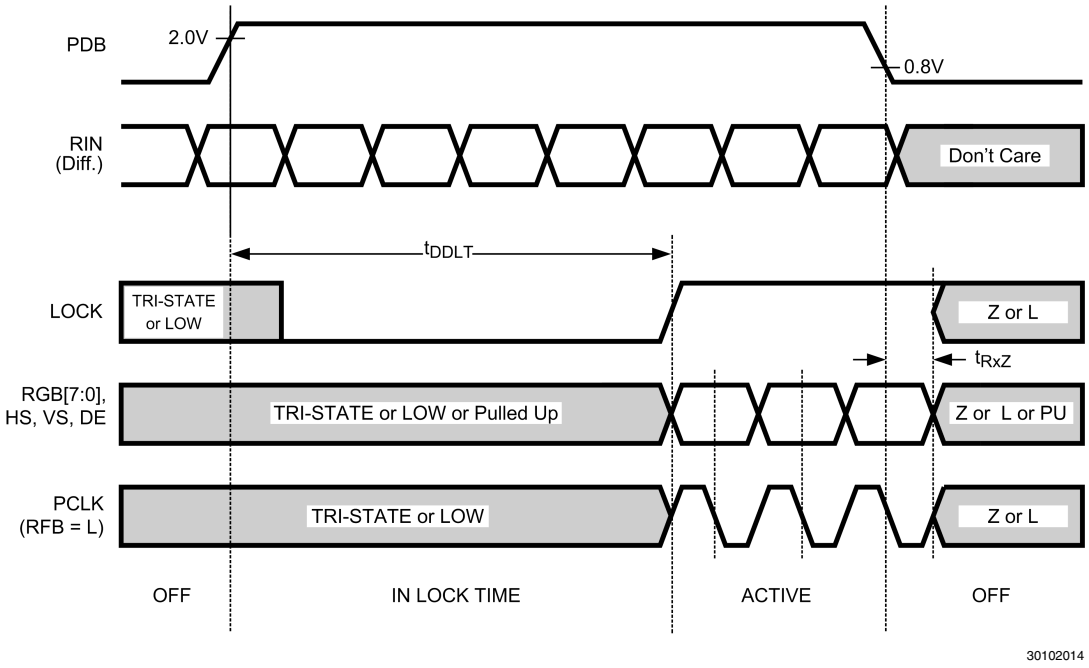


FIGURE 13. Deserializer PLL Lock Times and PDB TRI-STATE Delay

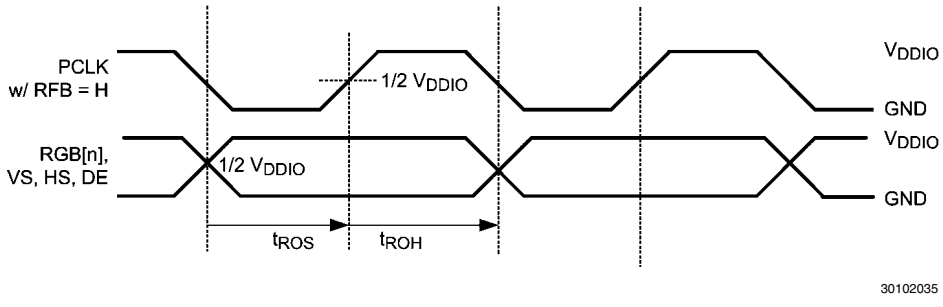


FIGURE 14. Deserializer Output Data Valid (Setup and Hold) Times with SSCG = Off

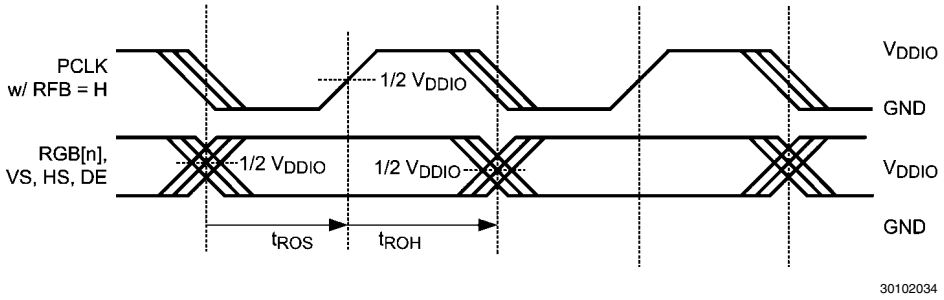


FIGURE 15. Deserializer Output Data Valid (Setup and Hold) Times with SSCG = On

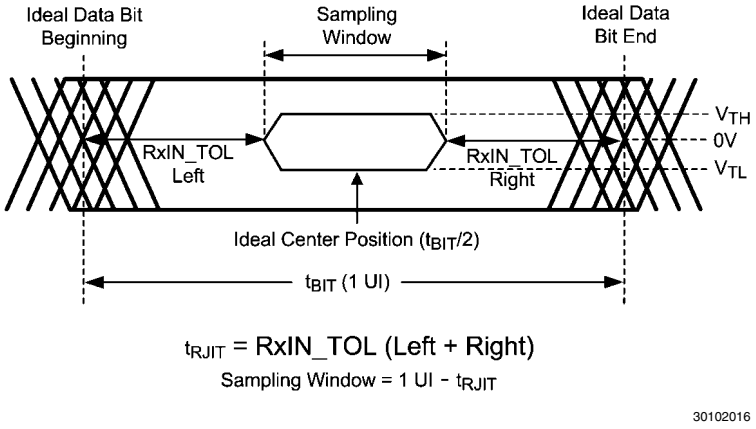


FIGURE 16. Receiver Input Jitter Tolerance

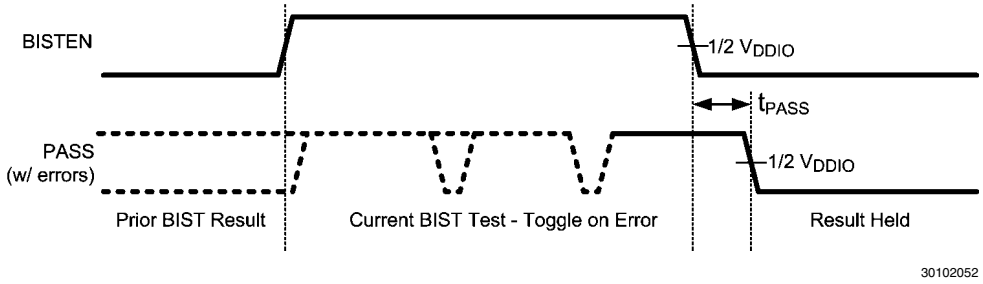


FIGURE 17. BIST PASS Waveform

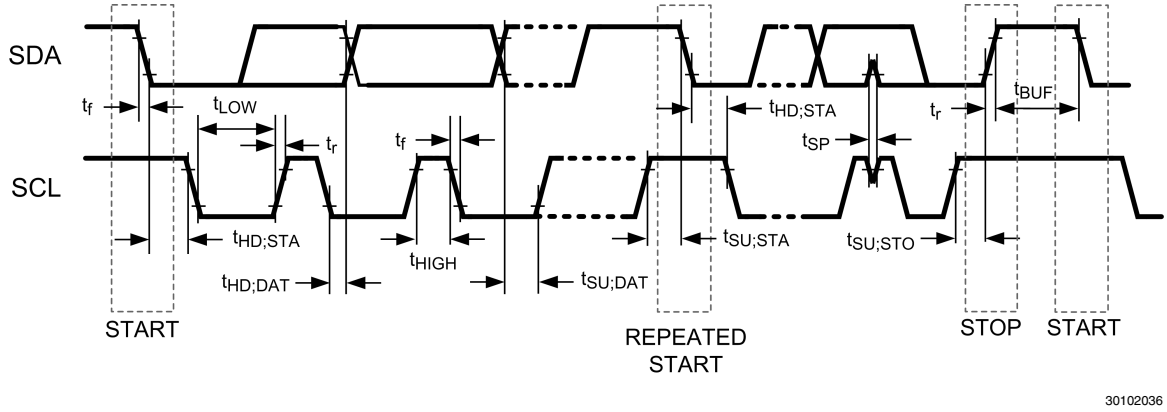


FIGURE 18. Serial Control Bus Timing Diagram

Functional Description

The DS90UR905Q / DS90UR906Q chipset transmits and receives 27-bits of data (24-high speed color bits and 3 low speed video control signals) over a single serial FPD-Link II pair operating at 140Mbps to 1.82Gbps. The serial stream also contains an embedded clock, video control signals and the DC-balance information which enhances signal quality and supports AC coupling. The pair is intended for use with each other but is backward compatible with previous generations of FPD-Link II as well.

The Des can attain lock to a data stream without the use of a separate reference clock source, which greatly simplifies system complexity and overall cost. The Des also synchronizes to the Ser regardless of the data pattern, delivering true automatic "plug and lock" performance. It can lock to the incoming serial stream without the need of special training patterns or sync characters. The Des recovers the clock and data by extracting the embedded clock information, validating and then deserializing the incoming data stream providing a parallel LVCMOS video bus to the display.

The DS90UR905Q / DS90UR906Q chipset can operate in 24-bit color depth (with VS,HS,DE encoded in the DCA bit) or in 18-bit color depth (with VS, HS, DE encoded in DCA or mapped into the high-speed data bits). In 18–bit color applications, the three video signals maybe sent encoded via the DCA bit (restrictions apply) or sent as "data bits" along with three additional general purpose signals.

Block Diagrams for the chipset are shown at the beginning of this datasheet.

Data Transfer

The DS90UR905Q / DS90UR906Q chipset will transmit and receive a pixel of data in the following format: C1 and C0 represent the embedded clock in the serial stream. C1 is always HIGH and C0 is always LOW. b[23:0] contain the scrambled RGB data. DCB is the DC-Balanced control bit. DCB is used to minimize the short and long-term DC bias on the signal lines. This bit determines if the data is unmodified or inverted. DCA is used to validate data integrity in the embedded data stream and can also contain encoded control (VS,HS,DE). Both DCA and DCB coding schemes are generated by the Ser and decoded by the Des automatically. *Figure 19 illustrates** the serial stream per PCLK cycle. ****Note: The figure only illustrates the bits but does not actually represent the bit location as the bits are scrambled and balanced continuously.*

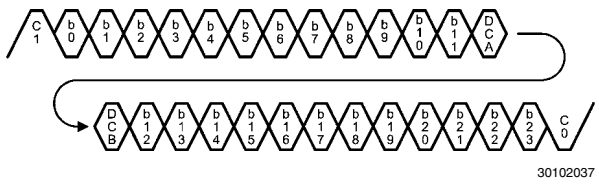


FIGURE 19. FPD-Link II Serial Stream (905/906)

Ser & Des OPERATING MODES AND BACKWARD COMPATIBILITY (CONFIG[1:0])

The DS90UR905Q / DS90UR906Q chipset is also backward compatible with previous generations of FPD-Link II. Configuration modes are provided for backwards compatibility with the DS90C241 / DS90C124 FPD-Link II Generation 1, and also the DS90UR241 / DS90UR124 FPD-Link II Generation 2 chipset by setting the respective mode with the CONFIG [1:0] pins on the Ser or Des as shown in *Table 1* and *Table 2*. The selection also determine whether the Video Control Signal filter feature is enabled or disabled in Normal mode. This feature may be controlled by pin or by Register.

TABLE 1. DS90UR905Q Ser Modes

CON FIG1	CON FIG0	Mode	Des Device
L	L	Normal Mode, Control Signal Filter disabled	DS90UR906Q
L	H	Normal Mode, Control Signal Filter enabled	DS90UR906Q
H	L	Backwards Compatible GEN2	DS90UR124, DS99R124
H	H	Backwards Compatible GEN1	DS90C124

TABLE 2. DS90UR906Q Des Modes

CON FIG1	CON FIG0	Mode	Ser Device
L	L	Normal Mode, Control Signal Filter disabled	DS90UR905Q
L	H	Normal Mode, Control Signal Filter enabled	DS90UR905Q
H	L	Backwards Compatible GEN2	DS90UR241
H	H	Backwards Compatible GEN1	DS90C241

VIDEO CONTROL SIGNAL FILTER — Ser and Des

When operating the devices in Normal Mode, the Video Control Signals (DE, HS, VS) have the following restrictions:

- Normal Mode with Control Signal Filter Enabled:
  DE and HS — Only 2 transitions per 130 clock cycles are transmitted, the transition pulse must be 3 PCLK or longer.
- Normal Mode with Control Signal Filter Disabled:
  DE and HS — Only 2 transitions per 130 clock cycles are transmitted, no restriction on minimum transition pulse.
- VS — Only 1 transition per 130 clock cycles are transmitted, minimum pulse width is 130 clock cycles.

Video Control Signals are defined as low frequency signals with limited transitions. Glitches of a control signal can cause a visual display error. This feature allows for the chipset to validate and filter out any high frequency noise on the control signals. See *Figure 20*.

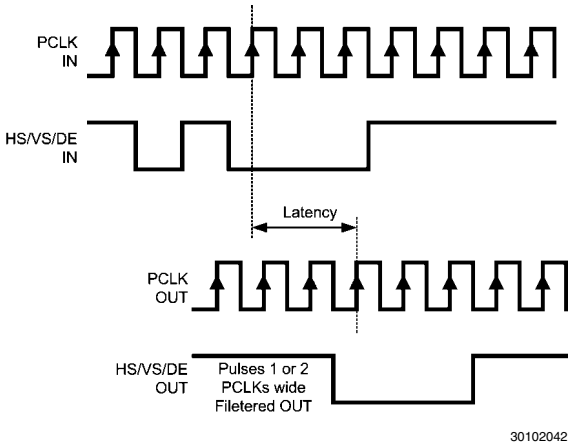


FIGURE 20. Video Control Signal Filter Waveform

SERIALIZER FUNCTIONAL DESCRIPTION

The Ser converts a wide parallel input bus to a single serial output data stream, and also acts as a signal generator for the chipset Built In Self Test (BIST) mode. The device can be configured via external pins or through the optional serial control bus. The Ser features enhance signal quality on the link by supporting: a selectable VOD level, a selectable de-emphasis signal conditioning and also the FPD-Link II data coding that provides randomization, scrambling, and DC Balanacing of the video data. The Ser includes multiple features to reduce EMI associated with display data transmission. This includes the randomization and scrambling of the data and also the system spread spectrum PCLK support. The Ser features power saving features with a sleep mode, auto stop clock feature, and optional LVCMOS (1.8 V) parallel bus compatibility.

See also the Functional Description of the chipset's serial control bus and BIST modes.

EMI Reduction Features

Ser — Spread Spectrum Compatibility

The Ser PCLK is capable of tracking spread spectrum clocking (SSC) from a host source. The PCLK will accept spread spectrum tracking up to 35kHz modulation and ±0.5, ±1 or ±2% deviations (center spread). The maximum conditions for the PCLK input are: a modulation frequency of 35kHz and amplitude deviations of ±2% (4% total).

Signal Quality Enhancers

Ser — VOD Select (VODSEL)

The Ser differential output voltage may be increased by setting the VODSEL pin High. When VODSEL is Low, the VOD is at the standard (default) level. When VODSEL is High, the DC VOD is increased in level. The increased VOD is useful in extremely high noise environments and also on extra long cable length applications. When using de-emphasis it is recommended to set VODSEL = H to avoid excessive signal attenuation especially with the larger de-emphasis settings. This feature may be controlled by the external pin or by register.

TABLE 3. Differential Output Voltage

Input	Effect	
VODSEL	VOD mV	VOD mVp-p
H	±420	840
L	±280	560

Ser — De-Emphasis (De-Emph)

The De-Emph pin controls the amount of de-emphasis beginning one full bit time after a logic transition that the Ser drives. This is useful to counteract loading effects of long or lossy cables. This pin should be left open for standard switching currents (no de-emphasis) or if controlled by register. De-emphasis is selected by connecting a resistor on this pin to ground, with R value between 0.5 kΩ to 1 MΩ, or by register setting. When using De-Emphasis it is recommended to set VODSEL = H.

TABLE 4. De-Emphasis Resistor Value

Resistor Value (kΩ)	De-Emphasis Setting
Open	Disabled
0.6	- 12 dB
1.0	- 9 dB
2.0	- 6 dB
5.0	- 3 dB

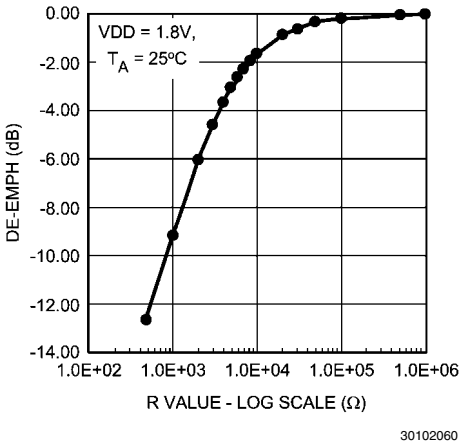


FIGURE 21. De-Emph vs. R value

Power Saving Features

Ser — Power Down Feature (PDB)

The Ser has a PDB input pin to ENABLE or POWER DOWN the device. This pin is controlled by the host and is used to save power, disabling the link when the display is not needed. In the POWER DOWN mode, the high-speed driver outputs are both pulled to VDD and present a 0V VOD state. Note – in POWER DOWN, the optional Serial Bus Control Registers are **RESET**.

Ser — Stop Clock Feature

The Ser will enter a low power SLEEP state when the PCLK is stopped. A STOP condition is detected when the input clock frequency is less than 3 MHz. The clock should be held at a static Low or high state. When the PCLK starts again, the Ser will then lock to the valid input PCLK and then transmits the RGB data to the Des. Note – in STOP CLOCK SLEEP, the optional Serial Bus Control Registers values are **RETAINED**.

1.8V or 3.3V VDDIO Operation

The Ser parallel bus and Serial Bus Interface can operate with 1.8 V or 3.3 V levels (V_{DDIO}) for host compatibility. The 1.8 V levels will offer lower noise (EMI) and also a system power savings.

Ser — Pixel Clock Edge Select (RFB)

The RFB pin determines the edge that the data is latched on. If RFB is High, input data is latched on the Rising edge of the PCLK. If RFB is Low, input data is latched on the Falling edge of the PCLK. Ser and Des maybe set differently. This feature may be controlled by the external pin or by register.

Optional Serial Bus Control

Please see the following section on the optional Serial Bus Control Interface.

Optional BIST Mode

Please see the following section on the chipset BIST mode for details.

DESERIALIZER FUNCTIONAL DESCRIPTION

The Des converts a single input serial data stream to a wide parallel output bus, and also provides a signal check for the chipset Built In Self Test (BIST) mode. The device can be configured via external pins and strap pins or through the optional serial control bus. The Des features enhance signal quality on the link by supporting: an equalizer input and also the FPD-Link II data coding that provides randomization, scrambling, and DC balanacing of the data. The Des includes multiple features to reduce EMI associated with display data transmission. This includes the randomization and scrambling of the data and also the output spread spectrum clock generation (SSCG) support. The Des features power saving features with a power down mode, and optional LVCMOS (1.8 V) interface compatibility.

Signal Quality Enhancers

Des — Input Equalizer Gain (EQ)

The Des can enable receiver input equalization of the serial stream to increase the eye opening to the Des input. Note this function cannot be seen at the RxIN+/- input but can be observed at the serial test port (CMLOUTP/N) enabled via the Serial Bus control registers. The equalization feature may be controlled by the external pin or by register.

TABLE 5. Receiver Equalization Configuration Table

INPUTS				Effect
EQ3	EQ2	EQ1	EQ0	
L	L	L	H	~1.5 dB
L	L	H	H	~3 dB
L	H	L	H	~4.5 dB
L	H	H	H	~6 dB
H	L	L	H	~7.5 dB
H	L	H	H	~9 dB
H	H	L	H	~10.5 dB
H	H	H	H	~12 dB
X	X	X	L	OFF*

* Default Setting is EQ = Off

EMI Reduction Features

Des — Output Slew (OS_PCLK/DATA)

The parallel bus outputs (RGB[7:0], VS, HS, DE and PCLK) of the Des feature a selectable output slew. The DATA ((RGB [7:0], VS, HS, DE) are controlled by strap pin or register bit OS_DATA. The PCLK is controlled by strap pin or register bit OS_PCLK. When the OS_PCLK/DATA = HIGH, the maximum slew rate is selected. When the OS_PCLK/DATA = LOW, the minimum slew rate is selected. Use the higher slew rate setting when driving longer traces or a heavier capacitive load.

Des — Common Mode Filter Pin (CMF) — Optional

The Des provides access to the center tap of the internal termination. A capacitor may be placed on this pin for additional common-mode filtering of the differential pair. This can be useful in high noise environments for additional noise rejection capability. A 0.1µF capacitor may be connected to this pin to Ground.

Des — SSCG Generation — Optional

The Des provides an internally generated spread spectrum clock (SSCG) to modulate its outputs. Both clock and data outputs are modulated. This will aid to lower system EMI. Output SSCG deviations to ±2.0% (4% total) at up to 35kHz modulations nominally are available. See *Table 6*. This feature may be controlled by external STRAP pins or by register.

TABLE 6. SSCG Configuration (LF_MODE = L) — Des Output

SSC[3:0] Inputs LF_MODE = L (20 - 65 MHz)				Result	
SSC3	SSC2	SSC1	SSC0	fdev (%)	fmod (kHz)
L	L	L	L	Off	Off
L	L	L	H	±0.5	PCLK/2168
L	L	H	L	±1.0	
L	L	H	H	±1.5	
L	H	L	L	±2.0	
L	H	L	H	±0.5	PCLK/1300
L	H	H	L	±1.0	
L	H	H	H	±1.5	
H	L	L	L	±2.0	
H	L	L	H	±0.5	PCLK/868
H	L	H	L	±1.0	
H	L	H	H	±1.5	
H	H	L	L	±2.0	
H	H	L	H	±0.5	PCLK/650
H	H	H	L	±1.0	
H	H	H	H	±1.5	

TABLE 7. SSCG Configuration (LF_MODE = H) — Des Output

SSC[3:0] Inputs LH_MODE = H (5 - 20 MHz)				Result	
SSC3	SSC2	SSC1	SSC0	fdev (%)	fmod (kHz)
L	L	L	L	Off	Off
L	L	L	H	±0.5	PCLK/620
L	L	H	L	±1.0	
L	L	H	H	±1.5	
L	H	L	L	±2.0	
L	H	L	H	±0.5	PCLK/370
L	H	H	L	±1.0	
L	H	H	H	±1.5	
H	L	L	L	±2.0	
H	L	L	H	±0.5	PCLK/258
H	L	H	L	±1.0	
H	L	H	H	±1.5	
H	H	L	L	±2.0	
H	H	L	H	±0.5	PCLK/192
H	H	H	L	±1.0	
H	H	H	H	±1.5	

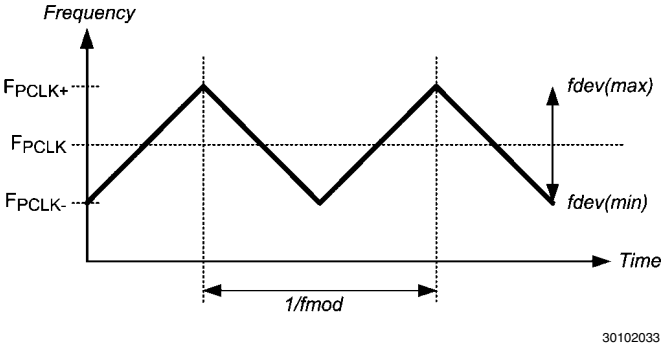


FIGURE 22. SSCG Waveform

1.8V or 3.3V VDDIO Operation

The Des parallel bus and Serial Bus Interface can operate with 1.8 V or 3.3 V levels (V_{DDIO}) for target (Display) compatibility. The 1.8 V levels will offer a lower noise (EMI) and also a system power savings.

Power Saving Features

Des — PowerDown Feature (PDB)

The Des has a PDB input pin to ENABLE or POWER DOWN the device. This pin can be controlled by the system to save power, disabling the Des when the display is not needed. An auto detect mode is also available. In this mode, the PDB pin is tied High and the Des will enter POWER DOWN when the serial stream stops. When the serial stream starts up again, the Des will lock to the input stream and assert the LOCK pin and output valid data. In POWER DOWN mode, the Data and PCLK output states are determined by the OSS_SEL status.

Note – in POWER DOWN, the optional Serial Bus Control Registers are **RESET**.

Des — Stop Stream SLEEP Feature

The Des will enter a low power SLEEP state when the input serial stream is stopped. A STOP condition is detected when the embedded clock bits are not present. When the serial stream starts again, the Des will then lock to the incoming signal and recover the data. Note – in STOP STREAM SLEEP, the optional Serial Bus Control Registers values are **RETAINED**.

Des — CLOCK-DATA RECOVERY STATUS FLAG (LOCK) and OUTPUT STATE SELECT (OSS_SEL)

When PDB is driven HIGH, the CDR PLL begins locking to the serial input and LOCK goes from TRI-STATE to LOW (depending on the value of the OSS_SEL setting). After the DS90UR906Q completes its lock sequence to the input serial data, the LOCK output is driven HIGH, indicating valid data and clock recovered from the serial input is available on the parallel bus and PCLK outputs. The PCLK output is held at its current state at the change from OSC_CLK (if this is enabled via OSC_SEL) to the recovered clock (or vice versa).

If there is a loss of clock from the input serial stream, LOCK is driven Low and the state of the RGB/VS/HS/DE outputs are based on the OSS_SEL setting (STRAP PIN configuration or register).

Des — Oscillator Output — Optional

The Des provides an optional PCLK output when the input clock (serial stream) has been lost. This is based on an internal oscillator. The frequency of the oscillator may be selected. This feature may be controlled by the external pin or by register. See *Table 9* and *Table 10*.

TABLE 8. OSS_SEL and PDB Configuration — Des Outputs

INPUTS			OUTPUTS			
Serial Input	**PDB**	**OSS_SEL**	**PCLK**	**RGB/HS/VS/DE**	**LOCK**	**PASS**
X	L	X	Z	Z	Z	Z
Static	H	L	L	L	L	L
Static	H	H	Z	Z*	L	L
Active	H	X	Active	Active	H	H
*NOTE — If pin is strapped HIGH, output will be pulled up						

TABLE 9. OSC (Oscillator) Mode — Des Output

INPUTS	OUTPUTS			
Embedded PCLK	**PCLK**	**RGB/HS/VS/DE**	**LOCK**	**PASS**
NOTE *	OSC Output	L	L	L
Present	Toggling	Active	H	H
* NOTE — Absent and OSC_SEL ≠ 000				

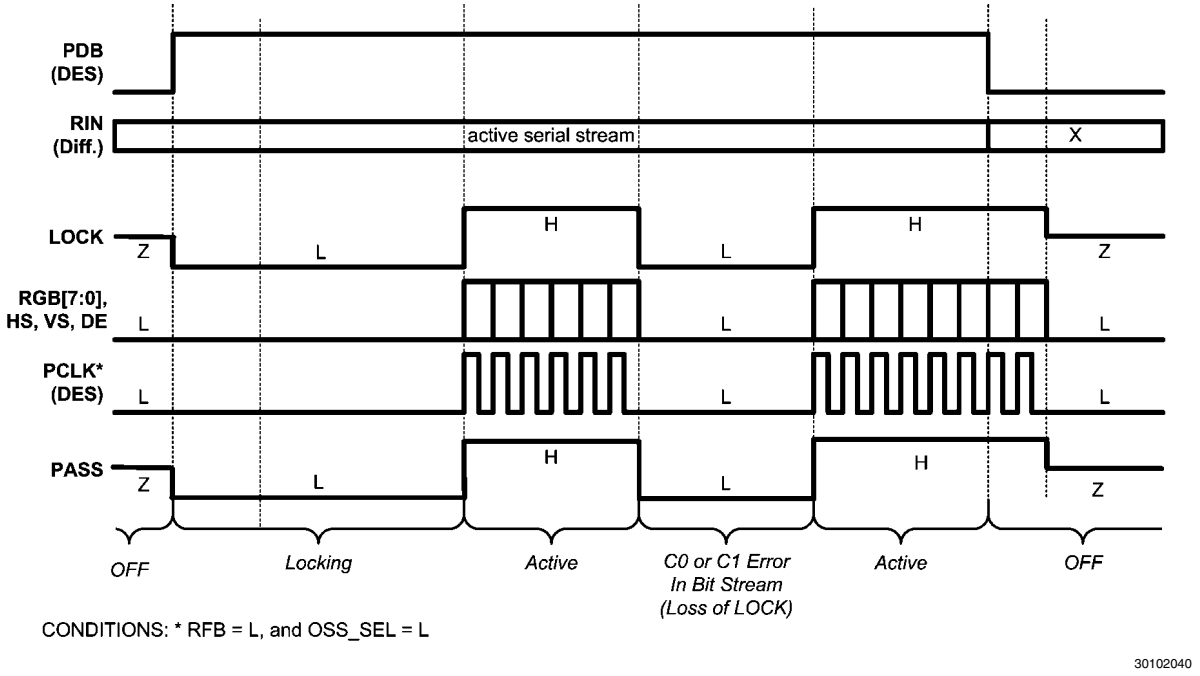


FIGURE 23. Des Outputs with Output State Select Low (OSS_SEL = L)

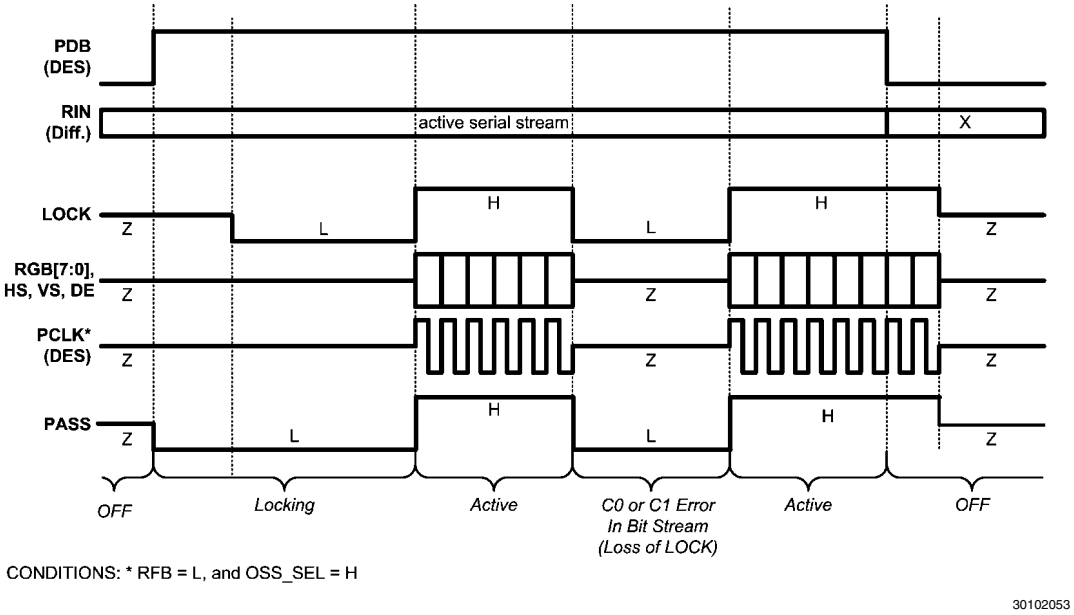
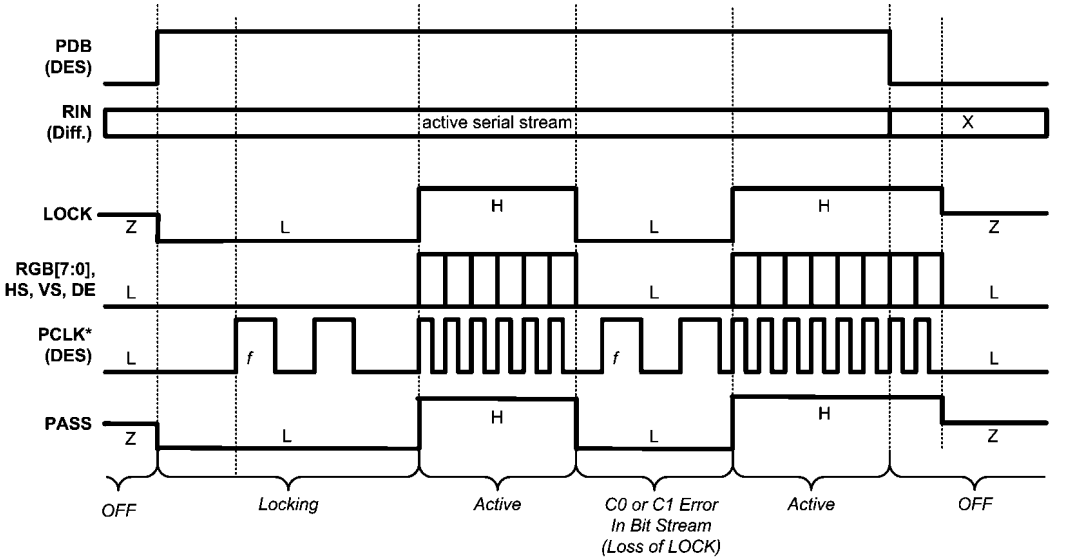


FIGURE 24. Des Outputs with Output State Select High (OSS_SEL = H)

TABLE 10. OSC_SEL (Oscillator) Configuration

OSC_SEL[2:0] INPUTS			PCLK Oscillator Output
OSC_SEL2	OSC_SEL1	OSC_SEL0	
L	L	L	Off – Feature Disabled – Default
L	L	H	50 MHz ±40%
L	H	L	25 MHz ±40%
L	H	H	16.7 MHz ±40%
H	L	L	12.5 MHz ±40%
H	L	H	10 MHz ±40%
H	H	L	8.3 MHz ±40%
H	H	H	6.3 MHz ±40%



CONDITIONS: * RFB = L, OSS_SEL = H , and OSC_SEL not equal to 000.

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FIGURE 25. Des Outputs with Output State High and PCLK Output Oscillator Option Enabled

Des — OP_LOW — Optional

The OP_ LOW feature is used to hold the LVCMOS outputs (except the LOCK output) at a LOW state. The user must toggle the OP_LOW Set/Reset register bit to release the outputs to the normal toggling state. Note that the release of the outputs can only occur when LOCK is HIGH. When the OP_LOW feature is enabled, anytime LOCK = LOW, the LVCMOS outputs will toggle to a LOW state again. The OP_ LOW strap pin feature is assigned to output PASS pin 42.

Restrictions on other straps:

1) Other straps should not be used in order to keep RGB[7:0], HS, VS, DE, and PCLK at a true LOW state. Other features should be selected thru I2C.

2) OSS_SEL function is not available when O/P_LOW is tied H.

Outputs RGB[7:0], HSYNC, VSYNC, DE, and PCLK are in TRI-STATE before PDB toggles HIGH because the OP_LOW strap value has not been recognized until the DS90UR906 powers up. *Figure 26* shows the user controlled release of OP_LOW and automatic reset of OP_LOW set on the falling edge of LOCK. *Figure 27* shows the user controlled release of OP_LOW and manual reset of OP_LOW set. Note manual reset of OP_LOW can only occur when LOCK is H.

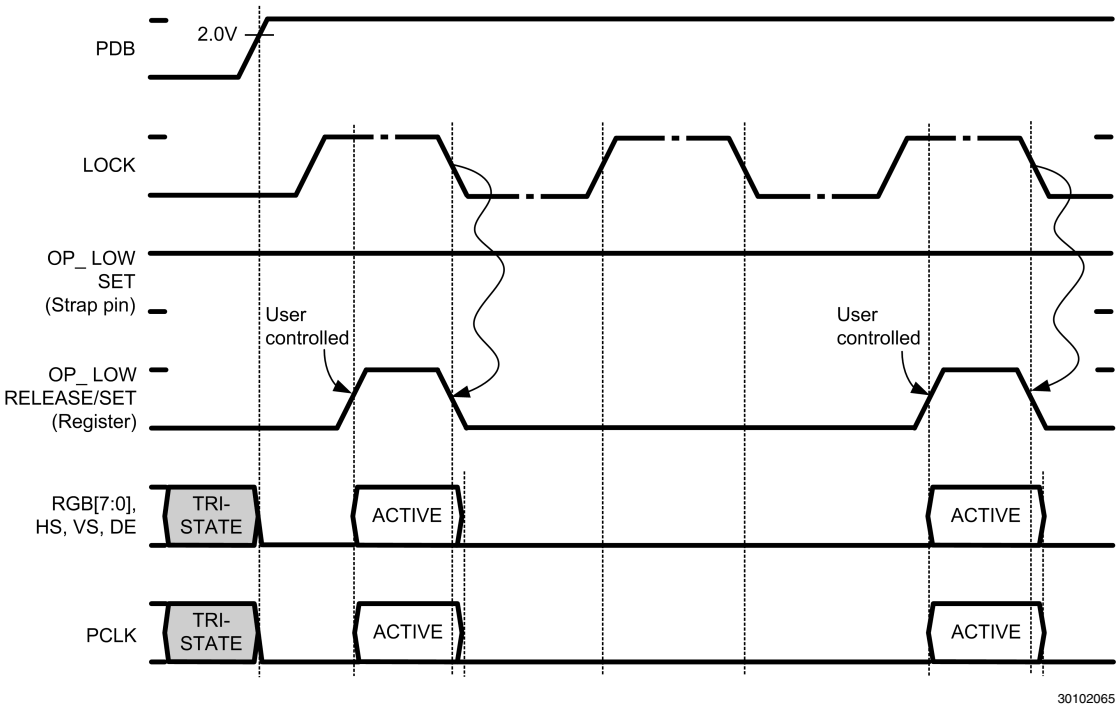


FIGURE 26. OP_LOW Auto Set

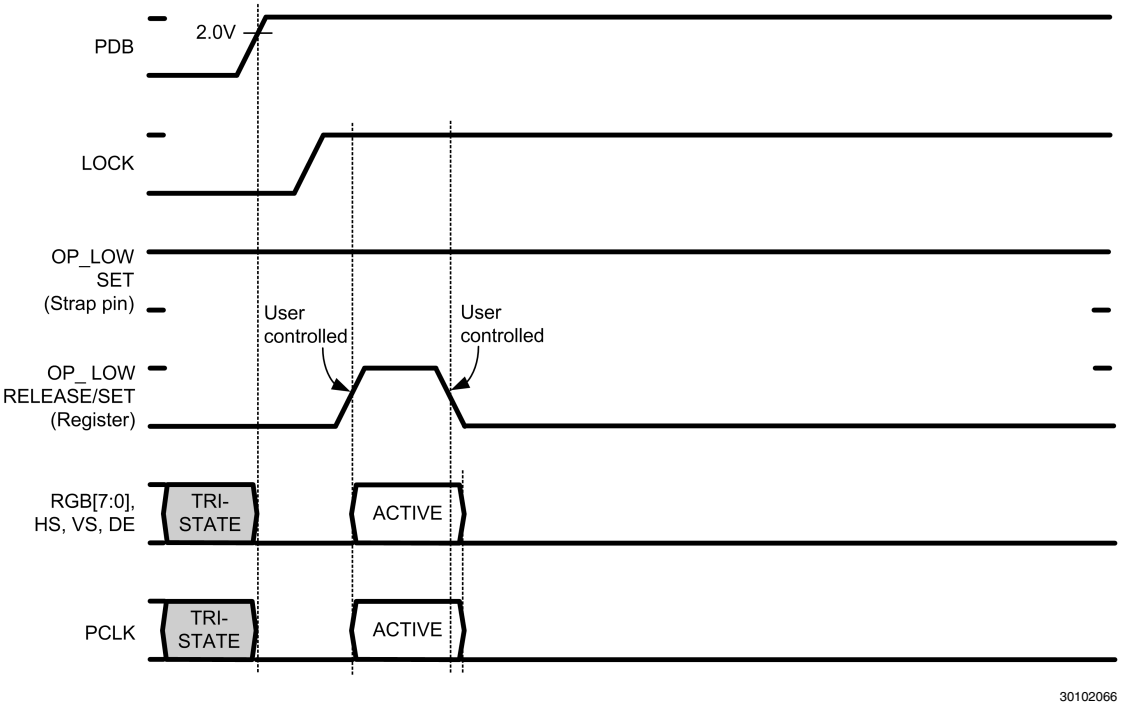


FIGURE 27. OP_LOW Manual Set/Reset

Des — Pixel Clock Edge Select (RFB)

The RFB pin determines the edge that the data is strobed on. If RFB is High, output data is strobed on the Rising edge of the PCLK. If RFB is Low, data is strobed on the Falling edge of the PCLK. This allows for inter-operability with downstream devices. The Des output does not need to use the same edge as the Ser input. This feature may be controlled by the external pin or by register.

Des — Control Signal Filter — Optional

The Des provides an optional Control Signal (VS, HS, DE) filter that monitors the three video control signals and eliminates any pulses that are 1 or 2 PCLKs wide. Control signals must be 3 pixel clocks wide (in its HIGH or LOW state, regardless of which state is active). This is set by the CONFIG [1:0] or by the Control Register. This feature may be controlled by the external pin or by Register.

Des — Low Frequency Optimization (LF_Mode)

This feature may be controlled by the external pin or by Register.

Des — Map Select

This feature may be controlled by the external pin or by Register.

TABLE 11. Map Select Configuration

INPUTS		Effect
MAPSEL1	MAPSEL0	
L	L	Bit 4, Bit 5 on LSB **DEFAULT**
L	H	LSB 0 or 1
H	H or L	LSB 0

Des — Strap Input Pins

Configuration of the device maybe done via configuration input pins and the STRAP input pins, or via the Serial Control Bus. The STRAP input pins share select parallel bus output pins. They are used to load in configuration values during the initial power up sequence of the device. Only a pull-up on the pin is required when a HIGH is desired. By default the pad has an internal pull down, and will bias Low by itself. The recommended value of the pull up is 10 kΩ to V_{DDIO}; open (NC) for Low, no pull-down is required (internal pull-down). If using the Serial Control Bus, no pull ups are required.

Optional Serial Bus Control

Please see the following section on the optional Serial Bus Control Interface.

Optional BIST Mode

Please see the following section on the chipset BIST mode for details.

Built In Self Test (BIST)

An optional At-Speed Built In Self Test (BIST) feature supports the testing of the high-speed serial link. This is useful in the prototype stage, equipment production, in-system test and also for system diagnostics. In the BIST mode only a input clock is required along with control to the Ser and Des BISTEN input pins. The Ser outputs a test pattern (PRBS7) and drives the link at speed. The Des detects the PRBS7 pattern and monitors it for errors. A PASS output pin toggles to flag any payloads that are received with 1 to 24 errors. Upon completion of the test, the result of the test is held on the PASS output until reset (new BIST test or Power Down). A high on PASS indicates NO ERRORS were detected. A Low on PASS indicates one or more errors were detected. The duration of the test is controlled by the pulse width applied to the Des BISTEN pin. During the BIST duration the deserializer data outputs toggle with a checkerboard pattern.

Inter-operability is supported between this FPD-Link II device and all FPD-Link II generations (Gen 1/2/3) — see respective datasheets for details on entering BIST mode and control.

Sample BIST Sequence

See *Figure 28* for the BIST mode flow diagram.

Step 1: Place the DS90UR905Q Ser in BIST Mode by setting Ser BISTEN = H. For the DS90UR905Q Ser or DS99R421 FPD-Link II Ser BIST Mode is enabled via the BISTEN pin. For the DS90C241 Ser or DS90UR241 Ser, BIST mode is enetered by setting all the input data of the device to Low state. A PCLK is required for all the Ser options. When the Des detects the BIST mode pattern and command (DCA and DCB code) the RGB and control signal outputs are shut off.

Step 2: Place the DS90UR906Q Des in BIST mode by setting the BISTEN = H. The Des is now in the BIST mode and checks the incoming serial payloads for errors. If an error in the payload (1 to 24) is detected, the PASS pin will switch low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.

Step 3: To Stop the BIST mode, the Des BISTEN pin is set Low. The Des stops checking the data and the final test result is held on the PASS pin. If the test ran error free, the PASS output will be High. If there was one or more errors detected, the PASS output will be Low. The PASS output state is held until a new BIST is run, the device is RESET, or Powered Down. The BIST duration is user controlled by the duration of the BISTEN signal.

Step 4: To return the link to normal operation, the Ser BISTEN input is set Low. The Link returns to normal operation.

Figure 29 shows the waveform diagram of a typical BIST test for two cases. Case 1 is error free, and Case 2 shows one with multiple errors. In most cases it is difficult to generate errors due to the robustness of the link (differential data transmission etc.), thus they may be introduced by greatly extending the cable length, faulting the interconnect, reducing signal condition enhancements (De-Emphasis, VODSEL, or Rx Equalization).

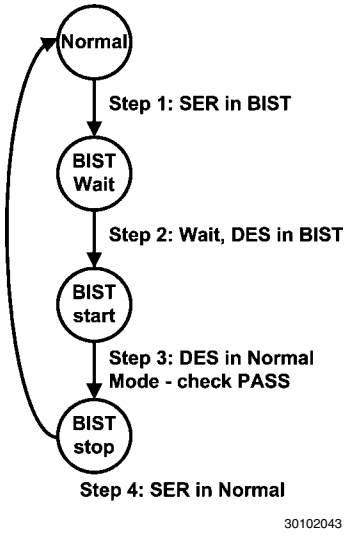


FIGURE 28. BIST Mode Flow Diagram

BER Calculations

It is possible to calculate the approximate Bit Error Rate (BER). The following is required:

- Pixel Clock Frequency (MHz)
- BIST Duration (seconds)
- BIST test Result (PASS)

The BER is less than or equal to one over the product of 24 times the PCLK rate times the test duration. If we assume a 65MHz PCLK, a 10 minute (600 second) test, and a PASS, the BERT is ≤ 1.07 X 10E-12

The BIST mode runs a check on the data payload bits. The LOCK pin also provides a link status. It the recovery of the C0 and C1 bits does not reconstruct the expected clock signal, the LOCK pin will switch Low. The combination of the LOCK and At-Speed BIST PASS pin provides a powerful tool for system evaluation and performance monitoring.

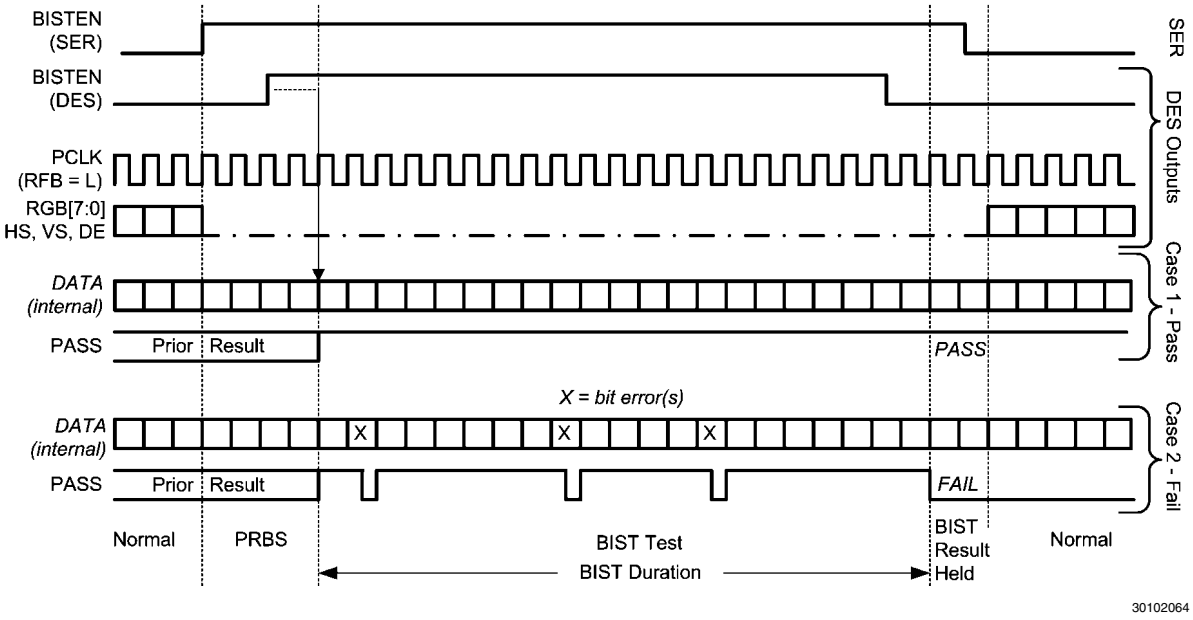


FIGURE 29. BIST Waveforms

Optional Serial Bus Control

The Ser and Des may also be configured by the use of a serial control bus that is I2C protocol compatible. By default, the I2C reg_0x00'h is set to 00'h and all configuration is set by control/strap pins. A write of 01'h to reg_0x00'h will enable/allow configuration by registers; this will override the control/strap pins. Multiple devices may share the serial control bus since multiple addresses are supported. See *Figure 30*.

The serial bus is comprised of three pins. The SCL is a Serial Bus Clock Input. The SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pull up resistor to V_{DDIO}. For most applications a 4.7 k pull up resistor to V_{DDIO} may be used. The resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled High, or driven Low.

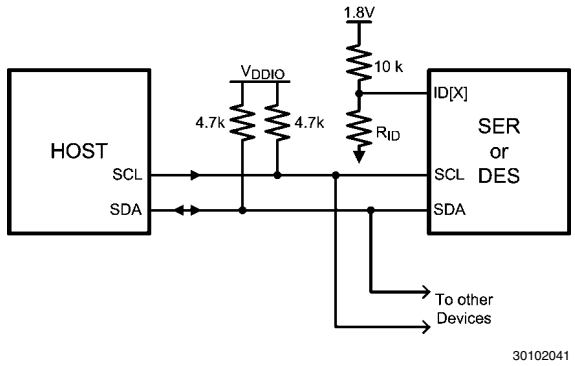


FIGURE 30. Serial Control Bus Connection

The third pin is the ID[X] pin. This pin sets one of four possible device addresses. Two different connections are possible. The pin may be pulled to V_{DD} (**1.8V, NOT V_{DDIO}**)) with a 10 kΩ resistor; or a 10 kΩ pull up resistor (to V_{DD} **1.8V, NOT V_{DDIO}**)) and a pull down resistor of the recommended value to set other three possible addresses may be used. See *Table 12* for the Ser and *Table 13* for the Des. Do not tie ID[x] directly to VSS.

The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SCL transitions Low while SDA is High. A STOP occurs when SDA transition High while SCL is also HIGH. See *Figure 31*

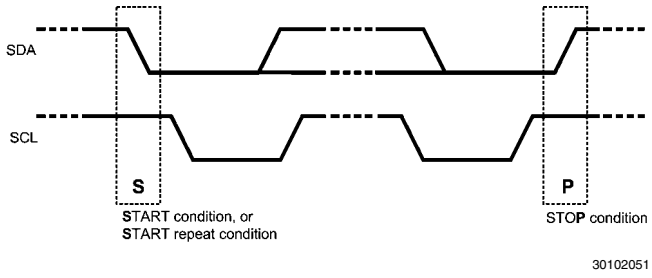


FIGURE 31. START and STOP Conditions

To communicate with a remote device, the host controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit (ACK). If a slave on the bus is addressed correctly, it Acknowledges (ACKs) the master by driving the SDA bus low. If the address doesn't match a device's slave address, it Not-acknowledges (NACKs) the master by letting SDA be pulled High. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a Start condition or a Repeated Start condition. All communication on the bus ends with a Stop condition. A READ is shown in *Figure 32* and a WRITE is shown in *Figure 33*.

Note: During initial power-up, a delay of 10ms will be required before the I2C will respond.

If the Serial Bus is not required, the three pins may be left open (NC).

TABLE 12. ID[x] Resistor Value – DS90UR905Q Ser

Resistor RID* kΩ (5% tol)	Address 7'b	Address 8'b 0 appended (WRITE)
0.47	7b' 110 1001 (h'69)	8b' 1101 0010 (h'D2)
2.7	7b' 110 1010 (h'6A)	8b' 1101 0100 (h'D4)
8.2	7b' 110 1011 (h'6B)	8b' 1101 0110 (h'D6)
Open	7b' 110 1110 (h'6E)	8b' 1101 1100 (h'DC)

TABLE 13. ID[x] Resistor Value – DS90UR906Q Des

Resistor RID* kΩ (5% tol)	Address 7'b	Address 8'b 0 appended (WRITE)
0.47	7b' 111 0001 (h'71)	8b' 1110 0010 (h'E2)
2.7	7b' 111 0010 (h'72)	8b' 1110 0100 (h'E4)
8.2	7b' 111 0011 (h'73)	8b' 1110 0110 (h'E6)
Open	7b' 111 0110 (h'76)	8b' 1110 1100 (h'EC)

*Note: RID ≠ 0 ohm, do not connect directly to VSS (GND), this is not a valid address.

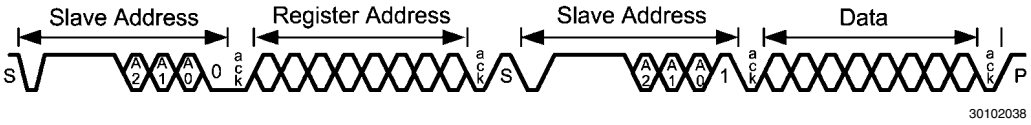


FIGURE 32. Serial Control Bus — READ

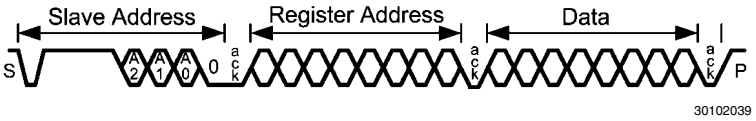


FIGURE 33. Serial Control Bus — WRITE

TABLE 14. SERIALIZER — Serial Bus Control Registers

ADD (dec)	ADD (hex)	Register Name	Bit(s)	R/W	Default (bin)	Function	Description
0	0	Ser Config 1	7	R/W	0	***Reserved***	***Reserved***
			6	R/W	0	***Reserved***	***Reserved***
			5	R/W	0	VODSEL	0: Low 1: High
			4	R/W	0	RFB	0: Data latched on Falling edge of PCLK 1: Data latched on Rising edge of PCLK
			3:2	R/W	00	CONFIG	00: Control Signal Filter Disabled 01: Control Signal Filter Enabled 10: DS90UR124, DS99R124 Mode 11: DS90C124 Mode
			1	R/W	0	SLEEP	Note – not the same function as $\overline{\text{PowerDown}}$ (PDB) 0: normal mode 1: Sleep Mode – **Register settings retained.**
			0	R/W	0	REG	0: Configurations set from control pins 1: Configuration set from registers (except I2C_ID)
1	1	Device ID	7	R/W	0	REG ID	0: Address from ID[x] Pin 1: Address from Register
			6:0	R/W	1101 000	ID[X]	Serial Bus Device ID, Four IDs are: 7b '1101 001 (h'69) 7b '1101 010 (h'6A) 7b '1101 011 (h'6B) 7b '1101 110 (h'6E) All other addresses are ***Reserved***.
2	2	De-Emphasis Control	7:5	R/W	000	De-E Setting	000: set by external Resistor 001: -1 dB 010: -2 dB 011: -3.3 dB 100: -5 dB 101: -6.7 dB 110: -9 dB 111: -12 dB
			4	R/W	0	De-E EN	0: De-Emphasis Enabled 1: De-Emphasis Disabled
			3:0	R/W	000	***Reserved***	***Reserved***

TABLE 15. DESERIALIZER — Serial Bus Control Registers

ADD (dec)	ADD (hex)	Register Name	Bit(s)	R/W	Default (bin)	Function	Description
0	0	Des Config 1	7	R/W	0	LFMODE	0: 20 to 65 MHz Operation 1: 5 to 20 MHz Operation
			6	R/W	0	OS_PCLK	0: Normal PCLK Output Slew 1: Increased PCLK Slew
			5	R/W	0	OS_DATA	0: Normal DATA OUTPUT Slew 1: Increased Data Slew
			4	R/W	0	RFB	0: Data strobed on Falling edge of PCLK 1: Data strobed on Rising edge of PCLK
			3:2	R/W	00	CONFIG	00: Normal Mode, Control Signal Filter Disabled 01: Normal Mode, Control Signal Filter Enabled 10: Backwards Compatible (DS90UR241) 11: Backwards Compatible (DS90C241)
			1	R/W	0	SLEEP	Note – not the same function as $\overline{\text{PowerDown}}$ (PDB) 0: normal mode 1: Sleep Mode – **Register settings retained.**
			0	R/W	0	REG Control	0: Configurations set from control pins / STRAP pins 1: Configurations set from registers (except I2C_ID)
1	1	Slave ID	7	R/W	0		0: Address from ID[X] Pin 1: Address from Register
			6:0	R/W	1110 000	ID[X]	Serial Bus Device ID, Four IDs are: 7b '1110 001 (h'71) 7b '1110 010 (h'72) 7b '1110 011 (h'73) 7b '1110 110 (h'76) All other addresses are ***Reserved***.
2	2	Des Features 1	7	R/W	0	OP_LOW Release/Set	0: set outputs state LOW (except LOCK) 1: release output LOW state, outputs toggling normally Note: This register only works during LOCK = 1.
			6	R/W	0	OSS_SEL	Output Sleep State Select 0: PCLK/RGB[7:0]/HS/VS/DE = L, LOCK = Normal, PASS = H 1: PCLK/RGB[7:0]/HS/VS/DE = Tri-State, LOCK = Normal, PASS = H
			5:4	R/W	00	MAP_SEL	Special for Backwards Compatible Mode 00: bit 4, 5 on LSB 01: LSB zero if all data is zero; one if any data is one 10: LSB zero 11: LSB zero
			3	R/W	0	OP_LOW strap bypass	0: strap will determine whether OP_LOW feature is ON or OFF 1: Turns OFF OP_LOW feature
			2:0	R/W	00	OSC_SEL	000: OFF 001: 50 MHz ±40% 010: 25 MHz ±40% 011: 16.7 MHz ±40% 100: 12.5 MHz ±40% 101: 10 MHz ±40% 110: 8.3 MHz ±40% 111: 6.3 MHz ±40%

ADD (dec)	ADD (hex)	Register Name	Bit(s)	R/W	Default (bin)	Function	Description
3	3	Des Features 2	7:5	R/W	000	EQ Gain	000: ~1.625 dB 001: ~3.25 dB 010: ~4.87 dB 011: ~6.5 dB 100: ~8.125 dB 101: ~9.75 dB 110: ~11.375 dB 111: ~13 dB
			4	R/W	0	EQ Enable	0: EQ = disabled 1: EQ = enabled
			3:0	R/W	0000	SSC	**IF LF_MODE = 0, then**: 000: SSCG OFF 0001: fdev = ±0.5%, fmod = PCLK/2168 0010: fdev = ±1.0%, fmod = PCLK/2168 0011: fdev = ±1.5%, fmod = PCLK/2168 0100: fdev = ±2.0%, fmod = PCLK/2168 0101: fdev = ±0.5%, fmod = PCLK/1300 0110: fdev = ±1.0%, fmod = PCLK/1300 0111: fdev = ±1.5%, fmod = PCLK/1300 1000: fdev = ±2.0%, fmod = PCLK/1300 1001: fdev = ±0.5%, fmod = PCLK/868 1010: fdev = ±1.0%, fmod = PCLK/868 1011: fdev = ±1.5%, fmod = PCLK/868 1100: fdev = ±2.0%, fmod = PCLK/868 1101: fdev = ±0.5%, fmod = PCLK/650 1110: fdev = ±1.0%, fmod = PCLK/650 1111: fdev = ±1.5%, fmod = PCLK/650 **IF LF_MODE = 1, then**: 000: SSCG OFF 0001: fdev = ±0.5%, fmod = PCLK/620 0010: fdev = ±1.0%, fmod = PCLK/620 0011: fdev = ±1.5%, fmod = PCLK/620 0100: fdev = ±2.0%, fmod = PCLK/620 0101: fdev = ±0.5%, fmod = PCLK/370 0110: fdev = ±1.0%, fmod = PCLK/370 0111: fdev = ±1.5%, fmod = PCLK/370 1000: fdev = ±2.0%, fmod = PCLK/370 1001: fdev = ±0.5%, fmod = PCLK/258 1010: fdev = ±1.0%, fmod = PCLK/258 1011: fdev = ±1.5%, fmod = PCLK/258 1100: fdev = ±2.0%, fmod = PCLK/258 1101: fdev = ±0.5%, fmod = PCLK/192 1110: fdev = ±1.0%, fmod = PCLK/192 1111: fdev = ±1.5%, fmod = PCLK/192
4	4	CMLOUT Config	7	R/W	0	Repeater Enable	0: Output CMLOUTP/N = disabled 1: Output CMLOUTP/N = enabled
			6:0	R/W	0000 000	***Reserved***	***Reserved***

Applications Information

DISPLAY APPLICATION

The DS90UR905Q/906Q chipset is intended for interface between a host (graphics processor) and a Display. It supports an 24-bit color depth (RGB888) and up to 1024 X 768 display formats. In a RGB888 application, 24 color bits (R[7:0], G[7:0], B[7:0]), Pixel Clock (PCLK) and three control bits (VS, HS and DE) are supported across the serial link with PCLK rates from 5 to 65 MHz. The chipset may also be used in 18-bit color applications. In this application three to six general purpose signals may also be sent from host to display.

The Des is expected to be located close to its target device. The interconnect between the Des and the target device is typically in the 1 to 3 inch separation range. The input capacitance of the target device is expected to be in the 5 to 10 pF range. Care should be taken on the PCLK output trace as this signal is edge sensitive and strobes the data. It is also assumed that the fanout of the Des is one. If additional loads need to be driven, a logic buffer or mux device is recommended.

TYPICAL APPLICATION CONNECTION

Figure 34 shows a typical application of the DS90UR905Q Ser in Pin control mode for a 65 MHz 24-bit Color Display Application. The LVDS outputs require 100 nF AC coupling capacitors to the line. The line driver includes internal termination. Bypass capacitors are placed near the power supply pins. At a minimum, four 0.1 µF capacitors and a 4.7 µF capacitor should be used for local device bypassing. System GPO (General Purpose Output) signals control the PDB and BISTEN pins. In this application the RFB pin is tied Low to latch data on the falling edge of the PCLK. The application assumes the companion Des (DS90UR906Q) therefore the configuration pins are also both tied Low. In this example the cable is long, therefore the VODSEL pin is tied High and a De-Emphasis value is selected by the resistor R1. The interface to the host is with 1.8 V LVCMOS levels, thus the VDDIO pin is connected also to the 1.8V rail. The Optional Serial Bus Control is not used in this example, thus the SCL, SDA and ID[x] pins are left open. A delay cap is placed on the PDB signal to delay the enabling of the device until power is stable.

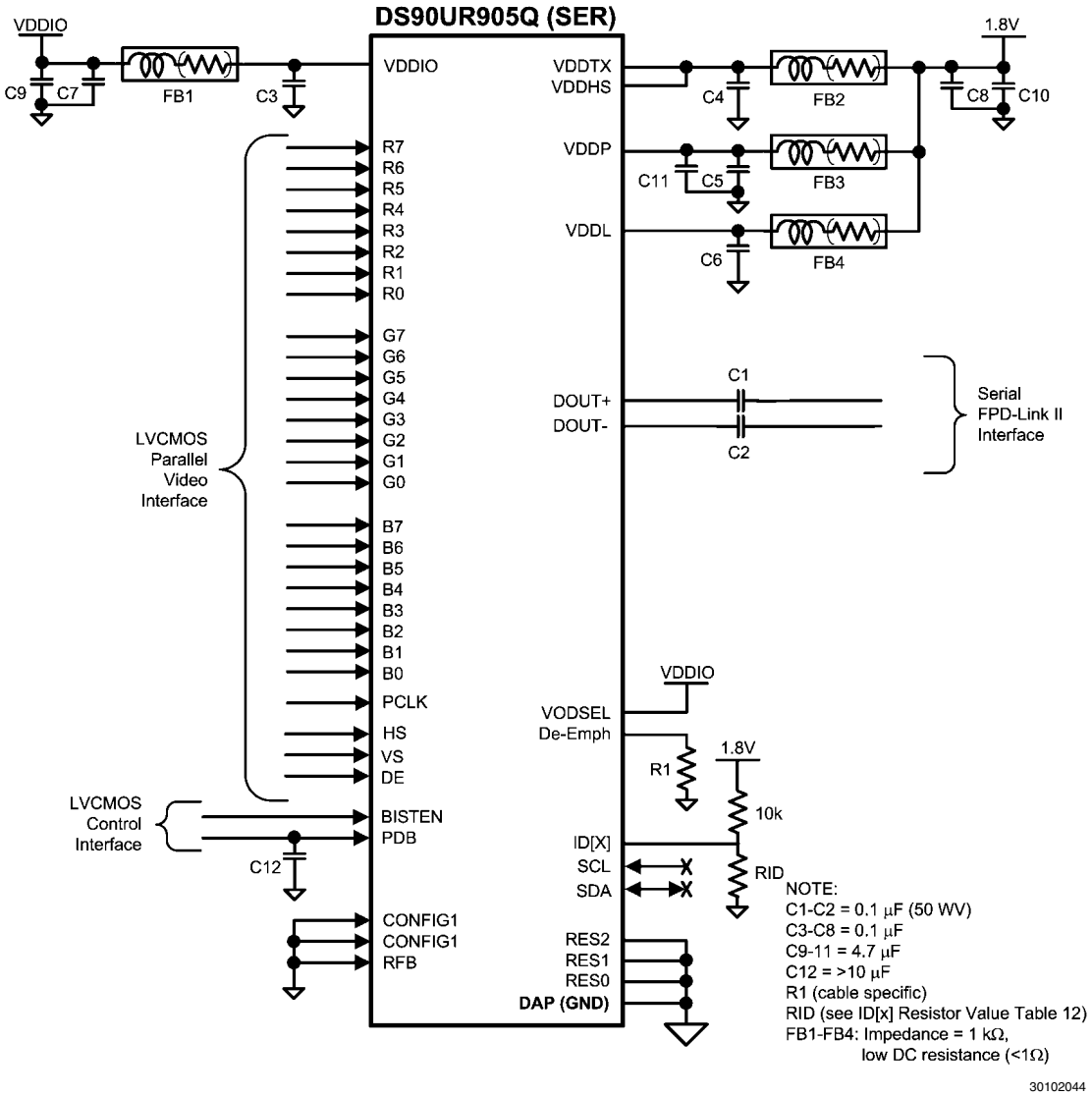


FIGURE 34. DS90UR905Q Typical Connection Diagram — Pin Control

Figure 35 shows a typical application of the DS90UR906Q Des in Pin/STRAP control mode for a 65 MHz 24-bit Color Display Application. The LVDS inputs utilize 100 nF coupling capacitors to the line and the Receiver provides internal termination. Bypass capacitors are placed near the power supply pins. At a minimum, seven 0.1 µF capacitors and two 4.7 µF capacitors should be used for local device bypassing. System GPO (General Purpose Output) signals control the PDB and the BISTEN pins. In this application the RRFB pin is tied Low to strobe the data on the falling edge of the PCLK.

Since the device in the Pin/STRAP mode, four 10 kΩ pull up resistors are used on the parallel output bus to select the desired device features. CONFIG[1:0] is set to 01'b for Normal Mode and Control Signal Filter ON, this is accomplished with the STRAP pull-up on B7. The receiver input equalizer is also enabled and set to provide 7.5 dB of gain, this is accomplished with EQ[3:0] set to 1001'b with STRAP pull ups on G4 and G7. To reduce parallel bus EMI, the SSCG feature is enabled and set to 30 kHz and ±1% with SSC[3:0] set to 0010'b and a STRAP pull-up on R4. The desired features are set with the use of the four pull up resistors.

The interface to the target display is with 3.3V LVCMOS levels, thus the VDDIO pin is connected to the 3.3 V rail. The optional Serial Bus Control is not used in this example, thus the SCL, SDA and ID[x] pins are left open. A delay cap is placed on the PDB signal to delay the enabling of the device until power is stable.

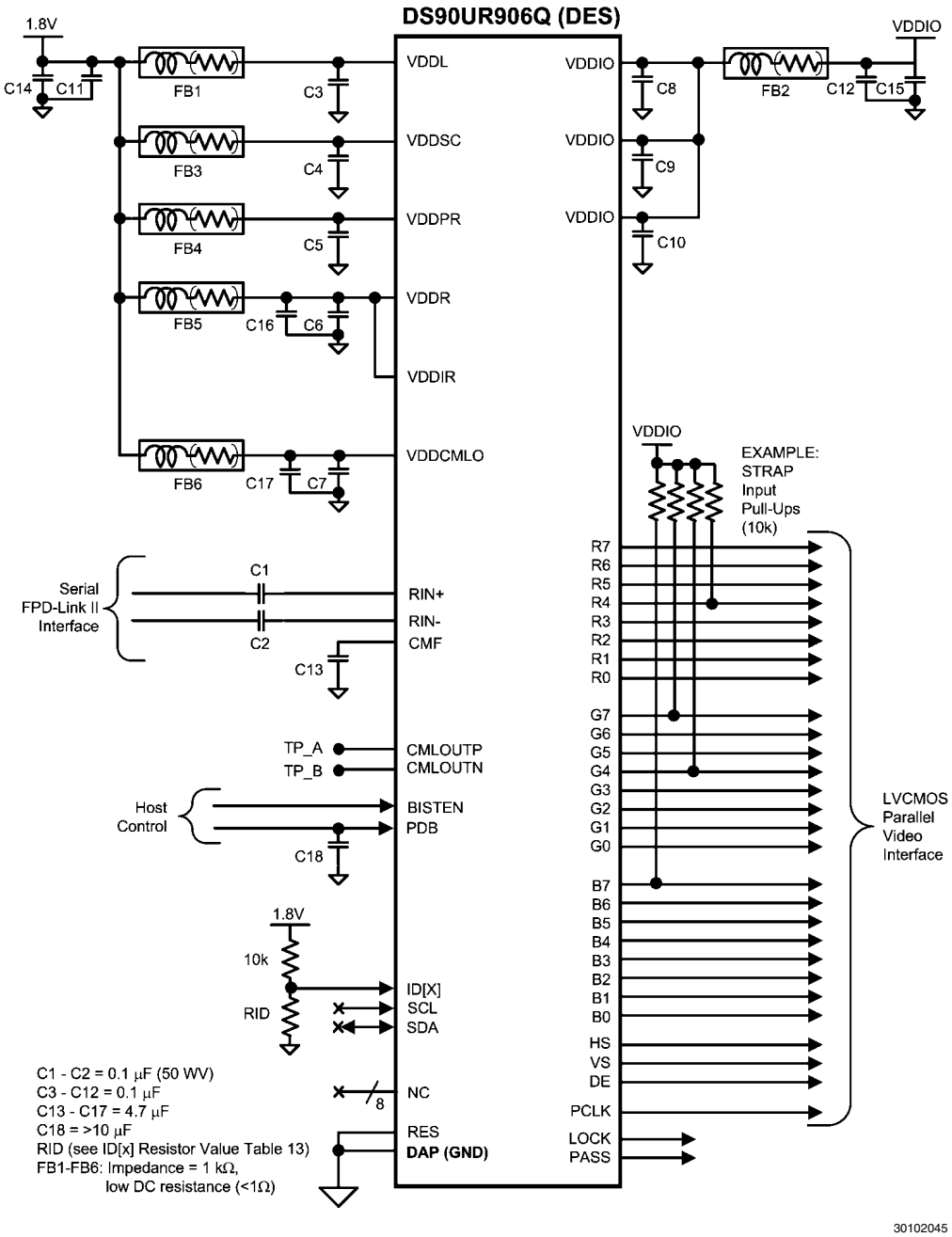


FIGURE 35. DS90UR906Q Typical Connection Diagram — Pin Control

POWER UP REQUIREMENTS AND PDB PIN

The VDD (V_{DDn} and V_{DDIO}) supply ramp should be faster than 1.5 ms with a monotonic rise. If slower then 1.5 ms then a capacitor on the PDB pin is needed to ensure PDB arrives after all the VDD have settled to the recommended operating voltage. When PDB pin is pulled to V_{DDIO}, it is recommended to use a 10 kΩ pull-up and a >10 uF cap to GND to delay the PDB input signal.

TRANSMISSION MEDIA

The Ser/Des chipset is intended to be used in a point-to-point configuration, through a PCB trace, or through twisted pair cable. The Ser and Des provide internal terminations providing a clean signaling environment. The interconnect for LVDS should present a differential impedance of 100 Ohms. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Shielded or un-shielded cables may be used depending upon the noise environment and application requirements.

LIVE LINK INSERTION

The Ser and Des devices support live pluggable applications. The automatic receiver lock to random data “plug & go” hot insertion capability allows the DS90UR906Q to attain lock to the active data stream during a live insertion event.

PCB LAYOUT AND POWER SYSTEM CONSIDERATIONS

Circuit board layout and stack-up for the LVDS Ser/Des devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50uF to 100uF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely-coupled differential lines of 100 Ohms are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Information on the LLP style package is provided in National Application Note: AN-1187.

LVDS INTERCONNECT GUIDELINES

See AN-1108 and AN-905 for full details.

- Use 100Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - S = space between the pair
  - 2S = space between pairs
  - 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Terminate as close to the TX outputs and RX inputs as possible

Additional general guidance can be found in the LVDS Owner’s Manual - available in PDF format from the National web site at: **www.national.com/lvds**

ALTERNATE COLOR / DATA MAPPING

Color Mapped data Pin names are provided to specify a recommended mapping for 24-bit Color Applications. Seven [7] is assumed to be the MSB, and Zero [0] is assumed to be the LSB. While this is recommended it is not required. When connecting to earlier generations of FPD-Link II Ser and Des devices, a color mapping review is recommended to ensure the correct connectivity is obtained. *Table 16* provides examples for interfacing to 18-bit applications with or without the video control signals embedded. The DS90UR906Q Des also provides additional flexibility with the MAP_SEL feature as well.

TABLE 16. Alternate Color / Data Mapping — See Text Below

18-bit RGB	18-bit RGB	24-bit RGB	905 Pin Name		906 Pin Name	24-bit RGB	18-bit RGB	18-bit RGB
LSB R0	GP0	RO	RO		R0	R0	GP0	LSB R0
R1	GP1	R1	R1		R1	R1	GP1	R1
R2	R0	R2	R2		R2	R2	R0	R2
R3	R1	R3	R3		R3	R3	R1	R3
R4	R2	R4	R4		R4	R4	R2	R4
MSB R5	R3	R5	R5		R5	R5	R3	MSB R5
LSB G0	R4	R6	R6		R6	R6	R4	LSB G0
G1	R5	R7	R7		R7	R7	R5	G1
G2	GP2	G0	G0		G0	G0	GP2	G2
G3	GP3	G1	G1		G1	G1	GP3	G3
G4	GO	G2	G2		G2	G2	G0	G4
MSB G5	G1	G3	G3		G3	G3	G1	MSB G5
LSB B0	G2	G4	G4		G4	G4	G2	LSB0
B1	G3	G5	G5		G5	G5	G3	B1
B2	G4	G6	G6		G6	G6	G4	B2
B3	G5	G7	G7		G7	G7	G5	B3
B4	GP4	B0	B0		B0	B0	GP4	B4
MSB B5	GP5	B1	B1		B1	B1	GP5	MSB B5
HS	B0	B2	B2		B2	B2	B0	HS
VS	B1	B3	B3		B3	B3	B1	VS
DE	B2	B4	B4		B4	B4	B2	DE
GP0	B3	B5	B5		B5	B5	B3	GP0
GP1	B4	B6	B6		B6	B6	B4	GP1
GP2	B5	B7	B7		B7	B7	B5	GP2
GND	HS	HS	HS		HS	HS	HS	GND
GND	VS	VS	VS		VS	VS	VS	GND
GND	DE	DE	DE		DE	DE	DE	GND
Scenario 3	**Scenario 2**	**Scenario 1**	**905 Pin Name**		**906 Pin Name**	**Scenario 1**	**Scenario 2**	**Scenario 3**

Scenario 3

Scenario 3 supports an 18-bit RGB color mapping, 3 un-embedded video control signals, and up to three general purpose signals.

Scenario 2

Scenario 2 supports an 18-bit RGB color mapping, 3 embedded video control signals, and up to six general purpose signals.

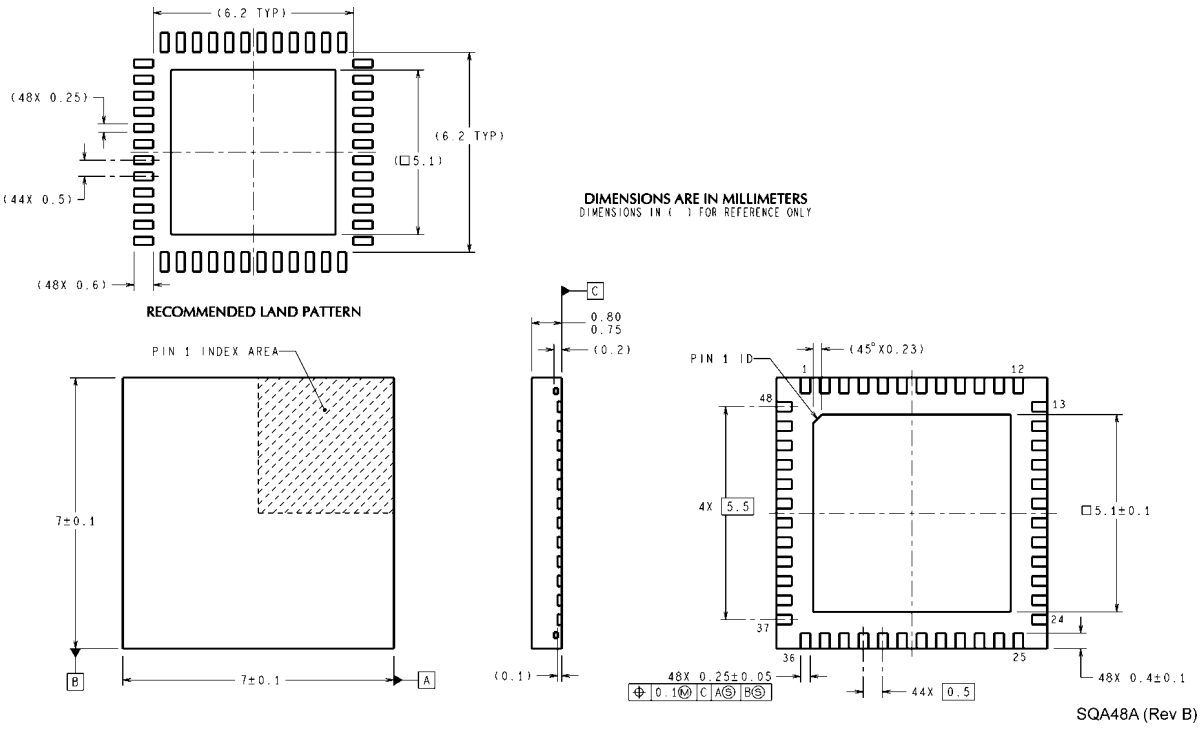
Scenario 1

Scenario 1 supports the 24-bit RGB color mapping, along with the 3 embedded video control signals. This is the native mode for the chipset.

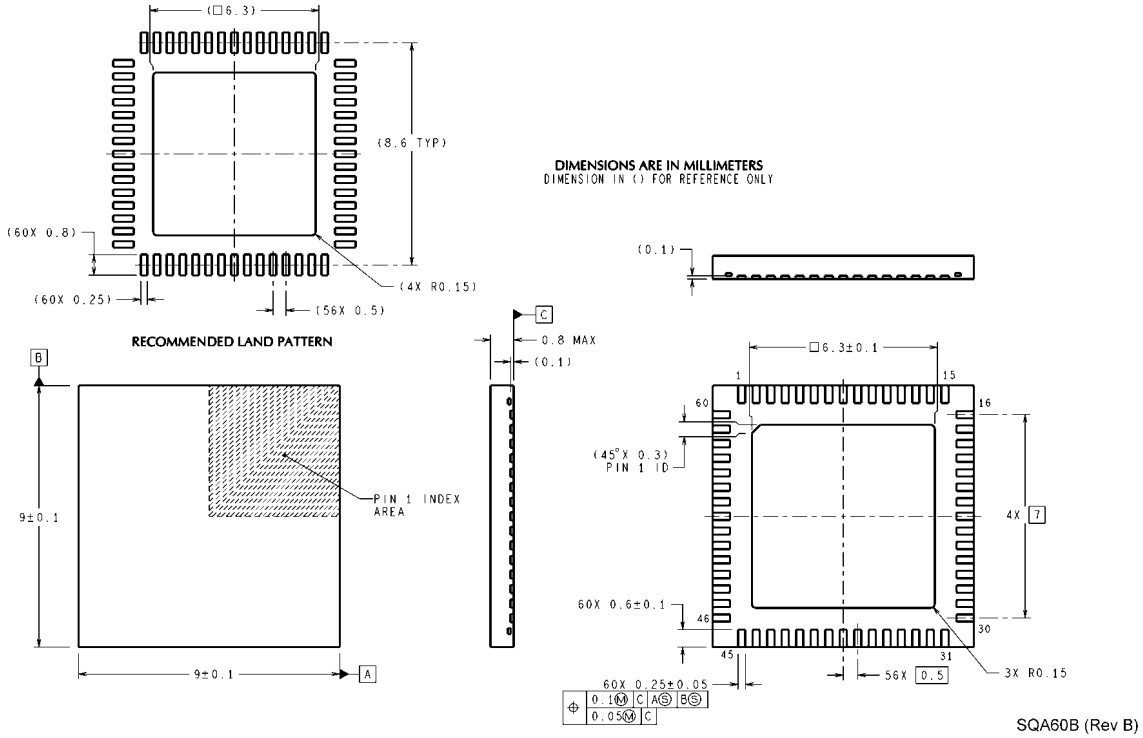
Revision History

- **2/01/2010**
- **DS90UR905Q DATASHEET LIMITS HAVE BEEN UPDATED PER CHARACTERIZATION RESULT AND ARE THE FINAL LIMITS**
- Updated TABLE 12: deleted ID[x] Address 7'b 110 1000 (h'68) (8'b 1101 0000 (h'D0))
- Updated TABLE 13: deleted ID[x] Address 7'b 111 0000 (h'70) (8'b 1110 0000 (h'E0))
- Updated DS90UR906Q Pin Diagram: strap changes on pin11, pin14, and pin42
- Updated DS90UR906Q Deserializer Pin Descriptions: RDS feature changed to OS_PCLK and OS_DATA. Added OP_LOW feature.
- Changed strap pin 14 feature from “RDS” to “OS_DATA” (Output Slew_DATA)
- Added strap to pin 11 “OS_PCLK” (Output Slew_PCLK)
- Added strap to pin 42 “OP_LOW” (Output LOW)
- Changed Table 14: ADD \ 1 \ bit \ 6:0 \ ID[x]: deleted Device ID 7b'1101 00 (h'68). Only four (4) IDs will be available.
- Changed Table 15: ADD \ 0 \ bit \ 6 \ OSS_SEL: “OSS_SEL” changed feature to “OS_PCLK” (Output Slew_PCLK). OSS_SEL moved to ADD \ 2 \ bit \ 6 \.
- Changed Table 15: ADD \ 0 \ bit \ 5 \ RDS: changed “RDS” feature to OS_DATA (Output Slew_DATA)
- Changed Table 15: ADD \ 1\ bit \ 6:0 \ ID[x]: deleted Device ID 7b'1110 00 (h'70). Only four (4) IDs will be available.
- Changed Table 15: ADD \ 2 \ bit \ 7 \ Reserved: changed “Reserved” to “OP_LOW”
- Changed Table 15: ADD \ 2 \ bit \ 6 \ Reserved: changed “Reserved” to “OSS_SEL”
- Updated DS90UR905Q Typical Connection Diagram — Pin Control. Ref 30102044
- Updated DS90UR906Q Typical Connection Diagram — Pin Control. Ref 30102045
- Created OP_LOW timing figure 26. Ref 30102065.
- Created OP_LOW timing figure27. Ref 30102066.
- Removed IDDT3 and IDDIOT3 (RANDOM pattern) because the limits are the same as checker board pattern.
- **2/08/2010**
- Minor corrections: Changed Iin from +/-10uA to +/-15uA in Serial Control bus section; added note 11 to: t_{XZR}, t_{PLD}, t_{SD}, t_{DJIT} and VOL (in Serial Control Bus Characteristics).
- **2/09/2010**
- Added “Note: During initial power-up, a delay of 10ms will be required before the I2C will respond.” in Optional Serial Bus Control description section.
- **2/11/2010**
- Removed Note 11 on t_{DJIT} and max values.
- **3/5/2010**
- Added reference to soldering profile.
- Added ESD CDM and ESD MM values.
- Updated θ_{JA} value.
- **5/25/2010**
- **DS90UR906 DATASHEET LIMITS HAVE BEEN UPDATED PER CHARACTERIZATION RESULTS**
- Corrected TABLE 14. SERIALIZER — Serial Bus Control Registers: register 5 from RFB to VODSEL and register 4 from VODSEL to RFB.
- **8/9/2010**
- Modified order information to include NOPB designation in NSPN column (replaced NSID column).
- Corrected on Page 10. ESD Rating to IEC 61000–4–2 from ISO 10605 (duplication).
- Added on Page 17. RPU = 10kΩ condition for the Serial Control Bus Characteristics of tR and tF.
- Removed ”Data Randomization & Scrambling”, Noise Margin” and “Typical Performance Curves” sections.
- **1/13/2011**
- Modified ESD to include IEC condition (330 Ohm, 150pF).
- Updated deserializer parameters: IDD1, IDDZ, IDDIOZ, IDDR, VOH, VOL, tROS, tRDC.
- Updated figures 14 and 15 to reflect data measurement at VDDIO/2
- Updated fig 35 — C13 changed to 4.7uF
- PASS pin functional change (Tables 8 & 9, Fig 23 & 24)

Physical Dimensions inches (millimeters) unless otherwise noted



48–pin LLP Package (7.0 mm x 7.0 mm x 0.8 mm, 0.5 mm pitch)
NS Package Number SQA48A



60–pin LLP Package (9.0 mm x 9.0 mm x 0.8 mm, 0.5 mm pitch)
NS Package Number SQA60B

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at: www.national.com

Products		Design Support	
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