National Semiconductor

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DS92LV2421/DS92LV2422

10 to 75 MHz, 24-bit Channel Link II Serializer and Deserializer

General Description

The DS92LV2421 (Serializer) / DS92LV2422 (Deserializer) chipset translates a parallel 24–bit LVCMOS data interface into a single high-speed CML serial interface with embedded clock information. This single serial stream eliminates skew issues between clock and data, reduces connector size and interconnect cost for transferring a 24-bit or less, bus over FR-4 printed circuit board backplanes, and balanced cables.

In addition to the 24-bit data bus interface, the DS92LV2421 and DS92LV2422 also features a 3-bit control bus for slow speed signals. This allows implementing video and display applications with up to 24–bits per pixel (RGB).

Programmable transmit de-emphasis, receive equalization, on-chip scrambling and DC balancing enables longer distance transmission over lossy cables and backplanes. The DS92LV2422 automatically locks to incoming data without an external reference clock or special sync patterns, providing easy "plug-and-go" operation. EMI is minimized by the use of low voltage differential signaling, receiver drive strength control, and spread spectrum clocking capability.

The DS92LV2421, DS92LV2422 chipset is programmable though an I2C interface as well as through pins. A built-in AT-SPEED BIST feature validates link integrity and may be used for system diagnostics.

The DS92LV2421 is offered in a 48-pin LLP and the DS92LV2422 is offered in a 60-pin LLP package. Both devices operate over the full industrial temperature range of -40° C to +85°C.

Features

- 24–bit data, 3–bit control, 10 – 75 MHz clock
- AC coupled STP interconnect cable up to 10 meters
- Integrated terminations on Ser and Des
- AT-SPEED link BIST mode and reporting pin
- Optional I2C compatible Serial Control Bus
- Power down mode minimizes power dissipation
- 1.8V or 3.3V compatible LVCMOS I/O interface
- -40° to +85°C temperature range
- >8 kV HBM

SERIALIZER — DS92LV2421

- Data scrambler for reduced EMI
- DC-balance encoder for AC coupling
- Selectable output VOD and adjustable de-emphasis

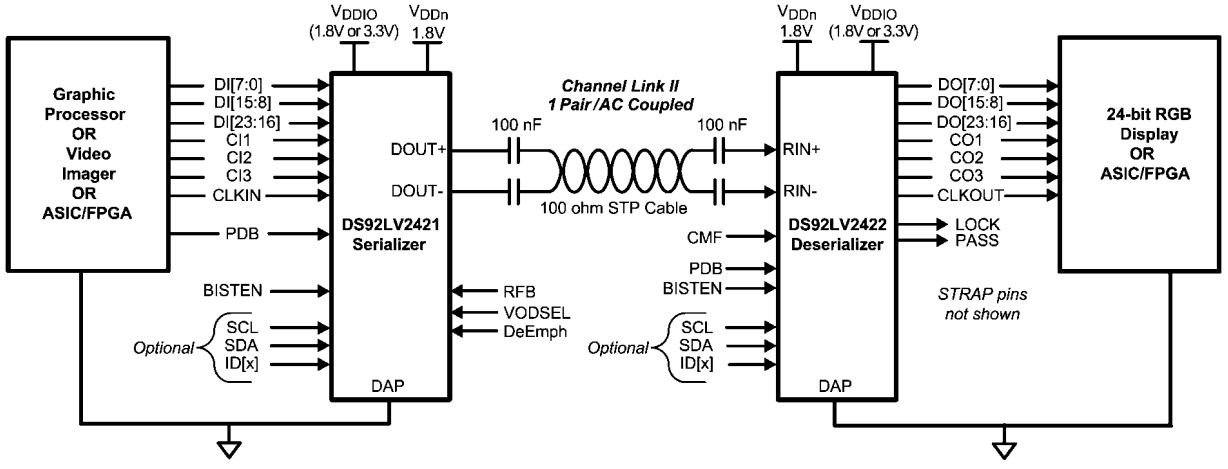
DESERIALIZER — DS92LV2422

- FAST random data lock; no reference clock required
- Adjustable input receiver equalization
- LOCK (real time link status) reporting pin
- EMI minimization on output parallel bus (SSCG)
- Output Slew control (OS)

Applications

- Embedded Video and Display
- Medical Imaging
- Factory Automation
- Office Automation — Printer, Scanner
- Security and Video Surveillance
- General purpose data communication

Applications Diagram



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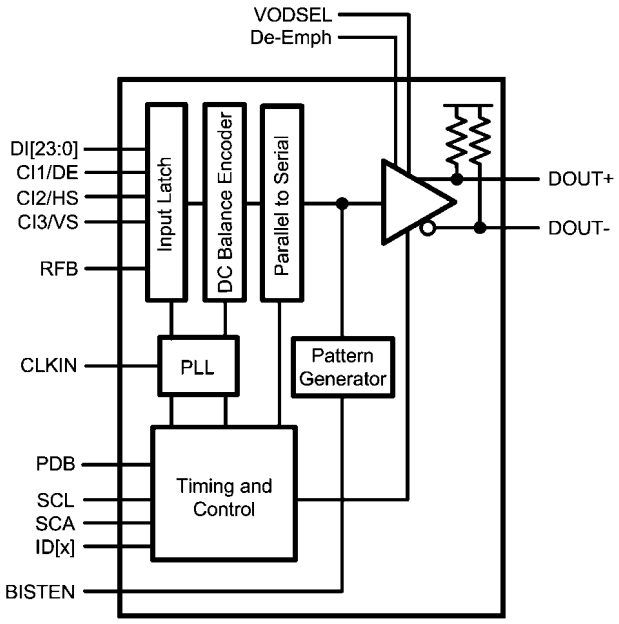
Block Diagrams



DS92LV2421 – SERIALIZER

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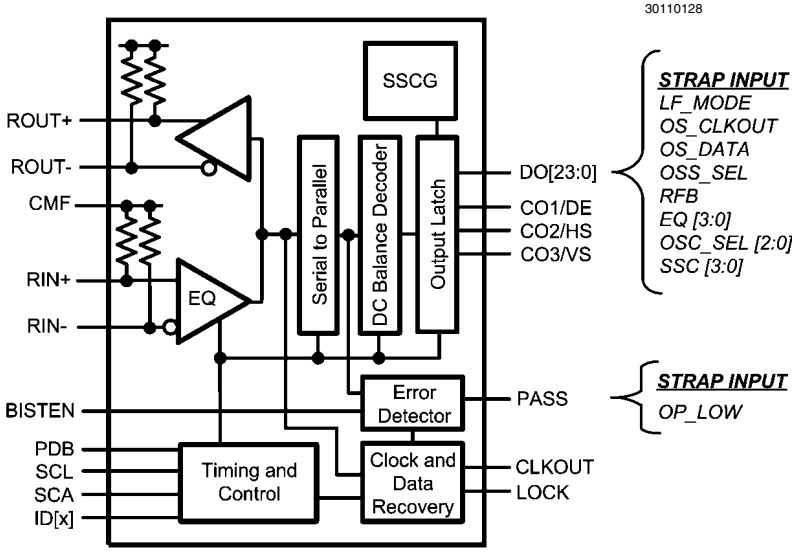

DS92LV2422 – DESERIALIZER

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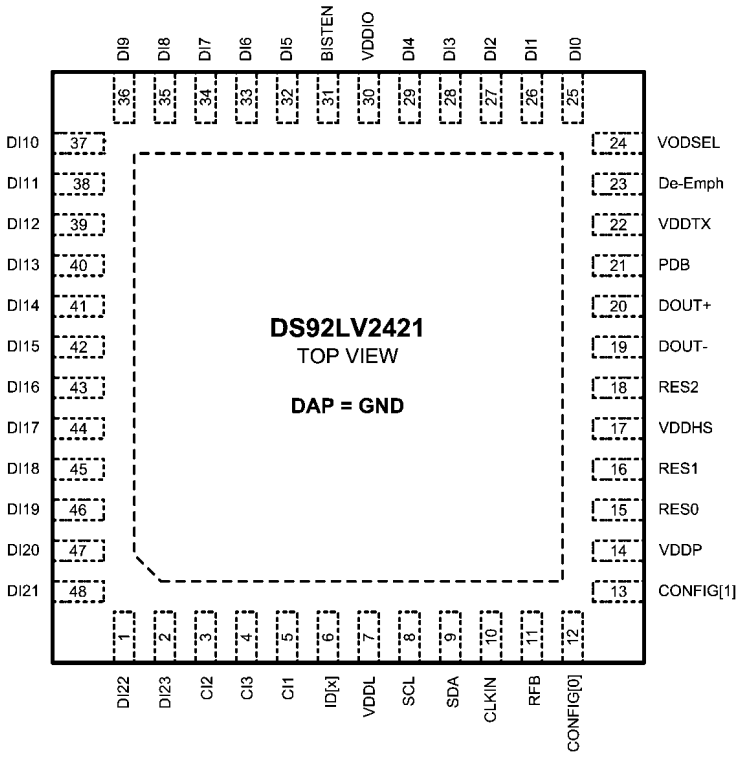
Ordering Information

NSID	Package Description	Quantity	SPEC	Package ID
DS92LV2421SQE	48–pin LLP, 7.0 X 7.0 X 0.8 mm, 0.5 mm pitch	250	NOPB	SQA48A
DS92LV2421SQ	48–pin LLP, 7.0 X 7.0 X 0.8 mm, 0.5 mm pitch	1000	NOPB	SQA48A
DS92LV2421SQX	48–pin LLP, 7.0 X 7.0 X 0.8 mm, 0.5 mm pitch	2500	NOPB	SQA48A
DS92LV2422SQE	60–pin LLP, 9.0 X 9.0 X 0.8 mm, 0.5 mm pitch	250	NOPB	SQA60B
DS92LV2422SQ	60–pin LLP, 9.0 X 9.0 X 0.8 mm, 0.5 mm pitch	1000	NOPB	SQA60B
DS92LV2422SQX	60–pin LLP, 9.0 X 9.0 X 0.8 mm, 0.5 mm pitch	2500	NOPB	SQA60B

DS92LV2421 Pin Diagram



Serializer - DS92LV2421 — Top View

DS92LV2421 Serializer Pin Descriptions

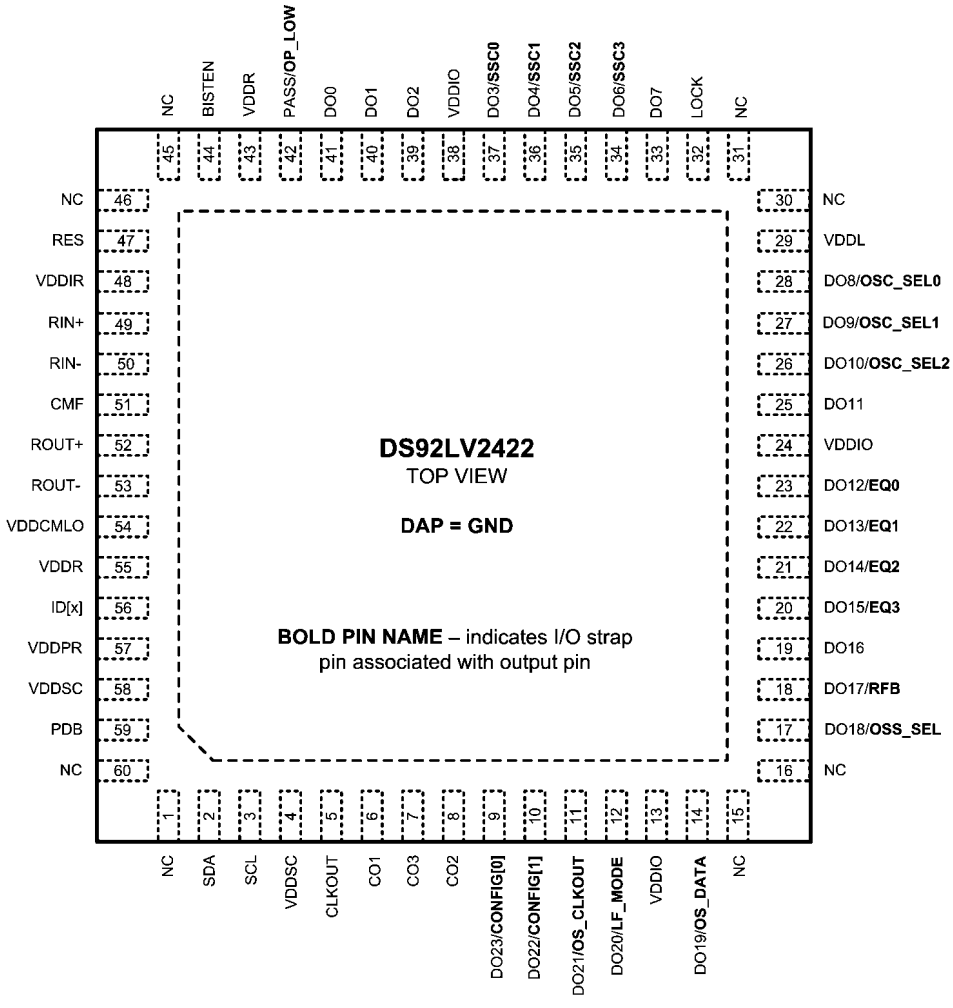
Pin Name	Pin #	I/O, Type	Description
LVCMOS Parallel Interface			
DI[7:0]	34, 33, 32, 29, 28, 27, 26, 25	I, LVCMOS w/ pull-down	Parallel Interface Data Input Pins For 8–bit RED Display: DI7 = R7 – MSB, DI0 = R0 – LSB.
DI[15:8]	42, 41, 40, 39, 38, 37, 36, 35	I, LVCMOS w/ pull-down	Parallel Interface Data Input Pins For 8–bit GREEN Display: DI15 = G7 – MSB, DI8 = G0 – LSB.
DI[23:16]	2, 1, 48, 47, 46, 45, 44, 43	I, LVCMOS w/ pull-down	Parallel Interface Data Input Pins For 8–bit BLUE Display: DI23 = B7 – MSB, DI16 = B0 – LSB.
CI1	5	I, LVCMOS w/ pull-down	Control Signal Input For Display/Video Application: CI1 = Data Enable Input Control signal pulse width must be 3 clocks or longer to be transmitted when the Control Signal Filter is enabled (CONFIG[1:0] = 01). There is no restriction on the minimum transition pulse when the Control Signal Filter is disabled (CONFIG[1:0] = 00). The signal is limited to 2 transitions per 130 clocks regardless of the Control Signal Filter setting.
CI2	3	I, LVCMOS w/ pull-down	Control Signal Input For Display/Video Application: CI2 = Horizontal Sync Input Control signal pulse width must be 3 clocks or longer to be transmitted when the Control Signal Filter is enabled (CONFIG[1:0] = 01). There is no restriction on the minimum transition pulse when the Control Signal Filter is disabled (CONFIG[1:0] = 00). The signal is limited to 2 transitions per 130 clocks regardless of the Control Signal Filter setting.
CI3	4	I, LVCMOS w/ pull-down	Control Signal Input For Display/Video Application: CI3 = Vertical Sync Input CI3 is limited to 1 transition per 130 clock cycles. Thus, the minimum pulse width allowed is 130 clock cycle wide.

Pin Name	Pin #	I/O, Type	Description
CLKIN	10	I, LVCMOS w/ pull-down	Clock Input Latch/data strobe edge set by RFB pin.
Control and Configuration			
PDB	21	I, LVCMOS w/ pull-down	Power-down Mode Input PDB = 1, Ser is enabled (normal operation). Refer to "Power Up Requirements and PDB Pin" in the Applications Information Section. PDB = 0, Ser is powered down. When the Ser is in the power-down state, the driver outputs (DOUT+/-) are both logic high, the PLL is shutdown, IDD is minimized. Control Registers are **RESET**.
VODSEL	24	I, LVCMOS w/ pull-down	Differential Driver Output Voltage Select (This is can also be control by I2C register.) VODSEL = 1, LVDS VOD is ±420 mV, 840 mVp-p (typ) — long cable / De-Emph apps VODSEL = 0, LVDS VOD is ±280 mV, 560 mVp-p (typ) — short cable (no De-emph), low power mode.
De-Emph	23	I, Analog w/ pull-up	De-Emphasis Control (This can also be controlled by I2C register access.) De-Emph = open (float) - disabled To enable De-emphasis, tie a resistor from this pin to GND or control via register. See *Table 4*.
RFB	11	I, LVCMOS w/ pull-down	Clock Input Latch/Data Strobe Edge Select (This can also be controlled by I2C register access.) RFB = 1, parallel interface data and control signals are latched on the rising clock edge. RFB = 0, parallel interface data and control signals are latched on the falling clock edge.
CONFIG [1:0]	13, 12	I, LVCMOS w/ pull-down	00: Control Signal Filter DISABLED 01: Control Signal Filter ENABLED 10: Reverse compatibility mode to interface with the DS90UR124 or DS99R124Q 11: Reverse compatibility mode to interface with the DS90C124
ID[x]	6	I, Analog	I2C Serial Control Bus Device ID Address Select — Optional Resistor to Ground and 10 kΩ pull-up to 1.8V rail. See *Table 11*.
SCL	8	I, LVCMOS	I2C Serial Control Bus Clock Input - Optional SCL requires an external pull-up resistor to V_{DDIO}.
SDA	9	I/O, LVCMOS Open Drain	I2C Serial Control Bus Data Input / Output - Optional SDA requires an external pull-up resistor V_{DDIO}.
BISTEN	31	I, LVCMOS w/ pull-down	BIST Mode — Optional BISTEN = 0, BIST is disabled (normal operation) BISTEN = 1, BIST is enabled
RES[2:0]	18, 16, 15	I, LVCMOS w/ pull-down	***Reserved*** - tie LOW
Channel-Link II — CML Serial Interface			
DOUT+	20	O, CML	Non–Inverting Output. The output must be AC Coupled with a 0.1 µF capacitor.
DOUT-	19	O, CML	Inverting Output. The output must be AC Coupled with a 0.1 µF capacitor.
Power and Ground (see NOTE below)			
VDDL	7	Power	Logic Power, 1.8 V ±5%
VDDP	14	Power	PLL Power, 1.8 V ±5%
VDDHS	17	Power	TX High Speed Logic Power, 1.8 V ±5%
VDDTX	22	Power	Output Driver Power, 1.8 V ±5%
VDDIO	30	Power	LVCMOS I/O Power, **1.8 V ±5% OR 3.3 V ±10%**
GND	DAP	Ground	DAP is the large metal contact at the bottom side, located at the center of the LLP package. **Connect to the ground plane** (GND) with at least 9 vias.

NOTE: 1= HIGH, 0 L= LOW

The VDD (V_{DDn} and V_{DDIO}) supply ramp should be faster than 1.5 ms with a monotonic rise. If slower then 1.5 ms then a capacitor on the PDB pin is needed to ensure PDB arrives after all the VDD have settled to the recommended operating voltage.

DS92LV2422 Pin Diagram



Deserializer - DS92LV2422 — Top View

DS92LV2422 Deserializer Pin Descriptions

Pin Name	Pin #	I/O, Type	Description
LVCMOS Parallel Interface			
DO[7:0]	33, 34, 35, 36, 37, 39, 40, 41	I, STRAP, O, LVCMOS	Parallel Interface Data Output Pins For 8–bit RED Display: DO7 = R7 – MSB, DO0 = R0 – LSB. In power-down (PDB = 0), outputs are controlled by the OSS_SEL (See *Table 8*). These pins are inputs during power-up (See STRAP Inputs).
DO[15:8]	20, 21, 22, 23, 25, 26, 27, 28	I, STRAP, O, LVCMOS	Parallel Interface Data Output Pins For 8–bit GREEN Display: DO15 = G7 – MSB, DO8 = G0 – LSB. In power-down (PDB = 0), outputs are controlled by the OSS_SEL (See *Table 8*). These pins are inputs during power-up (See STRAP Inputs).
DO[23:16]	9, 10, 11, 12, 14, 17, 18, 19	I, STRAP, O, LVCMOS	Parallel Interface Data Input Pins For 8–bit BLUE Display: DO23 = B7 – MSB, DO16 = B0 – LSB. In power-down (PDB = 0), outputs are controlled by the OSS_SEL (See *Table 8*). These pins are inputs during power-up (See STRAP Inputs).

Pin Name	Pin #	I/O, Type	Description
CO1	6	O, LVCMOS	Control Signal Output For Display/Video Application: CO1 = Data Enable Output Control signal pulse width must be 3 clocks or longer to be transmitted when the Control Signal Filter is enabled (CONFIG[1:0] = 01). There is no restriction on the minimum transition pulse when the Control Signal Filter is disabled (CONFIG[1:0] = 00). The signal is limited to 2 transitions per 130 clocks regardless of the Control Signal Filter setting. In power-down (PDB = 0), output is controlled by the OSS_SEL pin (See *Table 8*).
CO2	8	O, LVCMOS	Control Signal Output For Display/Video Application: CO2 = Horizontal Sync Output Control signal pulse width must be 3 clocks or longer to be transmitted when the Control Signal Filter is enabled (CONFIG[1:0] = 01). There is no restriction on the minimum transition pulse when the Control Signal Filter is disabled (CONFIG[1:0] = 00). The signal is limited to 2 transitions per 130 clocks regardless of the Control Signal Filter setting. In power-down (PDB = 0), output is controlled by the OSS_SEL pin (See *Table 8*).
CO3	7	O, LVCMOS	Control Signal Output For Display/Video Application: CO3 = Vertical Sync Output CO3 is different than CO1 and CO2 because it is limited to 1 transition per 130 clock cycles. Thus, the minimum pulse width allowed is 130 clock cycle wide. The CONFIG[1:0] pins have no affect on CO3 signal In power-down (PDB = 0), output is controlled by the OSS_SEL pin (See *Table 8*).
CLKOUT	5	O, LVCMOS	Pixel Clock Output In power-down (PDB = 0), output is controlled by the OSS_SEL pin (See *Table 8*). Data strobe edge set by RFB.
LOCK	32	O, LVCMOS	LOCK Status Output LOCK = 1, PLL is Locked, outputs are active LOCK = 0, PLL is unlocked, DO[23:0], CO1, CO2, CO3 and CLKOUT output states are controlled by OSS_SEL (See *Table 8*). May be used as Link Status or to flag when Video Data is active (ON/OFF).
PASS	42	O, LVCMOS	PASS Output (BIST Mode) PASS = 1, error free transmission PASS = 0, one or more errors were detected in the received payload Route to test point for monitoring, or leave open if unused.
Control and Configuration — STRAP PINS For a High State, use a 10 kΩ pull up to V_{DDIO}; for a Low State, the IO includes an internal pull down. The STRAP pins are read upon power-up and set device configuration. Pin Number listed along with shared data output name in square brackets.			
CONFIG[1:0]	10 [DO22], 9 [DO23]	STRAP I, LVCMOS w/ pull-down	00: Control Signal Filter DISABLED 01: Control Signal Filter ENABLED 10: Reverse compatibility mode to interface with the DS90UR241 or DS99R241 11: Reverse compatibility mode to interface with the DS90C241
LF_MODE	12 [DO20]	STRAP I, LVCMOS w/ pull-down	SSCG Low Frequency Mode Only required when SSCG is enabled, otherwise LF_MODE condition is a DON'T CARE (X). LF_MODE = 1, SSCG in low frequency mode (CLK = 10-20 MHz) LF_MODE = 0, SSCG in high frequency mode (CLK = 20-65 MHz) This can also be controlled by I2C register access.
OS_CLKOUT	11 [DO21]	STRAP I, LVCMOS w/ pull-down	Output CLKOUT Slew Select OS_CLKOUT = 1, Increased CLKOUT slew rate OS_CLKOUT = 0, Normal CLKOUT slew rate (default) This can also be controlled by I2C register access.

Pin Name	Pin #	I/O, Type	Description
OS_DATA	14 [DO19]	STRAP I, LVCMOS w/ pull-down	Output DO[23:0], CO1, CO2, CO3 Slew Select OS_DATA = 1, Increased DO slew rate OS_DATA = 0, Normal DO slew rate (default) This can also be controlled by I2C register access.
OP_LOW	42 [PASS]	STRAP I, LVCMOS w/ pull-down	Outputs held LOW when LOCK = 1 **NOTE: Do not use any other strap options with this strap function enabled** OP_LOW = 1: all outputs are held LOW during power up until released by programming OP_LOW release/set register HIGH. **NOTE: Before the device is powered up, the outputs are in TRI-STATE®** See *Figure 24* and *Figure 25* OP_LOW = 0: all outputs toggle normally as soon as LOCK goes HIGH (default) This can also be controlled by I2C register access.
OSS_SEL	17 [DO18]	STRAP I, LVCMOS w/ pull-down	Output Sleep State Select OSS_SEL is used in conjunction with PDB to determine the state of the outputs in Power Down (Sleep). (See *Table 8*). **NOTE: OSS_SEL STRAP CANNOT BE USED IF OP_LOW = 1** This can also be controlled by I2C register access.
RFB	18 [DO17]	STRAP I, LVCMOS w/ pull-down	Clock Output Strobe Edge Select RFB = 1, parallel interface data and control signals are strobed on the rising clock edge. RFB = 0, parallel interface data and control signals are strobed on the falling clock edge. This can also be controlled by I2C register access.
EQ[3:0]	20 [DO15], 21 [DO14], 22 [DO13], 23 [DO12]	STRAP I, LVCMOS w/ pull-down	Receiver Input Equalization (See *Table 5*). This can also be controlled by I2C register access.
OSC_SEL[2:0]	26 [DO10], 27 [DO9], 28 [DO8]	STRAP I, LVCMOS w/ pull-down	Oscillator Selectl (See *Table 9* and *Table 10*). This can also be controlled by I2C register access.
SSC[3:0]	34 [DO6], 35 [DO5], 36 [DO4], 37 [DO3]	STRAP I, LVCMOS w/ pull-down	Spread Spectrum Clock Generation (SSCG) Range Select (See *Table 6* and *Table 7*). This can also be controlled by I2C register access.
MAP_SEL[1:0]	40[D], 41 [D]	STRAP I, LVCMOS w/ pull-down	Bit mapping reverse compatibility / DS90UR241 Options Pin or Register Control Default setting is b'00.
Control and Configuration			
PDB	59	I, LVCMOS w/ pull-down	Power Down Mode Input PDB = 1, Des is enabled (normal operation). Refer to “Power Up Requirements and PDB Pin” in the Applications Information Section. PDB = 0, Des is in power-down. When the Des is in the power-down state, the LVCMOS output state is determined by *Table 8*. Control Registers are **RESET**.
ID[x]	56	I, Analog	I2C Serial Control Bus Device ID Address Select — Optional Resistor to Ground and 10 kΩ pull-up to 1.8V rail. (See *Table 11*).
SCL	3	I, LVCMOS	I2C Serial Control Bus Clock Input - Optional SCL requires an external pull-up resistor to V_{DDIO}.
SDA	2	I/O, LVCMOS Open Drain	I2C Serial Control Bus Data Input / Output - Optional SDA requires an external pull-up resistor to V_{DDIO}.
BISTEN	44	I, LVCMOS w/ pull-down	BIST Enable Input — Optional BISTEN = 0, BIST is disabled (normal operation) BISTEN = 1, BIST is enabled
RES	47	I, LVCMOS w/ pull-down	***Reserved*** - tie LOW

Pin Name	Pin #	I/O, Type	Description
NC	1, 15, 16, 30, 31, 45, 46, 60		Not Connected Leave pin open (float)
Channel-Link II — CML Serial Interface			
RIN+	49	I, CML	True Input. The input must be AC Coupled with a 0.1 µF capacitor.
RIN-	50	I, CML	Inverting Input. The input must be AC Coupled with a 0.1 µF capacitor.
CMF	51	I, Analog	Common-Mode Filter VCM center-tap is a virtual ground which may be ac-coupled to ground to increase receiver common mode noise immunity. Recommended value is 4.7 µF or higher.
ROUT+	52	O, CML	True Output — Receive Signal after the Equalizer NC if not used or connect to test point for monitor. Requires I2C control to enable.
ROUT-	53	O, CML	Inverting Output — Receive Signal after the Equalizer NC if not used or connect to test point for monitor. Requires I2C control to enable.
Power and Ground (see NOTE below)			
VDDL	29	Power	Logic Power, 1.8 V ±5%
VDDIR	48	Power	Input Power, 1.8 V ±5%
VDDR	43, 55	Power	RX High Speed Logic Power, 1.8 V ±5%
VDDSC	4, 58	Power	SSCG Power, 1.8 V ±5%
VDDPR	57	Power	PLL Power, 1.8 V ±5%
VDDCMLO	54	Power	RX High Speed Logic Power, 1.8 V ±5%
VDDIO	13, 24, 38	Power	LVCMOS I/O Power, **1.8 V ±5% OR 3.3 V ±10%** (V_{DDIO})
GND	DAP	Ground	DAP is the large metal contact at the bottom side, located at the center of the LLP package. **Connected to the ground plane** (GND) with at least 9 vias.

NOTE: 1 = HIGH, 0 = LOW

The VDD (V_{DDn} and V_{DDIO}) supply ramp should be faster than 1.5 ms with a monotonic rise. If slower then 1.5 ms then a capacitor on the PDB pin is needed to ensure PDB arrives after all the VDD have settled to the recommended operating voltage.

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage – V_{DDn} (1.8V)	−0.3V to +2.5V
Supply Voltage – V_{DDIO}	−0.3V to +4.0V
LVCMOS I/O Voltage	−0.3V to (VDDIO + 0.3V)
Receiver Input Voltage	−0.3V to (VDD + 0.3V)
Driver Output Voltage	−0.3V to (VDD + 0.3V)
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
48L LLP Package	
Maximum Power Dissipation Capacity at 25°C	225 mW
Derate above 25°C	1/ θ_{JA} mW / °C
θ_{JA} (with 9 thermal via)	27.1 °C/W
θ_{JC} (with 9 thermal via)	4.5 °C/W
60L LLP Package	
Maximum Power Dissipation Capacity at 25°C	525 mW
Derate above 25°C	1/ θ_{JA} mW / °C
θ_{JA} (with 9 thermal via)	24.6 °C/W
θ_{JC} (with 9 thermal via)	2.8 °C/W
ESD Rating (HBM)	≥±8 kV
ESD Rating (CDM)	≥±1 kV
ESD Rating (MM)	≥±250 V
ESD Rating (IEC 61000–4–2), R_D = 330Ω, C_S = 150pF	
Air Discharge (D_{OUT+}, D_{OUT-})	≥±25kV
Contact Discharge (D_{OUT+}, D_{OUT-})	≥±8kV
Air Discharge (R_{IN+}, R_{IN-})	≥±25kV
Contact Discharge (R_{IN+}, R_{IN-})	≥±8kV
For soldering specifications: see product folder at www.national.com and www.national.com/ms/MS/MS-SOLDERING.pdf	

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{DDn})	1.71	1.8	1.89	V
LVCMOS Supply Voltage (V_{DDIO})	1.71	1.8	1.89	V
OR				
LVCMOS Supply Voltage (V_{DDIO})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C
Clock Frequency	10		75	MHz
Supply Noise (*Note 10*)			50	mV_{P-P}

Serializer DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (*Note 2*, *Note 3*, *Note 4*)

Symbol	Parameter	Conditions		Pin/Freq.	Min	Typ	Max	Units
LVCMOS INPUT DC SPECIFICATIONS								
V_{IH}	High Level Input Voltage	V_{DDIO} = 3.0 to 3.6V		DI[23:0], CI1,CI2,CI3, CLKIN, PDB, VODSEL, RFB, BISTEN, CONFIG[1:0]	2.2		V_{DDIO}	V
		V_{DDIO} = 1.71 to 1.89V			0.65* V_{DDIO}		V_{DDIO}	V
V_{IL}	Low Level Input Voltage	V_{DDIO} = 3.0 to 3.6V			GND		0.8	V
		V_{DDIO} = 1.71 to 1.89V			GND		0.35* V_{DDIO}	V
I_{IN}	Input Current	V_{IN} = 0V or V_{DDIO}	V_{DDIO} = 3.0 to 3.6V		−15	±1	+15	µA
			V_{DDIO} = 1.7 to 1.89V		−15	±1	+15	µA

Symbol	Parameter	Conditions		Pin/Freq.	Min	Typ	Max	Units
CML DRIVER DC SPECIFICATIONS								
V_{OD}	Differential Output Voltage	R_L = 100Ω, De-emph = disabled, *Figure 2*	VODSEL = 0	DOUT+, DOUT-	±205	±280	±355	mV
			VODSEL = 1		±320	±420	±520	
V_{ODp-p}	Differential Output Voltage (DOUT+) – (DOUT-)		VODSEL = 0			560		mVp-p
			VODSEL = 1			840		mVp-p
ΔV_{OD}	Output Voltage Unbalance	R_L = 100Ω, De-emph = disabled, VODSEL = L				1	50	mV
V_{OS}	Offset Voltage – Single-ended At TP A & B, *Figure 1*	R_L = 100Ω, De-emph = disabled	VODSEL = 0			1.65		V
			VODSEL = 1			1.575		V
ΔV_{OS}	Offset Voltage Unbalance Single-ended At TP A & B, *Figure 1*	R_L = 100Ω, De-emph = disabled				1		mV
I_{OS}	Output Short Circuit Current	DOUT+/- = 0V, De-emph = disabled	VODSEL = 0			–36		mA
R_{TO}	Internal Output Termination Reistor			DOUT+, DOUT-	80	100	120	Ω
SUPPLY CURRENT								
I_{DDT1}	Serializer Supply Current (includes load current) R_L = 100 Ω, CLKIN = 75 MHz	Checker Board Pattern, De-emph = 3kΩ, VODSEL = H, *Figure 9*	V_{DD}= 1.89V	All V_{DD} pins		75	90	mA
I_{DDIOT1}			V_{DDIO}= 1.89V	V_{DDIO}		3	5	mA
			V_{DDIO} = 3.6V			11	15	mA
I_{DDT2}		Checker Board Pattern, De-emph = 6kΩ, VODSEL = L, *Figure 9*	V_{DD}= 1.89V	All V_{DD} pins		65	80	mA
I_{DDIOT2}			V_{DDIO}= 1.89V	V_{DDIO}		3	5	mA
			V_{DDIO} = 3.6V			11	15	mA
I_{DDZ}	Serializer Supply Current Power-down	PDB = 0V , (All other LVCMOS Inputs = 0V)	V_{DD}= 1.89V	All V_{DD} pins		40	1000	µA
I_{DDIOZ}			V_{DDIO}= 1.89V	V_{DDIO}		5	10	µA
			V_{DDIO} = 3.6V			10	20	µA

Deserializer DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
3.3 V I/O LVCMOS DC SPECIFICATIONS – V_{DDIO} = 3.0 to 3.6V							
V_{IH}	High Level Input Voltage		PDB, BISTEN	2.2		V_{DDIO}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
I_{IN}	Input Current	V_{IN} = 0V or V_{DDIO}		–15	±1	+15	µA
V_{OH}	High Level Output Voltage	I_{OH} = –0.5 mA, RDS = L	DO[23:0], CO1, CO2, CO3, CLKOUT, LOCK, PASS	2.4	V_{DDIO}		V
V_{OL}	Low Level Output Voltage	I_{OL} = +0.5 mA, RDS = L			GND	0.4	V
I_{OS}	Output Short Circuit Current	V_{DDIO} = 3.3V, V_{OUT} = 0V, OS_CLKOUT/DATA = L/H	CLKOUT		36		mA
	Output Short Circuit Current	V_{DDIO} = 3.3V, V_{OUT} = 0V, OS_CLKOUT/DATA = L/H	Outputs		37		mA
I_{OZ}	TRI-STATE® Output Current	PDB = 0V, OSS_SEL = 0V, V_{OUT} = 0V or V_{DDIO}	Outputs	–15		+15	µA

Symbol	Parameter	Conditions		Pin/Freq.	Min	Typ	Max	Units
1.8 V I/O LVCMOS DC SPECIFICATIONS – V_{DDIO} = 1.71 to 1.89V								
V_{IH}	High Level Input Voltage			PDB, BISTEN	1.235		V_{DDIO}	V
V_{IL}	Low Level Input Voltage				GND		0.595	V
I_{IN}	Input Current	V_{IN} = 0V or V_{DDIO}			−15	±1	+15	µA
V_{OH}	High Level Output Voltage	I_{OH} = −0.5 mA, RDS = L		DO[23:0], CO1, CO2, CO3, CLKOUT, LOCK, PASS	V_{DDIO} - 0.45	V_{DDIO}		V
V_{OL}	Low Level Output Voltage	I_{OL} = +0.5 mA, RDS = L			GND		0.2	V
I_{OS}	Output Short Circuit Current	V_{DDIO} = 1.8V, V_{OUT} = 0V, OS_CLKOUT/DATA = L/H		CLKOUT		18		mA
	Output Short Circuit Current	V_{DDIO} = 1.8V, V_{OUT} = 0V, OS_CLKOUT/DATA = L/H		Outputs		18		mA
I_{OZ}	TRI-STATE Output Current	PDB = 0V, OSS_SEL = 0V, V_{OUT} = 0V or V_{DDIO}		Outputs	-15		+15	µA
CML RECEIVER DC SPECIFICATIONS								
V_{TH}	Differential Input Threshold High Voltage	V_{CM} = +1.2V (Internal V_{BIAS})		RIN+, RIN-	+50			mV
V_{TL}	Differential Input Threshold Low Voltage				−50			mV
V_{CM}	Common Mode Voltage, Internal V_{BIAS}					1.2		V
I_{IN}	Input Current	V_{IN} = 0V or V_{DDIO}			-15		+15	µA
R_{TI}	Internal Input Termination Resistor			RIN+, RIN-	80	100	120	Ω
LOOP THROUGH CML DRIVER OUTPUT DC SPECIFICATIONS – EQ TEST PORT								
V_{OD}	Differential Output Voltage	R_L = 100Ω		ROUT+/-		542		mV
V_{OS}	Offset Voltage Single-ended	R_L = 100Ω				1.4		V
R_T	Internal Termination Resistor				80	100	120	Ω
SUPPLY CURRENT								
I_{DD1}	Deserializer Supply Current (includes load current) CLKOUT = 75 MHz	Checker Board Pattern, RDS = H, C_L = 4pF, *Figure 9*	V_{DD}= 1.89V	All V_{DD} pins		97	115	mA
I_{DDIO1}			V_{DDIO}=1.89V	V_{DDIO}		40	50	mA
			V_{DDIO} = 3.6V			75	85	mA
I_{DDZ}	Deserializer Supply Current Power Down	PDB = 0V, All other LVCMOS Inputs = 0V	V_{DD}= 1.89V	All V_{DD} pins		100	3000	µA
I_{DDIOZ}			V_{DDIO}=1.89V	V_{DDIO}		6	50	µA
			V_{DDIO} = 3.6V			12	100	µA

Recommended Serializer Timing for CLKIN Requirements

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{TCP}	Transmit Input CLKIN Period	10 MHz to 75 MHz, *Figure 4*	13.3	T	100	ns
t_{TCIH}	Transmit Input CLKIN High Time		0.4T	0.5T	0.6T	ns
t_{TCIL}	Transmit Input CLKIN Low Time		0.4T	0.5T	0.6T	ns
t_{CLKT}	CLKIN Input Transition Time		0.5		2.4	ns
SSC_{IN}	CLKIN Input – Spread Spectrum at 75 MHz	fmod			35	kHz
		fdev			±2	%

Serializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{LHT}	Ser Output Low-to-High Transition Time, *Figure 3*	R_L = 100Ω, De-emphasis = disabled, VODSEL = 0		200		ps
		R_L = 100Ω, De-emphasis = disabled, VODSEL = 1		200		ps
t_{HLT}	Ser Output High-to-Low Transition Time, *Figure 3*	R_L = 100Ω, De-emphasis = disabled, VODSEL = 0		200		ps
		R_L = 100Ω, De-emphasis = disabled, VODSEL = 1		200		ps
t_{DIS}	Input Data - Setup Time, *Figure 4*	DI[23:0], CI1, CI2, CI3 to CLKIN	2			ns
t_{DIH}	Input Data - Hold Time, *Figure 4*	CLKIN to DI[23:0], CI1, CI2, CI3	2			ns
t_{XZD}	Ser Ouput Active to OFF Delay, *Figure 6*			8	15	ns
t_{PLD}	Serializer PLL Lock Time, *Figure 5*	R_L = 100Ω		1.4	10	ms
t_{SD}	Serializer Delay - Latency, *Figure 7*	R_L = 100Ω		144*T	145*T	ns
t_{DJIT}	Ser Output Total Jitter, *Figure 8*	R_L = 100Ω, De-Emph = disabled, RANDOM pattern, CLKIN = 75MHz		0.28		UI
		R_L = 100Ω, De-Emph = disabled, RANDOM pattern, CLKIN = 43MHz		0.27		UI
		R_L = 100Ω, De-Emph = disabled, RANDOM pattern, CLKIN = 10MHz		0.35		UI
λ_{STXBW}	Serializer Jitter Transfer Function -3 dB Bandwidth	R_L = 100Ω, De-Emph = disabled, RANDOM pattern, CLKIN = 75MHz		3.3		MHz
		R_L = 100Ω, De-Emph = disabled, RANDOM pattern, CLKIN = 43MHz		2.3		MHz
		R_L = 100Ω, De-Emph = disabled, RANDOM pattern, CLKIN = 10MHz		0.8		MHz
δ_{STX}	Serializer Jitter Transfer Function Peaking	R_L = 100Ω, De-Emph = disabled, RANDOM pattern, CLKIN = 75MHz		0.86		dB
		R_L = 100Ω, De-Emph = disabled, RANDOM pattern, CLKIN = 43MHz		0.83		dB
		R_L = 100Ω, De-Emph = disabled, RANDOM pattern, CLKIN = 10MHz		0.28		dB

Deserializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{RCP}	CLK Output Period	$t_{RCP} = t_{TCP}$	CLKOUT	13.3	T	100	ns
t_{RDC}	CLK Output Duty Cycle	SSCG = OFF, 10 – 75 MHz		40	50	60	%
		SSCG = ON, 10 – 20MHz		35	59	65	%
		SSCG = ON, 10 – 65MHz		40	53	60	%
t_{CLH}	LVCMOS Low-to-High Transition Time, *Figure 10*	V_{DDIO} = 1.8V, C_L = 4pF, OS_CLKOUT/ DATA = L	CLKOUT		2.1		ns
		V_{DDIO} = 3.3V C_L = 4pF, OS_CLKOUT/ DATA = H			2.0		ns
t_{CHL}	LVCMOS High-to-Low Transition Time, *Figure 10*	V_{DDIO} = 1.8V, C_L = 4pF, OS_CLKOUT/ DATA = L	CLKOUT		1.6		ns
		V_{DDIO} = 3.3V C_L = 4pF, OS_CLKOUT/ DATA = H			1.5		ns
t_{ROS}	Data Valid before CLKOUT – Set Up Time, *Figure 14*	V_{DDIO} = 1.71 to 1.89V or 3.0 to 3.6V C_L = 4pF (lumped load)	DO[23:0], CO1, CO2, CO3	0.23	0.5		UI
t_{ROH}	Data Valid after CLKOUT – Hold Time, *Figure 14*	V_{DDIO} = 1.71 to 1.89V or 3.0 to 3.6V C_L = 4pF (lumped load)	DO[23:0], CO1, CO2, CO3	0.33	0.5		UI
t_{DDLT}	Deserializer Lock Time, *Figure 13*	SSC[3:0] = OFF, (*Note 6*)	CLKOUT = 10MHz		3		ms
		SSC[3:0] = OFF, (*Note 6*)	CLKOUT = 75MHz		4		ms
		SSC[3:0] = ON, (*Note 6*)	CLKOUT = 10MHz		30		ms
		SSC[3:0] = ON, (*Note 6*)	CLKOUT = 65MHz		6		ms
t_{DD}	Des Delay - Latency, *Figure 11*		CLKOUT = 10 to 75 MHz		139*T	140*T	ns
t_{DPJ}	Des Period Jitter	SSC[3:0] = OFF, (*Note 8*)	CLKOUT = 10 MHz		500	1000	ps
			CLKOUT = 65 MHz		550	1250	ps
			CLKOUT = 75 MHz		435	900	ps
t_{DCCJ}	Des Cycle-to-Cycle Jitter	SSC[3:0] = OFF, (*Note 9*)	CLKOUT = 10 MHz		375	900	ps
			CLKOUT = 65 MHz		500	1150	ps
			CLKOUT = 75 MHz		460	1000	ps
t_{IJT}	Des Input Jitter Tolerance, *Figure 16*	EQ = OFF, SSCG = OFF, CLKOUT = 75 MHz	jitter freq <2MHz		0.9		UI
			jitter freq >6MHz		0.5		UI
BIST Mode							
t_{PASS}	BIST PASS Valid Time, BISTEN = 1, *Figure 17*				1	10	µs

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
SSCG Mode							
f_{DEV}	Spread Spectrum Clocking Deviation Frequency		CLKOUT = 10 to 65 MHz, SSC[3:0] = ON	±0.5		±2	%
f_{MOD}	Spread Spectrum Clocking Modulation Frequency		CLKOUT = 10 to 65 MHz, SSC[3:0] = ON	8		100	kHz

Recommended Timing for the Serial Control Bus

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{SCL}	SCL Clock Frequency	Standard Mode			100	kHz
		Fast Mode			400	kHz
t_{LOW}	SCL Low Period	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
t_{HIGH}	SCL High Period	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
$t_{HD;STA}$	Hold time for a start or a repeated start condition, *Figure 18*	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
$t_{SU:STA}$	Set Up time for a start or a repeated start condition, *Figure 18*	Standard Mode	4.7			µs
		Fast Mode	0.6			µs
$t_{HD;DAT}$	Data Hold Time, *Figure 18*	Standard Mode	0		3.45	µs
		Fast Mode	0		0.9	µs
$t_{SU;DAT}$	Data Set Up Time, *Figure 18*	Standard Mode	250			ns
		Fast Mode	100			ns
$t_{SU;STO}$	Set Up Time for STOP Condition, *Figure 18*	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
t_{BUF}	Bus Free Time Between STOP and START, *Figure 18*	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
t_r	SCL & SDA Rise Time, *Figure 18*	Standard Mode			1000	ns
		Fast Mode			300	ns
t_f	SCL & SDA Fall Time, *Figure 18*	Standard Mode			300	ns
		Fast mode			300	ns

DC and AC Serial Control Bus Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Level	SDA and SCL	2.2		$V_{DD\ 3.3V}$	V
V_{IL}	Input Low Level Voltage	SDA and SCL	GND		0.8	V
V_{HY}	Input Hysteresis			>50		mV
V_{OL}		SDA, IOL = 3mA	0		0.4	V
I_{in}		SDA or SCL, Vin = V_{DDIO} or GND	-15		+15	µA
t_R	SDA RiseTime – READ	SDA, RPU = X, Cb ≤ 400pF		40		ns
t_F	SDA Fall Time – READ			25		ns
$t_{SU;DAT}$	Set Up Time – READ			520		ns
$t_{HD;DAT}$	Hold Up Time – READ			55		ns
t_{SP}	Input Filter			50		ns
C_{in}	Input Capacitance	SDA or SCL		<5		pF

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 2: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 3: Typical values represent most likely parametric norms at V_{DD} = 3.3V, Ta = +25 degC, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 4: Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except VOD, ΔVOD, VTH and VTL which are differential voltages.

Note 5: When the Serializer output is at TRI-STATE the Deserializer will lose PLL lock. Resynchronization / Relock must occur before data transfer require t_{PLD}

Note 6: t_{PLD} and t_{DDLT} is the time required by the serializer and deserializer to obtain lock when exiting power-down state with an active clock.

Note 7: UI – Unit Interval is equivalent to one serialized data bit width (1UI = 1 / 28*CLK). The UI scales with clock frequency.

Note 8: t_{DPJ} is the maximum amount the period is allowed to deviate over many samples.

Note 9: t_{DCCJ} is the maximum amount of jitter between adjacent clock cycles.

Note 10: Supply noise testing was done with minimum capacitors on the PCB. A sinusoidal signal is AC coupled to the V_{DDn} (1.8V) supply with amplitude = 100 mVp-p measured at the device V_{DDn} pins. Bit error rate testing of input to the Ser and output of the Des with 10 meter cable shows no error when the noise frequency on the Ser is less than 750 kHz. The Des on the other hand shows no error when the noise frequency is less than 400 kHz.

Note 11: Specification is guaranteed by characterization and is not tested in production.

Note 12: Specification is guaranteed by design and is not tested in production.

AC Timing Diagrams and Test Circuits

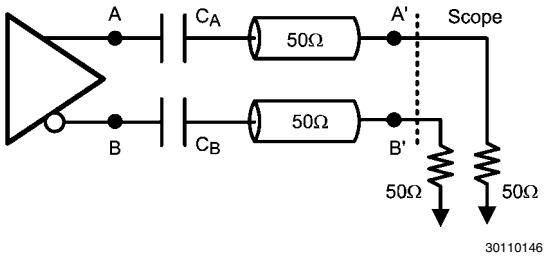


FIGURE 1. Serializer Test Circuit

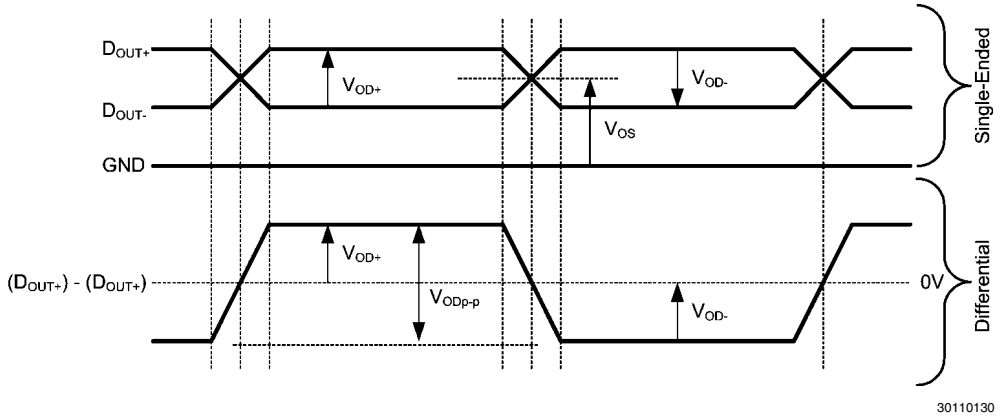


FIGURE 2. Serializer Output Waveforms

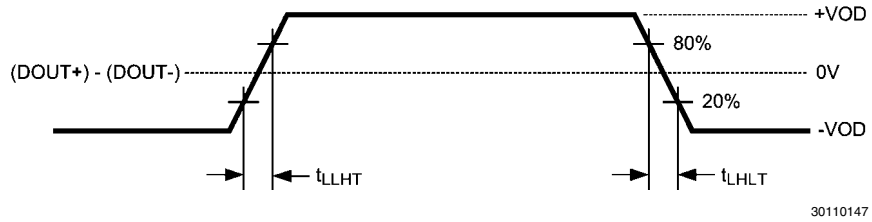


FIGURE 3. Serializer Output Transition Times

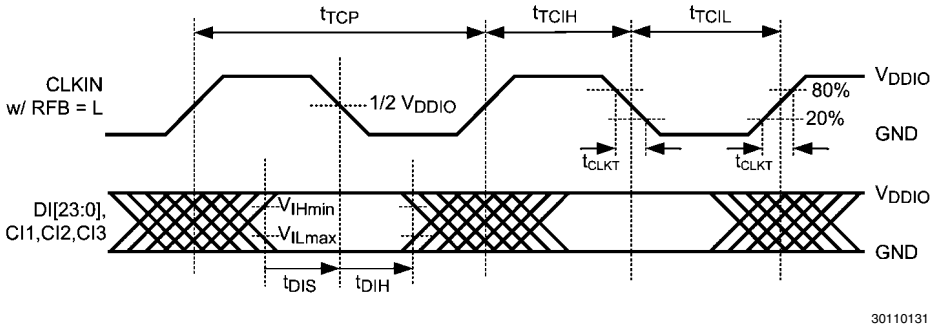


FIGURE 4. Serializer Input CLKIN Waveform and Set and Hold Times

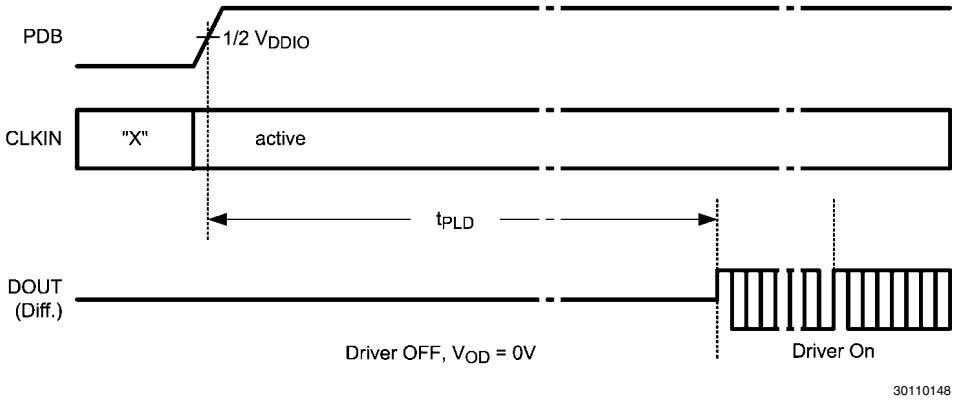


FIGURE 5. Serializer Lock Time

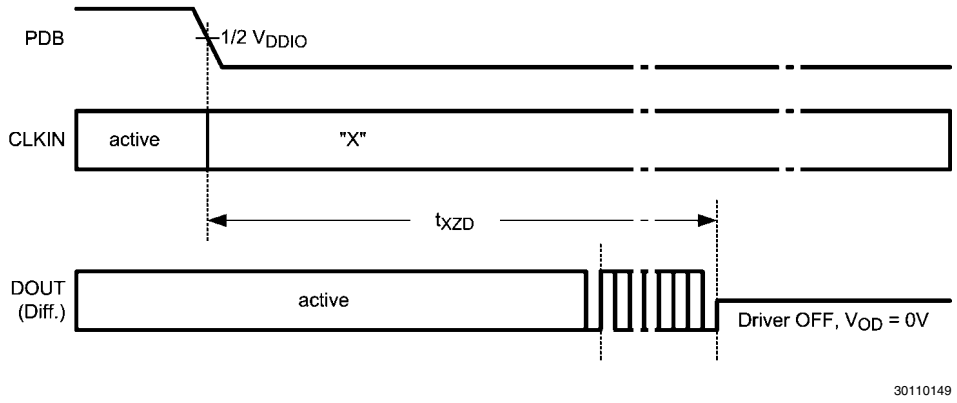


FIGURE 6. Serializer Disable Time

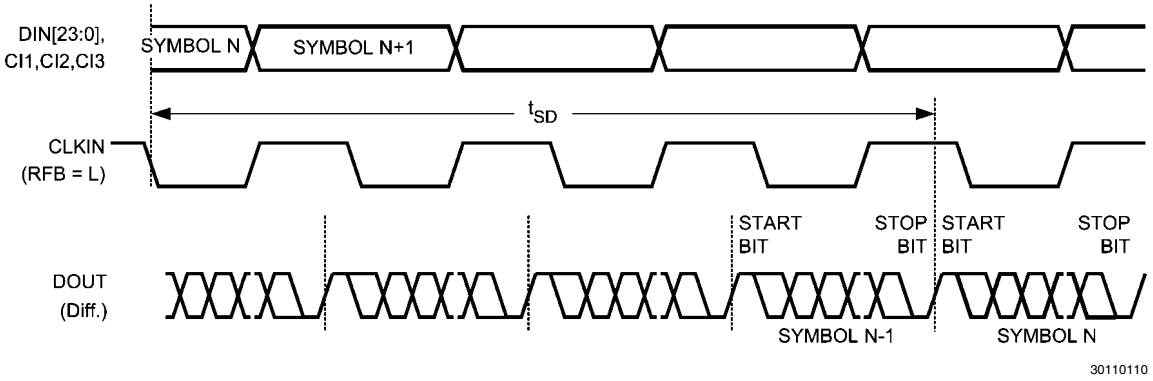


FIGURE 7. Serializer Latency Delay

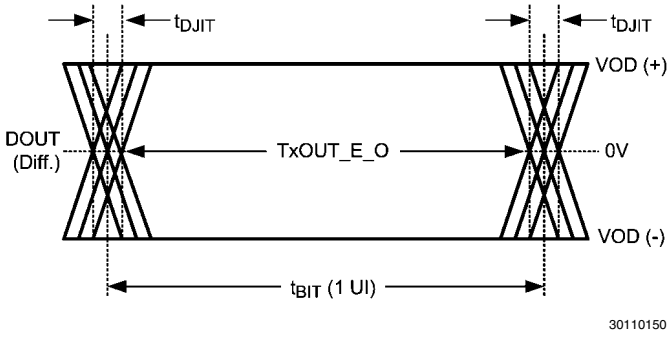


FIGURE 8. Serializer Output Jitter

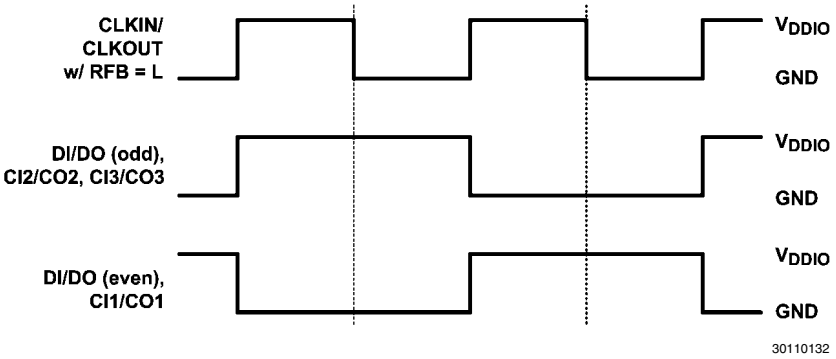


FIGURE 9. Checkerboard Data Pattern

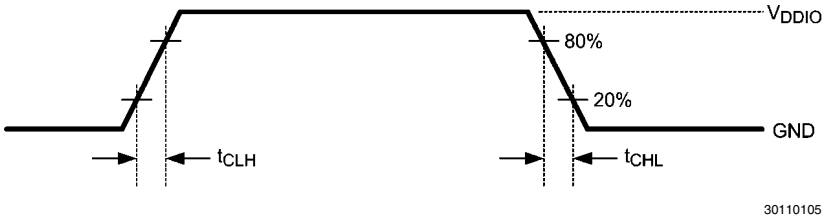


FIGURE 10. Deserializer LVCMOS Transition Times

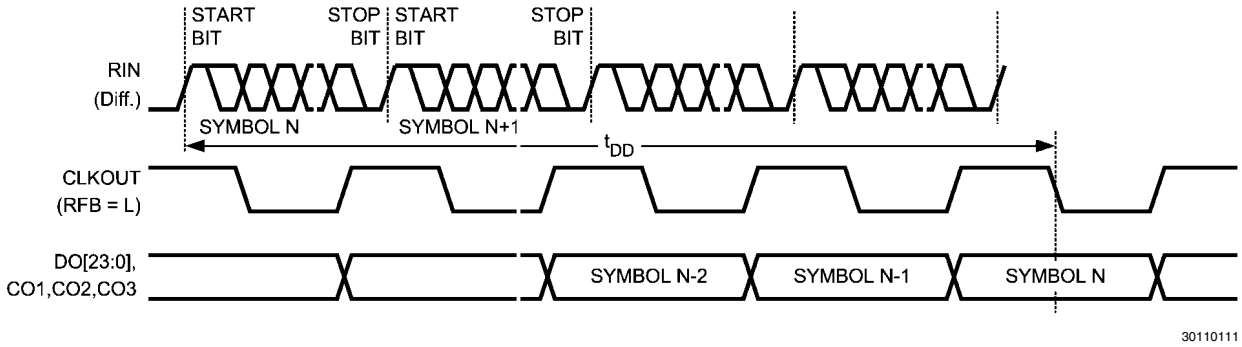


FIGURE 11. Deserializer Delay – Latency

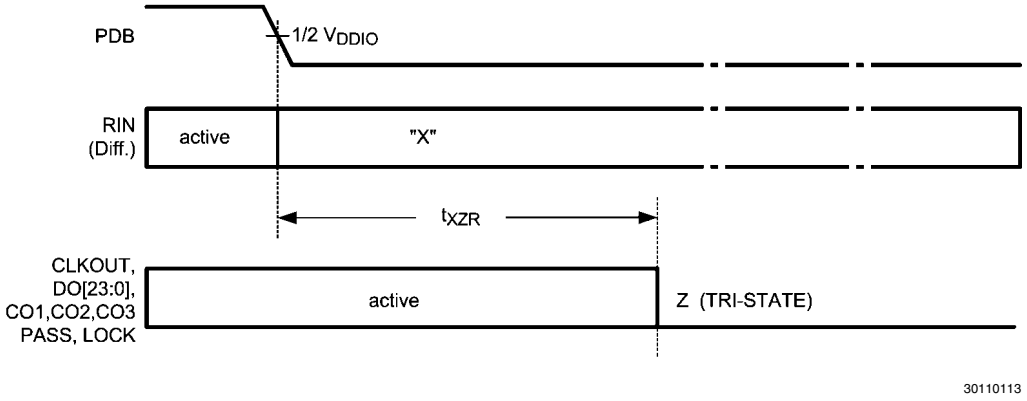


FIGURE 12. Deserializer Disable Time (OSS_SEL = 0)

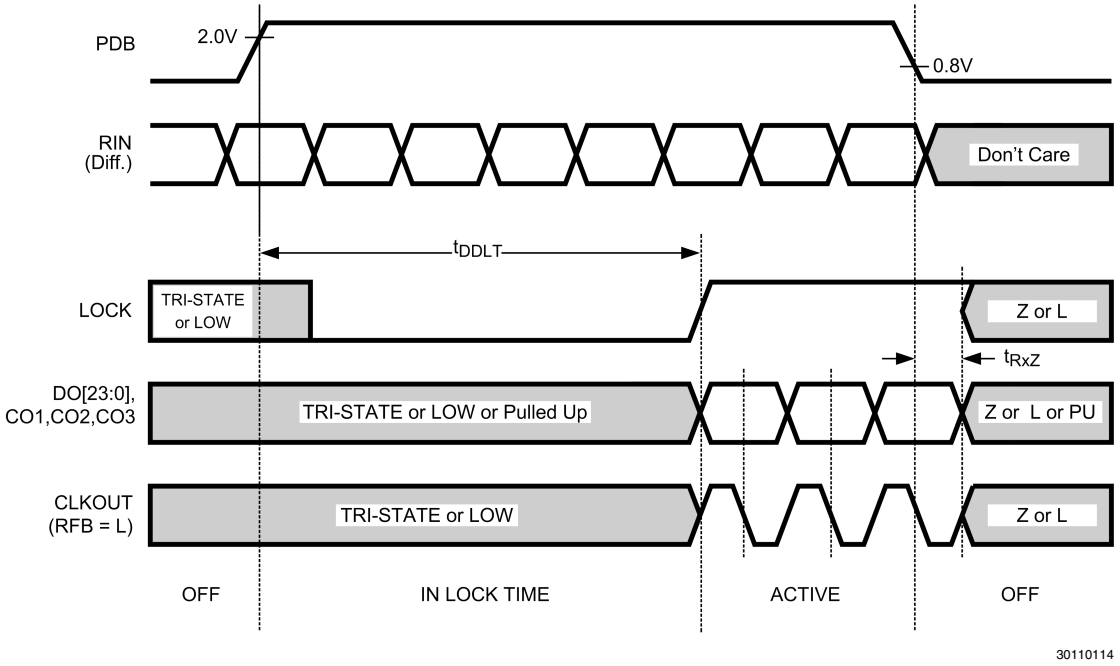


FIGURE 13. Deserializer PLL Lock Times and PDB TRI-STATE™ Delay

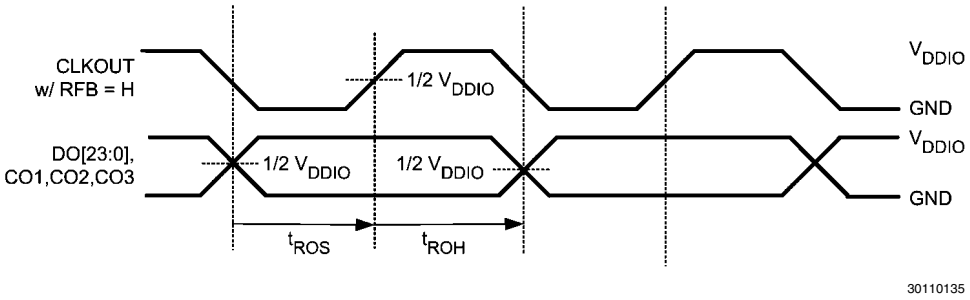


FIGURE 14. Deserializer Output Data Valid (Setup and Hold) Times with SSCG = Off

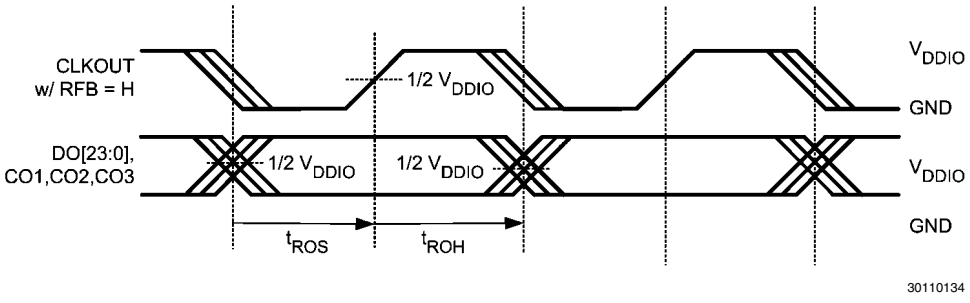


FIGURE 15. Deserializer Output Data Valid (Setup and Hold) Times with SSCG = On

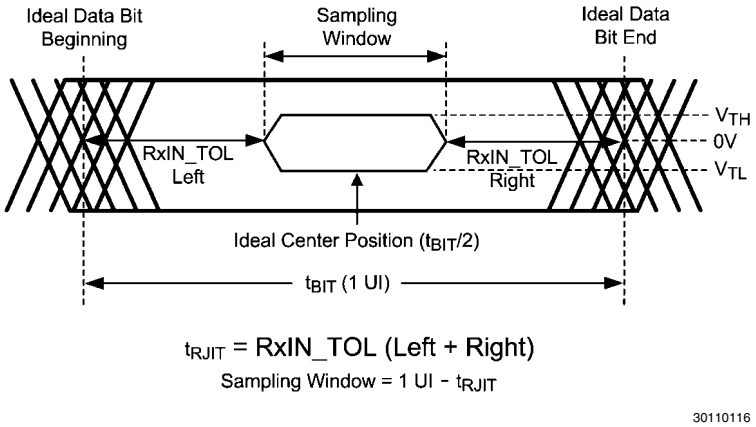


FIGURE 16. Receiver Input Jitter Tolerance

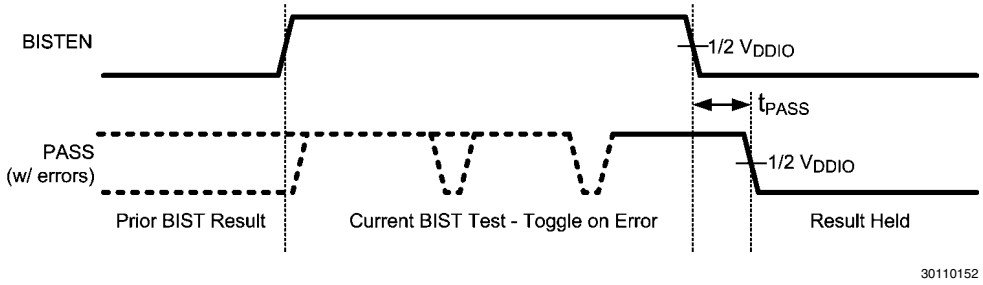


FIGURE 17. BIST PASS Waveform

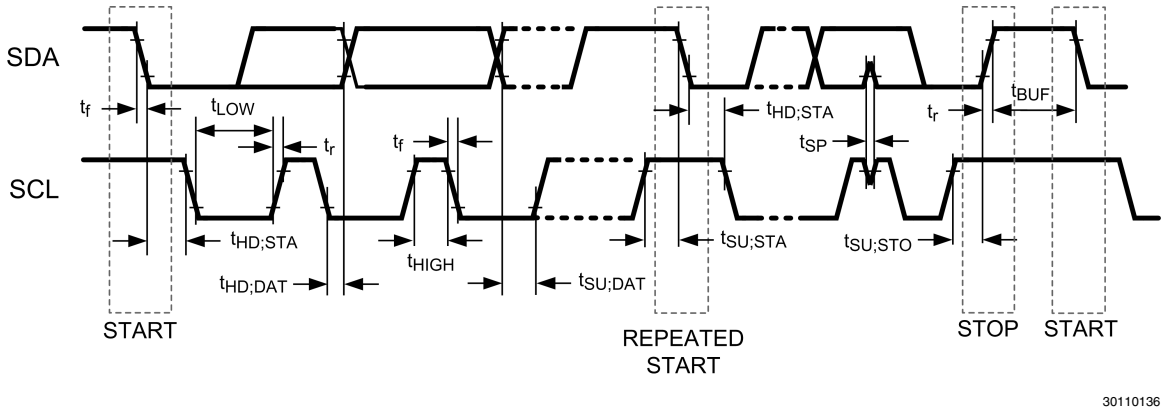


FIGURE 18. Serial Control Bus Timing Diagram

Functional Description

The DS92LV2421 / DS92LV2422 chipset transmits and receives 24-bits of data and 3 control signals over a single serial CML pair operating at 280 Mbps to 2.1 Gbps. The serial stream also contains an embedded clock, video control signals and the DC-balance information which enhances signal quality and supports AC coupling.

The Des can attain lock to a data stream without the use of a separate reference clock source, which greatly simplifies system complexity and overall cost. The Des also synchronizes to the Ser regardless of the data pattern, delivering true automatic “plug and lock” performance. It can lock to the incoming serial stream without the need of special training patterns or sync characters. The Des recovers the clock and data by extracting the embedded clock information, validating and then deserializing the incoming data stream providing a parallel LVCMOS video bus to the display or ASIC/FPGA.

The DS92LV2421 / DS92LV2422 chipset can operate in 24-bit color depth (with DE, HS, VS encoded within the serial data stream). In 18–bit color applications, the three video control signals maybe sent encoded within the serial bit stream (restrictions apply) along with six additional general purpose signals.

Block Diagrams for the chipset are shown at the beginning of this datasheet.

Data Transfer

The DS92LV2421 / DS92LV2422 chipset will transmit and receive a pixel of data in the following format: C1 and C0 represent the embedded clock in the serial stream. C1 is always HIGH and C0 is always LOW. The remaining 26 bit spaces contain the scrambled, encoded and DC-Balanced serial data.

SER & DES OPERATING MODES AND REVERSE COMPATIBILITY (CONFIG[1:0])

The DS92LV2421 / DS92LV2422 chipset is compatible with other single serial lane Channel Link II or FPD-Link II devices. Configuraiton modes are provided for reverse compatibility with the DS90C241 / DS90C124 and also the DS90UR241 / DS90UR124 by setting the respective mode with the CONFIG [1:0] pins on the Ser or Des as shown in Table and Table. This selection also determines whether the Control Signal Filter feature is enabled or disabled in the Normal mode. These configuration modes are selectable the the control pins only.

TABLE 1. DS92LV2421 Ser Modes

CONFIG1	CONFIG0	MODE	DES DEVICE
L	L	Normal Mode, Control Signal Filter disabled	DS92LV2422, DS92LV2412, DS92LV0422, DS92LV0412
L	H	Normal Mode, Control Signal Filter enabled	DS92LV2422, DS92LV2412, DS92LV0422, DS92LV0412
H	L	Reverse Compatibility Mode	DS90UR124, DS99R124
H	H	Reverse Compatibility Mode	DS90C124

TABLE 2. DS92LV2422 Des Modes

CONFIG1	CONFIG0	MODE	SER DEVICE
L	L	Normal Mode, Control Signal Filter disabled	DS92LV2421, DS92LV2411, DS92LV0421, DS92LV0411
L	H	Normal Mode, Control Signal Filter enabled	DS92LV2421, DS92LV2411, DS92LV0421, DS92LV0411
H	L	Reverse Compatibility Mode	DS90UR241, DS99R421
H	H	Reverse Compatibility Mode	DS90C241

VIDEO CONTROL SIGNAL FILTER — SER & DES

When operating the devices in Normal Mode, the Control Signals have the following restrictions:

- Normal Mode with Control Signal Filter Enabled: Control Signal 1 and Control Signal 2 — Only 2 transitions per 130 clock cycles are transmitted, the transition pulse must be 3 parallel clocks or longer.
- Normal Mode with Control Signal Filter Disabled: Control Signal 1 and Control Signal 2 — Only 2 transitions per 130 clock cycles are transmitted, no restriction on minimum transition pulse.
- Control Signal 3 — Only 1 transition per 130 clock cycles is transmitted , minimum pulse width is 130 clock cycles.

Control Signals are defined as low frequency signals with limited transition. Glitches of a control signal can cause a visual error in display applications. This feature allows for the chipset to validate and filter out any high frequency noise on the control signals. See Figure.

SERIALIZER Functional Description

The Ser converts a wide parallel input bus to a single serial output data stream, and also acts as a signal generator for the chipset Built In Self Test (BIST) mode. The device can be configured via external pins or through the optional serial control bus. The Ser features enhance signal quality on the link by supporting: a selectable VOD level, a selectable de-emphasis signal conditioning and also the Channel Link II data coding that provides randomization, scrambling, and DC Balanacing of the data. The Ser includes multiple features to reduce EMI associated with display data transmission. This includes the randomization and scrambling of the data and also the system spread spectrum clock support. The Ser features power saving features with a sleep mode, auto stop clock feature, and optional LVCMOS (1.8 V) parallel bus compatibility.

See also the Functional Description of the chipset's serial control bus and BIST modes.

EMI Reduction Features

Data Randomization & Scrambling

Channel Link II Ser / Des feature a 3 step encoding process which enables the use of AC coupled interconnects and also helps to manage EMI. The serializer first passes the parallel data through a scrambler which randomizes the data. The randomized data is then DC balanced. The DC balanced and randomized data then goes through a bit shuffling circuit and

is transmitted out on the serial line. This encoding process helps to prevent static data patterns on the serial stream. The resulting frequency content of the serial stream ranges from the parallel clock frequency to the nyquist rate. For example, if the Ser / Des chip set is operating at a parallel clock frequency of 75 MHz, the resulting frequency content of serial stream ranges from 75 MHz to 1.05 GHz (75 MHz *28 bits = 2.1 Gbps / 2 = 1.05 GHz).

Ser — Spread Spectrum Compatibility

The Ser CLKIN is capable of tracking spread spectrum clocking (SSC) from a host source. The CLKIN will accept spread spectrum tracking up to 35 kHz modulation and ±0.5, ±1 or ±2% deviations (center spread). The maximum conditions for the CLKIN input are: a modulation frequency of 35 kHz and amplitude deviations of ±2% (4% total).

Integrated Signal Conditioning Features — Ser

Ser — VOD Select (VODSEL)

The Ser differential output voltage may be increased by setting the VODSEL pin High. When VODSEL is Low, the VOD is at the standard (default) level. When VODSEL is High, the VOD is increased in level. The increased VOD is useful in extremely high noise environments and also on extra long cable length applications. When using de-emphasis it is recommended to set VODSEL = H to avoid excessive signal attenuation especially with the larger de-emphasis settings. This feature may be controlled by the external pin or by register.

TABLE 3. Differential Output Voltage

Input	Effect	
VODSEL	VOD mV	VOD mVp-p
H	±420	840
L	±280	560

Ser — De-Emphasis (De-Emph)

The De-Emph pin controls the amount of de-emphasis beginning one full bit time after a logic transition that the Ser drives. This is useful to counteract loading effects of long or lossy cables. This pin should be left open for standard switching currents (no de-emphasis) or if controlled by register. De-emphasis is selected by connecting a resistor on this pin to ground, with R value between 0.5 kΩ to 1 MΩ, or by register setting. When using De-Emphasis it is recommended to set VODSEL = H.

TABLE 4. De-Emphasis Resistor Value

Resistor Value (kΩ)	De-Emphasis Setting
Open	Disabled
0.6	- 12 dB
1.0	- 9 dB
2.0	- 6 dB
5.0	- 3 dB

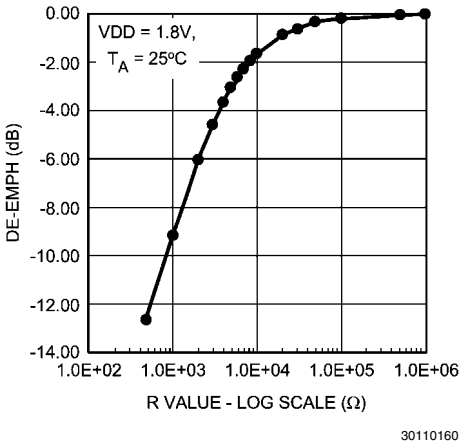


FIGURE 19. De-Emph vs. R value

Power Saving Features

Ser — Power Down Feature (PDB)

The Ser has a PDB input pin to ENABLE or POWER DOWN the device. This pin is controlled by the host and is used to save power, disabling the link when the it is not needed. In the POWER DOWN mode, the high-speed driver outputs are both pulled to VDD and present a 0V VOD state. Note – in POWER DOWN, the optional Serial Bus Control Registers are **RESET**.

Ser — Stop Clock Feature

The Ser will enter a low power SLEEP state when the CLKIN is stopped. A STOP condition is detected when the input clock frequency is less than 3 MHz. The clock should be held at a static Low or high state. When the CLKIN starts again, the Ser will then lock to the valid input clock and then transmits the serial data to the Des. Note – in STOP CLOCK SLEEP, the optional Serial Bus Control Registers values are **RETAINED**.

1.8V or 3.3V VDDIO Operation

The Ser parallel bus and Serial Bus Interface can operate with 1.8 V or 3.3 V levels (V_{DDIO}) for host compatibility. The 1.8 V levels will offer lower noise (EMI) and also a system power savings.

Ser — Pixel Clock Edge Select (RFB)

The RFB pin determines the edge that the data is latched on. If RFB is High, input data is latched on the Rising edge of the CLKIN. If RFB is Low, input data is latched on the Falling edge of the CLKIN. Ser and Des maybe set differently. This feature may be controlled by the external pin or by register.

Optional Serial Bus Control

Please see the following section on the optional Serial Bus Control Interface.

Optional BIST Mode

Please see the following section on the chipset BIST mode for details.

DESERIALIZER Functional Description

The Des converts a single input serial data stream to a wide parallel output bus, and also provides a signal check for the chipset Built In Self Test (BIST) mode. The device can be configured via external pins and strap pins or through the optional serial control bus. The Des features enhance signal quality on the link with an integrated equalizer on the serial input and Channel Link II data encoding which provides randomization, scrambling, and DC balanacing of the data. The Des includes multiple features to reduce EMI associated with data transmission. This includes the randomization and scrambling of the data, the output spread spectrum clock generation (SSCG) support and output clock and data slew rate select. The Des features power saving features with a power down mode, and optional LVCMOS (1.8 V) interface compatibility.

Integrated Signal Conditioning Features — Des

Des — Input Equalizer Gain (EQ)

The Des can enable receiver input equalization of the serial stream to increase the eye opening to the Des input. Note this function cannot be seen at the RxIN+/- input but can be observed at the serial test port (ROUT+/-) enabled via the Serial Bus control registers. The equalization feature may be controlled by the external pin or by register.

TABLE 5. Receiver Equalization Configuration Table

INPUTS				Effect
EQ3	EQ2	EQ1	EQ0	
L	L	L	H	~1.5 dB
L	L	H	H	~3 dB
L	H	L	H	~4.5 dB
L	H	H	H	~6 dB
H	L	L	H	~7.5 dB
H	L	H	H	~9 dB
H	H	L	H	~10.5 dB
H	H	H	H	~12 dB
X	X	X	L	OFF*
* Default Setting is EQ = Off				

EMI Reduction Features

Des — Output Slew Rate Select (OS_CLKOUT/OS_DATA)

The parallel data outputs and clock outputs of the deserializer feature selectable output slew rates. The slew rate of the CLKOUT pin is controlled by the strap pin or register OS_CLKOUT, while the data outputs (DO[23:0] and CO[3:1]) are controlled by the strap pin or register OS_DATA. When OS_CLKOUT/DATA = HIGH, the maxium slew rate is selected. When the OS_CLKOUT/DATA = LOW, the minimum slew rate is selected. Use the higher slew rate when driving longer traces or a heavier capacitive load.

Des — Common Mode Filter Pin (CMF) — Optional

The Des provides access to the center tap of the internal termination. A capacitor may be placed on this pin for additional common-mode filtering of the differential pair. This can be useful in high noise environments for additional noise rejection capability. A 4.7 µF capacitor may be connected to this pin to Ground.

Des — SSCG Generation — Optional

The Des provides an internally generated spread spectrum clock (SSCG) to modulate its outputs. Both clock and data outputs are modulated. This will aid to lower system EMI. Output SSCG deviations to ±2% (4% total) at up to 100 kHz modulations is available. Note: The device supports SSCG function with CLK = 10 MHz to 65 MHz. When the CLK = 65 MHz to 75 MHz, it is required to disable SSCG function (SSC [3:0] = 0000). See *Table 6*. This feature may be controlled by external STRAP pins or by register.

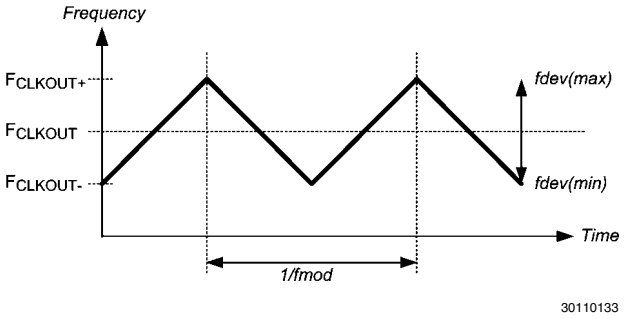


FIGURE 20. SSCG Waveform

TABLE 6. SSCG Configuration (LF_MODE = L) — Des Output

SSC[3:0] Inputs LF_MODE = L (20 - 65 MHz)				Result	
SSC3	SSC2	SSC1	SSC0	fdev (%)	fmod (kHz)
L	L	L	L	NA	Disable
L	L	L	H	±0.5	CLK/2168
L	L	H	L	±1.0	
L	L	H	H	±1.5	
L	H	L	L	±2.0	
L	H	L	H	±0.5	CLK/1300
L	H	H	L	±1.0	
L	H	H	H	±1.5	
H	L	L	L	±2.0	
H	L	L	H	±0.5	CLK/868
H	L	H	L	±1.0	
H	L	H	H	±1.5	
H	H	L	L	±2.0	
H	H	L	H	±0.5	CLK/650
H	H	H	L	±1.0	
H	H	H	H	±1.5	

TABLE 7. SSCG Configuration (LF_MODE = H) — Des Output

SSC[3:0] Inputs LH_MODE = H (10 - 20 MHz)				Result	
SSC3	SSC2	SSC1	SSC0	fdev (%)	fmod (kHz)
L	L	L	L	NA	Disable
L	L	L	H	±0.5	CLK/620
L	L	H	L	±1.0	
L	L	H	H	±1.5	
L	H	L	L	±2.0	
L	H	L	H	±0.5	CLK/370
L	H	H	L	±1.0	
L	H	H	H	±1.5	
H	L	L	L	±2.0	
H	L	L	H	±0.5	CLK/258
H	L	H	L	±1.0	
H	L	H	H	±1.5	
H	H	L	L	±2.0	
H	H	L	H	±0.5	CLK/192
H	H	H	L	±1.0	
H	H	H	H	±1.5	

1.8V or 3.3V VDDIO Operation

The Des parallel bus and Serial Bus Interface can operate with 1.8 V or 3.3 V levels (V_{DDIO}) for target (Display) compatibility. The 1.8 V levels will offer a lower noise (EMI) and also a system power savings.

Power Saving Features

Des — PowerDown Feature (PDB)

The Des has a PDB input pin to ENABLE or POWER DOWN the device. This pin can be controlled by the system to save power, disabling the Des when the display is not needed. An auto detect mode is also available. In this mode, the PDB pin is tied High and the Des will enter POWER DOWN when the serial stream stops. When the serial stream starts up again, the Des will lock to the input stream and assert the LOCK pin and output valid data. In POWER DOWN mode, the Data and CLKOUT output states are determined by the OSS_SEL status. Note – in POWER DOWN, the optional Serial Bus Control Registers are **RESET**.

Des — Stop Stream SLEEP Feature

The Des will enter a low power SLEEP state when the input serial stream is stopped. A STOP condition is detected when

the embedded clock bits are not present. When the serial stream starts again, the Des will then lock to the incoming signal and recover the data. Note – in STOP STREAM SLEEP, the optional Serial Bus Control Registers values are **RETAINED**.

Des — CLOCK-DATA RECOVERY STATUS FLAG (LOCK) and OUTPUT STATE SELECT (OSS_SEL)

When PDB is driven HIGH, the CDR PLL begins locking to the serial input and LOCK goes from TRI-STATE to LOW (depending on the value of the OSS_SEL setting). After the DS92LV2422 completes its lock sequence to the input serial data, the LOCK output is driven HIGH, indicating valid data and clock recovered from the serial input is available on the parallel bus and clock outputs. The CLKOUT output is held at its current state at the change from OSC_CLK (if this is enabled via OSC_SEL) to the recovered clock (or vice versa).

If there is a loss of clock from the input serial stream, LOCK is driven Low and the state of the outputs are based on the OSS_SEL setting (STRAP PIN configuration or register).

Des — Oscillator Output — Optional

The Des provides an optional clock output when the input clock (serial stream) has been lost. This is based on an internal oscillator. The frequency of the oscillator may be selected. This feature may be controlled by the external pin or by register. See *Table 9* and *Table 10*.

TABLE 8. OSS_SEL and PDB Configuration — Des Outputs

INPUTS			OUTPUTS			
Serial Input	**PDB**	**OSS_SEL**	**CLKOUT**	**DO[23:0], CO1, CO2, CO3**	**LOCK**	**PASS**
X	L	L	Z	Z	Z	Z
X	L	H	L	L	L	H
Static	H	L	Z	Z	L	H
Static	H	H	L	L	L	H
Active	H	X	Active	Active	H	H

TABLE 9. OSC (Oscillator) Mode — Des Output

INPUTS	OUTPUTS			
Embedded CLK	**CLKOUT**	**DO[23:0]/CO1/CO2/CO3**	**LOCK**	**PASS**
NOTE *	OSC Output	L	L	H
Present	Toggling	Active	H	H
* NOTE — Absent and OSC_SEL ≠ 000				

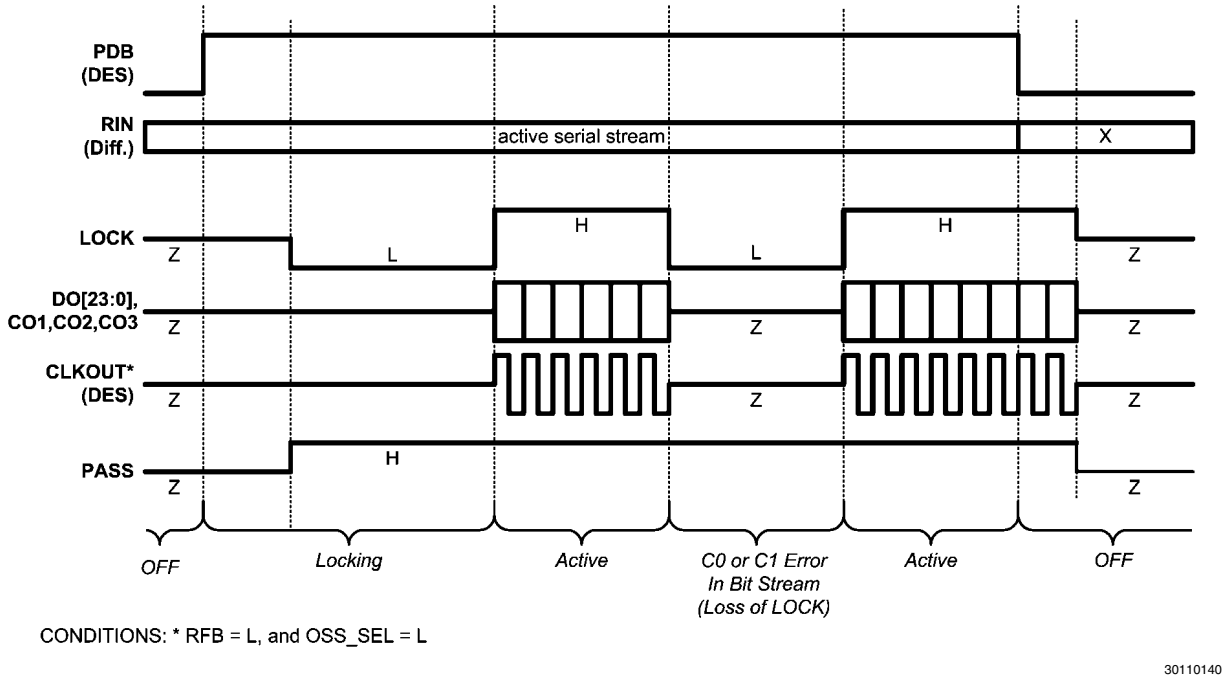


FIGURE 21. Des Outputs with Output State Select Low (OSS_SEL = L)

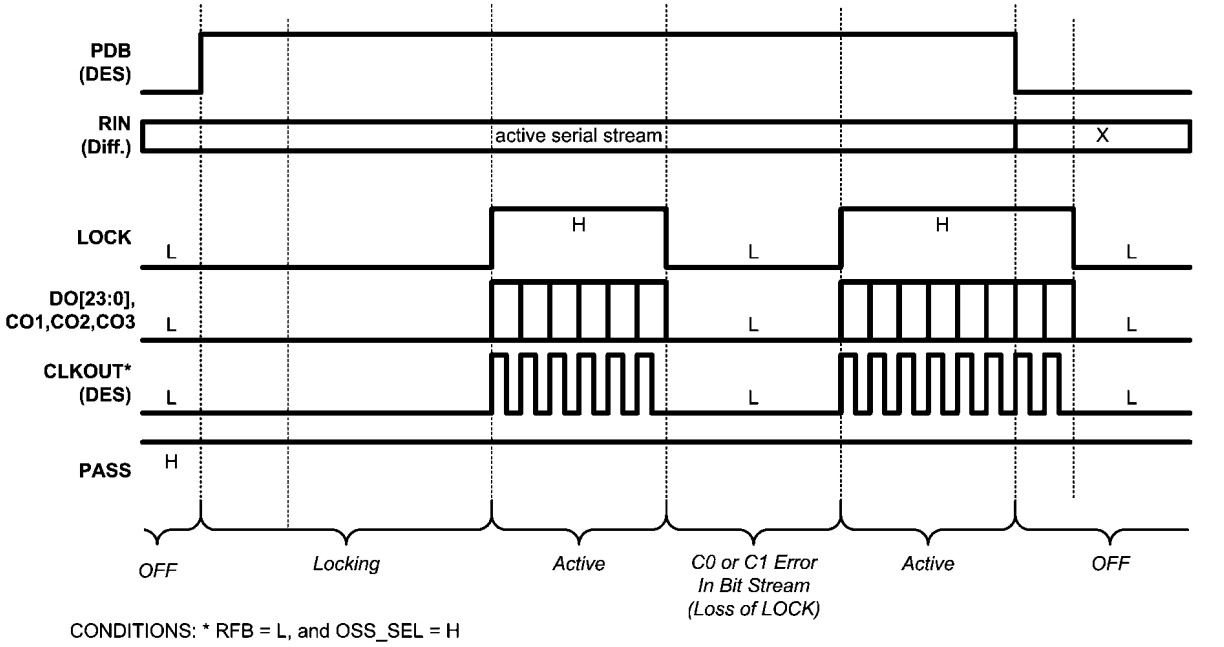
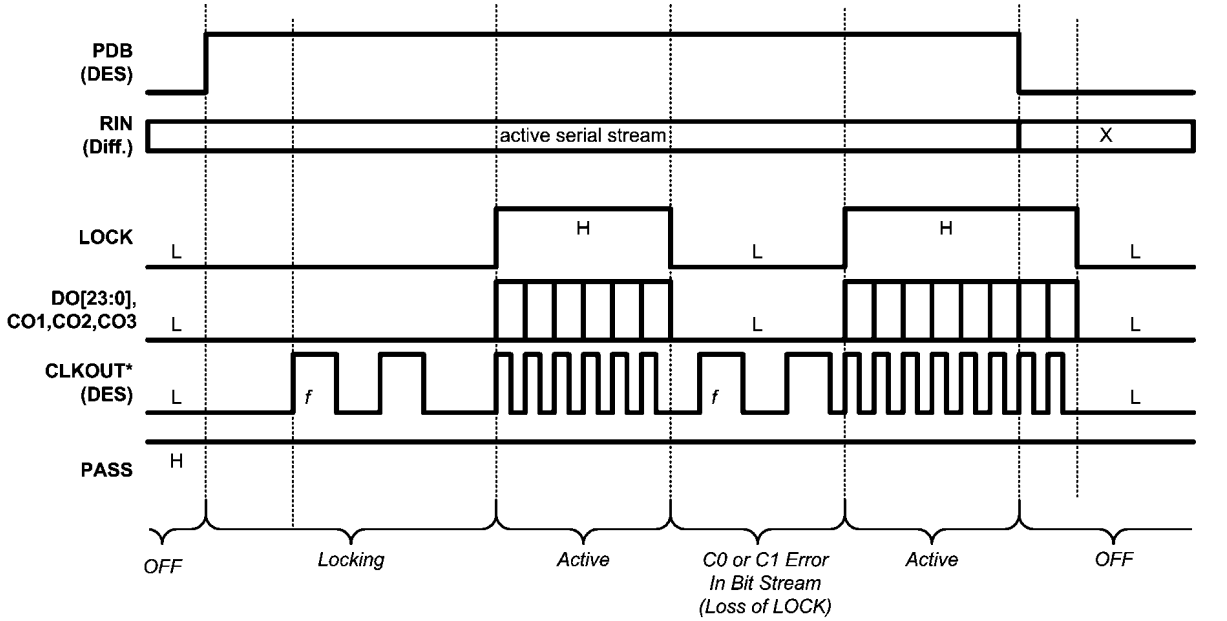


FIGURE 22. Des Outputs with Output State Select High (OSS_SEL = H)

TABLE 10. OSC_SEL (Oscillator) Configuration

OSC_SEL[2:0] INPUTS			CLKOUT Oscillator Frequency
OSC_SEL2	OSC_SEL1	OSC_SEL0	
L	L	L	Off – Feature Disabled – Default
L	L	H	50 MHz ±40%
L	H	L	25 MHz ±40%
L	H	H	16.7 MHz ±40%
H	L	L	12.5 MHz ±40%
H	L	H	10 MHz ±40%
H	H	L	8.3 MHz ±40%
H	H	H	6.3 MHz ±40%



CONDITIONS: * RFB = L, OSS_SEL = H , and OSC_SEL not equal to 000.

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FIGURE 23. Des Outputs with Output State High and CLK Output Oscillator Option Enabled

Des — OP_LOW — Optional

The OP_LOW feature is used to hold the LVCMOS outputs, except for the LOCK output, at a LOW state. When the OP_LOW feature is enabled, the LVCMOS outputs will be held at logic LOW while LOCK = LOW. The user must toggle the OP_LOW Set/Reset register bit to release the outputs to the normal toggling state. Note that the release of the outputs can only occur when LOCK is HIGH. The OP_LOW strap option is assigned to the PASS pin, at pin location 42.

Restrictions on other straps:

1. Other strap options should not be used in order to keep the data and clock outputs at a true logic LOW state. Other features should be selected through the I2C register interface.
2. The OSS_SEL feature is not available when OP_LOW is enabled.

Outputs DO[23:0], CO[3:1] and CLKOUT are in TRI-STATE™ before PDB toggles HIGH because the OP-LOW strap value has not been recognized until the DS92LV2422 powers up. *Figure 24* shows the user controlled release of the OP_LOW and automatic reset of OP_LOW set on the falling edge of LOCK. *Figure 25* shows the user controlled release of OP_LOW and manual reset of OP_LOW set. Note manual reset of OP_LOW can only occur when LOCK is HIGH.

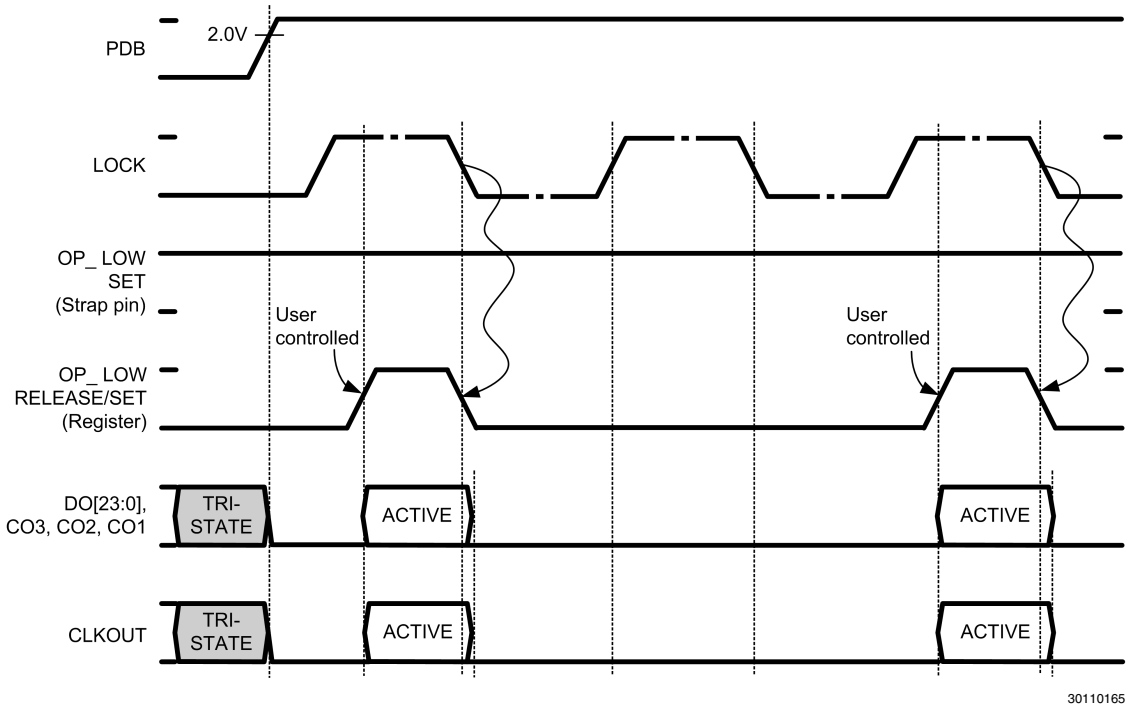


FIGURE 24. OP_LOW Auto Set

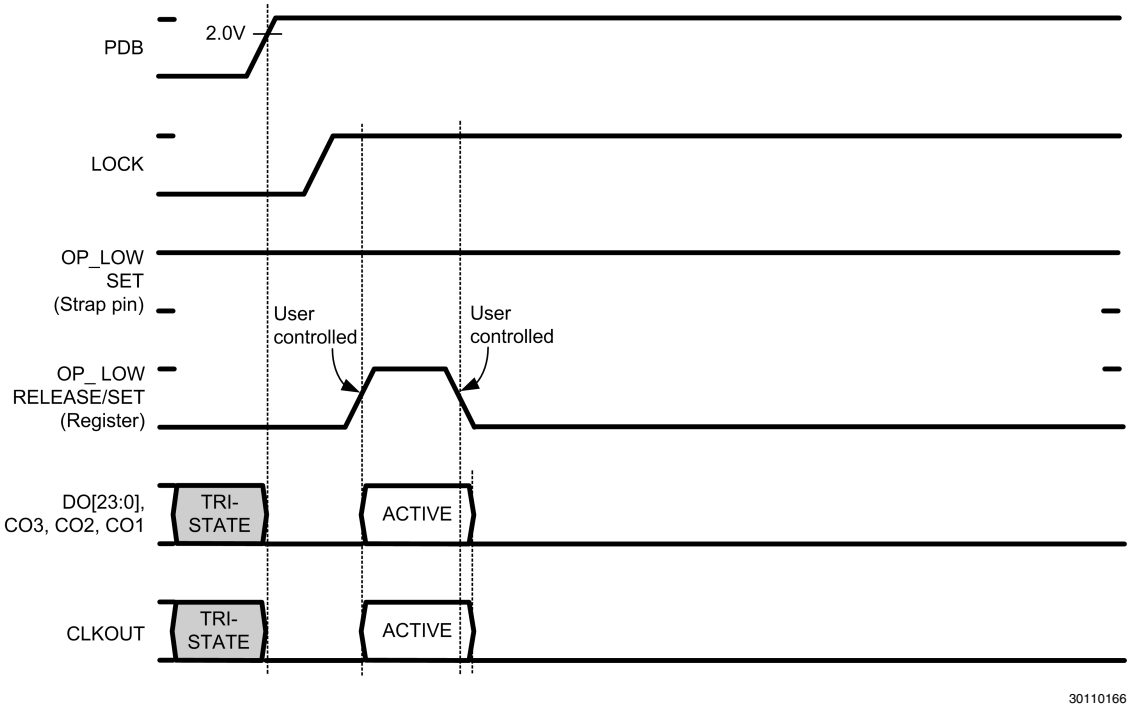


FIGURE 25. OP_LOW Manual Set/Reset

Des — Clock Edge Select (RFB)

The RFB pin determines the edge that the data is strobed on. If RFB is High, output data is strobed on the Rising edge of the CLKOUT. If RFB is Low, data is strobed on the Falling edge of the CLKOUT. This allows for inter-operability with downstream devices. The Des output does not need to use the same edge as the Ser input. This feature may be controlled by the external pin or by register.

Des — Control Signal Filter — Optional

The deserializer provides an optional Control Signal (C3, C2, C1) filter that monitors the three control signals and eliminates any pulses or glitches that are 1 or 2 parallel clock periods wide. Control signals must be 3 parallel clock periods wide (in its HIGH or LOW state, regardless of which state is active). This is set by the CONFIG[1:0] strap option or by I2C register control.

Des — SSCG Low Frequency Optimization (LF_Mode)

Text to come. This feature may be controlled by the external pin or by Register.

Des — Strap Input Pins

Configuration of the device maybe done via configuration input pins and the STRAP input pins, or via the Serial Control Bus. The STRAP input pins share select parallel bus output pins. They are used to load in configuration values during the initial power up sequence of the device. Only a pull-up on the pin is required when a HIGH is desired. By default the pad has an internal pull down, and will bias Low by itself. The recommended value of the pull up is 10 kΩ to V_{DDIO}; open (NC) for Low, no pull-down is required (internal pull-down). If using the Serial Control Bus, no pull ups are required.

Optional Serial Bus Control

Please see the following section on the optional Serial Bus Control Interface.

Optional BIST Mode

Please see the following section on the chipset BIST mode for details.

Built In Self Test (BIST)

An optional At-Speed Built In Self Test (BIST) feature supports the testing of the high-speed serial link. This is useful in the prototype stage, equipment production, in-system test and also for system diagnostics. In the BIST mode only a input clock is required along with control to the Ser and Des BISTEN input pins. The Ser outputs a test pattern (PRBS7) and drives the link at speed. The Des detects the PRBS7 pattern and monitors it for errors. A PASS output pin toggles to flag any payloads that are received with 1 to 24 errors. Upon completion of the test, the result of the test is held on the PASS output until reset (new BIST test or Power Down). A high on PASS indicates NO ERRORS were detected. A Low on PASS indicates one or more errors were detected. The duration of the test is controlled by the pulse width applied to the Des BISTEN pin.

Inter-operability is supported between this Channel Link II device and all Channel Link II generations (Gen 1/2/3) — see respective datasheets for details on entering BIST mode and control.

Sample BIST Sequence

See *Figure 26* for the BIST mode flow diagram.

Step 1: Place the DS92LV2421 Ser in BIST Mode by setting Ser BISTEN = H. For the DS92LV2421 Ser or DS99R421 Channel Link II Ser BIST Mode is enabled via the BISTEN pin. A CLKIN is required for BIST. When the Des detects the BIST mode pattern and command (DCA and DCB code) the data and control signal outputs are shut off.

Step 2: Place the DS92LV2422 Des in BIST mode by setting the BISTEN = H. The Des is now in the BIST mode and checks the incoming serial payloads for errors. If an error in the payload (1 to 24) is detected, the PASS pin will switch low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.

Step 3: To Stop the BIST mode, the Des BISTEN pin is set Low. The Des stops checking the data and the final test result is held on the PASS pin. If the test ran error free, the PASS output will be High. If there was one or more errors detected, the PASS output will be Low. The PASS output state is held until a new BIST is run, the device is RESET, or Powered Down. The BIST duration is user controlled by the duration of the BISTEN signal.

Step 4: To return the link to normal operation, the Ser BISTEN input is set Low. The Link returns to normal operation.

Figure 27 shows the waveform diagram of a typical BIST test for two cases. Case 1 is error free, and Case 2 shows one with multiple errors. In most cases it is difficult to generate errors due to the robustness of the link (differential data transmission etc.), thus they may be introduced by greatly extending the cable length, faulting the interconnect, reducing signal condition enhancements (De-Emphasis, VODSEL, or Rx Equalization).

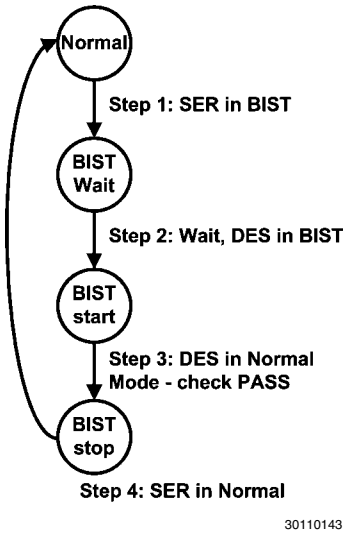


FIGURE 26. BIST Mode Flow Diagram

BER Calculations

It is possible to calculate the approximate Bit Error Rate (BER). The following is required:

- Clock Frequency (MHz)
- BIST Duration (seconds)
- BIST test Result (PASS)

The BER is less than or equal to one over the product of 24 times the CLK rate times the test duration. If we assume a 65 MHz clock, a 10 minute (600 second) test, and a PASS, the BERT is ≤ 1.07 X 10E-12

The BIST mode runs a check on the data payload bits. The LOCK pin also provides a link status. It the recovery of the C0 and C1 bits does not reconstruct the expected clock signal, the LOCK pin will switch Low. The combination of the LOCK and At-Speed BIST PASS pin provides a powerful tool for system evaluation and performance monitoring.

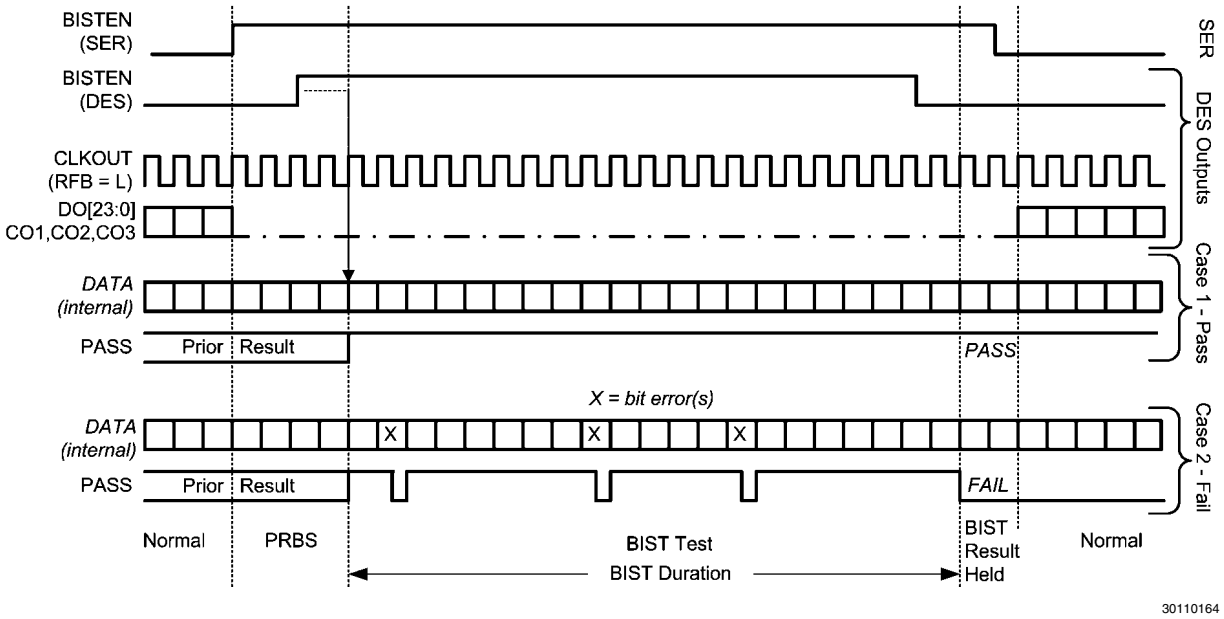


FIGURE 27. BIST Waveforms

Optional Serial Bus Control

The Ser and Des may also be configured by the use of a serial control bus that is I2C protocol compatible. By default, the I2C reg_0x00'h is set to 00'h and all configuration is set by control/strap pins. A write of 01'h to reg_0x00'h will enable/allow configuration by registers; this will override the control/strap pins. Multiple devices may share the serial control bus since multiple addresses are supported. See *Figure 28*.

The serial bus is comprised of three pins. The SCL is a Serial Bus Clock Input. The SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pull up resistor to V_{DDIO}. For most applications a 4.7 k pull up resistor to V_{DDIO} may be used. The resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled High, or driven Low.

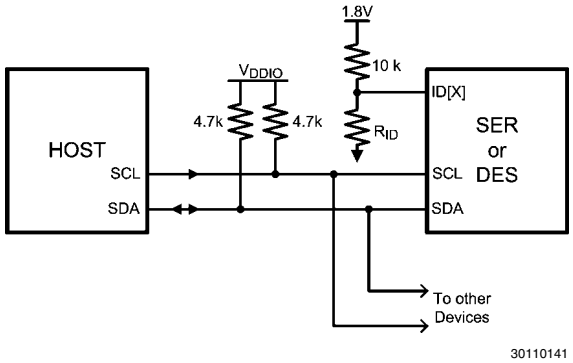


FIGURE 28. Serial Control Bus Connection

The third pin is the ID[X] pin. This pin sets one of five possible device addresses. Three different connections are possible. The pin may be tied to ground. The pin may be pulled to V_{DD} (**1.8V, NOT V_{DDIO}**)) with a 10 kΩ resistor. Or a 10 kΩ pull up resistor (to V_{DD} **1.8V, NOT V_{DDIO}**)) and a pull down resistor of the recommended value to set other three possible addresses may be used. See *Table 11* for the Ser and *Table 12* for the Des.

The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SCL transitions Low while SDA is High. A STOP occurs when SDA transition High while SCL is also HIGH. See *Figure 29*

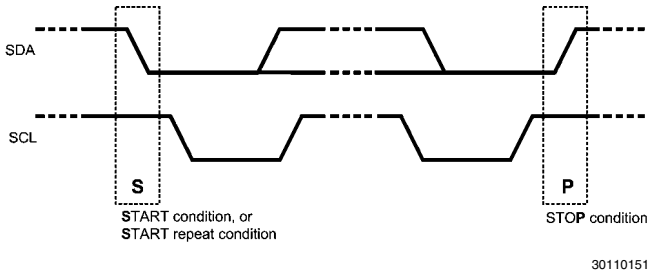


FIGURE 29. START and STOP Conditions

To communicate with a remote device, the host controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit (ACK). If a slave on the bus is addressed correctly, it Acknowledges (ACKs) the master by driving the SDA bus low. If the address doesn't match a device's slave address, it Not-acknowledges (NACKs) the master by letting SDA be pulled High. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a Start condition or a Repeated Start condition. All communication on the bus ends with a Stop condition. A READ is shown in *Figure 30* and a WRITE is shown in *Figure 31*.

If the Serial Bus is not required, the three pins may be left open (NC).

TABLE 11. ID[x] Resistor Value – DS92LV2421 Ser

Resistor RID kΩ	Address 7'b	Address 8'b 0 appended (WRITE)
0.47	7b' 110 1001 (h'69)	8b' 1101 0010 (h'D2)
2.7	7b' 110 1010 (h'6A)	8b' 1101 0100 (h'D4)
8.2	7b' 110 1011 (h'6B)	8b' 1101 0110 (h'D6)
Open	7b' 110 1110 (h'6E)	8b' 1101 1100 (h'DC)

TABLE 12. ID[x] Resistor Value – DS92LV2422 Des

Resistor RID kΩ	Address 7'b	Address 8'b 0 appended (WRITE)
0.47	7b' 111 0001 (h'71)	8b' 1110 0010 (h'E2)
2.7	7b' 111 0010 (h'72)	8b' 1110 0100 (h'E4)
8.2	7b' 111 0011 (h'73)	8b' 1110 0110 (h'E6)
Open	7b' 111 0110 (h'76)	8b' 1110 1100 (h'EC)

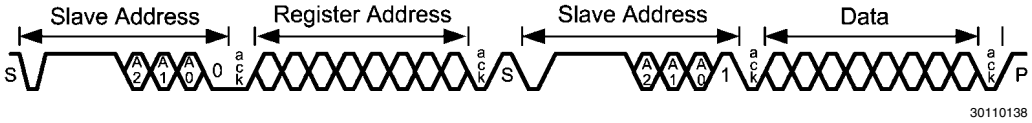


FIGURE 30. Serial Control Bus — READ

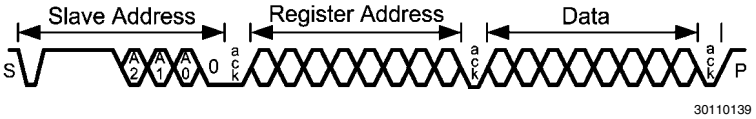


FIGURE 31. Serial Control Bus — WRITE

TABLE 13. SERIALIZER — Serial Bus Control Registers

ADD (dec)	ADD (hex)	Register Name	Bit(s)	R/W	Default (bin)	Function	Description
0	0	Ser Config 1	7	R/W	0	***Reserved***	***Reserved***
			6	R/W	0	***Reserved***	***Reserved***
			5	R/W	0	RFB	0: Data latched on Falling edge of CLKIN 1: Data latched on Rising edge of CLKIN
			4	R/W	0	VODSEL	0: Low 1: High
			3:2	R/W	00	CONFIG	00: Control Signal Filter Disabled 01: Control Signal Filter Enabled 10: Reserved 11: Reserved
			1	R/W	0	SLEEP	Note – not the same function as $\overline{\text{PowerDown}}$ (PDB) 0: normal mode 1: Sleep Mode – **Register settings retained.**
			0	R/W	0	REG	0: Configurations set from control pins 1: Configuration set from registers (except I2C_ID)
1	1	Device ID	7	R/W	0	REG ID	0: Address from ID[X] Pin 1: Address from Register
			6:0	R/W	1101 000	ID[X]	Serial Bus Device ID, Four IDs are: 7b '1101 001 (h'69) 7b '1101 010 (h'6A) 7b '1101 011 (h'6B) 7b '1101 110 (h'6E) All other addresses are ***Reserved***.
2	2	De-Emphasis Control	7:5	R/W	000	De-E Setting	000: set by external Resistor 001: -1 dB 010: -2 dB 011: -3.3 dB 100: -5 dB 101: -6.7 dB 110: -9 dB 111: -12 dB
			4	R/W	0	De-E EN	0: De-Emphasis Enabled 1: De-Emphasis Disabled
			3:0	R/W	000	***Reserved***	***Reserved***

TABLE 14. DESERIALIZER — Serial Bus Control Registers

ADD (dec)	ADD (hex)	Register Name	Bit(s)	R/W	Default (bin)	Function	Description
0	0	Des Config 1	7	R/W	0	LF_MODE	0: 20 to 65 MHz SSCG Operation 1: 10 to 20 MHz SSCG Operation
			6	R/W	0	OS_CLKOUT	0: Normal CLKOUT Slew Rate 1: Increased CLKOUT Slew Rate
			5	R/W	0	OS_DATA	0: Normal DATA Slew Rate 1: Increased DATA Slew Rate
			4	R/W	0	RFB	0: Data strobed on Falling edge of CLKOUT 1: Data strobed on Rising edge of CLKOUT
			3:2	R/W	00	CONFIG	00: Normal Mode, Control Signal Filter Disabled 01: Normal Mode, Control Signal Filter Enabled 10: Reserved 11: Reserved
			1	R/W	0	SLEEP	Note – not the same function as $\overline{\text{PowerDown}}$ (PDB) 0: Normal Mode 1: Sleep Mode – **Register settings retained.**
			0	R/W	0	REG Control	0: Configurations set from control pins / STRAP pins 1: Configurations set from registers (except I2C_ID)
1	1	Slave ID	7	R/W	0		0: Address from ID[X] Pin 1: Address from Register
			6:0	R/W	1110 000	ID[X]	Serial Bus Device ID, Four IDs are: 7b '1110 001 (h'71) 7b '1110 010 (h'72) 7b '1110 011 (h'73) 7b '1110 110 (h'76) All other addresses are ***Reserved***.
2	2	Des Features 1	7	R/W	0	OP_LOW	0: Set outputs state LOW (except LOCK) 1: Release output LOW state, outputs toggling normally **Note: This register only workds during LOCK = 1**
			6	R/W	0	OSS_SEL	Output Sleep State Select 0: CLKOUT, DO[23:0], CO1, CO2, CO3 = Tri-State, LOCK = Normal, PASS = H 1: CLKOUT, DO[23:0], CO1, CO2, CO3 = L, LOCK = Normal, PASS = H
			5:4	R/W	00	***Reserved***	***Reserved***
			3	R/W	0	OP_LOW Strap Bypass	0: Strap will determine whether OP_LOW feature is ON or OFF 1: Turns OFF OP_LOW feature
			2:0	R/W	00	OSC_SEL	000: disable 001: 50 MHz ±40% 010: 25 MHz ±40% 011: 16.7 MHz ±40% 100: 12.5 MHz ±40% 101: 10 MHz ±40% 110: 8.3 MHz ±40% 111: 6.3 MHz ±40%

ADD (dec)	ADD (hex)	Register Name	Bit(s)	R/W	Default (bin)	Function	Description
3	3	Des Features 2	7:5	R/W	000	EQ Gain	000: ~1.625 dB 001: ~3.25 dB 010: ~4.87 dB 011: ~6.5 dB 100: ~8.125 dB 101: ~9.75 dB 110: ~11.375 dB 111: ~13 dB
			4	R/W	0	EQ Enable	0: EQ = disable 1: EQ = enable
			3:0	R/W	0000	SSC	**IF LF_MODE = 0, then**: 000: SSCG disable 0001: fdev = ±0.5%, fmod = CLK/2168 0010: fdev = ±1.0%, fmod = CLK/2168 0011: fdev = ±1.5%, fmod = CLK/2168 0100: fdev = ±2.0%, fmod = CLK/2168 0101: fdev = ±0.5%, fmod = CLK/1300 0110: fdev = ±1.0%, fmod = CLK/1300 0111: fdev = ±1.5%, fmod = CLK/1300 1000: fdev = ±2.0%, fmod = CLK/1300 1001: fdev = ±0.5%, fmod = CLK/868 1010: fdev = ±1.0%, fmod = CLK/868 1011: fdev = ±1.5%, fmod = CLK/868 1100: fdev = ±2.0%, fmod = CLK/868 1101: fdev = ±0.5%, fmod = CLK/650 1110: fdev = ±1.0%, fmod = CLK/650 1111: fdev = ±1.5%, fmod = CLK/650 **IF LF_MODE = 1, then**: 000: SSCG disable 0001: fdev = ±0.5%, fmod = CLK/620 0010: fdev = ±1.0%, fmod = CLK/620 0011: fdev = ±1.5%, fmod = CLK/620 0100: fdev = ±2.0%, fmod = CLK/620 0101: fdev = ±0.5%, fmod = CLK/370 0110: fdev = ±1.0%, fmod = CLK/370 0111: fdev = ±1.5%, fmod = CLK/370 1000: fdev = ±2.0%, fmod = CLK/370 1001: fdev = ±0.5%, fmod = CLK/258 1010: fdev = ±1.0%, fmod = CLK/258 1011: fdev = ±1.5%, fmod = CLK/258 1100: fdev = ±2.0%, fmod = CLK/258 1101: fdev = ±0.5%, fmod = CLK/192 1110: fdev = ±1.0%, fmod = CLK/192 1111: fdev = ±1.5%, fmod = CLK/192
4	4	ROUT Config	7	R/W	0	Repeater Enable	0: Output ROUT+/- = disable 1: Output ROUT+/- = enable
			6:0	R/W	0000 000	***Reserved***	***Reserved***

Applications Information

DISPLAY APPLICATION

The DS92LV2421/DS92LV2422 chipset is intended for interface between a host (graphics processor) and a Display. It supports an 24-bit color depth (RGB888). In a RGB888 application, 24 color bits (D[23:0), Pixel Clock (CLKIN) and three control bits (C1, C2, C3) are supported across the serial link with CLK rates from 10 to 75 MHz. The chipset may also be used in 18-bit color applications. In this application three to six general purpose signals may also be sent from host to display.

The Des is expected to be located close to its target device. The interconnect between the Des and the target device is typically in the 1 to 3 inch separation range. The input capacitance of the target device is expected to be in the 5 to 10 pF range. Care should be taken on the CLK output trace as this signal is edge sensitive and strobes the data. It is also assumed that the fanout of the Des is one. If additional loads need to be driven, a logic buffer or mux device is recommended.

TYPICAL APPLICATION CONNECTION

Figure 32 shows a typical application of the DS92LV2421 Ser in Pin control mode for 24-bit Application. The LVDS outputs require 100 nF AC coupling capacitors to the line. The line driver includes internal termination. Bypass capacitors are placed near the power supply pins. At a minimum, four 0.1 µF capacitors and a 4.7 µF capacitor should be used for local device bypassing. System GPO (General Purpose Output) signals control the PDB and BISTEN pins. In this application the RFB pin is tied Low to latch data on the falling edge of the CLKIN. In this example the cable is long, therefore the VODSEL pin is tied High and a De-Emphasis value is selected by the resistor R1. The interface to the host is with 1.8 V LVCMOS levels, thus the VDDIO pin is connected also to the 1.8V rail. The optional Serial Bus control is not used in this example, thus the SCL, SDA and ID[x] pins are left open. A delay cap is placed on the PDB signal to delay the enabling of the device until power is stable.

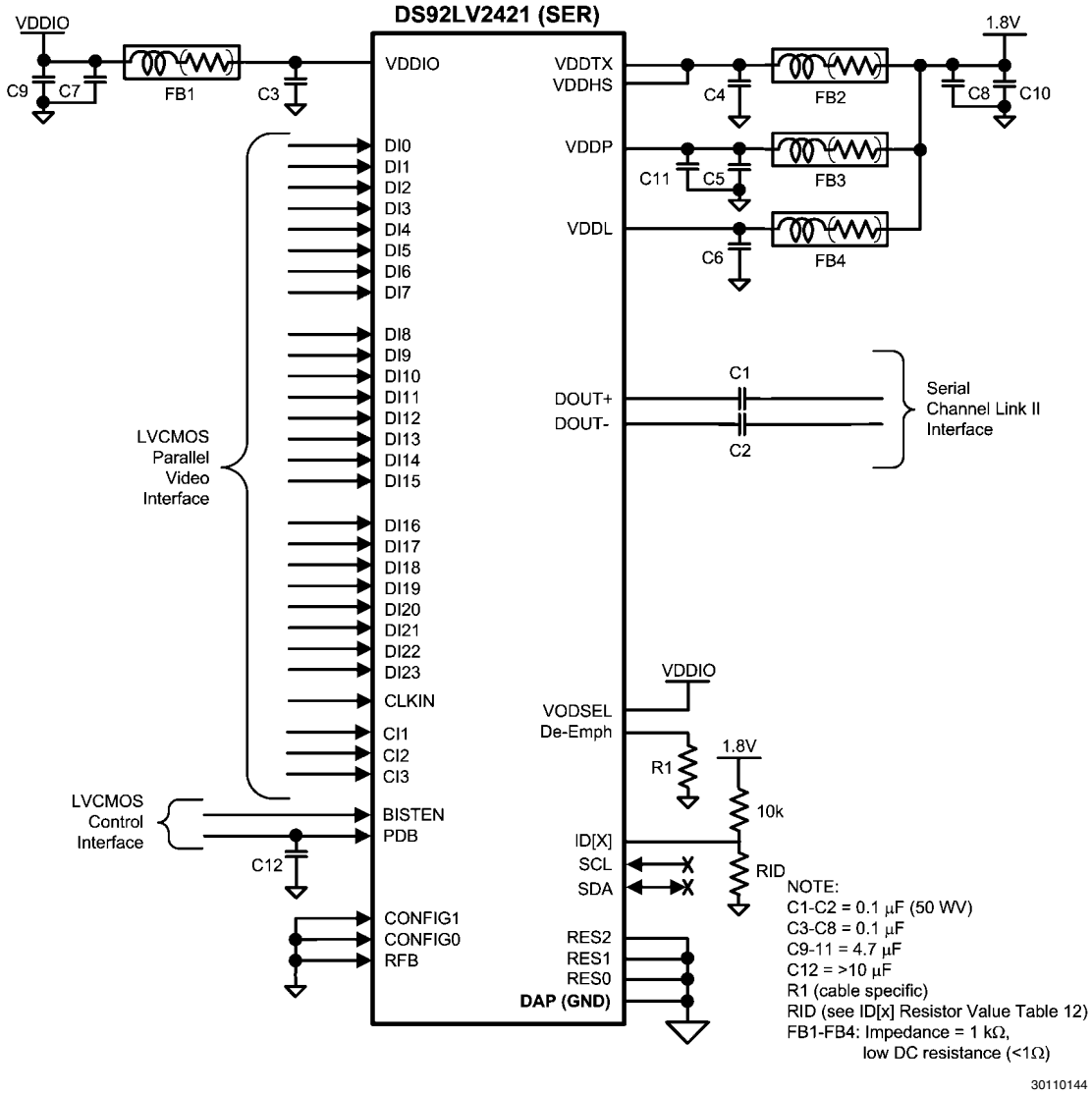


FIGURE 32. DS92LV2421 Typical Connection Diagram — Pin Control

Figure 33 shows a typical application of the DS92LV2422 Des in Pin/STRAP control mode 24-bit Application. The LVDS inputs utilize 100 nF coupling capacitors to the line and the receiver provides internal termination. Bypass capacitors are placed near the power supply pins. At a minimum, seven 0.1 µF capacitors and two 4.7 µF capacitors should be used for local device bypassing. System GPO (General Purpose Output) signals control the PDB and the BISTEN pins. In this application the RFB pin is tied Low to strobe the data on the falling edge of the CLKOUT.

Since the device in the Pin/STRAP mode, four 10 kΩ pull up resistors are used on the parallel output bus to select the desired device features. CFEN is set to 1 for Normal Mode with Control Signal Filter enabled, this is accomplished with the STRAP pull-up on DO23. The receiver input equalizer is also enabled and set to provide 7.5 dB of gain, this is accomplished with EQ[3:0] set to 1001'b with STRAP pull ups on DO12 and DO15. To reduce parallel bus EMI, the SSCG feature is enabled and set to fmod = CLK/2168 and ±1% with SSC[3:0] set to 0010'b and a STRAP pull-up on DO4. The desired features are set with the use of the four pull up resistors.

The interface to the target display is with 3.3V LVCMOS levels, thus the VDDIO pin is connected to the 3.3 V rail. The optional Serial Bus Control is not used in this example, thus the SCL, SDA and ID[x] pins are left open. A delay cap is placed on the PDB signal to delay the enabling of the device until power is stable.

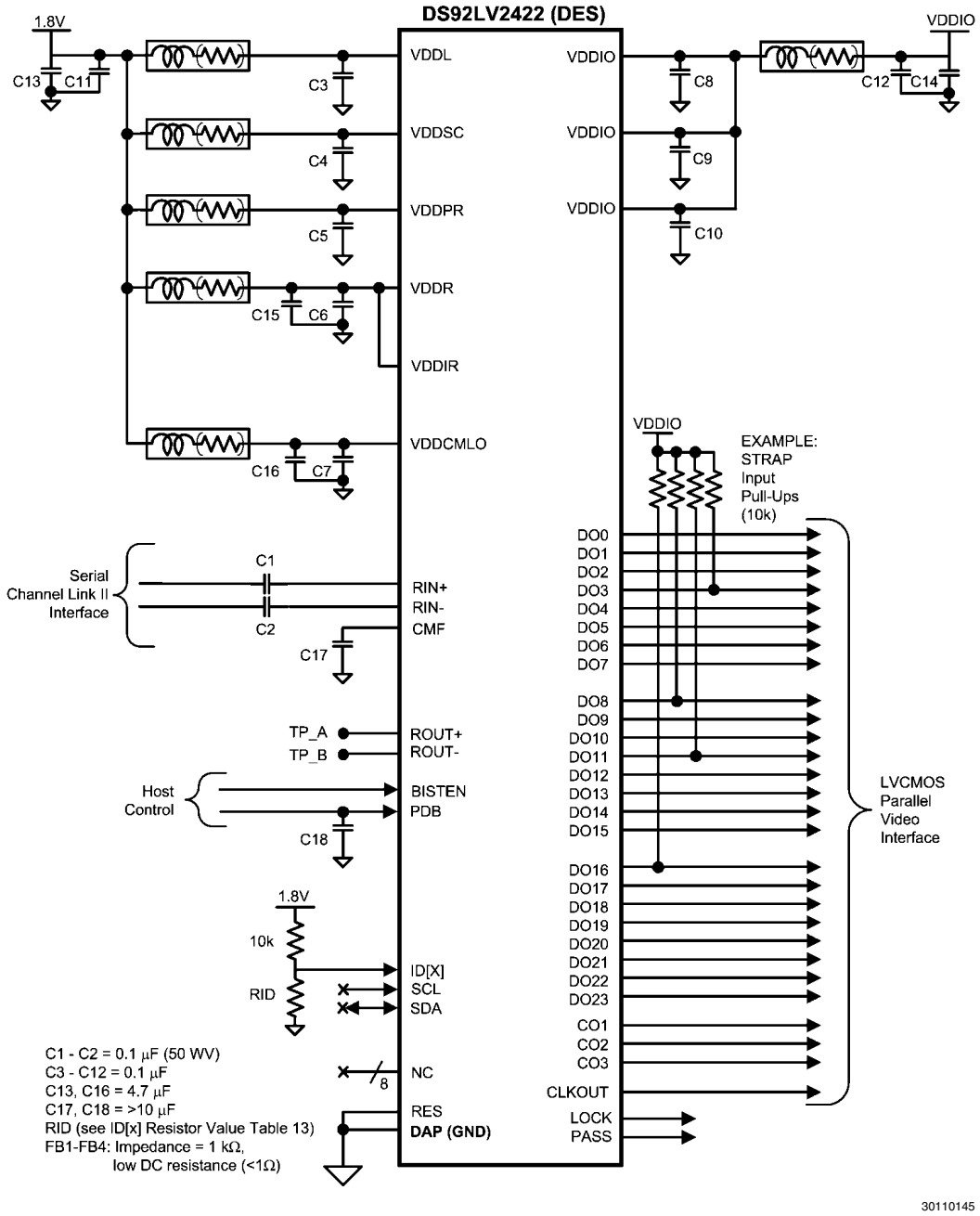


FIGURE 33. DS92LV2422 Typical Connection Diagram — Pin Control

POWER UP REQUIREMENTS AND PDB PIN

The VDD (V_{DDn} and V_{DDIO}) supply ramp should be faster than 1.5 ms with a monotonic rise. If slower then 1.5 ms then a capacitor on the PDB pin is needed to ensure PDB arrives after all the VDD have settled to the recommended operating voltage. When PDB pin is pulled to V_{DDIO}, it is recommended to use a 10 kΩ pull-up and a 22 uF cap to GND to delay the PDB input signal.

TRANSMISSION MEDIA

The Ser/Des chipset is intended to be used in a point-to-point configuration, through a PCB trace, or through twisted pair cable. The Ser and Des provide internal terminations providing a clean signaling environment. The interconnect for LVDS should present a differential impedance of 100 Ohms. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Shielded or un-shielded cables may be used depending upon the noise environment and application requirements.

LIVE LINK INSERTION

The Ser and Des devices support live pluggable applications. The automatic receiver lock to random data “plug & go” hot insertion capability allows the DS92LV2422 to attain lock to the active data stream during a live insertion event.

PCB LAYOUT AND POWER SYSTEM CONSIDERATIONS

Circuit board layout and stack-up for the LVDS Ser/Des devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50uF to 100uF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely-coupled differential lines of 100 Ohms are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Information on the LLP style package is provided in National Application Note: AN-1187.

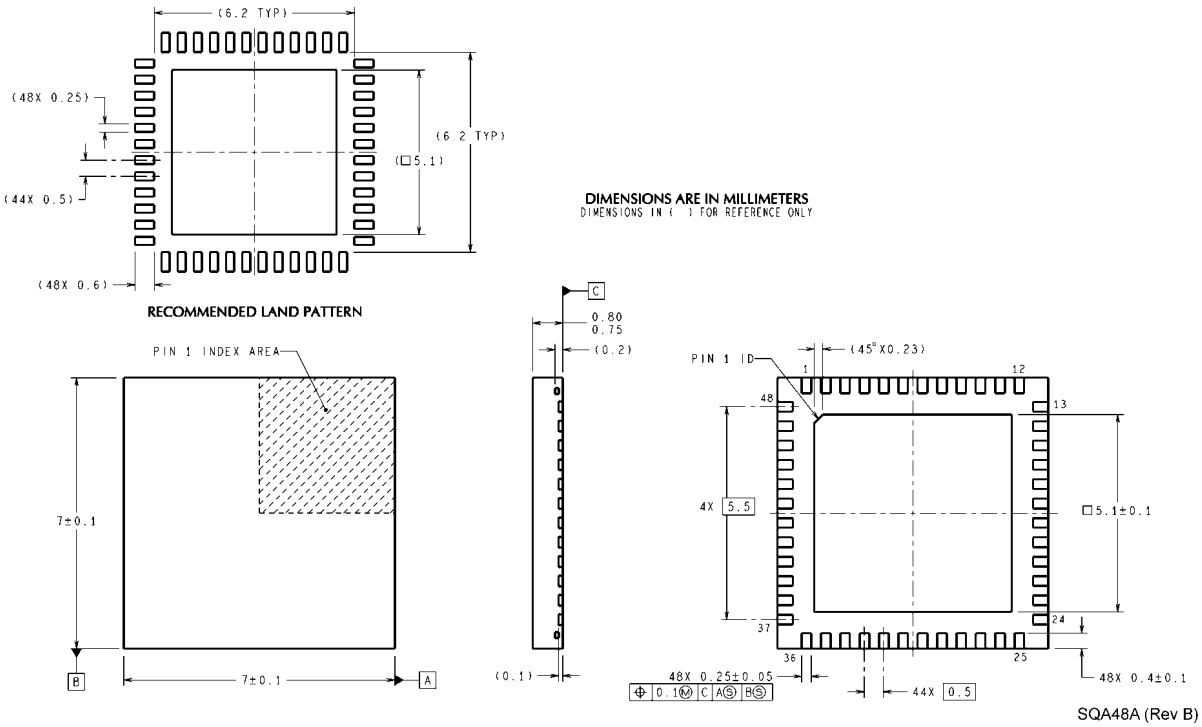
LVDS INTERCONNECT GUIDELINES

See AN-1108 and AN-905 for full details.

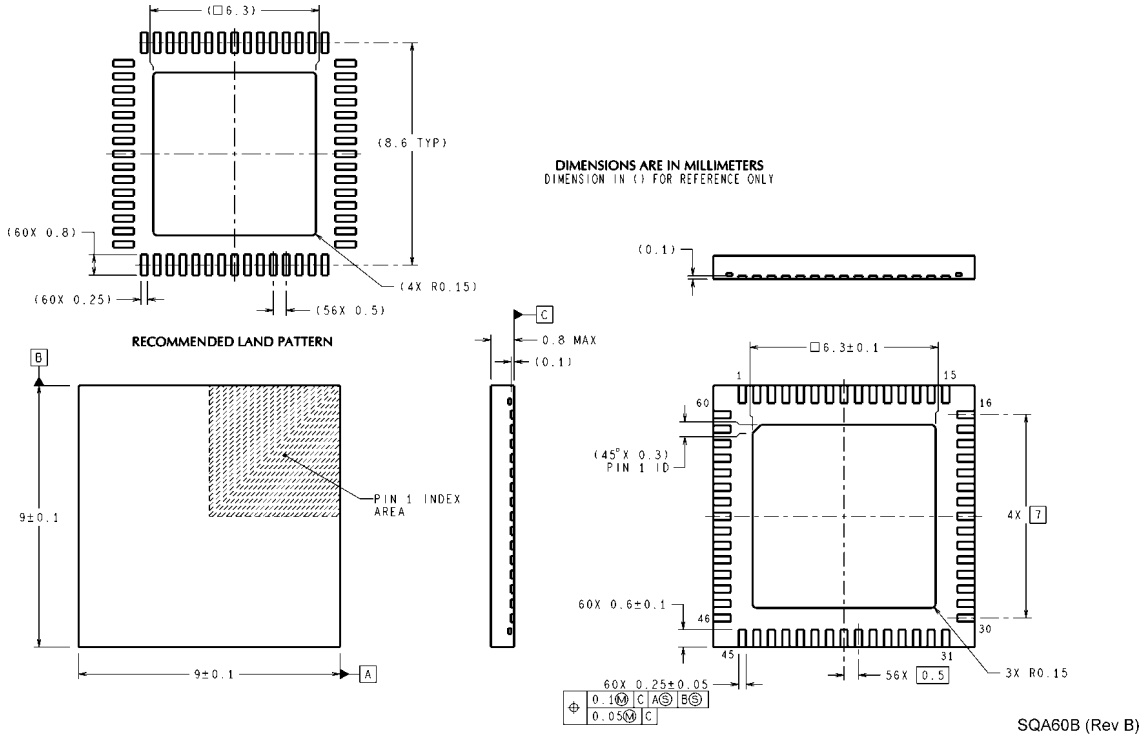
- Use 100Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  – S = space between the pair
  – 2S = space between pairs
  – 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Terminate as close to the TX outputs and RX inputs as possible

Additional general guidance can be found in the LVDS Owner’s Manual - available in PDF format from the National web site at: **www.national.com/lvds**

Physical Dimensions inches (millimeters) unless otherwise noted



48–pin LLP Package (7.0 mm x 7.0 mm x 0.8 mm, 0.5 mm pitch)
NS Package Number SQA48A



60–pin LLP Package (9.0 mm x 9.0 mm x 0.8 mm, 0.5 mm pitch)
NS Package Number SQA60B

Notes

Notes

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