CORTINA™

Product Brief

Cortina Systems® IXF1110 10-port Gigabit Ethernet Media Access Controller With System Packet Interface Level 4 Phase 2 (SPI-4.2)

Product Description

The Cortina Systems® IXF1110 SPI-4.2 Ethernet Media Access Controller (IXF1110 MAC), is a member of the Cortina Systems, Inc. (Cortina™) SPI-4.2 MAC family of enterprise switching building blocks.

The IXF1110 MAC is a 10-port Gigabit Ethernet MAC that provides a 10 Gigabit, system-level interface to 10 individual 1000 Mbps full-duplex Ethernet MACs. System Packet Interface Level 4 Phase 2 (SPI-4.2) is the high performance interface to the network processor or switching ASIC. An integrated SerDes provides a PHY interface that enables direct connection to SFP optical modules, helping reduce PCB real estate usage and system cost.

The highly integrated IXF1110 MAC reduces the number of components required to enable non-blocking, fiber-based, Gigabit Ethernet solutions. This integration makes the IXF1110 MAC highly desirable as a low power, cost-effective, communications building block in high-end, modular switching applications.

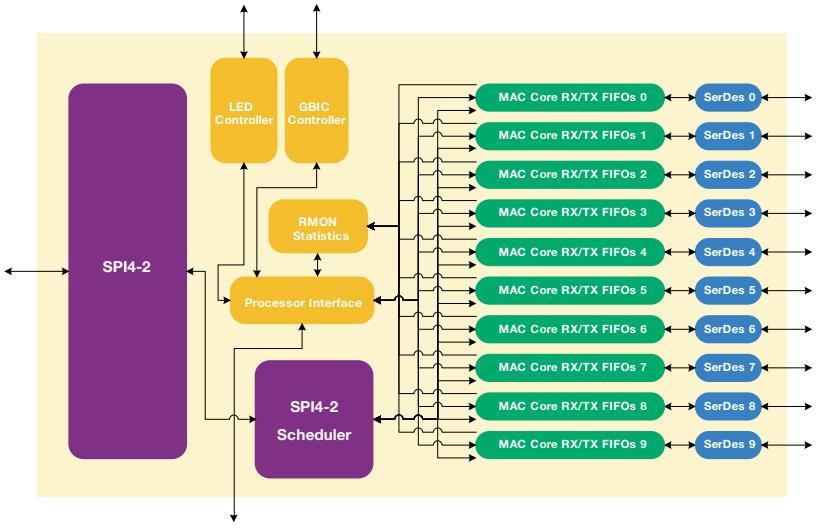
Cortina's Implementation of SPI-4.2

Local area networks using 10 GbE and metropolitan area networks using OC-192 are converging on SPI-4.2 as a standard system interface defined by the Optical Internetworking Forum (OIF). SPI-4.2 enables the communications industry to address the challenge of supporting different networking technologies, while reducing overall system cost. Silicon suppliers are addressing this challenge by providing interoperable SPI-4.2 MAC solutions that reduce the development complexity of high-end switching systems.

Addressing the needs for design flexibility in 10 Gigabit-capable modular switching systems, Cortina's SPI-4.2 MAC family implements leading-edge Dynamic Phase Alignment (DPA) technology. DPA compensates for signal degradation caused by impedance mis-matches introduced by system connectors or extended PCB trace lengths.

Cortina's implementation of SPI-4.2 offers high performance and robustness through the following features:

- Utilization of a combination of static and **dynamic phase alignment** empowers designers with the most flexible and robust design scenario in routing SPI-4.2 over long trace lengths and through connectors
- Support of 400 MHz **double data rate clock** accommodates for the additional bandwidth needed to support overhead functions like in-band management—without impacting the full performance of 10 Gbps Ethernet data rates
- Implementation of a **receive FIFO** status channel improves the efficiency of flow control in nonblocking, high performance systems
- Cost-effective **MAC memory architecture** supports high performance with minimal memory usage



IXF1110 MAC Block Diagram

Features	Benefits
• Ten IEEE 802.3*-compliant 1000 BASE-T MAC ports in 552 CBGA	• Offers high integration for low-cost connectivity
• SPI-4.2 with Dynamic Phase Alignment	• Allows accurate data transfer over longer trace lengths and through multiple connectors
• SPI-4.2 interface supports 400 MHz clock	• Supports in-band management functions at full 10 Gbps data rate
• Supports 10 independent 1000 Mbps full-duplex operation with integrated SerDes and optics control bus	• Enables easier routing to PHY devices using fewer pins than GMII
• 32-bit microprocessor interface	• Enables statistics gathering and configuration during initialization
• Internal 17.0 KB receive FIFO and 4.5 KB transmit FIFO per channel	• Allows non-blocking support for reception and transmission of jumbo frames
• Compliance with IEEE 802.3x* standard PAUSE command frames	• Allows MAC to off-load flow control tasks from system processors
• RMON statistics	• Allows for remote monitoring of port activity
• JTAG and boundary scan	• Enables reduced test time in a system environment
• Broadcast, multicast, and unicast address filtering	• Controls the amount of traffic on LANs
• Serial LED Interface	• Provides the data for 30 separate direct drive LEDs and allows three LEDs per MAC port
• Independent enable/disable of any port	• Reduces system power
• .18 µm process technology (CMOS)	• Lowers power consumption

Cortina in Communications

Cortina is a leading supplier of intelligent communication solutions through continuous innovations in advanced port processing and intelligent port connectivity to the Core, Metro, Access and Enterprise Market Segments. With our state-of-the-art high speed analog digital integration, we deliver a wide suite of products that address our customers' performance, density and flexibility needs enabling faster time-to-market, longer time-in-market, and increased revenue opportunities. Working closely with our customers to understand their system requirements and anticipate their needs, we are creating the foundation ingredients for new generations of services.

*Other names and brands may be claimed as the property of others.

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