Freescale Semiconductor
Application Note

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i.MX28 Layout and Design Guidelines

This application note describes proper design, placement, and PCB routing techniques for the i.MX28 processor.

CONTENTS

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1 PCB Stack-up

At minimum, the PCB should use a 4 or 6 layer stack-up. An 8 layer board may be required for extremely dense PCBs that have multiple DRAM components. The 4 and 6 layer PCB stack-ups below keep a GND plane adjacent to the power planes as well as the i.MX28 processor. This increases the capacitance and reduces the gap between the GND and power planes. It will also ensure the signals on the top layer have a solid GND reference plane and reduces the GND via impedance between the i.MX28 processor and GND plane. This helps to reduce PCB and i.MX28 processor radiated emissions. The 6 layer PCB stack-up has an additional solid ground plane on layer 5. This further improves the radiated emissions performance of the PCB by ensuring all PCB layers have an adjacent GND reference plane.

- Recommended 4 layer PCB stack-up:
  - Layer 1 (Top) - i.MX28 location - signal + ground plane fill
  - Layer 2 (Inner1) - complete ground plane, no signal traces
  - Layer 3 (Inner2) - power planes + few signal traces if necessary
  - Layer 4 (Bottom) - signal + ground plane fill

- Recommended 6 Layer PCB stack-up
  - Layer 1 (Top) - i.MX28 location - signal + ground plane fill
  - Layer 2 (Inner1) - complete ground plane, no signal traces
  - Layer 3 (Inner2) - power plane + few signal traces if necessary
  - Layer 4 (Inner3) - signal
  - Layer 5 (Inner4) - complete ground plane, no signal traces
  - Layer 6 (bottom) - signal + ground plane fill

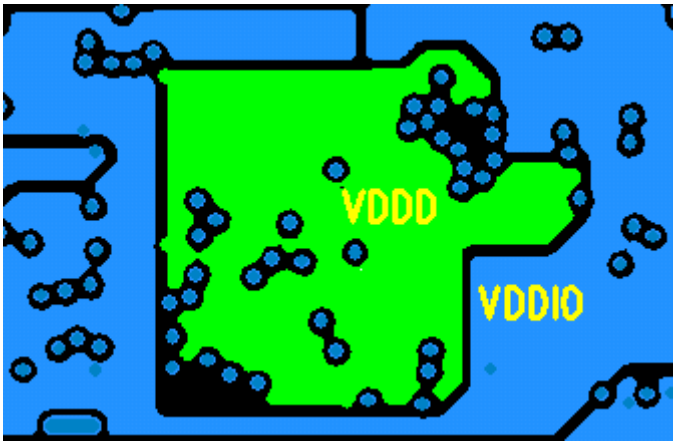
2 PCB Planes

2.1 Ground Plane

Use at least one internal ground plane. It is recommend to use a solid ground plane without splits for analog and digital GND planes. This allows for a continuous GND plane and helps to avoid radiated emissions, ESD, and noise problems that result from signal traces crossing plane splits.

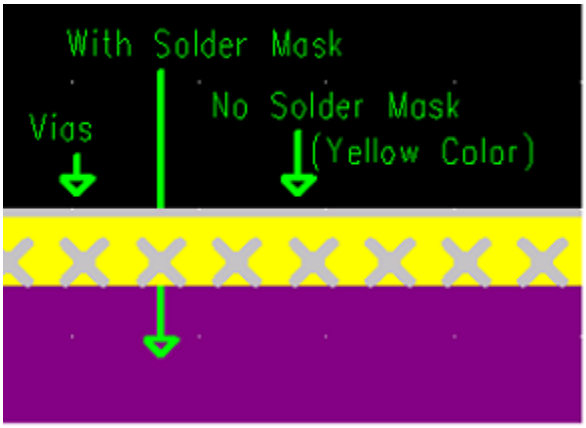
2.2 Power Planes

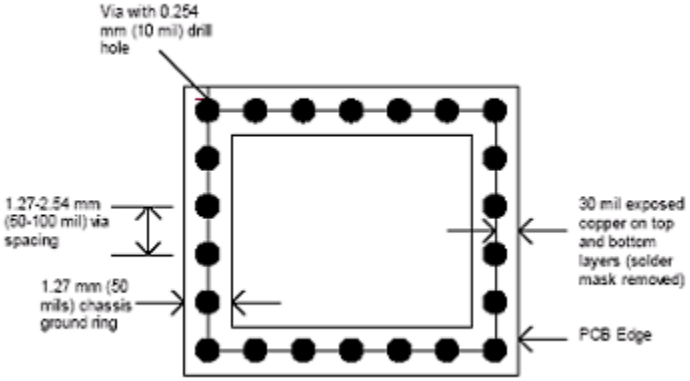
Split the power plane layer into separate VDDD (digital core), VDDA (analog supply), and VDDIO (digital I/O supply) power planes. The example layout below shows a VDDD and VDDIO plane split.



2.3 Chassis Ground Ring

Create a chassis ground ring connecting the entire perimeter of the PCB. The purpose of this is to improve ESD performance and help reduce radiated emissions. The chassis ground ring should be a minimum of 1.27 mm (50 mils) wide, if possible, and be routed on all layers with the rings stitched together with GND vias. On top and bottom layers the solder mask should be cleared from the ground ring as shown below.





3 PMU and DC-DC Converter

The i.MX28 processor has an integrated power management unit (PMU) that includes a multi-channel output DCDC converter. This section describes the important layout considerations for the PMU.

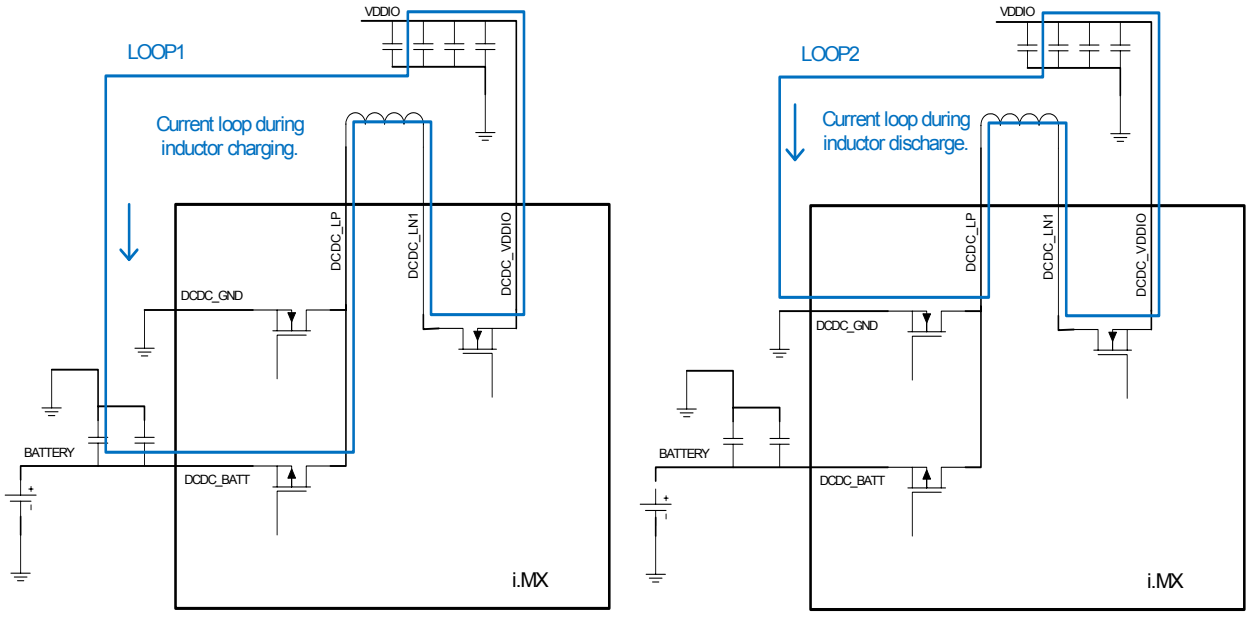
3.1 Vias

- Use at least two ground vias immediately next to the DCDC_GND pin. The DCDC_GND pin switches large amounts of current at a high frequency; decreasing the impedance to the ground plane reduces DCDC converter noise and increases stability.

- Make sure the DCDC_GND pin has a good low impedance connection to the other i.MX28 ground pins. If a voltage difference is created between the DCDC_GND pin and the other i.MX28 VSS pins, the system may be more susceptible to ESD failure.
- The power inductor traces should be 15-20 mils thick and should not use vias. If for some reason the power inductor cannot be placed on the same side of the PCB as the i.MX28, then multiple vias should be used to connect the inductor to the i.MX28 DC-DC converter pins.
- All vias used for the i.MX28 PMU power (VDD) and ground (VSS) pins, including the DCDC_GND pin, should have a drill hole size of 8 mils or larger to ensure a low impedance/inductive path between the pin and the PCB power/ground plane.

3.2 Minimize Switching Current Loops

The DCDC converter switching current loop area should be kept as small as possible to reduce the radiated emissions. There are two switching current loops as shown below. LOOP1: This occurs during the portion of the duty cycle when the inductor is being charged. LOOP2: This occurs during the flyback portion of the duty cycle when the inductor is supplying all of the current to the load.

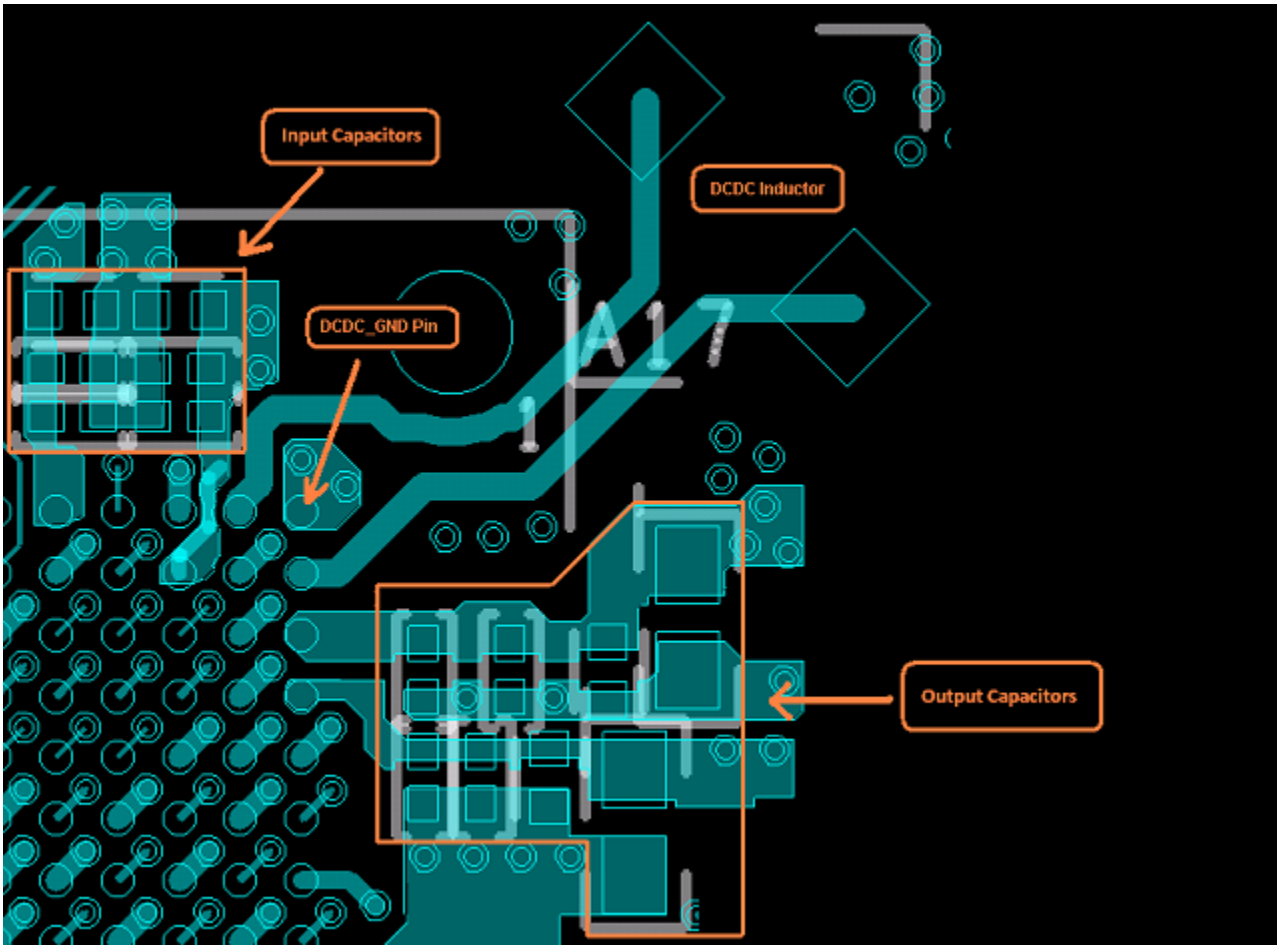


Minimizing the current loop areas can be accomplished by making sure the following layout rules are followed:

- Place the DCDC_BATT pin input capacitors as close as possible to the DCDC_BATT pin (less than 5mm away).
- Place the DCDC inductor as close as possible to the DCDC_LP and DCDC_LN pins.
- Route the inductor traces close together.

- Place the DCDC output capacitors as close as possible to their respective DCDC output pins (less than 5mm away): DCDC_VDDIO, DCDC_VDDA, DCDC_VDDD.
- Place the ground connections of the DCDC_BATT input capacitors as close as possible to both the DCDC_GND pin and the ground connections of the DCDC output capacitors.
- Place the ground connections of the DCDC output capacitors as close as possible to both the DCDC_GND pin and the ground connections of the DCDC_BATT pin input capacitors.

The drawing below shows an optimal layout for the top layer placement and routing of the DCDC converter.



3.3 Battery Connection

- Route the positive battery terminal on the power plane layer using a minimum trace width of 30 mils (0.762mm). A thicker trace may be required for longer battery trace runs (using a plane is best).
- Connect the negative battery terminal directly to the ground plane(s) as well as to the top and bottom ground fill using multiple vias (3 or more).

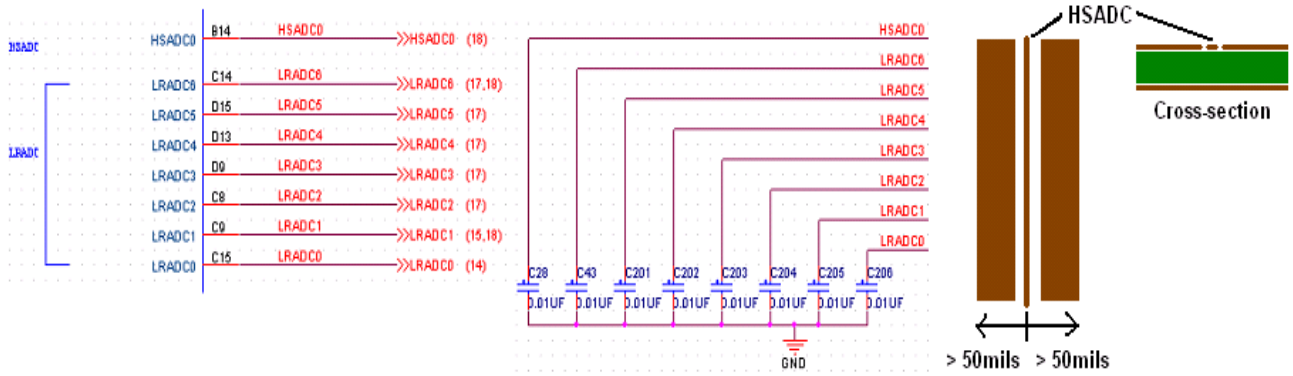
- Try placing the negative battery terminal close to the DCDC_GND pin if possible. This will reduce the length of the DCDC switching current ground return path and reduce overall PCB noise.

4 Analog

Place sensitive analog components including the low resolution ADC (LRADC), high speed ADC (HSADC), crystal circuit, analog audio, etc. in a section of the PCB that is isolated from digital components and traces.

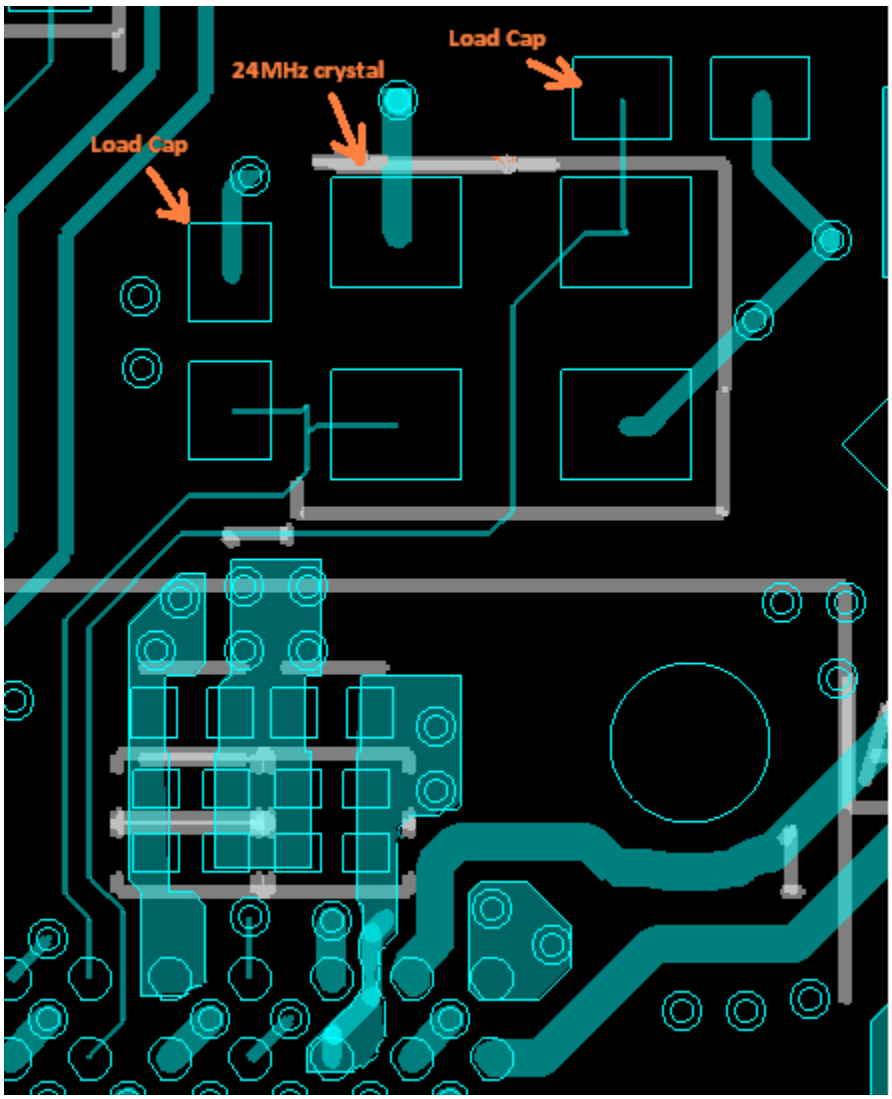
4.1 Analog-to-Digital Converters

- 0.01uF capacitors should be placed close to the LRADC input pins and away from digital and DCDC components and traces.
- The LRADC and HSADC traces should be routed adjacent to a ground plane the entire length of the trace. Crossing plane splits should be avoided. The traces should be routed far away from digital and DCDC components and traces.
- Minimal capacitance, no greater than 0.01uF, should be placed on the HSADC pin due to its high sample rate; 2Msps with 12 bit resolution. Placing a large amount of capacitance on the HSADC trace can reduce the accuracy and conversion speed due to limiting the analog signal rate of change.
- The HSADC signal must be routed only adjacent to ground planes – above and below if placed on an internal layer. It should be routed at least 50 mils away from other traces. At least 50mils of ground shielding on both sides of trace is recommended as shown below.



4.2 Crystal

- Place the crystal and load capacitors as close as possible to the XTALI and XTALO pins.
- Place the VDD_XTAL capacitor close to the VDD_XTAL pin, and ground the capacitor away from digital traces.
- These rules apply to both the 24.000 MHz and 32.768 kHz crystal circuits. The drawing below shows an example layout for the 24.000 MHz crystal circuit. In this drawing, all circuit components are routed on the top layer above a ground plane.

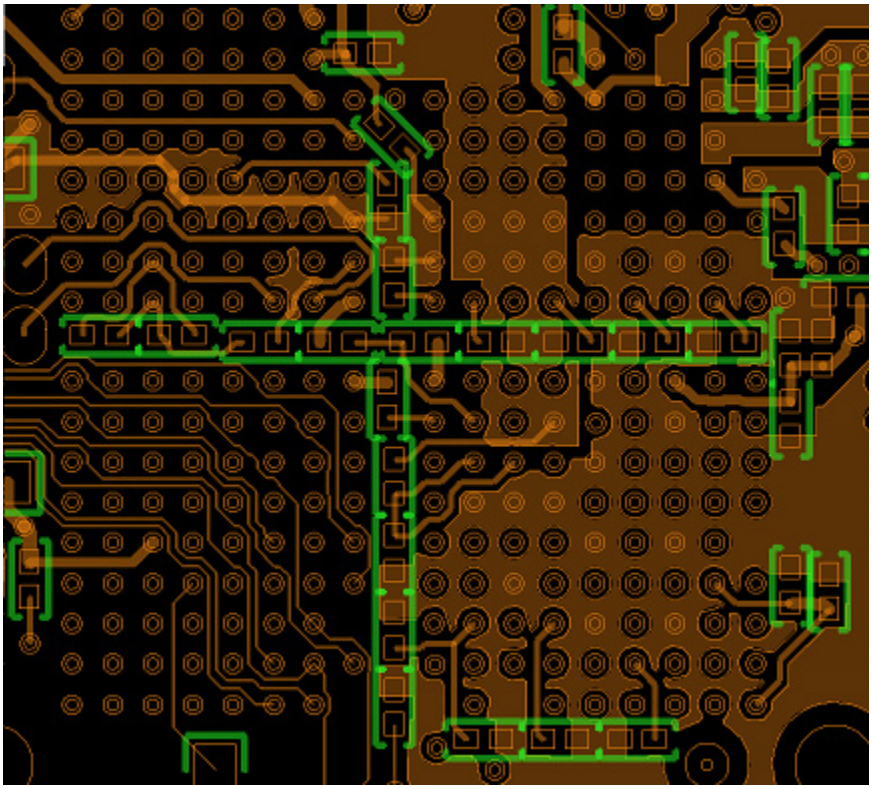


5 DRAM Memory

5.1 DRAM supply de-coupling

- Each i.MX28 EMI supply pin and DRAM memory supply pin must have its own via. The via must connect to a broad power plane which has (if possible) capacitors for each via. The more capacitors the better.
- One of the most critical issues is not the signal timing. It is power and/or GND bounce or noise due to poorly supplied i.MX DRAM supply pins and/or DRAM memory supply pins. Something as simple as the layout engineer using too few vias to connect the supply pins may cause the DRAM memory interface to fail.

- Vias can be strategically placed to create channels for the supply bypass capacitors to be placed underneath the i.MX28 processor and close to the EMI supply pins as shown below:



5.2 Routing

The guidelines below mainly focus on DDR2 routing (including low voltage,1.5V, DDR2). However, most of the these guidelines also apply to mDDR.

Summary of key signal groups:

- Address/Command (Ax, BAx, RAS#, CAS#, WE#)
  - — Single ended, parallel, terminated to VTT, registered on rising edge of clock.
- Control (CS#, CKE, ODT)
  - — Single ended, parallel, terminated to VTT, registered on rising edge of clock.
  - — Each bank has its own control signal (less loading).
- Clocks (CLK, CLK#)
  - — Differential, terminated on die with ODT.
- Data mask (DQMx)
  - — Single ended input, terminated on die with ODT.
  - — One data mask for each byte lane.

- Data (DQx)
  - Single ended, bi-directional, synchronized to data strobes, terminated on die with ODT.
  - Registered on rising and falling edges of data strobe.
- Data Strobes (DQSx)
  - Differential, bi-directional, terminated on die with ODT.
  - One differential pair for each byte lane.

Signal group layout guidelines:

- DQS/DQ/DQM
  - A data group (DQ) has an associated strobe (DQS) and data mask (DQM).
  - All DQS/DQ/DQM groups should be length matched as closely as possible given layout and placement constraints to minimize skew within the group and across the channel.
  - Overall length mismatch between byte lanes should be less than 500 mils.
- Use a wide trace / plane if possible for VREF.
- Address and Command signals
  - Should be length matched to each other within 200 mils.
  - Traces routed with a 50-60 ohms single ended impedance.
- Data signals (DQx)
  - All data signals within a byte lane length must be matched to within 100 mils of each other (the closer the matching, the better).
  - Lengths must be matched within 100 mils of the corresponding data strobes (the closer the matching, the better).
  - Traces routed with a 50-60 ohms single ended impedance.
- Data strobes (DQSx)
  - 1 per byte lane.
  - Clock pair length should be matched within 25 mils.
  - Length must be matched within 100 mils of the corresponding data byte lane (the closer the matching, the better).
  - 100 ohm +/- 10% differential impedance, 50-60 ohms single ended impedance on the individual traces.
- Data masks (DQMx)
  - 1 per byte lane.
  - Length must be matched within 100 mils of the corresponding data byte lane (the closer the matching, the better).
  - Traces routed with a 50-60 ohms single ended impedance.
- DRAM clock (EMI_CLK / EMI_CLKn)
  - Clock pair lengths should be matched within 25 mils.

  - 100 ohm +/- 10% differential impedance, 50-60 ohms single ended impedance on the individual traces.
  - During a write cycle, the i.MX28 must satisfy the timing specs between DQS and CK to facilitate the reliable transfer of data. To satisfy the clock to strobe (DQS) relationship, it is preferable that the clock length be between the shortest and longest strobe lengths.
- EMI_DDR_OPEN and EMI_DDR_OPEN_FB
  - These pins are specific to the i.MX28 DRAM memory controller and must be connected together. The total routed length from one pin to the other needs to be the following:
    - CLK routed distance + DQS routed distance

Other important guidelines:

- The DRAM DATA, DQM (data mask) and DQS (strobe) signals should use the same number of vias and route on the same layers and number of layers.
- Matching the numbers of vias and layers used is more important than matching the trace length.
- Route all DRAM traces over a solid GND plane with no discontinuities or plane splits on the layers adjacent to the DRAM traces (both above and below). It is important that the board designer provide these signals with a solid reference plane to control the characteristic impedance and provide a smaller loop area between the signals and the return currents. The EMI/DRAM power plane can also be used as the reference/return plane, but the GND plane is preferred and has the quietest return path for the signals.
- Isolate and protect the VREF trace/plane from noise.
- Keep data groups away from address and control signal lines to avoid cross talk.
- DRAM traces should be routed at short as possible to reduce trace capacitance and minimize reflections.

5.3 Minimizing Reflections

If possible, keep the DRAM DATA, DQM, STROBE, and CLOCK traces short enough so that a maximum of 30% of the edge appears on the trace. To put it in equation form:

Trace Length <= (0.3 x Rise/Fall Time x 15 cm/ns).

The speed of a signal edge travelling from sender to receiver on widely used FR4 material is about 1/5 the speed of light (or 15 cm/ns).

The full reflection occurs if the time for an edge travelling from sender (i.MX) to receiver (DRAM) is >= the rise/fall time of the signal. Example:

If the rise/fall time = 0.5ns and trace length = 7.5cm, the receiver still sees zero volts even though the sender is now driving at the maximum DRAM supply voltage. Because the full edge is now on the line, full reflection occurs.

So for this example, the signal traces should not exceed 2.25cm (30% of 7.5cm). This is valid for the distance between one sender and one receiver.

Note that this example calculation is for a point-to-point connection. If more than 1 memory device is connected to the bus, the rise / fall time will be slower and the trace length may be longer.

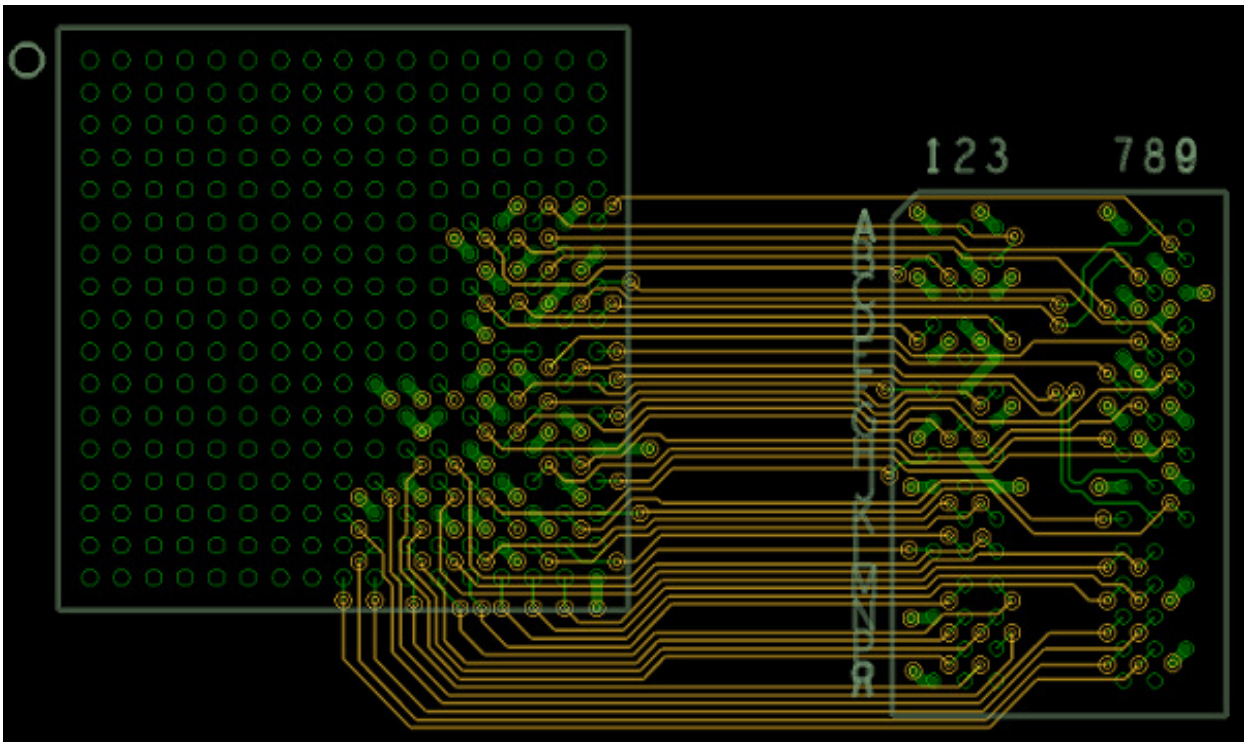
Control signals like CS, ADDRESS, RAS, CAS, and WE are not critical and can be routed without these constraints.

5.4 Routing to Multiple DRAM Devices

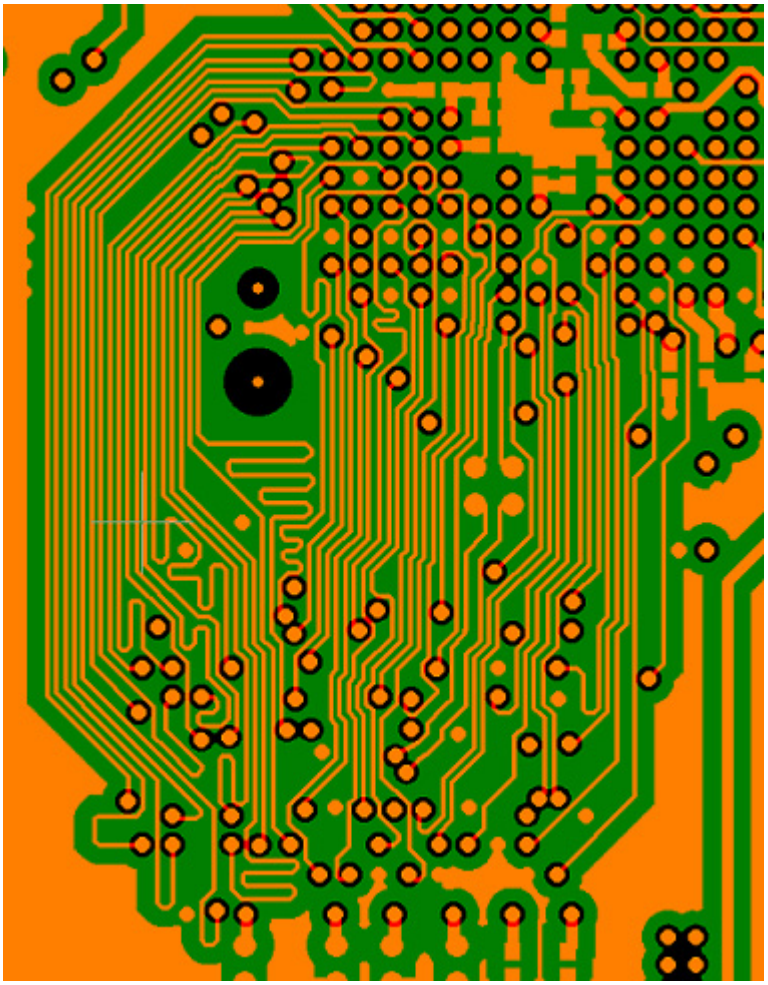
- In terminated systems, “daisy chain” routing is recommended because the impedance can be matched along the whole trace. In non-terminated systems, Y routing is much better because it makes the trace lengths shorter, which reduces the capacitive loading.
- For 2 external DRAM components, pin swapping the data signals within a byte lane can be performed to improve/optimize routing. This is particularly useful when the one DRAM is placed on the top side of the board and the other is placed on the bottom side.

5.5 Layout Examples

The i.MX28 processor EMI pin locations have been optimized to facilitate single layer DRAM signal routing. The layout example below shows an ideal fan-out between the i.MX28 processor and a DDR2 memory device where nearly all the routing is accomplished on a signal layer. The routing can be achieved with low cost PCB manufacturing using 5 mils trace/space and 8/16 through-hole vias. Note that this layout shows fan-out only, differential pair routing is not complete, and does not include length matching.



Another good example layout that can be followed is the i.MX28 EVK (evaluation kit) PCB. The PCB layout source files can be downloaded from the Freescale i.MX28 support webpage. The image below shows the bottom layer routing of the DDR2 interface. The key item to notice is that all the DDR2 traces are routed entirely above a solid ground plane (green background) and do not cross any plane splits or other traces.

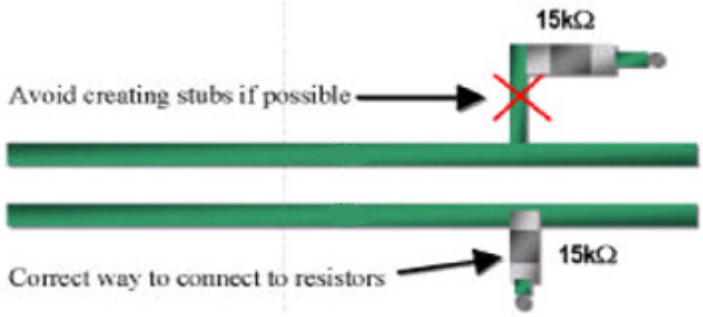


6 SD/MMC/SDIO Card and SPI interfaces

This SDIO and SPI interfaces are serial data in/out interfaces. The SDIO interface consists of clock and command signal lines and up to 8 data lines. The SPI interface consists of a clock line and up to 4 data lines (for quad I/O SPI). These interfaces can be high speed, 50MHz or higher, and double data rate for the eMMC4.4 standard. Because of this, is it important to follow these layout guidelines.

- Trace capacitance should be minimized.
- Avoid crossing plane splits as this will degrade signal integrity and increase radiated emissions.
- Trace length matching may be beneficial in some cases where the trace length routing is long (>3 inches).

- Any external pull-up resistors should be placed close to the signal trace to minimize stubs and stray capacitance as shown below.



7 USB

- USB signal lines should be routed on top or bottom layers to allow for tight control of 90 ohm differential impedance requirement.
- Maintain parallelism between USB differential signals needed to achieve 90ohms differential impedance between D+ and D- for the entire routed length. Slight deviations from this will normally occur due to package, USB jack footprints, and routing to connector pins. The number and length of the deviations should be kept to a minimum.
- Use an impedance calculator to determine the trace width and spacing required for the specific board stack up and material being used. This should also be verified with the PCB manufacturer before routing is finalized.
- Minimize the length of high-speed clock and periodic signal traces that run parallel to the USB signal lines to minimize crosstalk. High speed and periodic signals should be kept at least 50 mils away from USB D+/D-.
- All other signals should be kept at least 20 mils away from the high-speed USB signal pairs to help prevent crosstalk.

7.1 Common USB Routing Mistakes

- Stubs - Avoid creating unnecessary stubs by placing any component footprints over the path of the D+/D- traces. If a stub is unavoidable in the design, no stub should be greater than 200 mils in length.
- Crossing a plane split - The USB data lines should never cross a power or ground plane split. This causes unpredictable return path currents, which can cause signal quality failures as well as EMI problems.
- Failure to maintain parallelism – Failing to maintain parallelism will cause impedance discontinuities that will directly affect signal quality. It also contributes to the trace-length mismatch and will cause an increase in signal skew.

8 Ethernet

8.1 Component Placement

- If the magnetic is a discrete component, then it should be placed no greater than 1 inch away from the ethernet jack.
- The distance between the ethernet PHY and the magnetics should be 25mm (1 in.) or greater. The 1 in. design rule is considered good design practice among PHY vendors to isolate the PHY from the magnetics.
- Keep the PHY device and the differential TX/RX pairs at least 1 inch from the edge of the PCB, up to the magnetics. For an integrated magnetics ethernet jack, the differential pairs should be routed to the back of the integrated jack, away from the board edge.
- The 49.9 ohm pull-up resistors on RX/TX should be placed within 400 mils of the ethernet PHY and should be placed next to the RX/TX pairs to minimize stubs. This also ensures similar RX/TX transmit paths.

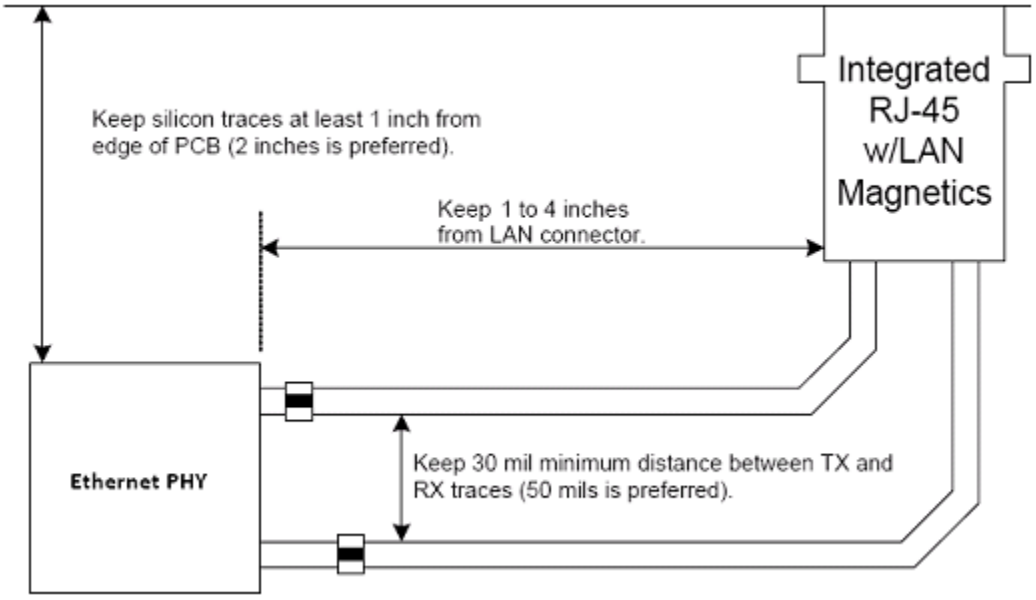
8.2 Ethernet Clock

In RMII mode, the i.MX28 processor supplies the 50MHz ethernet clock signal to the ethernet PHY. This signal must be routed very carefully due to its high speed. Poor layout of this signal can cause ethernet PHY clocking issues. To prevent any issues, follow these guidelines:

- Minimize trace length. This will help to minimize trace capacitance, which can slow the edge rates of the ethernet clock. It will also minimize the chances of picking up noise from other source on the PCB such as high speed digital traces or current switching power planes/traces.
- Route the clock in isolation away from other traces and noise sources.
- Must be routed over a continuous ground plane. It should not be routed across any plane splits or traces on adjacent layers.

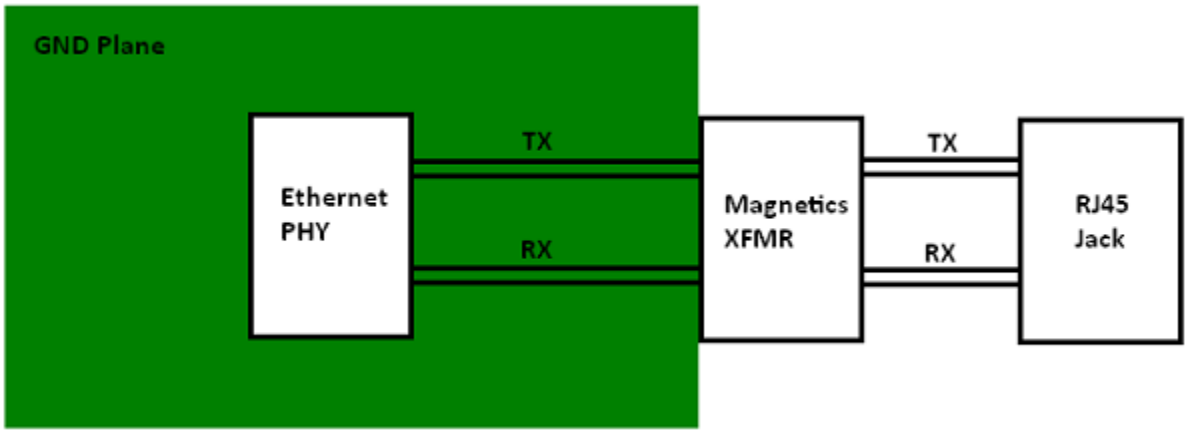
8.3 Ethernet TX and RX pairs between the ethernet PHY and the magnetics

- Must be routed with 100 ohm differential impedance and 50 ohm single ended impedance.
- Must be routed over a solid ground plane to maintain a controlled impedance over the entire trace route.
- Trace lengths for each pair should be matched.
- Use a minimum distance of 30 mils between TX and RX pairs.



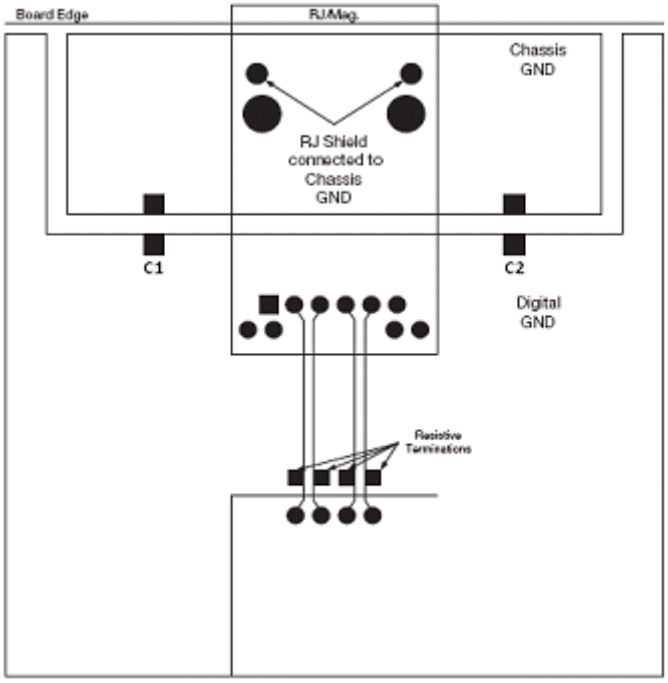
8.4 Ethernet Jacks and Magnetics:

- Discrete magnetics module
  - If using a discrete magnetics module, a ground plane must not be placed under the magnetics, the RJ45 connector, or the area between the magnetics and RJ45 connector.
  - A ground plane should be placed underneath the RX and TX pairs between the ethernet PHY and magnetics module as shown below.



- RJ45 Jack with integrated magnetics

— A ground plane should be placed under the TX/RX pairs between the ethernet PHY and integrated RJ45 jack.
— A separate ethernet chassis ground should be placed under the RJ45 jack.
— The chassis ground should be connected to the rest of the PCB GND with capacitor stuffing options, which is useful for determining which values and location will provide the best EMI performance.
— An example drawing is shown below.



9 ESD and Radiated Emissions

- Ideally, the PCB design should use 6 or more layers, with solid power and ground planes. With 4 layers, ESD immunity and radiated emissions performance may be compromised.
- All components with ground chassis shields (USB jack, buttons, etc.) should connect the shield to the PCB chassis ground ring.
- Ferrite beads should be placed on each signal line connecting to an external cable (except for USB - see below). These ferrite beads must be placed as close to the PCB jack as possible.
- Ferrite beads should NOT be placed on the USB D+/D- signal lines as this can cause USB signal integrity problems. For radiated emissions problems due to USB, a common mode choke may be placed on the D+/D- signal lines. However, in most cases, it should not be required if the PCB layout is satisfactory. Ideally, the common mode choke should be approved for high speed USB use or tested thoroughly to verify there are no signal integrity issues created.

- It is preferred that ferrite beads should have a minimum impedance of 500 ohms @ 100MHz with the exception of the ferrite on USB_5V.

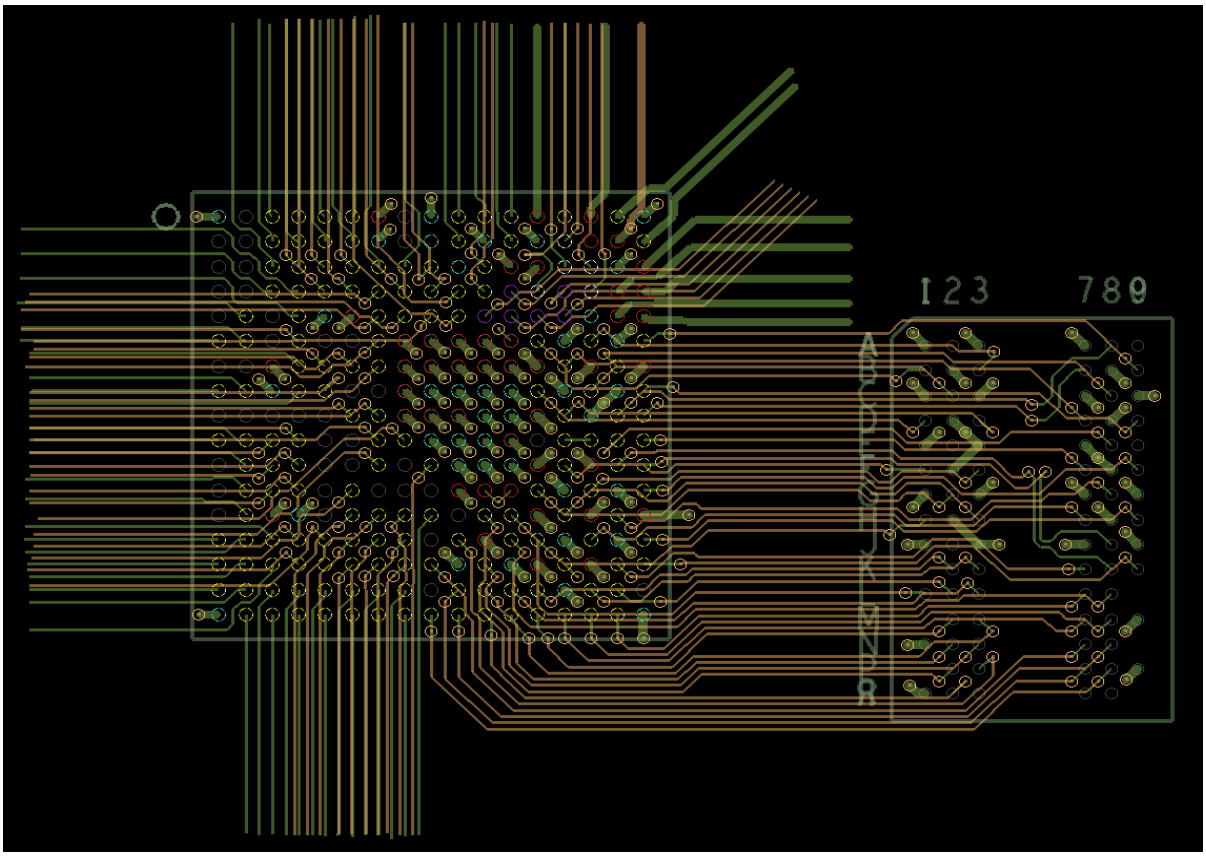
10 Industrial Design

The recommendations below are aimed at improving the system ESD performance.

- Buttons or switches on the housing should be non-conductive.
- The USB jack should be covered by a non-conductive case or rubber plug.
- If metal or conductive player housings are used, they should be designed to allow equal charge distribution on all sides of the PCB.
- Air gaps between buttons and the housing should be kept as small as possible.

11 2-Layer Escape Routing Example

The i.MX283 family member feature set and pinout is optimized to allow for 2 layer escape routing using PCB industry standard 5 mil trace/space and 8/16 through-hole vias. This will also allow for 4 layer PCB designs in most cases depending on other board peripherals. The example layout below shows a 2 layer escape route. The Allegro source layout file for this escape route is available for download from the Freescale i.MX28 support web page.



12 Optimizing for Low-Cost

- Follow the MX283 2-layer escape routing example above. This example route uses standard 5/5 mil trace/spacing and 8/16 through-hole vias and enables use of a low-cost 4-layer PCB.

13 Revision History

Table 1 provides the revision history for this application note.

Table 1. Document Revision History

Rev. Number	Date	Substantive Change(s)
0	09/21/2010	Initial release.

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