ARM Cortex™-M0

32-BIT MICROCONTROLLER

NuMicro™ Family
NUC120 Product Brief

For additional information or questions, please contact: Nuvoton Technology Corporation.

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1 GENERAL DESCRIPTION

The NuMicro™ NUC100 Series is 32-bit microcontrollers with embedded ARM® Cortex™-M0 core for industrial control and applications which need rich communication interfaces. The Cortex™-M0 is the newest ARM® embedded processor with 32-bit performance and at a cost equivalent to traditional 8-bit microcontroller. NuMicro™ NUC100 Series includes NUC100, NUC120, NUC130 and NUC140 product line.

The NuMicro™ NUC120 USB Line with USB 2.0 full-speed function embeds Cortex™-M0 core running up to 50 MHz with 32K/64K/128K-byte embedded flash, 4K/8K/16K-byte embedded SRAM, and 4K-byte loader ROM for the ISP. It also equips with plenty of peripheral devices, such as Timers, Watchdog Timer, RTC, PDMA, UART, SPI/MICROWIRE, I^2C, I^2S, PWM Timer, GPIO, PS2, USB 2.0 FS Device, 12-bit ADC, Analog Comparator, Low Voltage Reset Controller and Brown-out Detector.

Product Line	UART	SPI	I^2C	USB	LIN	CAN	PS2	I^2S
NUC100	•	•	•				•	•
NUC120	•	•	•	•			•	•
NUC130	•	•	•		•	•	•	•
NUC140	•	•	•	•	•	•	•	•

Table 1-1 Connectivity Supported Table

2 FEATURES

The equipped features are dependent on the product line and their sub products.

2.1 NuMicro™ NUC120 Features – USB Line

- Core
  - ARM® Cortex™-M0 core runs up to 50 MHz
  - One 24-bit system timer
  - Supports low power sleep-mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Build-in LDO for wide operating voltage ranges from 2.5V to 5.5V
- Flash EPROM Memory
  - 32K/64K/128K bytes Flash EPROM for program code (128KB only support in Medium Density)
  - 4KB flash for ISP loader
  - Support In-system program(ISP) application code update
  - 512 byte page erase for flash
  - Configurable data flash address and size for 128KB system, fixed 4KB data flash for the 32KB and 64KB system (Only support 4KB data flash in Low Density)
  - Support 2 wire ICP update through SWD/ICE interface
  - Support fast parallel programming mode by external programmer
- SRAM Memory
  - 4K/8K/16K bytes embedded SRAM (16KB only support in Medium Density)
  - Support PDMA mode
- PDMA (Peripheral DMA)
  - Support 9 channels PDMA for automatic data transfer between SRAM and peripherals (Only support 1 channel in Low Density)
- Clock Control
  - Flexible selection for different applications
  - Build-in 22.1184 MHz OSC (Trimmed to 1%) for system operation, and low power 10 kHz OSC for watchdog and wakeup sleep operation
  - Support one PLL, up to 50 MHz, for high performance system operation
  - External 4~24 MHz crystal input for USB and precise timing operation
  - External 32.768 kHz crystal input for RTC function and low power system operation
- GPIO
  - Four I/O modes:
    - Quasi bi-direction
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin can be configured as interrupt source with edge/level setting
  - High driver and high sink IO mode support
- Timer
  - Support 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
  - Independent clock source for each timer

- Provides one-shot, periodic, toggle and auto-reload counting operation modes

- Watch Dog Timer
  - Multiple clock sources
  - 8 selectable time out period from 6ms ~ 3.0sec (depends on clock source)
  - WDT can wake up from power down or sleep mode
  - Interrupt or reset selectable on watchdog time-out
- RTC
  - Support software compensation by setting frequency compensate register (FCR)
  - Support RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Support Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Support periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Support wake up function
- PWM/Capture
  - Built-in up to four 16-bit PWM generators provide eight PWM outputs or four complementary paired PWM outputs
  - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit prescaler and one Dead-Zone generator for complementary paired PWM
  - Up to eight 16-bit digital Capture timers (shared with PWM timers) provide eight rising/falling capture inputs
  - Support Capture interrupt
- UART
  - Up to three UART controllers (Low Density only support 2 UART controllers)
  - UART ports with flow control (TXD, RXD, CTS and RTS)
  - UART0 with 63-byte FIFO is for high speed
  - UART1/2(optional) with 15-byte FIFO for standard device
  - Support IrDA (SIR) function
  - Support RS-485 9 bit mode and direction control. (Low Density Only)
  - Programmable baud-rate generator up to 1/16 system clock
  - Support PDMA mode
- SPI
  - Up to four sets of SPI controller
  - Master up to 20 MHz, and Slave up to 10 MHz
  - Support SPI/MICROWIRE master/slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 1 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently
  - 2 slave/device select lines when it is as the master, and 1 slave/device select line when it is as the slave
  - Support byte suspend mode in 32-bit transmission
  - Support PDMA mode

- I^2C
  - Up to two sets of I^2C device
  - Master/Slave up to 1Mbit/s
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allow versatile rate control
  - Support multiple address recognition (four slave address with mask option)
- I^2S
  - Interface with external audio CODEC
  - Operate as either master or slave mode
  - Capable of handling 8, 16, 24 and 32 bit word sizes
  - Mono and stereo audio data supported
  - I^2S and MSB justified data format supported
  - Two 8 word FIFO data buffers are provided, one for transmit and one for receive
  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Support two DMA requests, one for transmit and one for receive
- PS2 Device Controller
  - Host communication inhibit and request to send detection
  - Reception frame error detection
  - Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
  - Double buffer for data reception
  - S/W override bus
- USB 2.0 Full-Speed Device
  - One set of USB 2.0 FS Device 12Mbps
  - On-chip USB Transceiver
  - Provide 1 interrupt source with 4 interrupt events
  - Support Control, Bulk In/Out, Interrupt and Isochronous transfers
  - Auto suspend function when no bus signaling for 3 ms
  - Provide 6 programmable endpoints
  - Include 512 Bytes internal SRAM as USB buffer
  - Provide remote wakeup capability
- EBI (External bus interface) support (Low Density 64-pin Package Only)
  - Accessible space: 64KB in 8-bit mode or 128KB in 16-bit mode
  - Support 8bit/16bit data width
  - Support byte write in 16bit data width mode
- ADC
  - 12-bit SAR ADC with 600K SPS
  - Up to 8-ch single-end input or 4-ch differential input
  - Single scan/single cycle scan/continuous scan
  - Each channel with individual result register
  - Scan on enabled channels
  - Threshold voltage detection
  - Conversion start by software programming or external input
  - Support PDMA Mode

- Analog Comparator
  - Up to two analog comparator
  - External input or internal bandgap voltage selectable at negative node
  - Interrupt when compare result change
  - Power down wake up
- One built-in temperature sensor with 1℃ resolution
- Brown-out detector
  - With 4 levels: 4.5V/3.8V/2.7V/2.2V
  - Support Brownout Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage levels: 2.0V
- Operating Temperature: -40℃~85℃
- Packages:
  - All Green package (RoHS)
  - LQFP 100-pin / 64-pin / 48-pin (100-pin for Medium Density Only)

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NuMicro™ NUC120 Products Selection Guide

3.1.1 NuMicro™ NUC120 Medium Density USB Line Selection Guide

Part number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity						I^2S	Comp.	PWM	ADC	RTC	EBI	ISP ICP	Package
							UART	SPI	I^2C	USB	LIN	CAN								
NUC120LD3AN	64 KB	16 KB	4 KB	4 KB	up to 31	4x32-bit	2	1	2	1	-	-	1	1	4	8x12-bit	v	-	v	LQFP48
NUC120LE3AN	128 KB	16 KB	Definable	4 KB	up to 31	4x32-bit	2	1	2	1	-	-	1	1	4	8x12-bit	v	-	v	LQFP48
NUC120RD3AN	64 KB	16 KB	4 KB	4 KB	up to 45	4x32-bit	2	2	2	1	-	-	1	2	6	8x12-bit	v	-	v	LQFP64
NUC120RE3AN	128 KB	16 KB	Definable	4 KB	up to 45	4x32-bit	2	2	2	1	-	-	1	2	6	8x12-bit	v	-	v	LQFP64
NUC120VD2AN	64 KB	8 KB	4 KB	4 KB	up to 76	4x32-bit	3	4	2	1	-	-	1	2	8	8x12-bit	v	-	v	LQFP100
NUC120VD3AN	64 KB	16 KB	4 KB	4 KB	up to 76	4x32-bit	3	4	2	1	-	-	1	2	8	8x12-bit	v	-	v	LQFP100
NUC120VE3AN	128 KB	16 KB	Definable	4 KB	up to 76	4x32-bit	3	4	2	1	-	-	1	2	8	8x12-bit	v	-	v	LQFP100

3.1.2 NuMicro™ NUC120 Low Density USB Line Selection Guide

Part number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity						I^2S	Comp.	PWM	ADC	RTC	EBI	ISP ICP	Package
							UART	SPI	I^2C	USB	LIN	CAN								
NUC120LC1BN	32 KB	4 KB	4 KB	4 KB	up to 31	4x32-bit	2	1	2	1	-	-	1	1	4	8x12-bit	v	-	v	LQFP48
NUC120LD1BN	64 KB	4 KB	4 KB	4 KB	up to 31	4x32-bit	2	1	2	1	-	-	1	1	4	8x12-bit	v	-	v	LQFP48
NUC120LD2BN	64 KB	8 KB	4 KB	4 KB	up to 31	4x32-bit	2	1	2	1	-	-	1	1	4	8x12-bit	v	-	v	LQFP48
NUC120RC1BN	32 KB	4 KB	4 KB	4 KB	up to 45	4x32-bit	2	2	2	1	-	-	1	2	4	8x12-bit	v	v	v	LQFP64
NUC120RD1BN	64 KB	4 KB	4 KB	4 KB	up to 45	4x32-bit	2	2	2	1	-	-	1	2	4	8x12-bit	v	v	v	LQFP64
NUC120RD2BN	64 KB	8 KB	4 KB	4 KB	up to 45	4x32-bit	2	2	2	1	-	-	1	2	4	8x12-bit	v	v	v	LQFP64

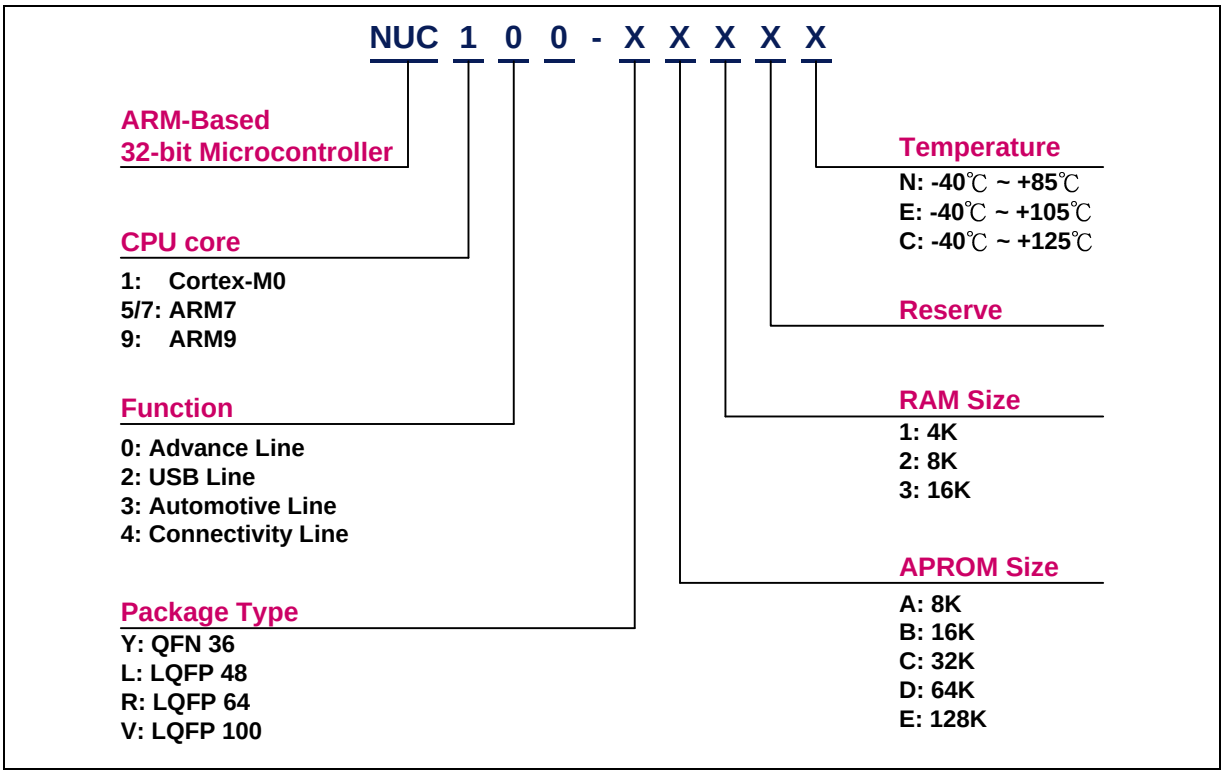


Figure 3-1 NuMicro™ NUC100 Series selection code

3.2 Pin Configuration

3.2.1 NuMicro™ NUC120 Medium Density Pin Diagram

3.2.1.1 NuMicro™ NUC120 LQFP 100 pin

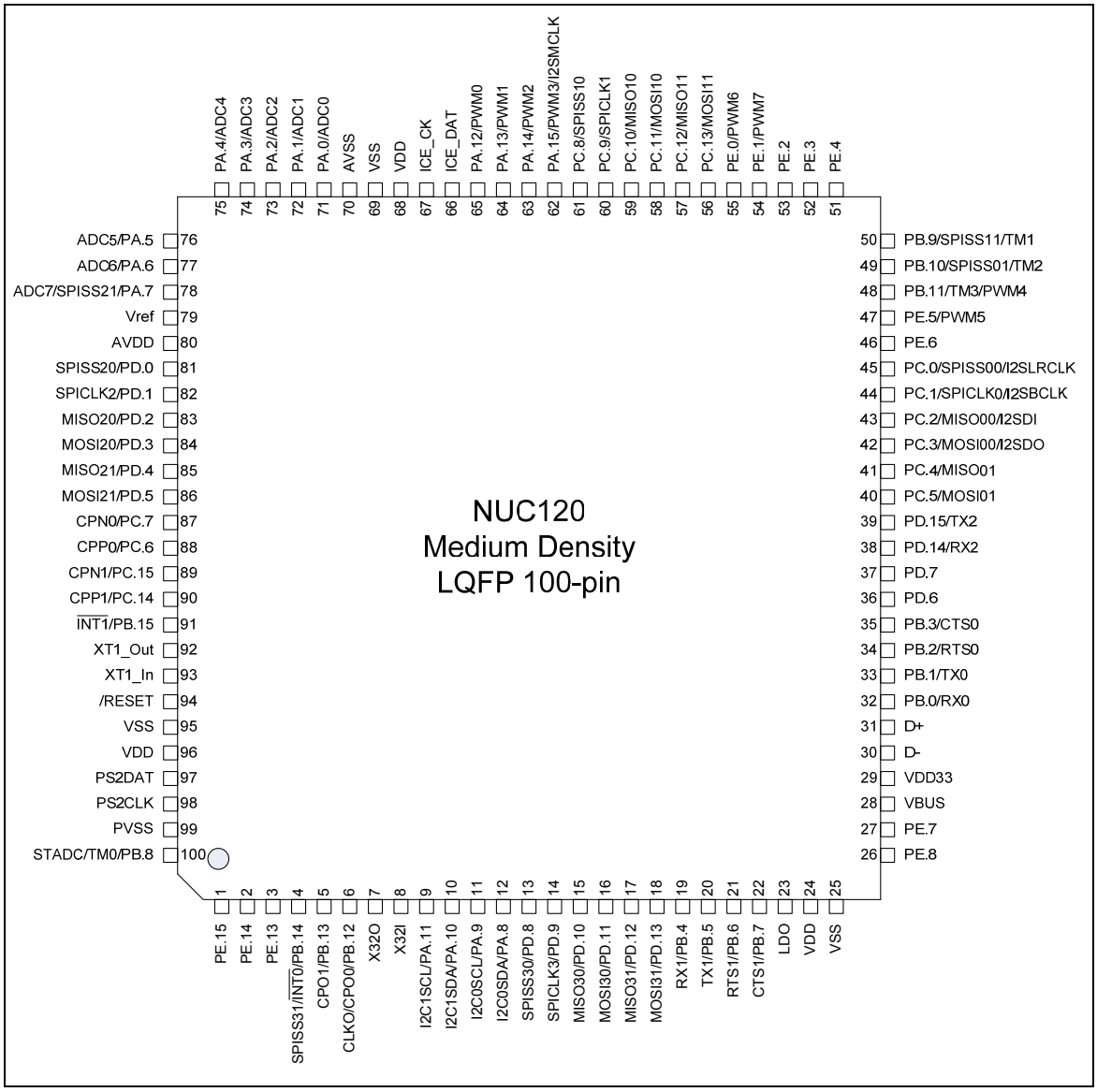


Figure 3-2 NuMicro™ NUC120 Medium Density LQFP 100-pin Pin Diagram

3.2.1.2 NuMicro™ NUC120 LQFP 64 pin

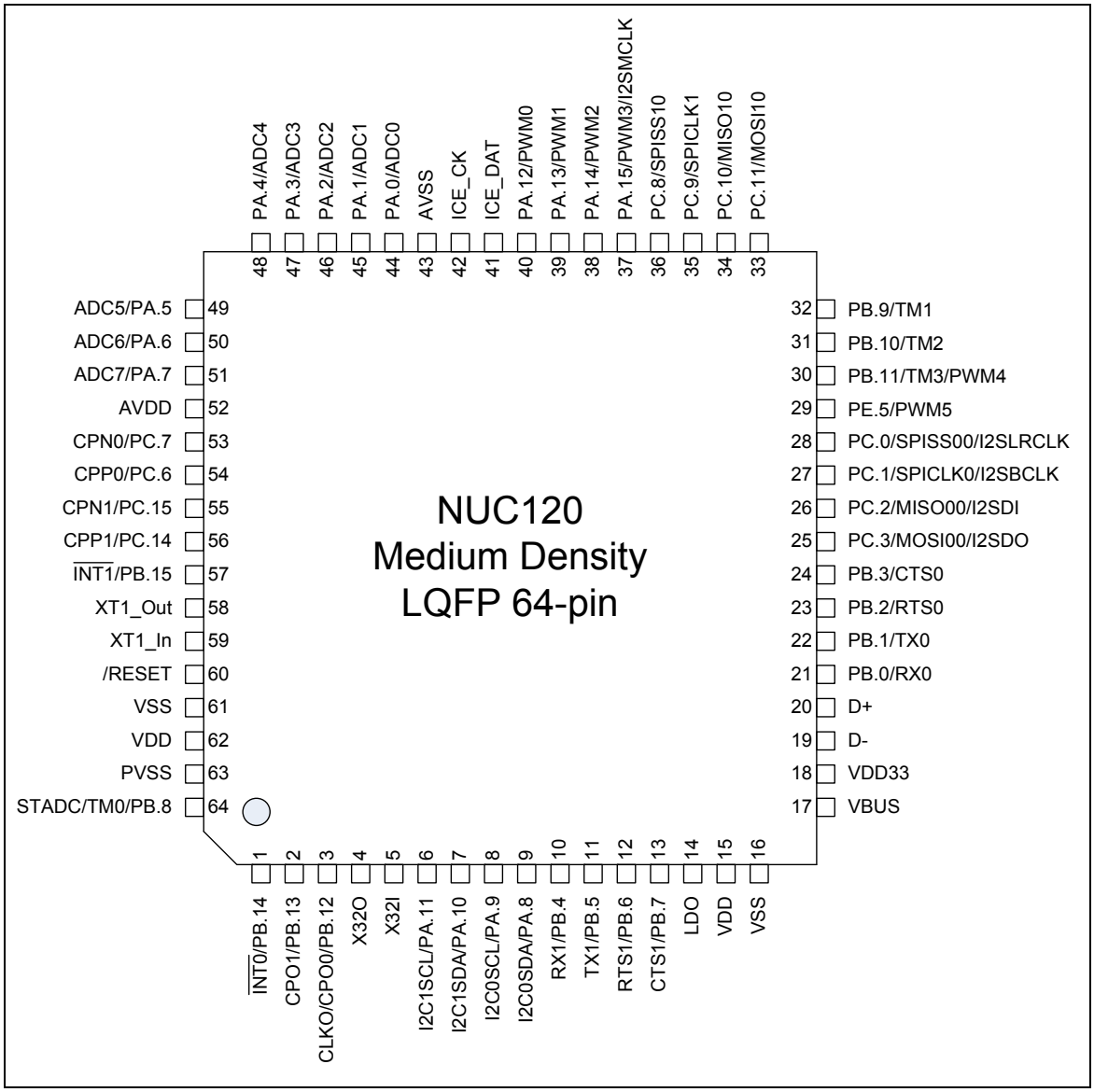


Figure 3-3 NuMicro™ NUC120 Medium Density LQFP 64-pin Pin Diagram

3.2.1.3 NuMicro™ NUC120 LQFP 48 pin

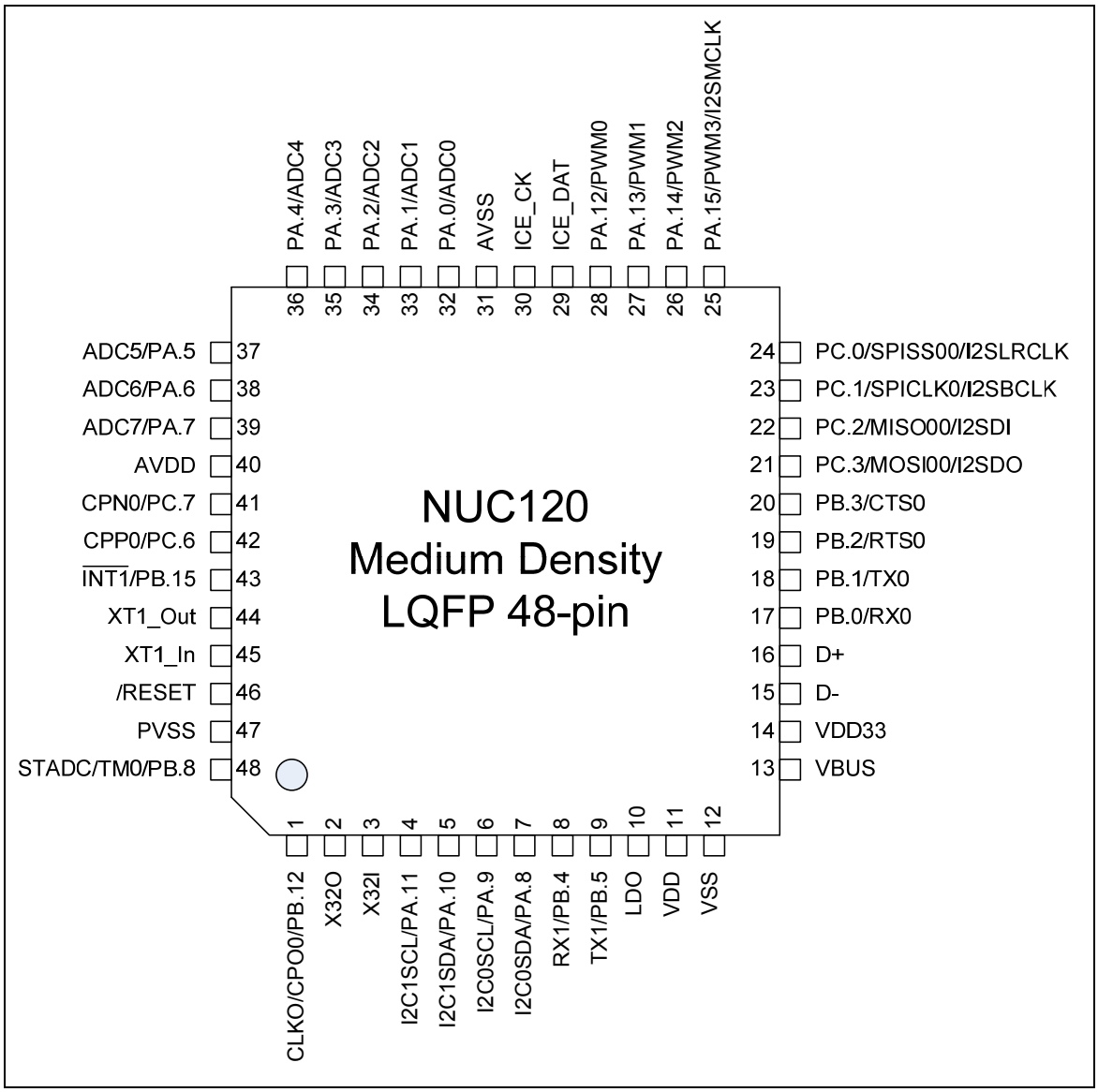


Figure 3-4 NuMicro™ NUC120 Medium Density LQFP 48-pin Pin Diagram

3.2.2 NuMicro™ NUC120 Low Density Pin Diagram

3.2.2.1 NuMicro™ NUC120 LQFP 64 pin

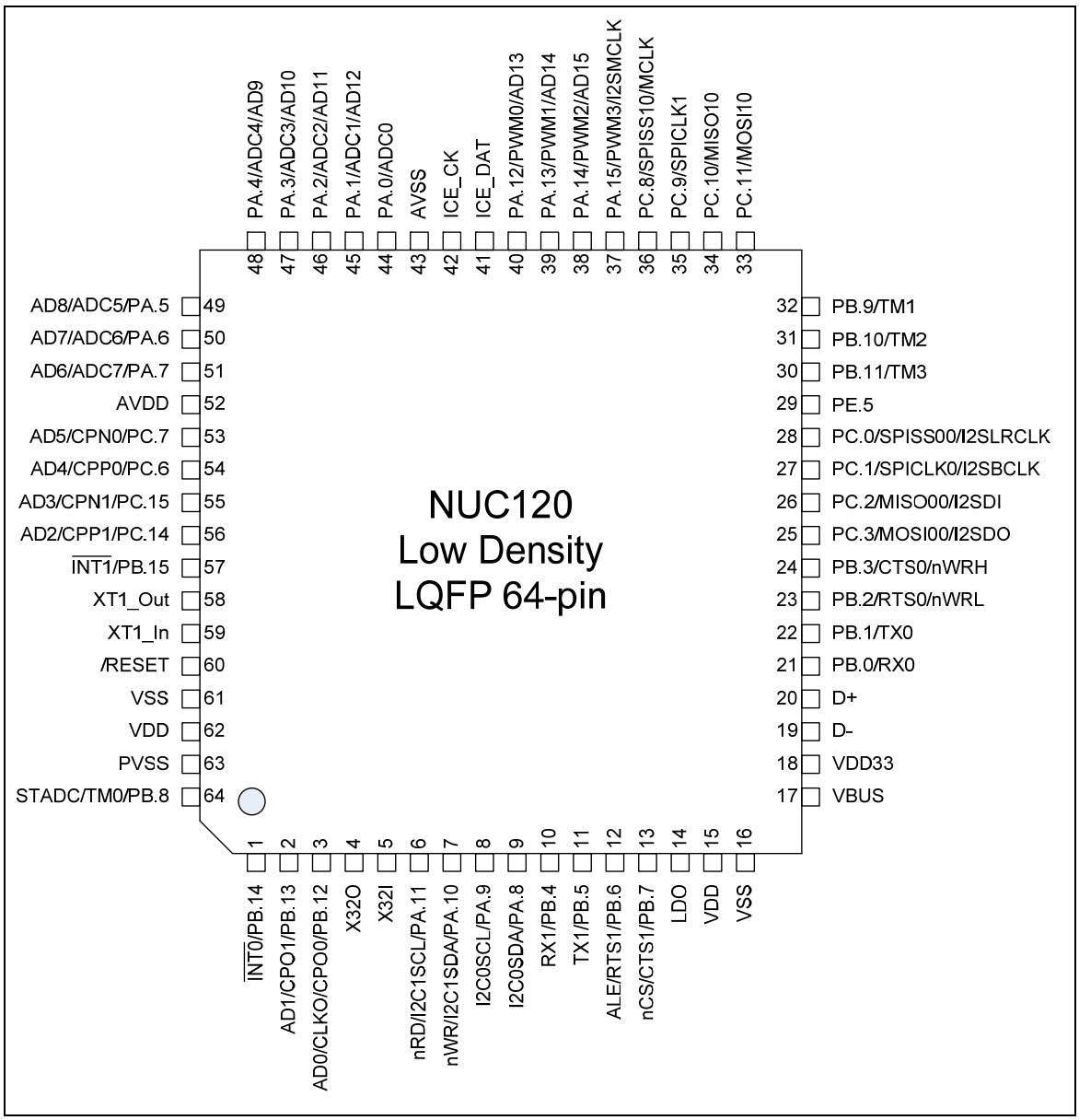


Figure 3-5 NuMicro™ NUC120 Low Density LQFP 64-pin Pin Diagram

3.2.2.2 NuMicro™ NUC120 LQFP 48 pin

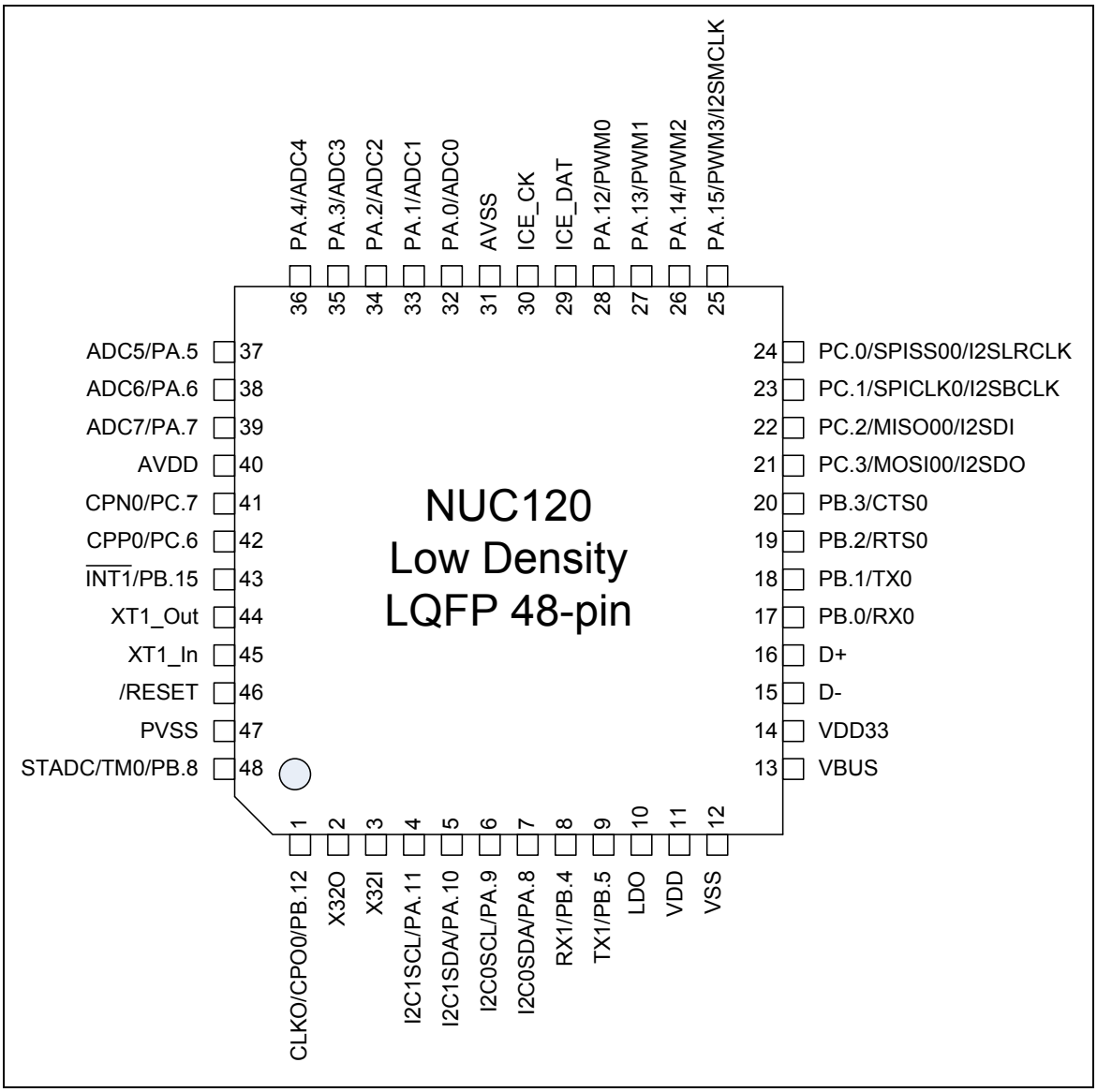


Figure 3-6 NuMicro™ NUC120 Low Density LQFP 48-pin Pin Diagram

4 ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	VDD–VSS	-0.3	+7.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into VDD		-	120	mA
Maximum Current out of VSS			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

4.2 DC Electrical Characteristics

4.2.1 NuMicro™ NUC100/NUC120/NUC130/NUC140 Medium Density DC Electrical Characteristics

(VDD-VSS=3.3V, TA = 25°C, FOSC = 50 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	2.5		5.5	V	V_{DD} =2.5V ~ 5.5V up to 50 MHz
Power Ground	V_{SS} AV_{SS}	-0.3			V	
LDO Output Voltage	V_{LDO}	-10%	2.5	+10%	V	V_{DD} > 2.7V
Analog Operating Voltage	AV_{DD}	0		V_{DD}	V	
Analog Reference Voltage	Vref	0		AV_{DD}	V	
Operating Current Normal Run Mode @ 50MHz	I_{DD1}		54		mA	V_{DD} = 5.5V@50MHz, enable all IP and PLL, XTAL=12MHz
	I_{DD2}		31		mA	V_{DD} = 5.5V@50MHz, disable all IP and enable PLL, XTAL=12MHz
	I_{DD3}		51		mA	V_{DD} = 3V@50MHz, enable all IP and PLL, XTAL=12MHz
	I_{DD4}		28		mA	V_{DD} = 3V@50MHz, disable all IP and enable PLL, XTAL=12MHz
Operating Current Normal Run Mode @ 12MHz	I_{DD5}		22		mA	V_{DD} = 5.5V@12MHz, enable all IP and disable PLL, XTAL=12MHz
	I_{DD6}		14		mA	V_{DD} = 5.5V@12MHz, disable all IP and disable PLL, XTAL=12MHz
	I_{DD7}		20		mA	V_{DD} = 3V@12MHz, enable all IP and disable PLL, XTAL=12MHz

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
	I_{DD8}		12		mA	V_{DD} = 3V@12MHz, disable all IP and disable PLL, XTAL=12MHz
Operating Current Normal Run Mode @ 4MHz	I_{DD9}		15		mA	V_{DD} = 5V@4MHz, enable all IP and disable PLL, XTAL=4MHz
	I_{DD10}		11		mA	V_{DD} = 5V@4MHz, disable all IP and disable PLL, XTAL=4MHz
	I_{DD11}		13		mA	V_{DD} = 3V@4MHz, enable all IP and disable PLL, XTAL=4MHz
	I_{DD12}		9		mA	V_{DD} = 3V@4MHz, disable all IP and disable PLL, XTAL=4MHz
Operating Current Idle Mode @ 50MHz	I_{IDLE1}		38		mA	V_{DD}= 5.5V@50MHz, enable all IP and PLL, XTAL=12MHz
	I_{IDLE2}		15		mA	V_{DD}=5.5V@50MHz, disable all IP and enable PLL, XTAL=12MHz
	I_{IDLE3}		35		mA	V_{DD} = 3V@50MHz, enable all IP and PLL, XTAL=12MHz
	I_{IDLE4}		13		mA	V_{DD} = 3V@50MHz, disable all IP and enable PLL, XTAL=12MHz
Operating Current Idle Mode @ 12MHz	I_{IDLE5}		13		mA	V_{DD} = 5.5V@12MHz, enable all IP and disable PLL, XTAL=12MHz
	I_{IDLE6}		5.5		mA	V_{DD} = 5.5V@12MHz, disable all IP and disable PLL, XTAL=12MHz
	I_{IDLE7}		12		mA	V_{DD} = 3V@12MHz, enable all IP and disable PLL, XTAL=12MHz
	I_{IDLE8}		4		mA	V_{DD} = 3V@12MHz, disable all IP and disable PLL, XTAL=12MHz

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating Current Idle Mode @ 4MHz	I_{IDLE9}		8.5		mA	V_{DD} = 5V@4MHz, enable all IP and disable PLL, XTAL=4MHz
	I_{IDLE10}		3.5		mA	V_{DD} = 5V@4MHz, disable all IP and disable PLL, XTAL=4MHz
	I_{IDLE11}		7		mA	V_{DD} = 3V@4MHz, enable all IP and disable PLL, XTAL=4MHz
	I_{IDLE12}		2.5		mA	V_{DD} = 3V@4MHz, disable all IP and disable PLL, XTAL=4MHz
Standby Current Power-down Mode (Deep Sleep Mode)	I_{PWD1}		23		μA	V_{DD} = 5.5V, RTC OFF, No load @ Disable BOV function
	I_{PWD2}		18		μA	V_{DD} = 3.3V, RTC OFF, No load @ Disable BOV function
	I_{PWD3}		28		μA	V_{DD} = 5.5V, RTC run , No load @ Disable BOV function
	I_{PWD4}		22		μA	V_{DD} = 3.3V, RTC run , No load @ Disable BOV function
Input Current PA, PB, PC, PD, PE (Quasi-bidirectional mode)	I_{IN1}		-50	-60	μA	V_{DD} = 5.5V, V_{IN} = 0V or V_{IN}=V_{DD}
Input Current at /RESET[1]	I_{IN2}	-55	-45	-30	μA	V_{DD} = 3.3V, V_{IN} = 0.45V
Input Leakage Current PA, PB, PC, PD, PE	I_{LK}	-2	-	+2	μA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current PA~PE (Quasi-bidirectional mode)	I_{TL} [3]	-650	-	-200	μA	V_{DD} = 5.5V, V_{IN}<2.0V
Input Low Voltage PA, PB, PC, PD, PE (TTL input)	V_{IL1}	-0.3	-	0.8	V	V_{DD} = 4.5V
		-0.3	-	0.6		V_{DD} = 2.5V
Input High Voltage PA, PB, PC, PD, PE (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.5	-	V_{DD} +0.2		V_{DD} =3.0V
Input Low Voltage PA, PB, PC, PD, PE (Schmitt input)	V_{IL2}				V	
Input High Voltage PA, PB, PC, PD, PE (Schmitt input)	V_{IH2}		0.2V_{DD}		V	
Hysteresis voltage of PA~PE (Schmitt input)	V_{HY}		0.2V_{DD}		V	

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Input Low Voltage XT1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.4		V_{DD} = 3.0V
Input High Voltage XT1[*2]	V_{IH3}	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.4	-	V_{DD} +0.2		V_{DD} = 3.0V
Input Low Voltage X32I[*2]	V_{IL4}	0	-	0.4	v	
Input High Voltage X32I[*2]	V_{IH4}	1.7		2.5	V	
Negative going threshold (Schmitt input), /RESET	V_{ILS}	-0.5	-	$0.3V_{DD}$	V	
Positive going threshold (Schmitt input), /RESET	V_{IHS}	$0.7V_{DD}$	-	V_{DD}+0.5	V	
Source Current PA, PB, PC, PD, PE (Quasi-bidirectional Mode)	I_{SR11}	-300	-370	-450	μA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR12}	-50	-70	-90	μA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR12}	-40	-60	-80	μA	V_{DD} = 2.5V, V_S = 2.0V
Source Current PA, PB, PC, PD, PE (Push-pull Mode)	I_{SR21}	-20	-24	-28	mA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR22}	-4	-6	-8	mA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR22}	-3	-5	-7	mA	V_{DD} = 2.5V, V_S = 2.0V
Sink Current PA, PB, PC, PD, PE (Quasi-bidirectional and Push-pull Mode)	I_{SK1}	10	16	20	mA	V_{DD} = 4.5V, V_S = 0.45V
	I_{SK1}	7	10	13	mA	V_{DD} = 2.7V, V_S = 0.45V
	I_{SK1}	6	9	12	mA	V_{DD} = 2.5V, V_S = 0.45V
Brownout voltage with BOV_VL [1:0] =00b	$V_{BO2.2}$	2.1	2.2	2.3	V	
Brownout voltage with BOV_VL [1:0] =01b	$V_{BO2.7}$	2.6	2.7	2.8	V	
Brownout voltage with BOV_VL [1:0] =10b	$V_{BO3.8}$	3.7	3.8	3.9	V	
Brownout voltage with BOV_VL [1:0] =11b	$V_{BO4.5}$	4.4	4.5	4.6	V	
Hysteresis range of BOD voltage	V_{BH}	30	-	150	mV	V_{DD} = 2.5V~5.5V

Note:

1. /RESET pin is a Schmitt trigger input.

2. Crystal Input is a CMOS input.

3. Pins of PA, PB, PC, PD and PE can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5V, 5he transition current reaches its maximum value when V_{IN} approximates to 2V.

4.2.2 NuMicro™ NUC100/NUC120/NUC130/NUC140 Low Density DC Electrical Characteristics

(VDD-VSS=3.3V, TA = 25°C, FOSC = 50 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	2.5		5.5	V	V_{DD} =2.5V ~ 5.5V up to 50 MHz
Power Ground	V_{SS} AV_{SS}	-0.3			V	
LDO Output Voltage	V_{LDO}	-10%	2.5	+10%	V	V_{DD} > 2.7V
Analog Operating Voltage	AV_{DD}	0		V_{DD}	V	
Analog Reference Voltage	Vref	0		AV_{DD}	V	
Operating Current Normal Run Mode @ 50MHz	I_{DD1}		46		mA	V_{DD} = 5.5V@50MHz, enable all IP and PLL, XTAL=12MHz
	I_{DD2}		30		mA	V_{DD} = 5.5V@50MHz, disable all IP and enable PLL, XTAL=12MHz
	I_{DD3}		44		mA	V_{DD} = 3V@50MHz, enable all IP and PLL, XTAL=12MHz
	I_{DD4}		28		mA	V_{DD} = 3V@50MHz, disable all IP and enable PLL, XTAL=12MHz
Operating Current Normal Run Mode @ 12MHz	I_{DD5}		19		mA	V_{DD} = 5.5V@12MHz, enable all IP and disable PLL, XTAL=12MHz
	I_{DD6}		13		mA	V_{DD} = 5.5V@12MHz, disable all IP and disable PLL, XTAL=12MHz
	I_{DD7}		17		mA	V_{DD} = 3V@12MHz, enable all IP and disable PLL, XTAL=12MHz
	I_{DD8}		11.5		mA	V_{DD} = 3V@12MHz, disable all IP and disable PLL, XTAL=12MHz

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating Current Normal Run Mode @ 4MHz	I_{DD9}		13.5		mA	V_{DD} = 5V@4MHz, enable all IP and disable PLL, XTAL=4MHz
	I_{DD10}		10		mA	V_{DD} = 5V@4MHz, disable all IP and disable PLL, XTAL=4MHz
	I_{DD11}		12		mA	V_{DD} = 3V@4MHz, enable all IP and disable PLL, XTAL=4MHz
	I_{DD12}		8		mA	V_{DD} = 3V@4MHz, disable all IP and disable PLL, XTAL=4MHz
Operating Current Idle Mode @ 50MHz	I_{IDLE1}		30		mA	V_{DD}= 5.5V@50MHz, enable all IP and PLL, XTAL=12MHz
	I_{IDLE2}		13		mA	V_{DD}=5.5V@50MHz, disable all IP and enable PLL, XTAL=12MHz
	I_{IDLE3}		28		mA	V_{DD} = 3V@50MHz, enable all IP and PLL, XTAL=12MHz
	I_{IDLE4}		12		mA	V_{DD} = 3V@50MHz, disable all IP and enable PLL, XTAL=12MHz
Operating Current Idle Mode @ 12MHz	I_{IDLE5}		11		mA	V_{DD} = 5.5V@12MHz, enable all IP and disable PLL, XTAL=12MHz
	I_{IDLE6}		5		mA	V_{DD} = 5.5V@12MHz, disable all IP and disable PLL, XTAL=12MHz
	I_{IDLE7}		10		mA	V_{DD} = 3V@12MHz, enable all IP and disable PLL, XTAL=12MHz
	I_{IDLE8}		4		mA	V_{DD} = 3V@12MHz, disable all IP and disable PLL, XTAL=12MHz
Operating Current Idle Mode	I_{IDLE9}		7		mA	V_{DD} = 5V@4MHz, enable all IP and disable PLL, XTAL=4MHz

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
@ 4MHz	I_{IDLE10}		3.5		mA	V_{DD} = 5V@4MHz, disable all IP and disable PLL, XTAL=4MHz
	I_{IDLE11}		6		mA	V_{DD} = 3V@4MHz, enable all IP and disable PLL, XTAL=4MHz
	I_{IDLE12}		2.5		mA	V_{DD} = 3V@4MHz, disable all IP and disable PLL, XTAL=4MHz
Standby Current Power-down Mode (Deep Sleep Mode)	I_{PWD1}		17		μA	V_{DD} = 5.5V, RTC OFF, No load @ Disable BOV function
	I_{PWD2}		14.5		μA	V_{DD} = 3.3V, RTC OFF, No load @ Disable BOV function
	I_{PWD3}		20		μA	V_{DD} = 5.5V, RTC run , No load @ Disable BOV function
	I_{PWD4}		17		μA	V_{DD} = 3.3V, RTC run , No load @ Disable BOV function
Input Current PA, PB, PC, PD, PE (Quasi-bidirectional mode)	I_{IN1}		-50	-60	μA	V_{DD} = 5.5V, V_{IN} = 0V or V_{IN}=V_{DD}
Input Current at /RESET[1]	I_{IN2}	-55	-45	-30	μA	V_{DD} = 3.3V, V_{IN} = 0.45V
Input Leakage Current PA, PB, PC, PD, PE	I_{LK}	-2	-	+2	μA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current PA~PE (Quasi-bidirectional mode)	I_{TL} [3]	-650	-	-200	μA	V_{DD} = 5.5V, V_{IN}<2.0V
Input Low Voltage PA, PB, PC, PD, PE (TTL input)	V_{IL1}	-0.3	-	0.8	V	V_{DD} = 4.5V
		-0.3	-	0.6		V_{DD} = 2.5V
Input High Voltage PA, PB, PC, PD, PE (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.5	-	V_{DD} +0.2		V_{DD} =3.0V
Input Low Voltage PA, PB, PC, PD, PE (Schmitt input)	V_{IL2}	-0.5	-	0.2V_{DD}	V	
Input High Voltage PA, PB, PC, PD, PE (Schmitt input)	V_{IH2}	0.4V_{DD}	-	V_{DD} +0.5	V	
Input Low Voltage XT1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.4		V_{DD} = 3.0V
Input High Voltage XT1[*2]	V_{IH3}	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.4	-	V_{DD} +0.2		V_{DD} = 3.0V

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Input Low Voltage X32I[*2]	V_{IL4}	0	-	0.4	v	
Input High Voltage X32I[*2]	V_{IH4}	1.7		2.5	V	
Negative going threshold (Schmitt input), /RESET	V_{ILS}	-0.5	-	$0.3V_{DD}$	V	
Positive going threshold (Schmitt input), /RESET	V_{IHS}	$0.7V_{DD}$	-	V_{DD}+0.5	V	
Source Current PA, PB, PC, PD, PE (Quasi-bidirectional Mode)	I_{SR11}	-300	-370	-450	μA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR12}	-50	-70	-90	μA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR12}	-40	-60	-80	μA	V_{DD} = 2.5V, V_S = 2.0V
Source Current PA, PB, PC, PD, PE (Push-pull Mode)	I_{SR21}	-20	-24	-28	mA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR22}	-4	-6	-8	mA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR22}	-3	-5	-7	mA	V_{DD} = 2.5V, V_S = 2.0V
Sink Current PA, PB, PC, PD, PE (Quasi-bidirectional and Push-pull Mode)	I_{SK1}	10	16	20	mA	V_{DD} = 4.5V, V_S = 0.45V
	I_{SK1}	7	10	13	mA	V_{DD} = 2.7V, V_S = 0.45V
	I_{SK1}	6	9	12	mA	V_{DD} = 2.5V, V_S = 0.45V
Brownout voltage with BOV_VL [1:0] =00b	$V_{BO2.2}$	2.1	2.2	2.3	V	
Brownout voltage with BOV_VL [1:0] =01b	$V_{BO2.7}$	2.6	2.7	2.8	V	
Brownout voltage with BOV_VL [1:0] =10b	$V_{BO3.8}$	3.7	3.8	3.9	V	
Brownout voltage with BOV_VL [1:0] =11b	$V_{BO4.5}$	4.4	4.5	4.6	V	
Hysteresis range of BOD voltage	V_{BH}	30	-	150	mV	V_{DD} = 2.5V~5.5V

Note:

1. /RESET pin is a Schmitt trigger input.

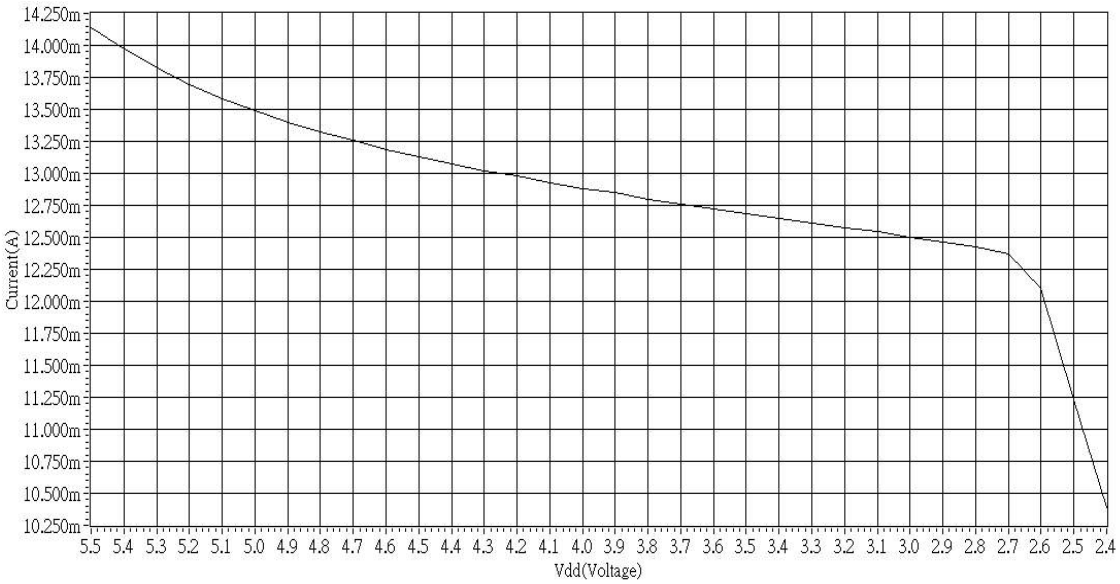
2. Crystal Input is a CMOS input.

3. Pins of PA, PB, PC, PD and PE can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5V, 5he transition current reaches its maximum value when V_{IN} approximates to 2V.

4.2.3 Operating Current Curve (Test condition: run NOP)

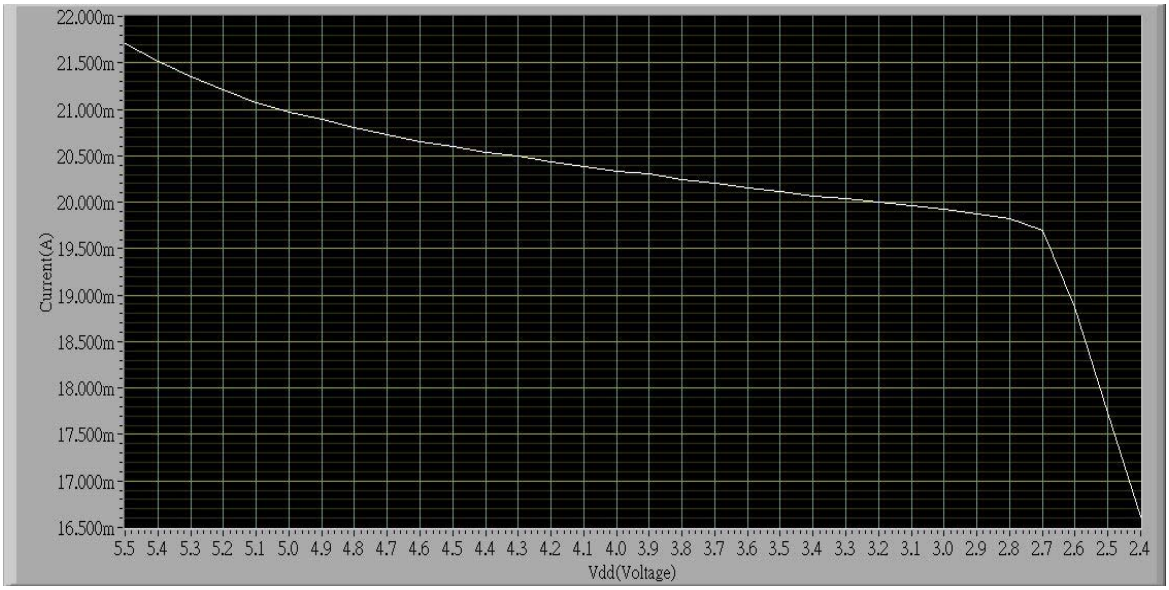
1. XTAL clock = 12 MHz, PLL disable, all-IP disable:

Unit: mA



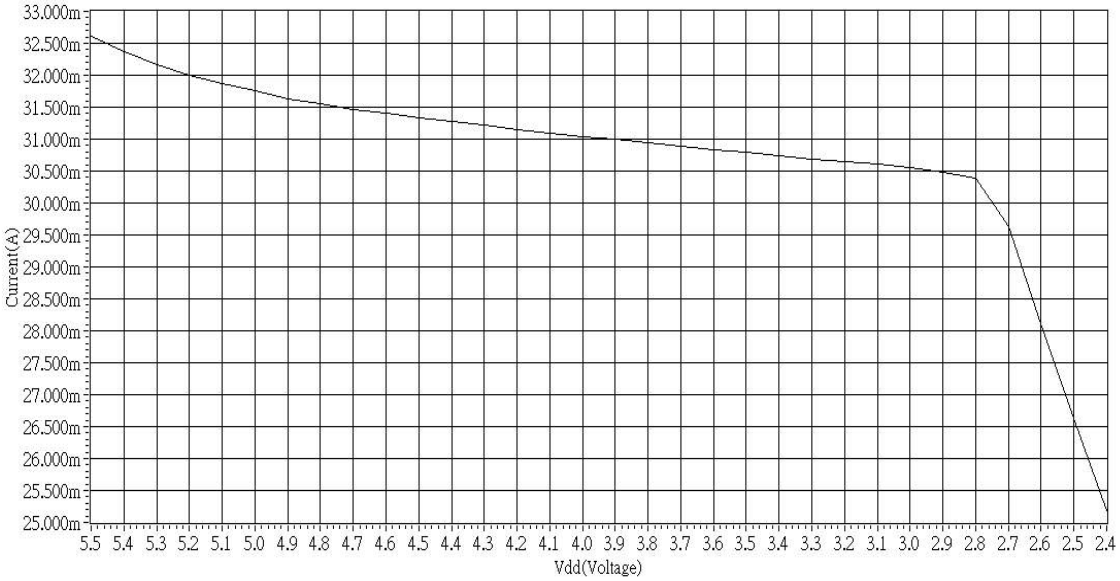
2. XTAL clock = 12 MHz, PLL disable, all-IP enable

Unit: mA



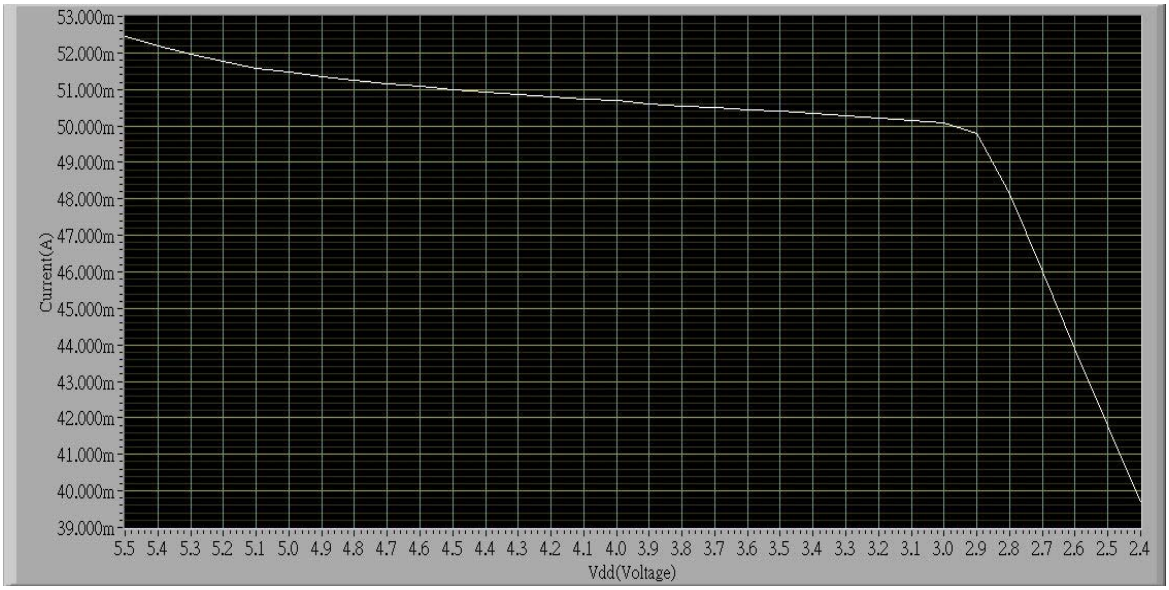
3. XTAL clock = 12 MHz, PLL enable, all-IP disable

Unit: mA



4. XTAL clock = 12 MHz, PLL enable, all-IP enable

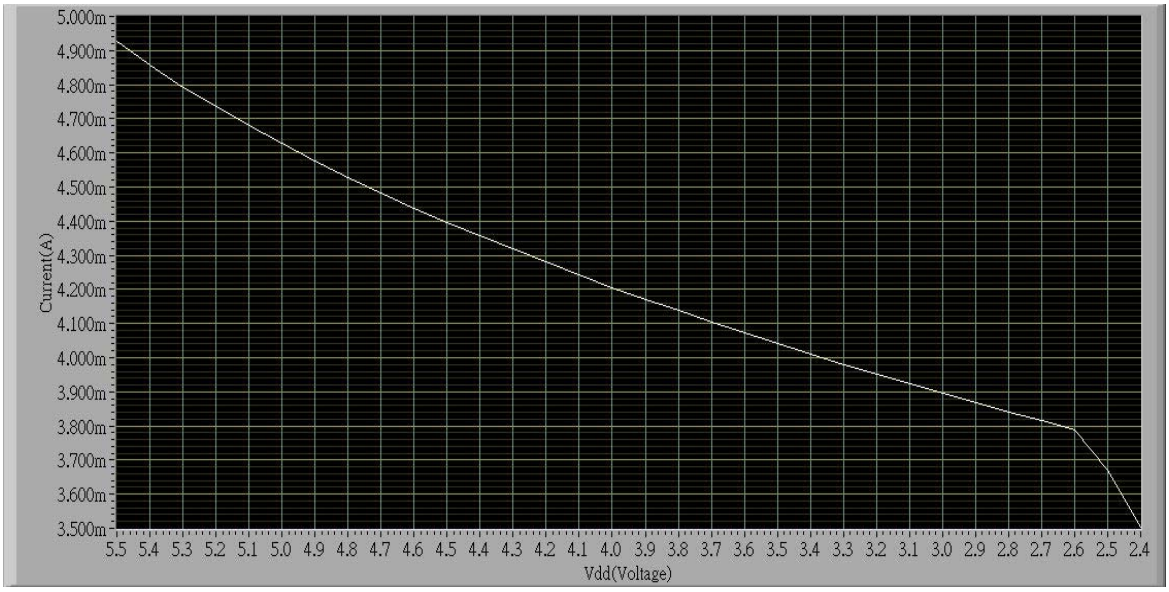
Unit: mA



4.2.4 Idle Current Curve

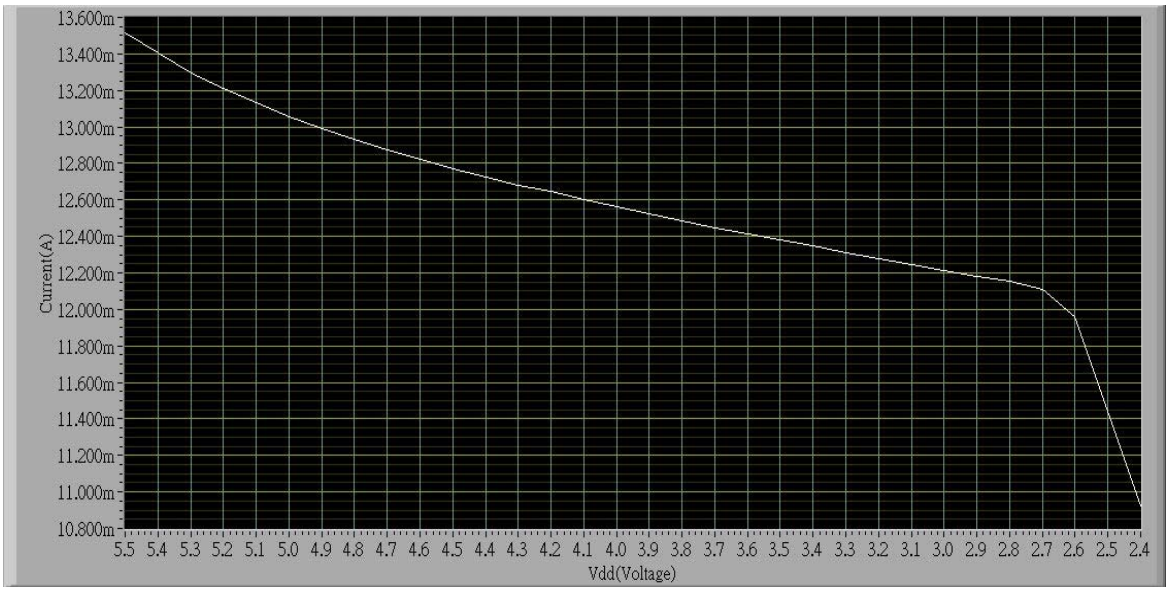
1. XTAL clock = 12 MHz, PLL disable, all-IP disable

Unit: mA



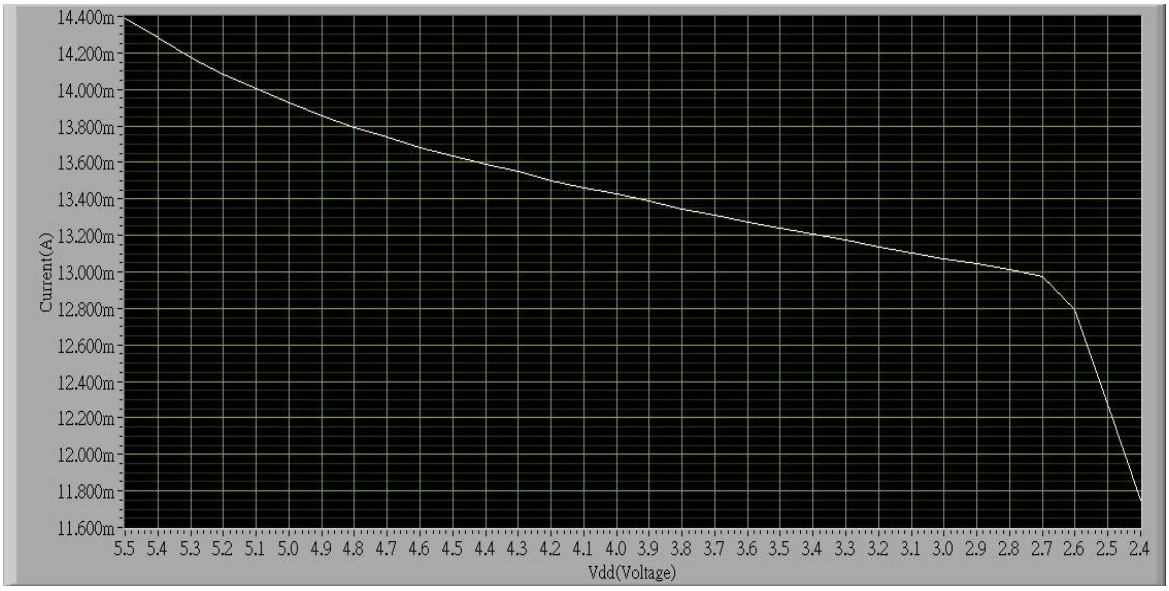
2. XTAL clock = 12 MHz, PLL disable, all-IP enable

Unit: mA



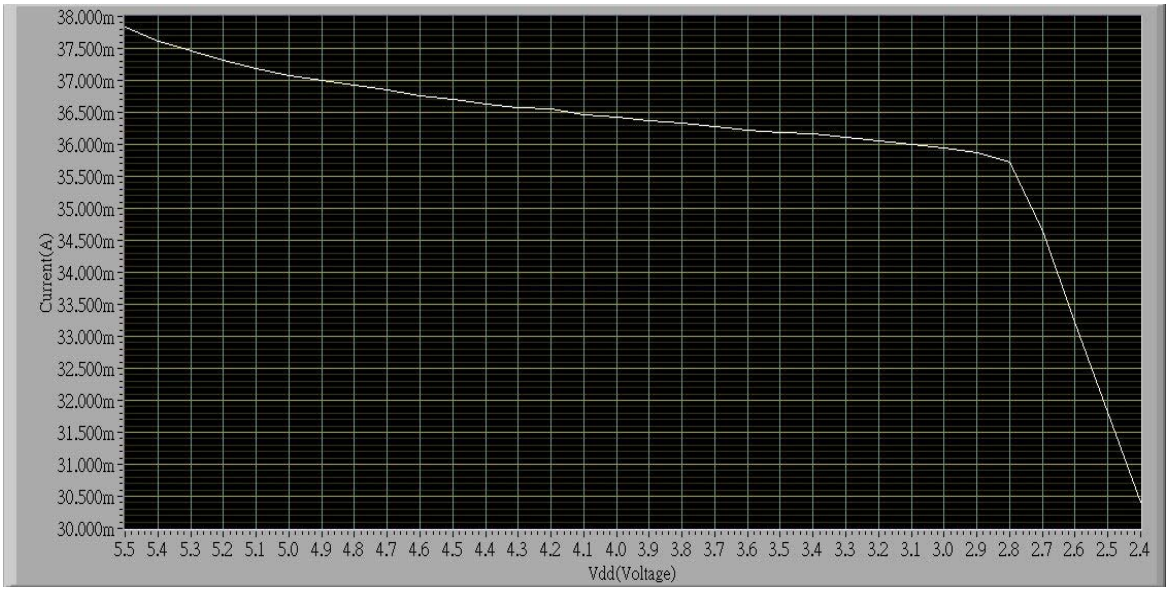
3. XTAL clock = 12 MHz, PLL enable, all-IP disable

Unit: mA



4. XTAL clock = 12 MHz, PLL enable, all-IP enable

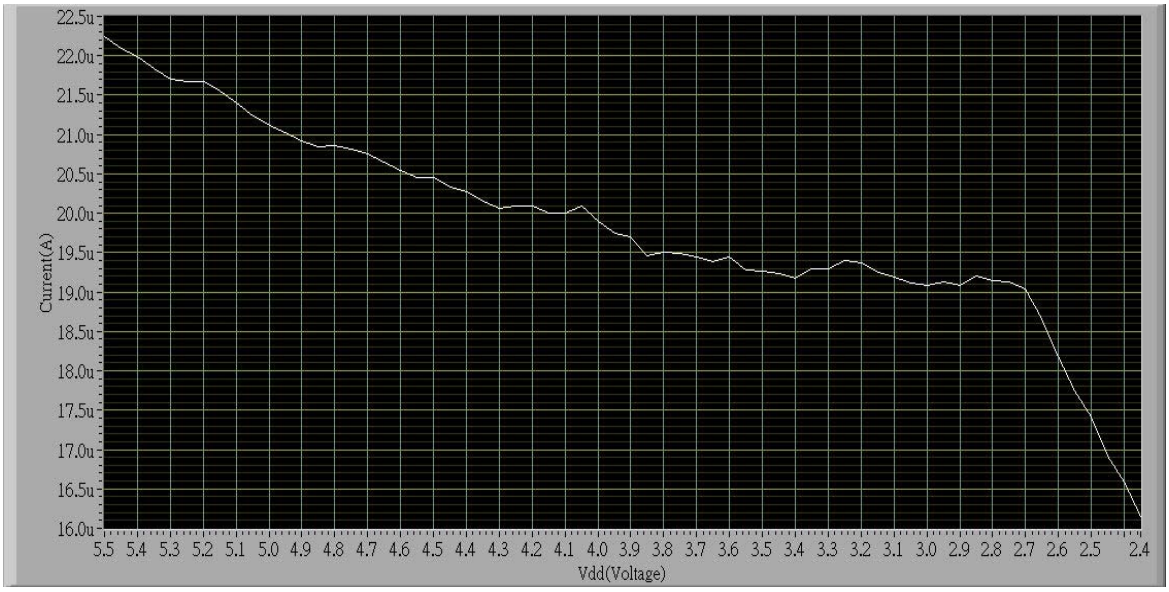
Unit: mA



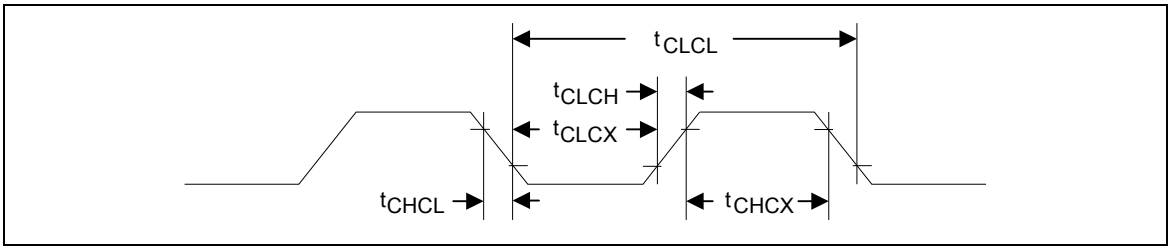
4.2.5 Power Down Current Curve

XTAL clock = 12 MHz, PLL Disable

Unit: mA



4.3 AC Electrical Characteristics



Note: Duty cycle is 50%.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CHCX}	Clock High Time		20	-	-	nS
t_{CLCX}	Clock Low Time		20	-	-	nS
t_{CLCH}	Clock Rise Time		-	-	10	nS
t_{CHCL}	Clock Fall Time		-	-	10	nS

4.3.1 External 4~24MHz Crystal

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	4	12	24	MHz
Temperature	-	-40	-	85	℃
VDD	-	2.5	5	5.5	V

4.3.1.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4MHz ~ 24 MHz	without	without	without

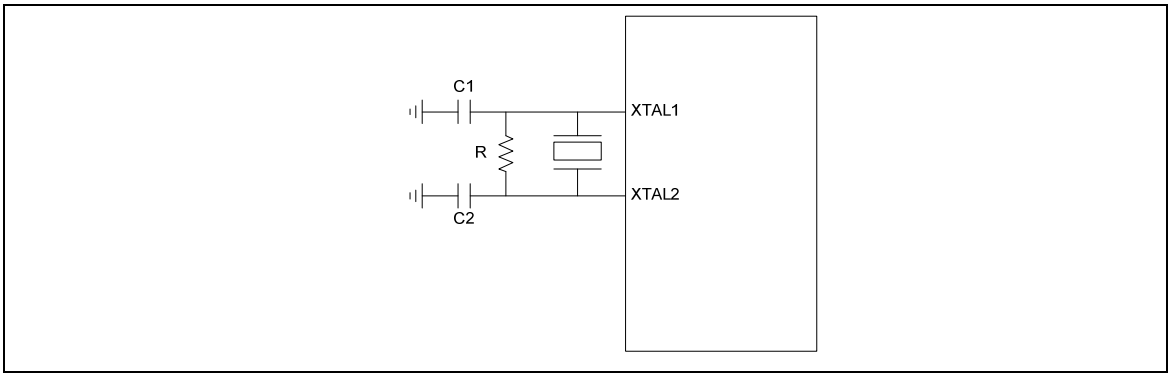


Figure 4-1 Typical Crystal Application Circuit

4.3.2 External 32.768 kHz Crystal

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	-	32.768	-	kHz
Temperature	-	-40	-	85	℃
VDD	-	2.5	-	5.5	V

4.3.3 Internal 22.1184 MHz Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage[1]	-	2.5	-	5.5	V
Center Frequency	-	-	22.1184	-	MHz
Calibrated Internal Oscillator Frequency	+25 C; V_{DD} =5V	-1	-	+1	%
	-40 C~+85 C; VDD=2.5V~5.5V	-3	-	+3	%
Operation Current	V_{DD} =5V	-	500	-	uA

4.3.4 Internal 10 kHz Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage[1]	-	2.5	-	5.5	V
Center Frequency	-	-	10	-	kHz
Calibrated Internal Oscillator Frequency	+25 C; V_{DD} =5V	-30	-	+30	%
	-40 C~+85 C; V_{DD}=2.5V~5.5V	-50	-	+50	%

Note: Internal operation voltage comes from LDO.

4.4 Analog Characteristics

4.4.1 Specification of 12-bit SARADC

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
-	Resolution	-	-	12	Bit
DNL	Differential nonlinearity error	-	±3	-	LSB
INL	Integral nonlinearity error	-	±4	-	LSB
EO	Offset error	-	±1	10	LSB
EG	Gain error (Transfer gain)	-	1	1.005	-
-	Monotonic	Guaranteed			
FADC	ADC clock frequency	-	-	20	MHz
TCAL	Calibration time	-	127	-	Clock
TS	Sample time	-	7	-	Clock
TADC	Conversion time	-	13	-	Clock
FS	Sample rate	-	-	600	K SPS
VLDO	Supply voltage	-	2.5	-	V
VADD		3	-	5.5	V
IDD	Supply current (Avg.)	-	0.5	-	mA
IDDA		-	1.5	-	mA
VREF	Reference voltage	-	VDDA	-	V
IREFP	Reference current (Avg.)	-	1	-	mA
VIN	Reference voltage	0	-	VREF	V
CIN	Capacitance	-	5	-	pF

4.4.2 Specification of LDO & Power management

PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
Input Voltage	2.7	5	5.5	V	V_{DD} input voltage
Output Voltage	-10%	2.5	+10%	V	V_{DD} > 2.7V
Temperature	-40	25	85	℃	
Quiescent Current (PD=0)	-	100	-	uA	
Quiescent Current (PD=1)	-	5	-	uA	
Iload (PD=0)	-	-	100	mA	
Iload (PD=1)	-	-	100	uA	
Cbp	-	1	-	uF	Resr=1ohm
Cload	-	250	-	pF	

Note:

1. It is recommended that a 10uF or higher capacitor and a 100nF bypass capacitor are connected between VDD and the closest VSS pin of the device.

2. For ensuring power stability, a 4.7uF or higher capacitor must be connected between LDO pin and the closest VSS pin of the device. Also a 100nF bypass capacitor between LDO and VSS help suppressing output noise.

4.4.3 Specification of Low Voltage Reset

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	1.7	-	5.5	V
Quiescent current	VDD5V=5.5V	-	-	5	uA
Temperature	-	-40	25	85	℃
Threshold voltage	Temperature=25°	1.7	2.0	2.3	V
	Temperature=-40°	-	2.4	-	V
	Temperature=85°	-	1.6	-	V
Hysteresis	-	0	0	0	V

4.4.4 Specification of Brownout Detector

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	2.5	-	5.5	V
Quiescent current	AVDD=5.5V	-	-	125	μA
Temperature	-	-40	25	85	℃
Brown-out voltage	BOV_VL[1:0]=11	4.4	4.5	4.6	V
	BOV_VL [1:0]=10	3.7	3.8	3.9	V
	BOV_VL [1:0]=01	2.6	2.7	2.8	V
	BOV_VL [1:0]=00	2.1	2.2	2.3	V
Hysteresis	-	30	-	150	mV

4.4.5 Specification of Power-On Reset (5V)

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Temperature	-	-40	25	85	℃
Reset voltage	V+	-	2	-	V
Quiescent current	Vin>reset voltage	-	1	-	nA

4.4.6 Specification of Temperature Sensor

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltage[1]		2.5	-	5.5	V
Temperature		-40	-	125	℃
Current consumption		6.4	-	10.5	uA
Gain		-1.95	-2	-2.05	mV/℃
Offset	Temp=0 ℃	688	708	730	mV

Note: Internal operation voltage comes form LDO.

4.4.7 Specification of Comparator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Temperature	-	-40	25	85	℃
VDD	-	2.4	3	5.5	V
VDD current	20uA@VDD=3V	-	20	40	uA
Input offset voltage	-	-	5	15	mV
Output swing	-	0.1	-	VDD-0.1	V
Input common mode range	-	0.1	-	VDD-1.2	V
DC gain	-	-	70	-	dB
Propagation delay	@VCM=1.2V & VDIFF=0.1V	-	200	-	ns
Comparison voltage	20mV@VCM=1V 50mV@VCM=0.1V 50mV@VCM=VDD-1.2 @10mV for non-hysteresis	10	20	-	mV
Hysteresis	One bit control W/O & W. hysteresis @VCM=0.4V ~ VDD-1.2V	-	±10	-	mV
Wake up time	@CINP=1.3V CINN=1.2V	-	-	2	us

4.4.8 Specification of USB PHY

4.4.8.1 USB DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input high (driven)		2.0			V
V_{IL}	Input low				0.8	V
V_{DI}	Differential input sensitivity	|PADP-PADM|	0.2			V
V_{CM}	Differential common-mode range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single-ended receiver threshold		0.8		2.0	V
	Receiver hysteresis			200		mV
V_{OL}	Output low (driven)		0		0.3	V
V_{OH}	Output high (driven)		2.8		3.6	V
V_{CRS}	Output signal cross voltage		1.3		2.0	V
R_{PU}	Pull-up resistor		1.425		1.575	kΩ
R_{PD}	Pull-down resistor		14.25		15.75	kΩ
V_{TRM}	Termination Voltage for upstream port pull up (RPU)		3.0		3.6	V
Z_{DRV}	Driver output resistance	Steady state drive*		10		Ω
C_{IN}	Transceiver capacitance	Pin to GND			20	pF

*Driver output resistance doesn't include series resistor resistance.

4.4.8.2 USB Full-Speed Driver Electrical Characteristics

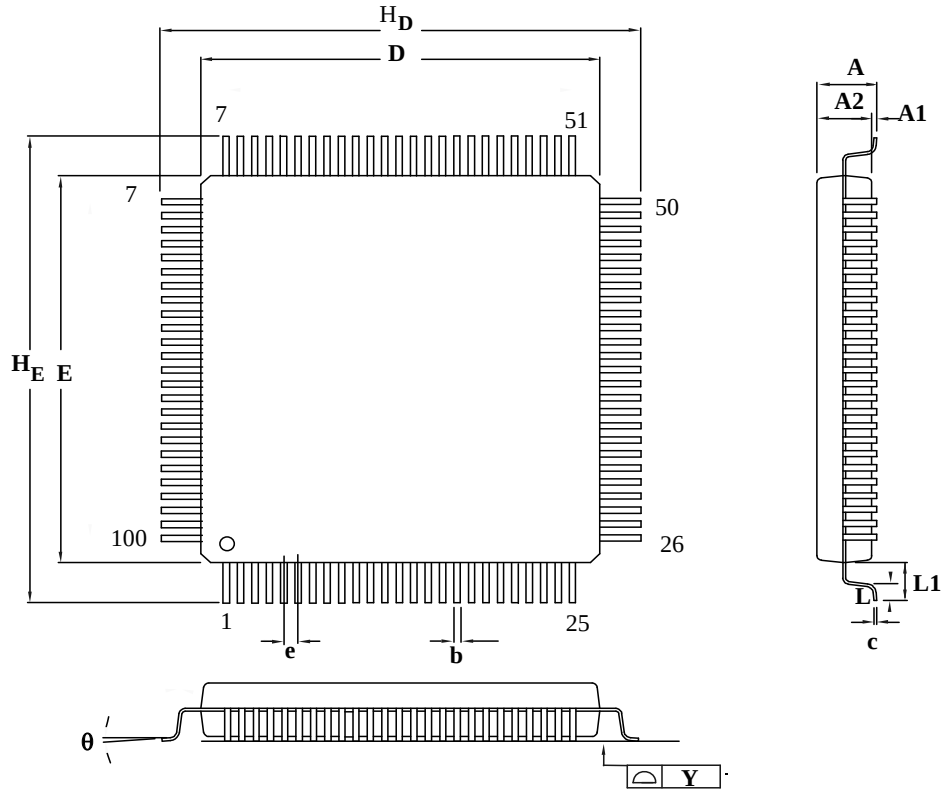
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{FR}	Rise Time	C_L=50p	4		20	ns
T_{FF}	Fall Time	C_L=50p	4		20	ns
T_{FRFF}	Rise and fall time matching	$T_{FRFF}=T_{FR}/T_{FF}$	90		111.11	%

4.4.8.3 USB Power Dissipation

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{VDDREG} (Full Speed)	VDDD and VDDREG Supply Current (Steady State)	Standby		50		uA
		Input mode				uA
		Output mode				uA

5 PACKAGE DIMENSIONS

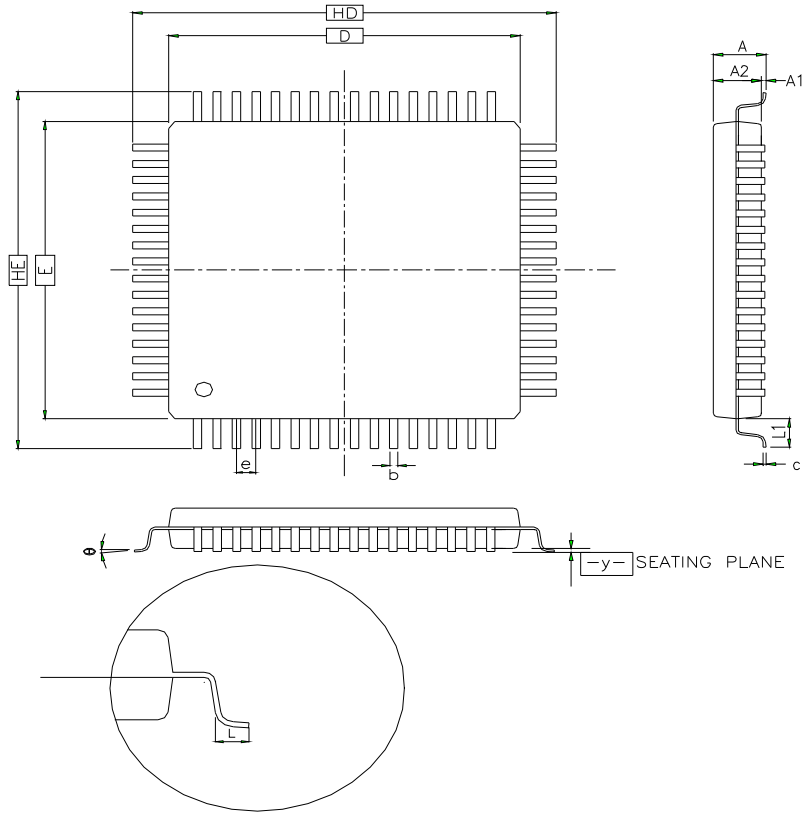
5.1 100L LQFP (14x14x1.4 mm footprint 2.0mm)



Controlling Dimension : Millimeters

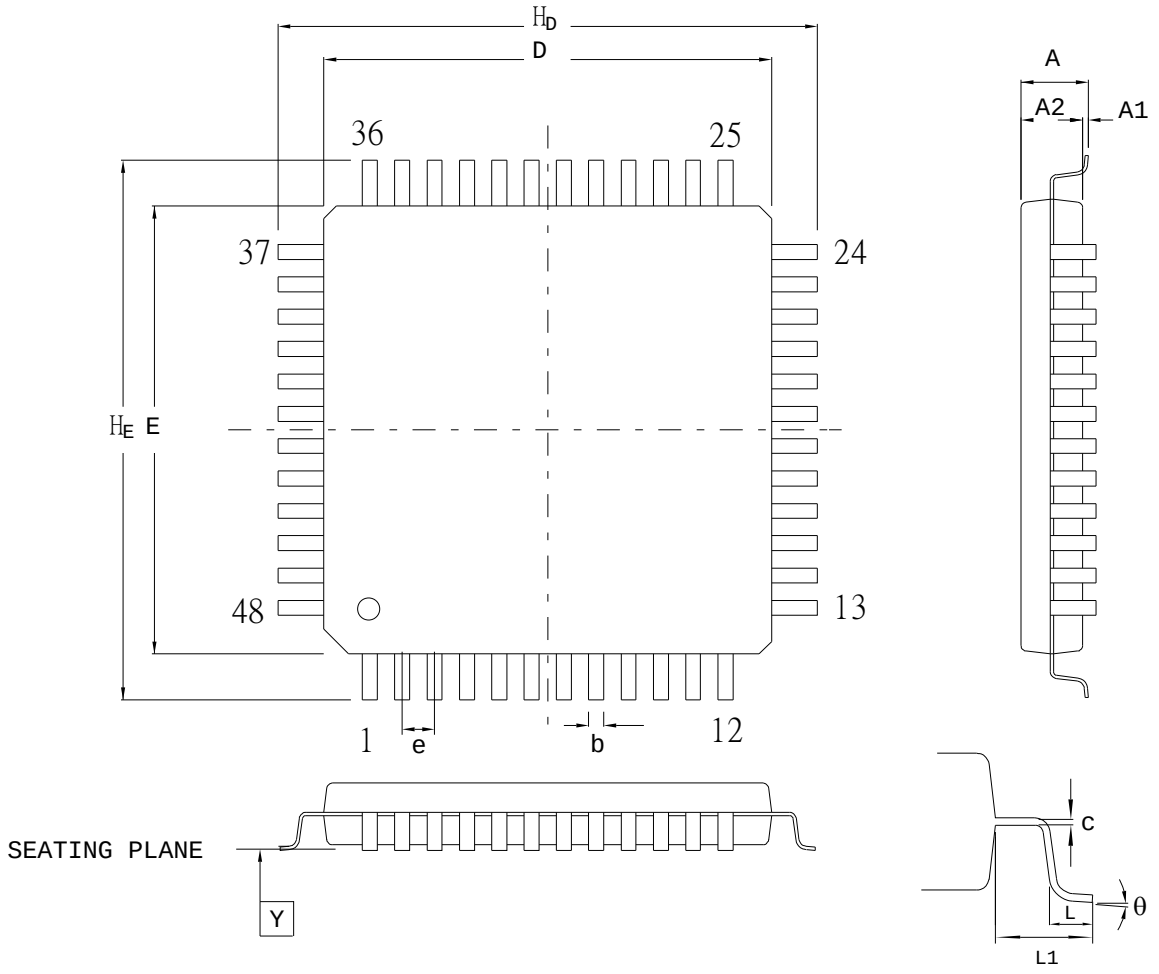
Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A1	0.002	—	—	0.05	—	—
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.556	13.90	14.00	14.10
E	0.547	0.551	0.556	13.90	14.00	14.10
e	—	0.020	—	—	0.50	—
HD	0.622	0.630	0.638	15.80	16.00	16.20
HE	0.622	0.630	0.638	15.80	16.00	16.20
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	—	0.039	—	—	1.00	—
y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

5.2 64L LQFP (10x10x1.4mm footprint 2.0 mm)



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.008	0.011	0.17	0.20	0.27
c	0.004	—	0.008	0.09	—	0.20
D	—	0.393	—	—	10.00	—
E	—	0.393	—	—	10.00	—
e	—	0.020	—	—	0.50	—
H_D	—	0.472	—	—	12.00	—
H_E	—	0.472	—	—	12.00	—
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
y	—	0.004	—	—	0.10	—
θ	0°	3.5°	7°	0°	3.5°	7°

5.3 48L LQFP (7x7x1.4mm footprint 2.0mm)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7 °	0°	—	7 °

6 REVISION HISTORY

VERSION	DATE	PAGE/ CHAP.	DESCRIPTION
V1.12	April 9, 2010	-	Initial issued
V1.13	May 31, 2010	4.2	Add operation current of DC characteristics
V1.14	Aug. 23, 2010	4.2	Modify operation current of DC characteristics
V2.00	Nov. 11, 2010	-	Update low density and selection table

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.