



ARM Cortex™ -M0
32-BIT MICROCONTROLLER

NuMicro Family
M058/M0516 Product Brief

TABLE OF CONTENTS

1	GENERAL DESCRIPTION	5
2	FEATURES	6
3	BLOCK DIAGRAM	10
4	SELECTION TABLE	11
5	PIN CONFIGURATION	12
5.1	QFN 33 pin	12
5.2	LQFP 48 pin	13
5.3	Pin Description	14
6	TYPICAL APPLICATION CIRCUIT	17
7	ELECTRICAL CHARACTERISTICS	18
7.1	Absolute Maximum Ratings	18
7.2	DC Electrical Characteristics	19
7.3	AC Electrical Characteristics	22
7.3.1	External Crystal	22
7.3.2	External Oscillator	22
7.3.3	Typical Crystal Application Circuits	22
7.3.4	Internal 22.1184 MHz RC Oscillator	23
7.3.5	Internal 10kHz RC Oscillator	23
7.4	Analog Characteristics	24
7.4.1	Specification of 600kHz sps 12-bit SARADC	24
7.4.2	Specification of LDO & Power management	24
7.4.3	Specification of Low Voltage Reset	25
7.4.4	Specification of Brownout Detector	25
7.4.5	Specification of Power-On Reset (5V)	26
7.5	SPI Dynamic characteristics	27
8	PACKAGE DIMENSIONS	29
8.1	LQFP-48 (7x7x1.4mm ² Footprint 2.0mm)	29
8.2	QFN-33 (5X5 mm ² , Thickness 0.8mm, Pitch 0.5 mm)	30
9	REVISION HISTORY	31

LIST OF FIGURES

Figure 3–1 NuMicro™ M051 Series Block Diagram	10
Figure 4–1 NuMicro™ Naming Rule	11
Figure 5–1 NuMicro™ M051 Series QFN33 Pin Diagram	12
Figure 5–2 NuMicro™ M051 Series LQFP-48 Pin Diagram	13
Figure 8–1 Typical Crystal Application Circuit	23
Figure 8–2 SPI Master timing	28
Figure 8–3 SPI Slave timing	28

LIST OF TABLES

Table 4–1 NuMicro™ M051 Series Product Selection Guide.....	11
Table 5–1 NuMicro™ M051 Series Pin Description	16

1 GENERAL DESCRIPTION

The NuMicro M051™ series is a 32-bit microcontroller with embedded ARM® Cortex™-M0 core for industrial control and applications which need rich communication interfaces. The Cortex™-M0 is the newest ARM embedded processor with 32-bit performance and at a cost equivalent to traditional 8-bit microcontroller. The NuMicro M051™ series includes M052, M054, M058 and M0516 families.

The M058/M0516 can run up to 50 MHz. Thus it can afford to support a variety of industrial control and applications which need high CPU performance. The M058/M0516 has 32K/64K-byte embedded flash, 4K-byte data flash, 4K-byte flash for the ISP, and 4K-byte embedded SRAM.

Many system level peripheral functions, such as I/O Port, EBI (External Bus Interface), Timer, UART, SPI, I2C, PWM, ADC, Watchdog Timer and Brownout Detector, have been incorporated into the M058/M0516 in order to reduce component count, board space and system cost. These useful functions make the M058/M0516 powerful for a wide range of applications.

Additionally, the M058/M0516 is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product.

2 FEATURES

- Core
 - ARM® Cortex™ -M0 core runs up to 50 MHz.
 - One 24-bit system timer.
 - Supports low power sleep-mode.
 - A single-cycle 32-bit hardware multiplier.
 - NVIC for the 32 interrupt inputs, each with 4-levels of priority.
 - Supports Serial Wire Debug (SWD) interface and 2 watchpoints/4 breakpoints.
- Built-in LDO for Wide Operating Voltage Range: 2.5V to 5.5V
- Memory
 - 32KB/64KB Flash memory for program memory (APROM)
 - 4KB Flash memory for data memory (DataFlash)
 - 4KB Flash memory for loader (LDROM)
 - 4KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
 - Programmable system clock source
 - 4~24 MHz external crystal input
 - 22.1184 MHz internal oscillator (trimmed to 1% accuracy)
 - 10 kHz low-power oscillator for Watchdog Timer and wake-up in sleep mode
 - PLL allows CPU operation up to the maximum 50MHz
- I/O Port
 - Up to 40 general-purpose I/O (GPIO) pins for LQFP-48 package
 - Four I/O modes:
 - ◆ Quasi bi-direction

- ◆ Push-Pull output
- ◆ Open-Drain output
- ◆ Input only with high impedance
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports high driver and high sink IO mode
- Timer
 - Provides four channel 32-bit timers, one 8-bit pre-scale counter with 24-bit up-timer for each timer.
 - Independent clock source for each timer.
 - 24-bit timer value is readable through TDR (Timer Data Register)
 - Provides one-shot, periodic and toggle operation modes.
- Watchdog Timer
 - Multiple clock sources
 - Supports wake up from power down or sleep mode
 - Interrupt or reset selectable on watchdog time-out
- PWM
 - Built-in up to four 16-bit PWM generators; providing eight PWM outputs or four complementary paired PWM outputs
 - Individual clock source, clock divider, 8-bit pre-scalar and dead-zone generator for each PWM generator
 - PWM interrupt synchronized to PWM period
 - 16-bit digital Capture timers (shared with PWM timers) with rising/falling capture inputs
 - Supports capture interrupt
- UART
 - Up to two sets of UART device

- Programmable baud-rate generator
- Buffered receiver and transmitter, each with 15 bytes FIFO
- Optional flow control function (CTS and RTS)
- Supports IrDA(SIR) function
- Supports RS485 function
- SPI
 - Up to two sets of SPI device.
 - Supports master/slave mode
 - Master mode clock rate up to 20 MHz, and slave mode clock rate up to 10 MHz
 - Full duplex synchronous serial data transfer
 - Variable length of transfer data from 1 to 32 bits
 - MSB or LSB first data transfer
 - Rx latching data can be either at rising edge or at falling edge of serial clock
 - Tx sending data can be either at rising edge or at falling edge of serial clock
 - Supports Byte suspend mode in 32-bit transmission
- I2C
 - Supports master/slave mode
 - Bidirectional data transfer between masters and slaves
 - Multi-master bus (no central master).
 - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
 - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
 - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
 - Programmable clocks allow versatile rate control.

- Supports multiple address recognition (four slave address with mask option)
- ADC
 - 12-bit SAR ADC with 600k SPS
 - Up to 8-ch single-ended input or 4-ch differential input
 - Supports single mode/burst mode/single-cycle scan mode/continuous scan mode
 - Each channel with an individual result register
 - Supports conversion value monitoring (or comparison) for threshold voltage detection
 - Conversion can be started either by software trigger or external pin trigger
- EBI (External Bus Interface) for external memory-mapped device access
 - Accessible space: 64KB in 8-bit mode or 128KB in 16-bit mode
 - Supports 8-bit/16-bit data width
- In-System Programming (ISP) and In-Circuit Programming (ICP)
- Brownout Detector
 - With 4 levels: 4.5V/3.8V/2.7V/2.2V
 - Supports brownout interrupt and reset option
- LVR (Low Voltage Reset)
 - Threshold voltage levels: 2.0V
- Operating Temperature: -40°C~85°C
- Packages:
 - Green package (RoHS)
 - 48-pin LQFP, 33-pin QFN

3 BLOCK DIAGRAM

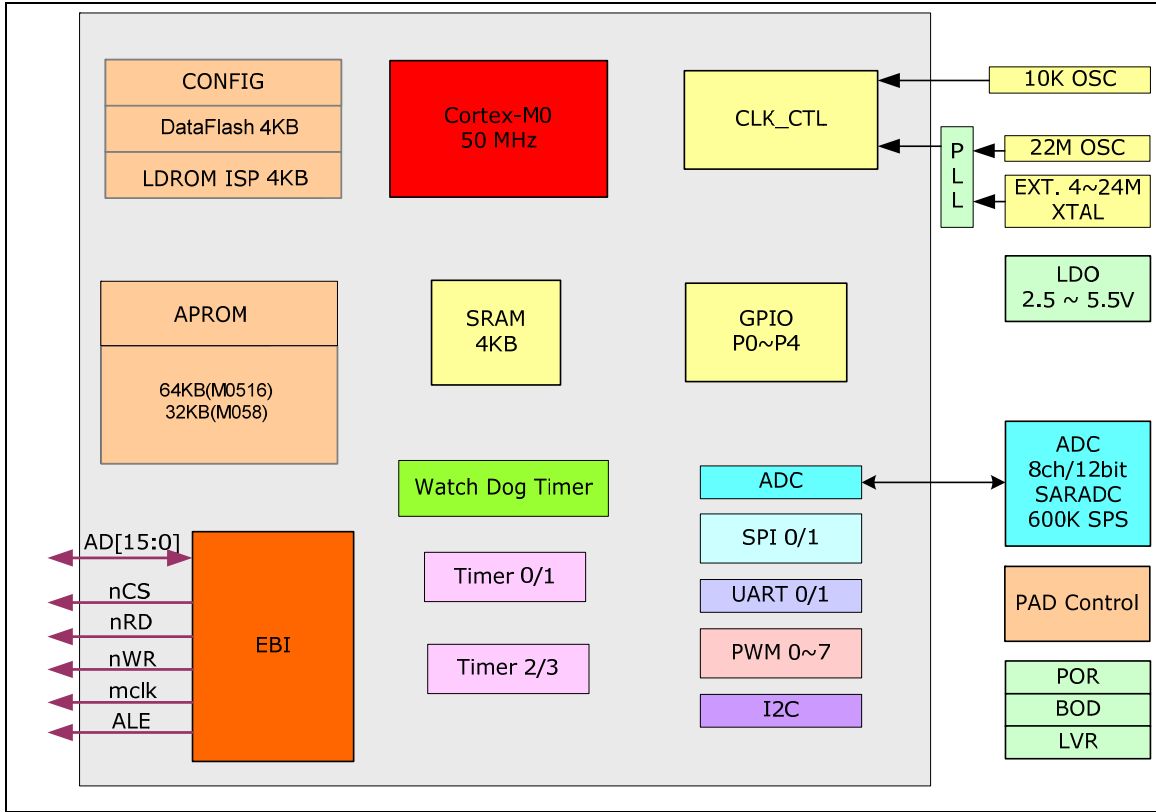


Figure 3–1 NuMicro™ M051 Series Block Diagram

4 SELECTION TABLE

M058/M0516 Selection Guide

Part No.	APROM	RAM	Data Flash	LDROM	I/O	Timer	Connectivity			PWM	ADC	EBI	ISP ICP	Package
							UART	SPI	I2C					
M058LAN	32KB	4KB	4KB	4KB	40	4x32-bit	2	2	1	8	8x12-bit	v	v	LQFP48
M058ZAN	32KB	4KB	4KB	4KB	24	4x32-bit	2	1	1	5	5x12-bit		v	QFN 33
M0516LAN	64KB	4KB	4KB	4KB	40	4x32-bit	2	2	1	8	8x12-bit	v	v	LQFP48
M0516ZAN	64KB	4KB	4KB	4KB	24	4x32-bit	2	1	1	5	5x12-bit		v	QFN 33

Table 4–1 NuMicro™ M051 Series Product Selection Guide

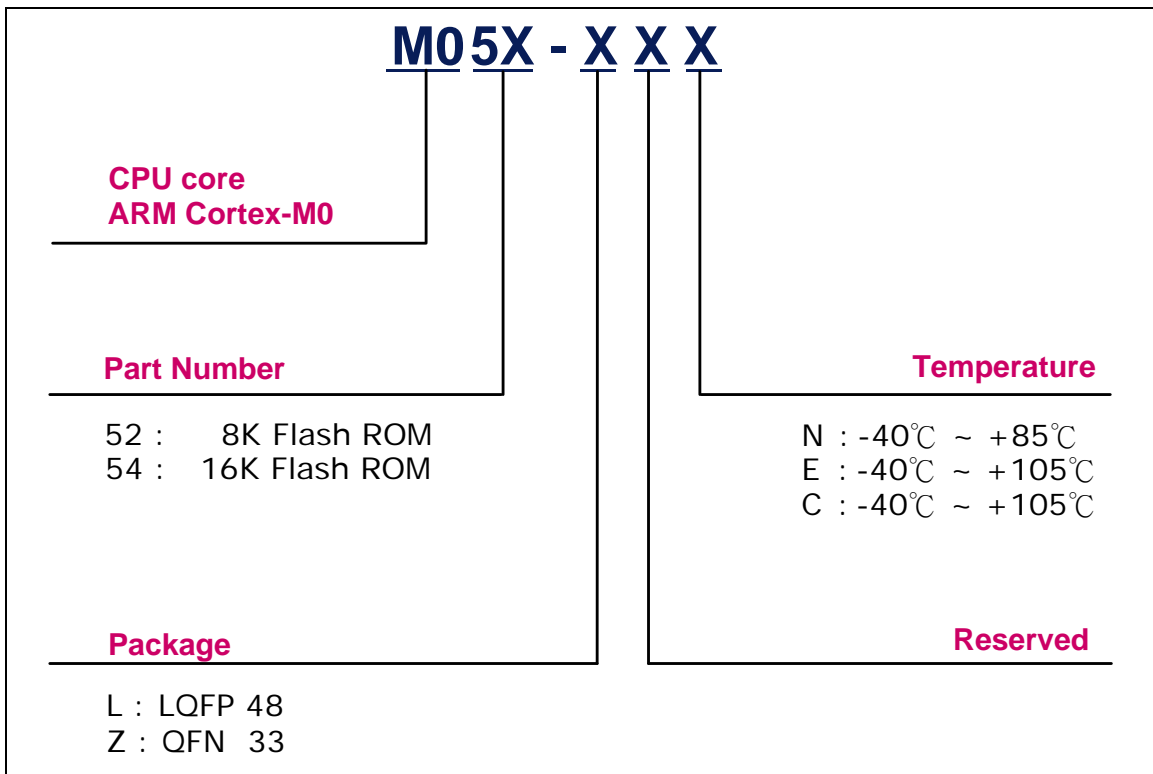


Figure 4–1 NuMicro M051™ Naming Rule

5 PIN CONFIGURATION

5.1 QFN 33 pin

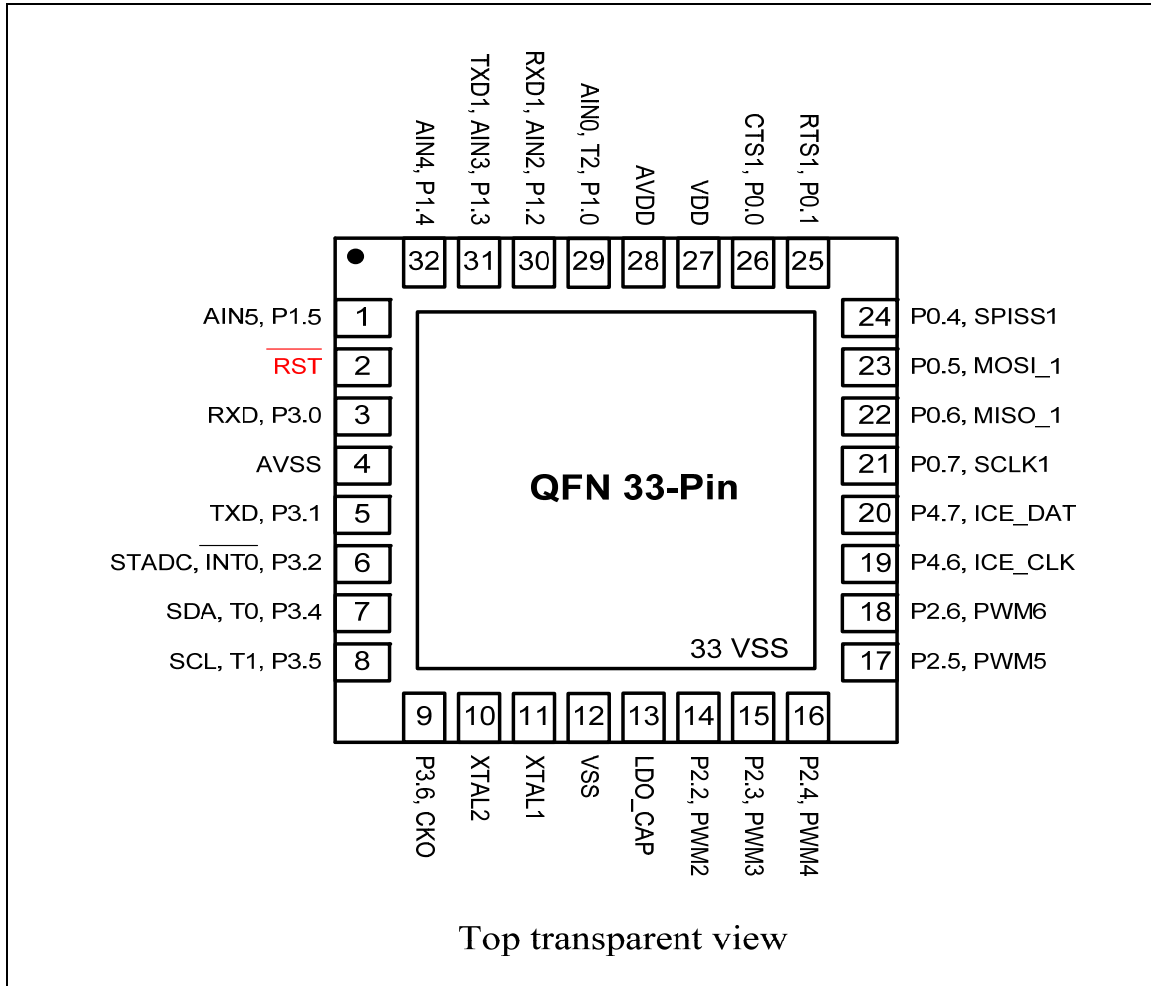


Figure 5–1 NuMicro™ M051 Series QFN33 Pin Diagram

5.2 LQFP 48 pin

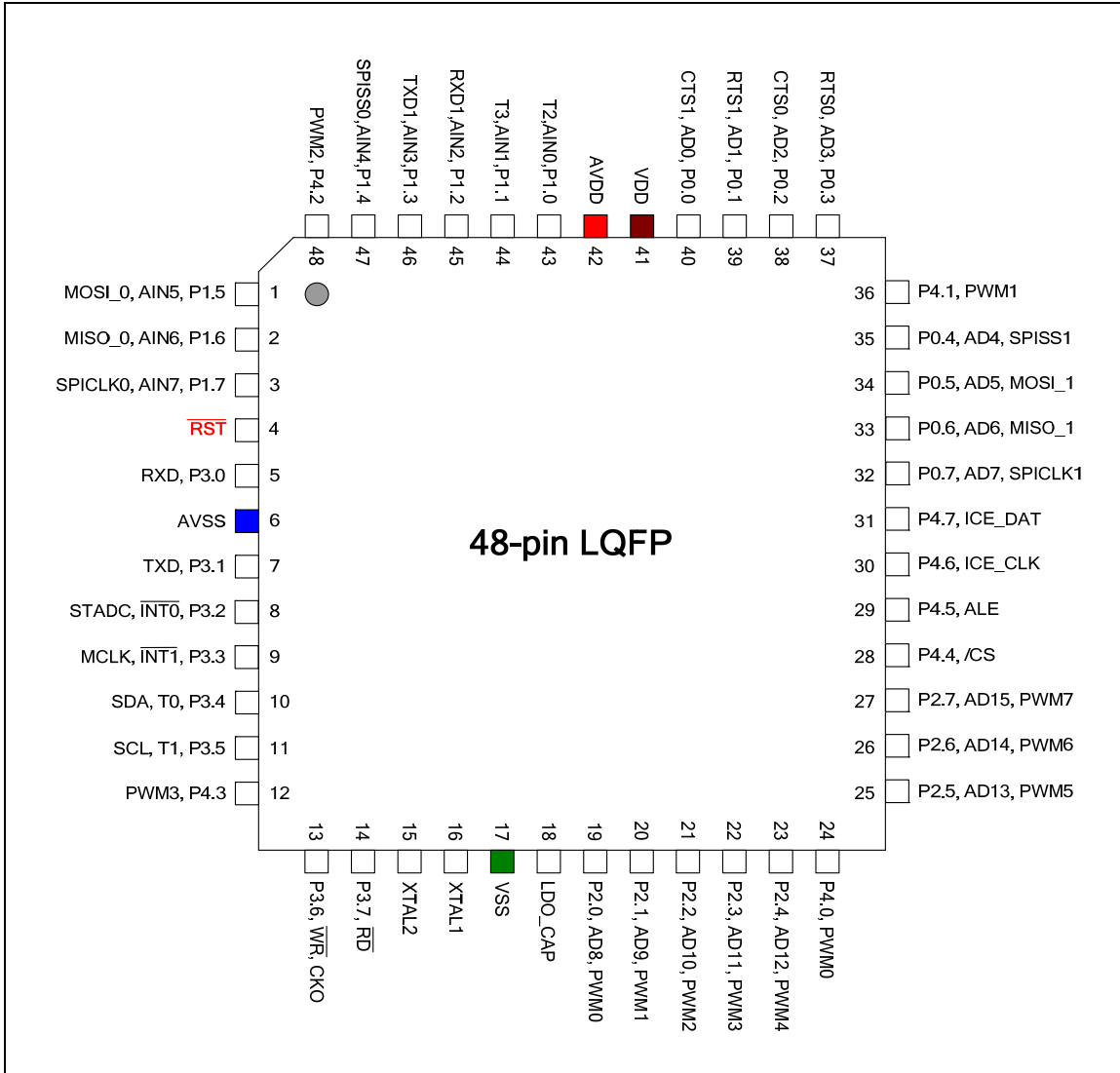


Figure 5–2 NuMicro™ M051 Series LQFP-48 Pin Diagram

5.3 Pin Description

Pin number		Symbol	Alternate Function		Type ^[1]	Description
QFN33	LQFP48		1	2		
11	16	XTAL1			I (ST)	CRYSTAL1: This is the input pin to the internal inverting amplifier. The system clock is from external crystal or resonator when FOSC[1:0] (CONFIG3[1:0]) are both logic 1 by default.
10	15	XTAL2			O	CRYSTAL2: This is the output pin from the internal inverting amplifier. It emits the inverted signal of XTAL1.
27	41	VDD			P	POWER SUPPLY: Supply voltage Digital V _{DD} for operation.
12	17	VSS			P	GROUND: Digital Ground potential.
33						
28	42	AVDD			P	POWER SUPPLY: Supply voltage Analog AV _{DD} for operation.
4	6	AVSS			P	GROUND: Analog Ground potential.
13	18	LDO_C AP			P	LDO: LDO output pin Note: It needs to be connected with a 10uF capacitor.
2	4	/RST			I (ST)	RESET: /RST pin is a Schmitt trigger input pin for hardware device reset. A "Low" on this pin for 768 clock counter of Internal RC 22.1184 MHz while the system clock is running will reset the device. /RST pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
26	40	P0.0	CTS1	AD0	D, I/O	PORT0: Port 0 is an 8-bit four mode output pin and two mode input. Its multifunction pins are for CTS1, RTS1, CTS0, RTS0, SPISS1, MOSI_1, MISO_1, and SPICLK1. P0 has an alternative function as AD[7:0] while external memory interface (EBI) is enabled. These pins which are SPISS1, MOSI_1, MISO_1, and SPICLK1 for the SPI function used. CTS0/1: Clear to Send input pin for UART0/1
25	39	P0.1	RTS1	AD1	D, I/O	
NC	38	P0.2	CTS0	AD2	D, I/O	
NC	37	P0.3	RTS0	AD3	D, I/O	
24	35	P0.4	SPISS1	AD4	D, I/O	

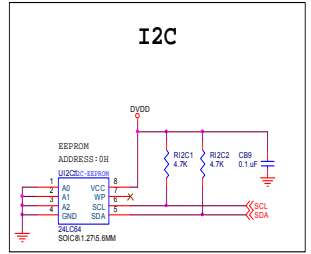
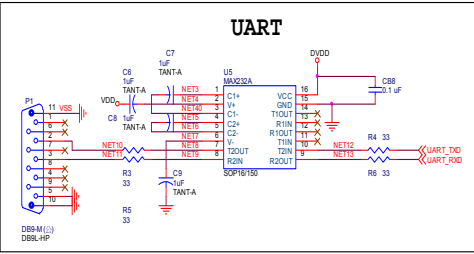
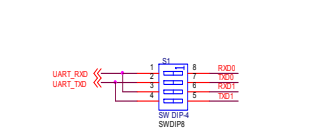
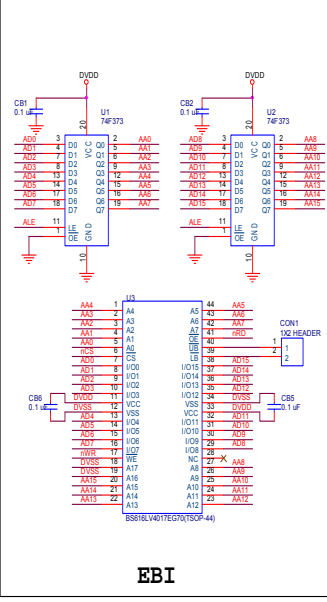
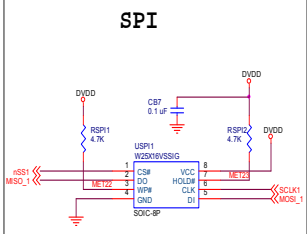
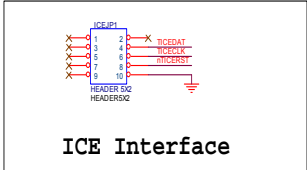
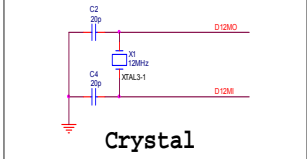
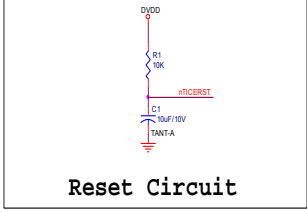
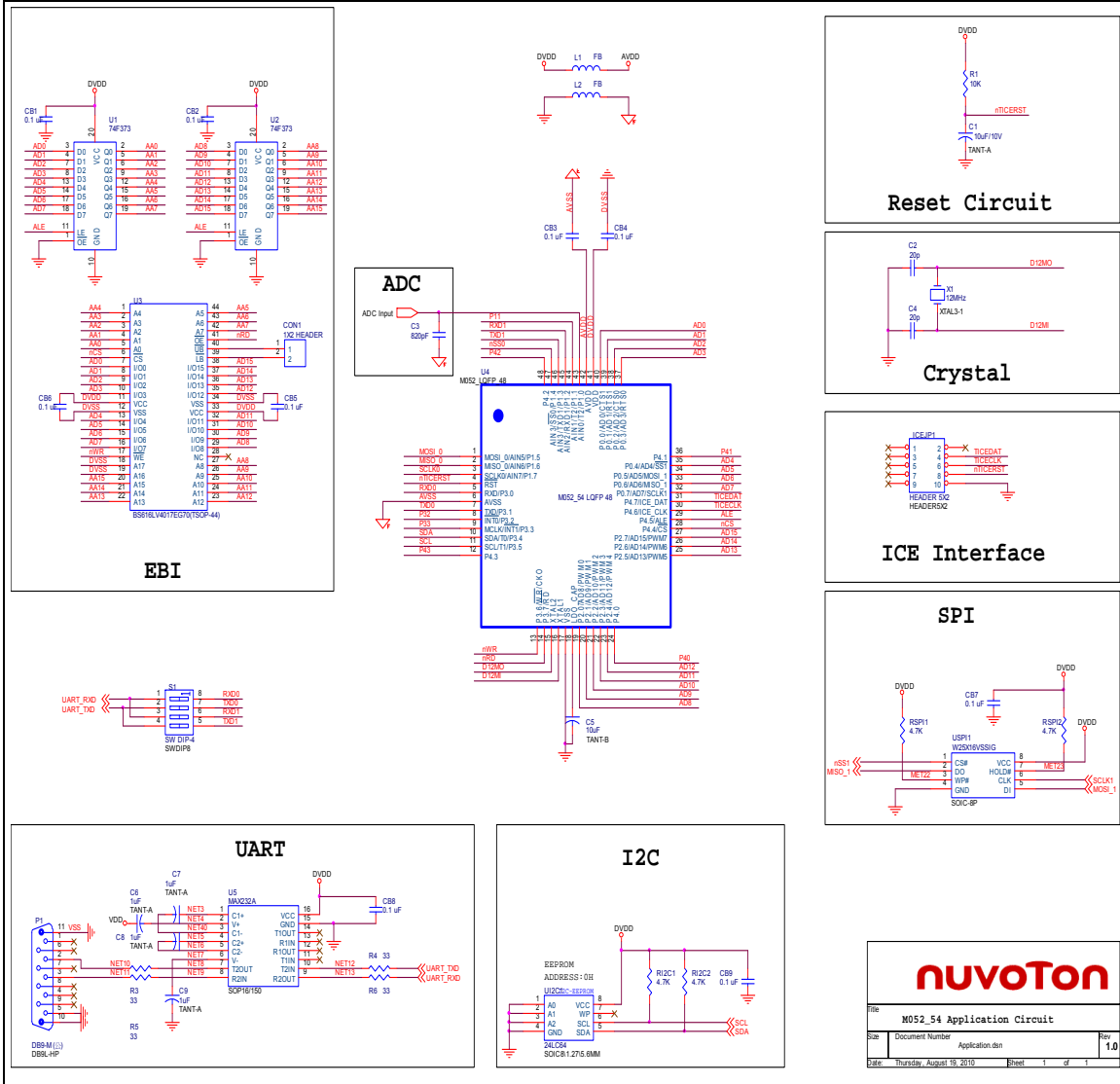
Pin number		Symbol	Alternate Function		Type ^[1]	Description
QFN33	LQFP48		1	2		
23	34	P0.5	MOSI_1	AD5	D, I/O	RTS0/1: Request to Send output pin for UART0/1
22	33	P0.6	MISO_1	AD6	D, I/O	
21	32	P0.7	SPICLK1	AD7	D, I/O	
29	43	P1.0	T2	AIN0	I/O	<p>PORT1: Port 1 is an 8-bit four mode output pin and two mode input. Its multifunction pins are for T2, T3, RXD1, TXD1, SPISS0, MOSI_0, MISO_0, and SPICLK0.</p> <p>T2: Timer2 external input</p> <p>T3: Timer3 external input</p> <p>These pins which are SPISS0, MOSI_0, MISO_0, and SPICLK0 for the SPI function used.</p> <p>These pins which are AIN0~AIN7 for the 12 bits ADC function used.</p> <p>The RXD1/TXD1 pins are for UART1 function used.</p>
NC	44	P1.1	T3	AIN1	I/O	
30	45	P1.2	RXD1	AIN2	I/O	
31	46	P1.3	TXD1	AIN3	I/O	
32	47	P1.4	SPISS0	AIN4	I/O	
1	1	P1.5	MOSI_0	AIN5	I/O	
NC	2	P1.6	MISO_0	AIN6	I/O	
NC	3	P1.7	SPICLK0	AIN7	I/O	
NC	19	P2.0	PWM0	AD8	D, I/O	<p>PORT2: Port 2 is an 8-bit four mode output pin and two mode input. It has an alternative function</p> <p>P2 has an alternative function as AD[15:8] while external memory interface (EBI) is enabled.</p> <p>These pins which are PWM0~PWM7 for the PWM function.</p>
NC	20	P2.1	PWM1	AD9	D, I/O	
14	21	P2.2	PWM2	AD10	D, I/O	
15	22	P2.3	PWM3	AD11	D, I/O	
16	23	P2.4	PWM4	AD12	D, I/O	
17	25	P2.5	PWM5	AD13	D, I/O	
18	26	P2.6	PWM6	AD14	D, I/O	
NC	27	P2.7	PWM7	AD15	D, I/O	
3	5	P3.0	RXD		I/O	<p>PORT3: Port 3 is an 8-bit four mode output pin and two mode input. Its multifunction pins are for RXD, TXD, INT0 ,</p>
5	7	P3.1	TXD		I/O	

Pin number		Symbol	Alternate Function		Type ^[1]	Description
QFN33	LQFP48		1	2		
6	8	P3.2	$\overline{\text{INT0}}$	STADC	I/O	$\overline{\text{INT1}}$, T0, T1, $\overline{\text{WR}}$, and $\overline{\text{RD}}$. T0: Timer0 external input
NC	9	P3.3	$\overline{\text{INT1}}$	MCLK	I/O	T1: Timer1 external input
7	10	P3.4	T0	SDA	I/O	The RXD/TXD pins are for UART0 function used. The SDA/SCL pins are for I2C function used.
8	11	P3.5	T1	SCL	I/O	MCLK: EBI clock output pin. CKO: HCLK clock output
9	13	P3.6	$\overline{\text{WR}}$	CKO	I/O	The STADC pin is for ADC external trigger input.
NC	14	P3.7	$\overline{\text{RD}}$		I/O	
NC	24	P4.0	PWM0		I/O	PORT4: Port 4 is an 8-bit four mode output pin and two mode input. Its multifunction pins are for /CS, ALE, ICE_CLK and ICE_DAT. /CS for EBI (External Bus Interface) used. ALE (Address Latch Enable) is used to enable the address latch that separates the address from the data on Port 0 and Port 2. The ICE_CLK/ICE_DAT pins are for JTAG-ICE function used. PWM0-3 can be used from P4.0-P4.3 when EBI is active.
NC	36	P4.1	PWM1		I/O	
NC	48	P4.2	PWM2		I/O	
NC	12	P4.3	PWM3		I/O	
NC	28	P4.4	/CS		I/O	
NC	29	P4.5	ALE		I/O	
19	30	P4.6	ICE_CLK		I/O	
20	31	P4.7	ICE_DAT		I/O	

Table 5–1 NuMicro™ M051 Series Pin Description

[1] I/O type description. I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pins, ST: Schmitt trigger.

6 TYPICAL APPLICATION CIRCUIT



M052_54 Application Circuit			
Size	Document Number	Application.dsn	Rev 1.0
Date	Thursday, August 18, 2010	Sheet 1 of 1	

7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	VDD-VSS	-0.3	+7.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Oscillator Frequency	1/t _{CLCL}	0	40	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into V _{DD}		-	120	mA
Maximum Current out of V _{SS}			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affect the life and reliability of the device.

7.2 DC Electrical Characteristics

(V_{DD}-V_{SS}=2.5~5.5V, T_A = 25°C, F_{OSC} = 50 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V _{DD}	2.5		5.5	V	V _{DD} =2.5V ~ 5.5V up to 50 MHz
Power Ground	V _{SS} AV _{SS}	-0.3			V	
LDO Output Voltage	V _{LDO}	-10%	2.45	+10%	V	V _{DD} > 2.7V
Band Gap Analog Input	V _{BG}	-5%	1.26	+5%	V	V _{DD} =2.5V ~ 5.5V
Analog Operating Voltage	AV _{DD}	0		V _{DD}	V	
Operating Current Normal Run Mode @ 50 MHz	I _{DD1}		32		mA	V _{DD} = 5.5V@50 MHz, enable all IP and PLL, XTAL=12 MHz
	I _{DD2}		24		mA	V _{DD} =5.5V@50 MHz, disable all IP and enable PLL, XTAL=12 MHz
	I _{DD3}		31		mA	V _{DD} = 3V@50 MHz, enable all IP and PLL, XTAL=12 MHz
	I _{DD4}		23		mA	V _{DD} = 3V@50 MHz, disable all IP and enable PLL, XTAL=12 MHz
Operating Current Normal Run Mode @ 12 MHz	I _{DD5}		17		mA	V _{DD} = 5.5V@ 12MHz, enable all IP and disable PLL, XTAL=12 MHz
	I _{DD6}		14		mA	V _{DD} = 5.5V@12 MHz, disable all IP and disable PLL, XTAL=12 MHz
	I _{DD7}		16		mA	V _{DD} = 3V@12 MHz, enable all IP and disable PLL, XTAL=12 MHz
	I _{DD8}		13		mA	V _{DD} = 3V@12 MHz, disable all IP and disable PLL, XTAL=12 MHz
Operating Current Normal Run Mode @ 4 MHz	I _{DD9}		12		mA	V _{DD} = 5.5V@4 MHz, enable all IP and disable PLL, XTAL=4MHz
	I _{DD10}		10		mA	V _{DD} = 5.5V@4 MHz, disable all IP and disable PLL, XTAL=4MHz
	I _{DD11}		10		mA	V _{DD} = 3V@4 MHz, enable all IP and disable PLL, XTAL=4MHz
	I _{DD12}		9		mA	V _{DD} = 3V@4 MHz, disable all IP and disable PLL, XTAL=4 MHz
Operating Current	I _{IDLE1}		19		mA	V _{DD} = 5.5V@50 MHz, enable all IP and PLL, XTAL=12 MHz

Idle Mode @ 50 MHz	I_{IDLE2}		11		mA	$V_{DD}=5.5V@50$ MHz, disable all IP and enable PLL, XTAL=12 MHz
	I_{IDLE3}		18		mA	$V_{DD} = 3V@50$ MHz, enable all IP and PLL, XTAL=12 MHz
	I_{IDLE4}		10		mA	$V_{DD} = 3V@50$ MHz, disable all IP and enable PLL, XTAL=12 MHz
Operating Current Idle Mode @ 12 MHz	I_{IDLE5}		10		mA	$V_{DD} = 5.5V@12$ MHz, enable all IP and disable PLL, XTAL=12 MHz
	I_{IDLE6}		7		mA	$V_{DD} = 5.5V@12$ MHz, disable all IP and disable PLL, XTAL=12 MHz
	I_{IDLE7}		9		mA	$V_{DD} = 3V@12$ MHz, enable all IP and disable PLL, XTAL=12 MHz
	I_{IDLE8}		6		mA	$V_{DD} = 3V@12$ MHz, disable all IP and disable PLL, XTAL=12 MHz
Operating Current Idle Mode @ 4 MHz	I_{IDLE9}		5		mA	$V_{DD} = 5.5V@4$ MHz, enable all IP and disable PLL, XTAL=4 MHz
	I_{IDLE10}		4		mA	$V_{DD} = 5.5V@4$ MHz, disable all IP and disable PLL, XTAL=4 MHz
	I_{IDLE11}		4		mA	$V_{DD} = 3V@4$ MHz, enable all IP and disable PLL, XTAL=4 MHz
	I_{IDLE12}		3		mA	$V_{DD} = 3V@4$ MHz, disable all IP and disable PLL, XTAL=4 MHz
Standby Current Power-down Mode (Deep Sleep Mode)	I_{PWD1}		15		μA	$V_{DD} = 5.5V$, No load @ Disable BOV function
	I_{PWD2}		11		μA	$V_{DD} = 3.0V$, No load @ Disable BOV function
Input Current P0/1/2/3/4 (Quasi-bidirectional mode)	I_{IN1}		-50	-60	μA	$V_{DD} = 5.5V$, $V_{IN} = 0.4V$
Input Leakage Current P0/1/2/3/4	I_{LK}	-2	-	+2	μA	$V_{DD} = 5.5V$, $0 < V_{IN} < V_{DD}$
Logic 1 to 0 Transition Current P0/1/2/3/4 (Quasi-bidirectional mode)	$I_{TL}^{[3]}$	-650	-	-200	μA	$V_{DD} = 5.5V$, $V_{IN} < 2.0V$
Input Low Voltage P0/1/2/3/4 (TTL input)	V_{IL1}	-0.3	-	0.8	V	$V_{DD} = 4.5V$
		-0.3	-	0.6		$V_{DD} = 2.5V$
Input High Voltage P0/1/2/3/4 (TTL input)	V_{IH1}	2.0	-	$V_{DD} + 0.2$	V	$V_{DD} = 5.5V$
		1.5	-	$V_{DD} + 0.2$		$V_{DD} = 3.0V$
Input Low Voltage XT1 ^[2]	V_{IL3}	0	-	0.8	V	$V_{DD} = 4.5V$
		0	-	0.4		$V_{DD} = 3.0V$
Input High Voltage XT1 ^[2]	V_{IH3}	3.5	-	$V_{DD} + 0.2$	V	$V_{DD} = 5.5V$
		2.4	-	$V_{DD} + 0.2$		$V_{DD} = 3.0V$
Negative going threshold (Schmitt input), /RST	V_{ILS}	-0.5	-	$0.3V_{DD}$	V	

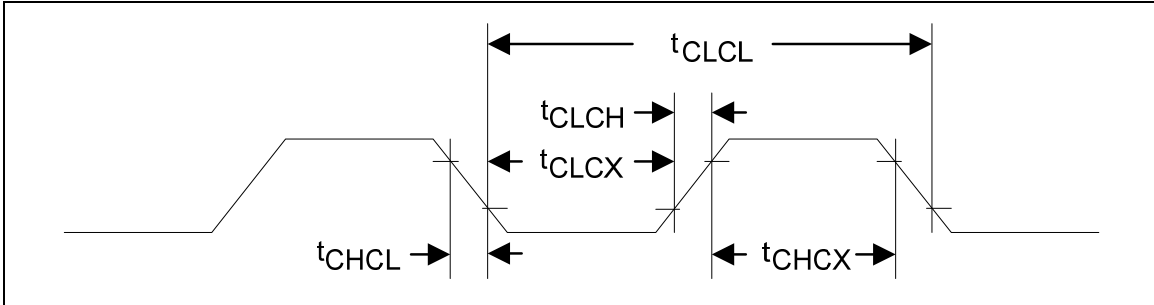
Positive going threshold (Schmitt input), /RST	V_{IHS}	$0.7V_{DD}$	-	$V_{DD}+0.5$	V	
Internal /RST pin pull up resistor	R_{RST}	40		150	K Ω	
Negative going threshold (Schmitt input), P0/1/2/3/4	V_{ILS}	-0.5	-	$0.2V_{DD}$	V	
Positive going threshold (Schmitt input), P0/1/2/3/4	V_{IHS}	$0.4V_{DD}$	-	$V_{DD}+0.5$	V	
Source Current P0/1/2/3/4 (Quasi-bidirectional Mode)	I_{SR11}	-300	-370	-450	μA	$V_{DD} = 4.5V, V_S = 2.4V$
	I_{SR12}	-50	-70	-90	μA	$V_{DD} = 2.7V, V_S = 2.2V$
	I_{SR12}	-40	-60	-80	μA	$V_{DD} = 2.5V, V_S = 2.0V$
Source Current P0/1/2/3/4 (Push-pull Mode)	I_{SR21}	-20	-24	-28	mA	$V_{DD} = 4.5V, V_S = 2.4V$
	I_{SR22}	-4	-6	-8	mA	$V_{DD} = 2.7V, V_S = 2.2V$
	I_{SR22}	-3	-5	-7	mA	$V_{DD} = 2.5V, V_S = 2.0V$
Sink Current P0/1/2/3/4 (Quasi-bidirectional and Push-pull Mode)	I_{SK1}	10	16	20	mA	$V_{DD} = 4.5V, V_S = 0.45V$
	I_{SK1}	7	10	13	mA	$V_{DD} = 2.7V, V_S = 0.45V$
	I_{SK1}	6	9	12	mA	$V_{DD} = 2.5V, V_S = 0.45V$
Brownout voltage with BOV_VL [1:0] =00b	$V_{BO2.2}$	2.1	2.2	2.3	V	
Brownout voltage with BOV_VL [1:0] =01b	$V_{BO2.7}$	2.6	2.7	2.8	V	
Brownout voltage with BOV_VL [1:0] =10b	$V_{BO3.8}$	3.7	3.8	3.9	V	
Brownout voltage with BOV_VL [1:0] =11b	$V_{BO4.5}$	4.4	4.5	4.6	V	
Hysteresis range of BOD voltage	V_{BH}	30	-	150	mV	$V_{DD} = 2.5V\sim 5.5V$

Notes:

1. /RST pin is a Schmitt trigger input.
2. XTAL1 is a CMOS input.
3. Pins of P0, P1, P2, P3 and P4 can source a transition current when they are being externally driven from 1 to 0. In the condition of $V_{DD}=5.5V$, the transition current reaches its maximum value when V_{in} approximates to 2V.

7.3 AC Electrical Characteristics

7.3.1 External Crystal



Note: Duty cycle is 50%.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITION
Clock High Time	t_{CHCX}	20	-	125	nS	
Clock Low Time	t_{CLCX}	20	-	125	nS	
Clock Rise Time	t_{CLCH}	-	-	10	nS	
Clock Fall Time	t_{CHCL}	-	-	10	nS	

7.3.2 External Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	4	12	24	MHz
Temperature	-	-40	-	85	°C
V_{DD}	-	2.5	5	5.5	V
Operating current	12 MHz@ $V_{DD} = 5V$	-	5	-	mA

7.3.3 Typical Crystal Application Circuits

CRYSTAL	C1	C2
4 MHz ~ 24 MHz	Optional (Depend on crystal specification)	

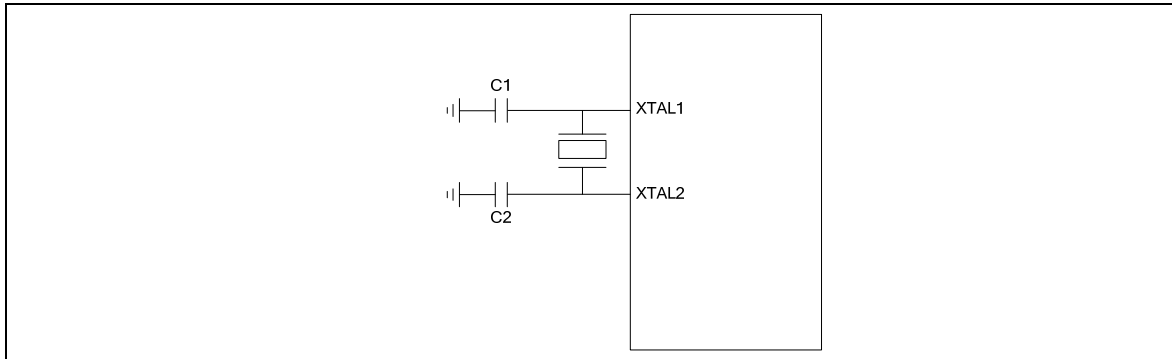


Figure 7-1 Typical Crystal Application Circuit

7.3.4 Internal 22.1184 MHz RC Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage ^[1]	-	2.5	-	5.5	V
Center Frequency	-	-	22.1184	-	MHz
Calibrated Internal Oscillator Frequency	+25 C; V _{DD} =5V	-1	-	+1	%
	-40 C~+85 C; V _{DD} =2.5V~5.5V	-3	-	+3	%
Accuracy of Un-calibrated Internal Oscillator Frequency	-40 C~+85 C; V _{DD} =2.5V~5.5V	-25	-	+25	%
Operating current	V _{DD} =5V	-	500	-	uA

7.3.5 Internal 10kHz RC Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage ^[1]	-	2.5	-	5.5	V
Center Frequency	-	-	10	-	kHz
Calibrated Internal Oscillator Frequency	+25 C; V _{DD} =5V	-30	-	+30	%
	-40 C~+85 C; V _{DD} =2.5V~5.5V	-50	-	+50	%
Operating current	V _{DD} =5V	-	5	-	uA

Notes:

1. Internal operation voltage comes from LDO.

7.4 Analog Characteristics

7.4.1 Specification of 600kHz sps 12-bit SARADC

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
Resolution	-	-	-	12	Bit
Differential nonlinearity error	DNL	-	±1.2	-	LSB
Integral nonlinearity error	INL	-	±1.5	-	LSB
Offset error	EO	-	+4	10	LSB
Gain error (Transfer gain)	EG	-	+7	1.005	-
Monotonic	-	Guaranteed			-
ADC clock frequency	FADC	-	-	20	MHz
Calibration time	TCAL	-	127	-	Clock
Sample time	TS	-	7	-	Clock
Conversion time	TADC	-	13	-	Clock
Sample rate	FS	-	-	600	k sps
Supply voltage	V _{LDO}	-	2.5	-	V
	V _{ADD}	3	-	5.5	V
Supply current (Avg.)	IDD	-	0.5	-	mA
	IDDA	-	1.5	-	mA
Input voltage range	V _{IN}	0	-	AVDD	V
Capacitance	C _{IN}	-	5	-	pF

7.4.2 Specification of LDO & Power management

PARAMETER	MIN	TYP	MAX	UNIT	NOTE
Input Voltage	2.7	5	5.5	V	V _{DD} input voltage
Output Voltage (bypass=0)	-10%	2.45	+10%	V	LDO output voltage
Output Voltage (bypass=1)	-10%	Input Voltage	+10%	V	Input Voltage < 2.7V
Quiescent Current	-	100	-	uA	

Publication Release Date: Mar 08, 2011
Revision V1.1

(PD=0, bypass=0)					
Quiescent Current (PD=1, bypass=0)	-	5	-	uA	
Quiescent Current (PD=1, bypass=1)	-	5	-	uA	
Iload (PD=0)	-	-	100	mA	
Iload (PD=1)	-	-	100	uA	
Cbp	-	1u	-	F	Resr=1ohm
Cload	-	250p	-	F	

Note:

1. It is recommended that a 10uF or higher capacitor and a 100nF bypass capacitor are connected between VDD and the closest VSS pin of the device.

7.4.3 Specification of Low Voltage Reset

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	1.7	-	5.5	V
Quiescent current	VDD5V=5.5V	-	-	5	uA
Threshold voltage	Temperature=25°	1.7	2.0	2.3	V
	Temperature=-40°	-	2.4	-	V
	Temperature=85°	-	1.6	-	V
Hysteresis	-	0	0	0	V

7.4.4 Specification of Brownout Detector

Parameter	Condition	Min.	Typ.	Max.	Unit
Operation voltage	-	2.5	-	5.5	V
Quiescent current	AVDD=5.5V	-	-	125	μA
Temperature	-	-40	25	85	°C
Brownout voltage	BOV_VL[1:0]=11	4.4	4.5	4.6	V

Publication Release Date: Mar 08, 2011
Revision V1.1

	BOV_VL [1:0]=10	3.7	3.8	3.9	V
	BOV_VL [1:0]=01	2.6	2.7	2.8	V
	BOV_VL [1:0]=00	2.1	2.2	2.3	V
Hysteresis	-	30m	-	150m	V

7.4.5 Specification of Power-On Reset (5V)

Parameter	Condition	Min.	Typ.	Max.	Unit
Reset voltage	V+	-	2	-	V
Quiescent current	Vin>reset voltage	-	1	-	nA

7.5 SPI Dynamic characteristics

Symbol	Parameter	Min	Typ	Max	Unit
SPI master mode (VDD = 4.5V ~ 5.5V, 30pF loading Capacitor)					
t_{DS}	Data setup time	26	-	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	-	6	ns
SPI master mode (VDD = 3.0V ~ 3.6V, 30pF loading Capacitor)					
t_{DS}	Data setup time	39	-	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	-	10	ns
SPI slave mode (VDD = 4.5V ~ 5.5V, 30pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	$2 \cdot PCLK + 4$	-	-	ns
t_V	Data output valid time	-	-	$2 \cdot PCLK + 27$	ns
SPI slave mode (VDD = 3.0V ~ 3.6V, 30pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	$2 \cdot PCLK + 8$	-	-	ns
t_V	Data output valid time	-	-	$2 \cdot PCLK + 40$	ns

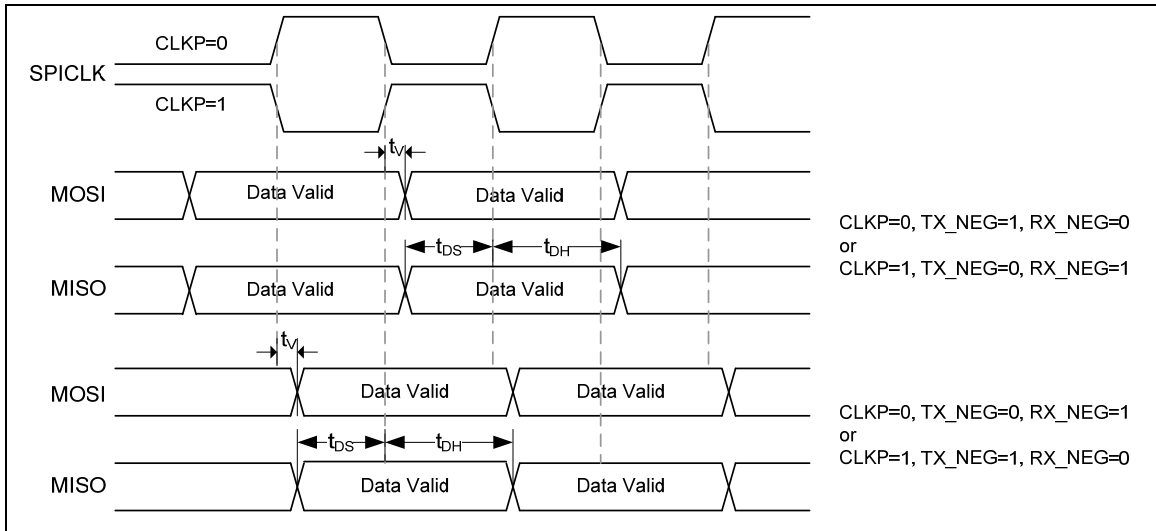


Figure 7-2 SPI Master timing

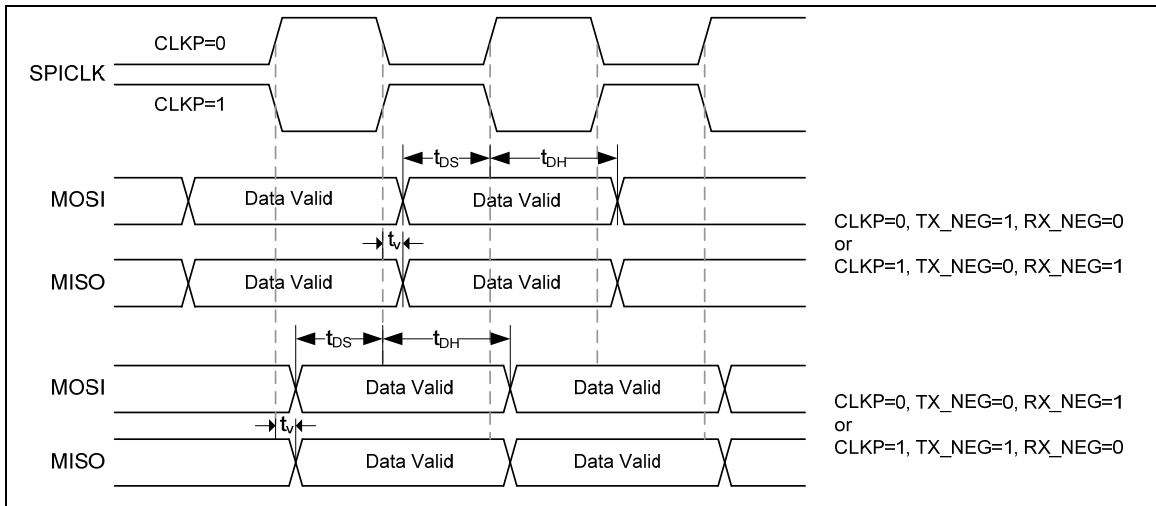
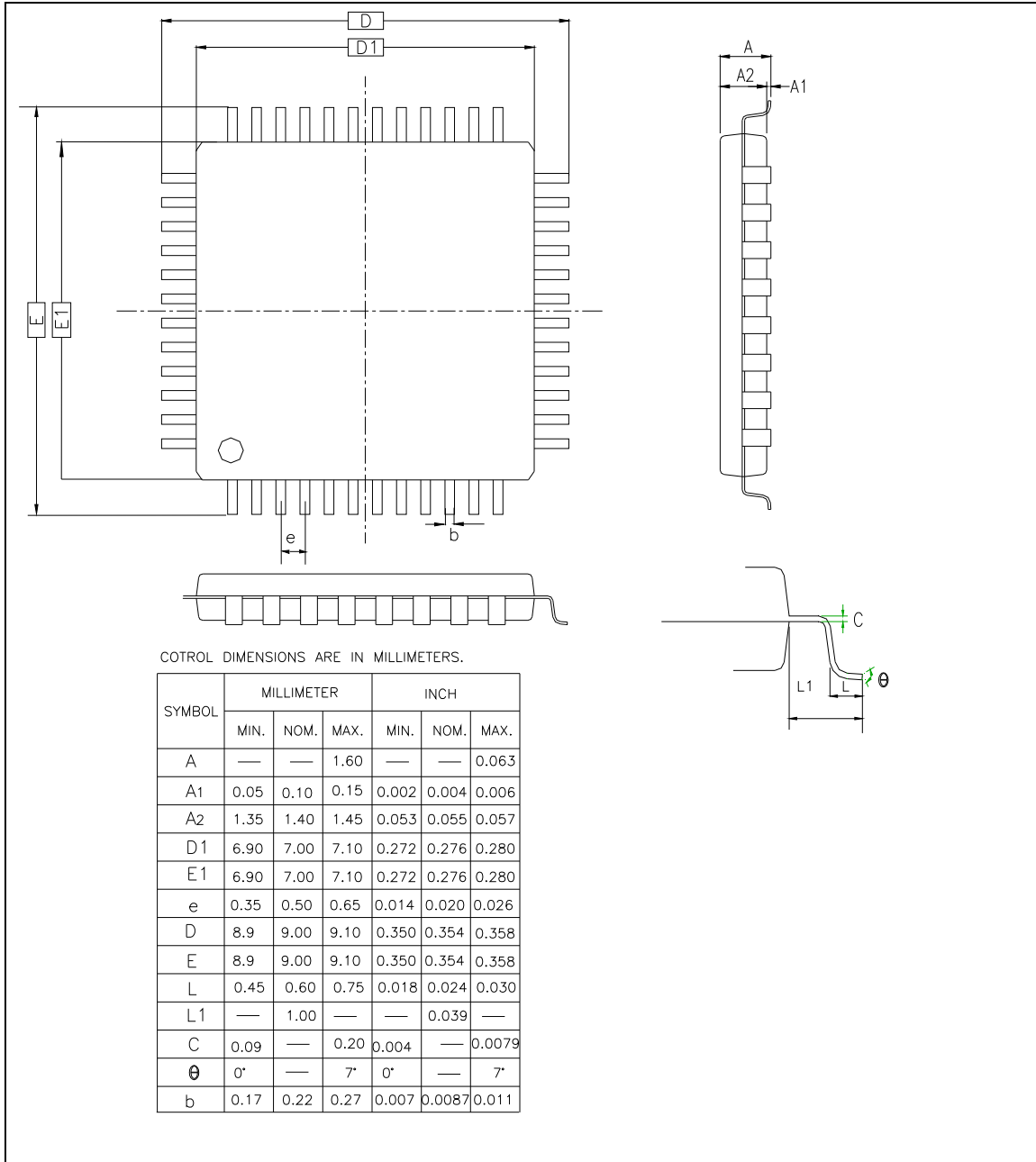


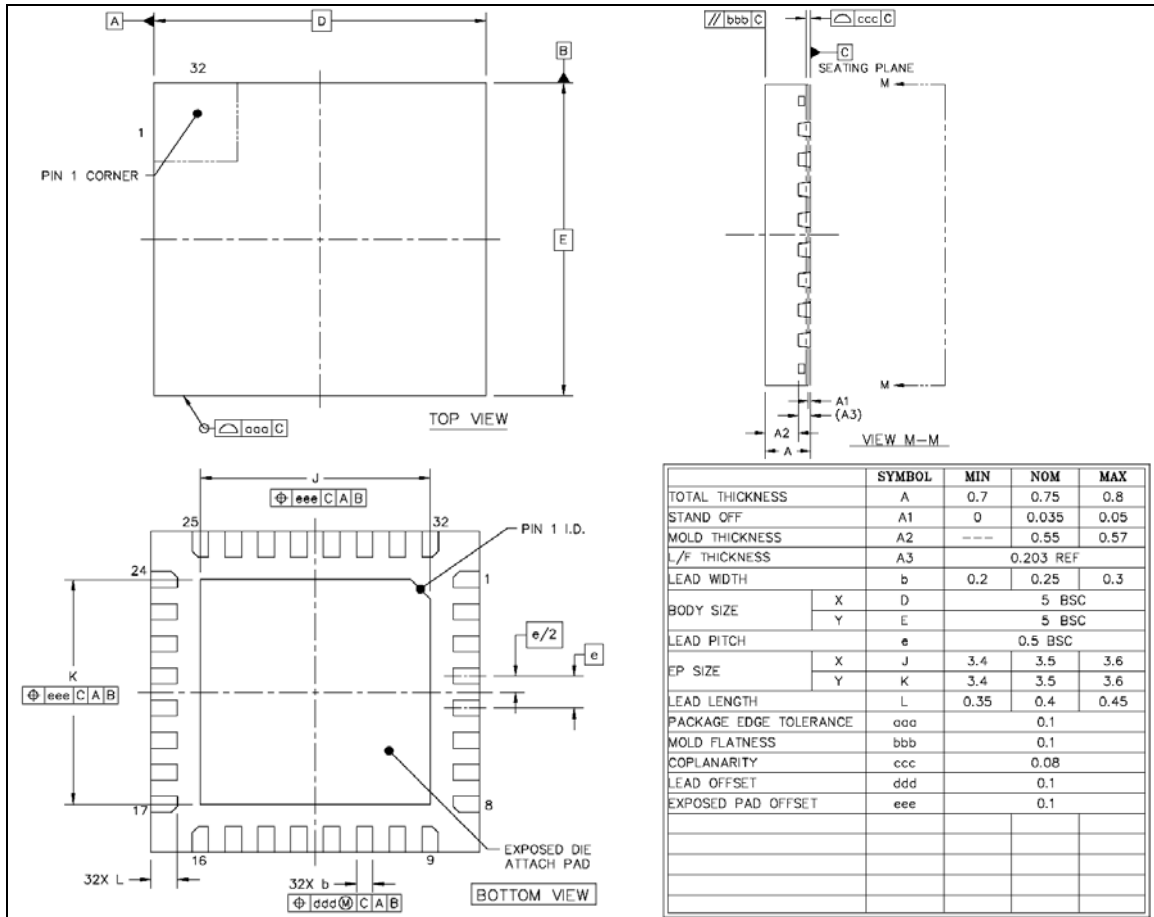
Figure 7-3 SPI Slave timing

8 PACKAGE DIMENSIONS

8.1 LQFP-48 (7x7x1.4mm² Footprint 2.0mm)



8.2 QFN-33 (5X5 mm², Thickness 0.8mm, Pitch 0.5 mm)



9 REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
V1.0	Jan 31, 2011	-	Initial issued
V1.1	Mar 08, 2011	25	Removed the Note 2 of Table 7.4.2

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