Freescale Semiconductor
Technical Data

Document Number: MRF6V3090N
Rev. 0, 4/2010

RoHS

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

MRF6V3090NR1
MRF6V3090NR5
MRF6V3090NBR1
MRF6V3090NBR5

Designed for broadband commercial and industrial applications with frequencies from 470 to 860 MHz. Devices are suitable for use in broadcast applications.

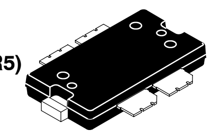
- Typical DVB-T OFDM Performance: V_{DD} = 50 Volts, I_{DQ} = 350 mA, P_{out} = 18 Watts Avg., f = 860 MHz, 8K Mode, 64 QAM, Input Signal PAR = 9.5 dB @ 0.01% Probability on CCDF.
  Power Gain — 22.0 dB
  Drain Efficiency — 28.5%
  ACPR @ 4 MHz Offset — -62.0 dBc @ 4 kHz Bandwidth
- Capable of Handling 10:1 VSWR, All Phase Angles, @ 50 Vdc, 860 MHz, 90 Watts CW Output Power

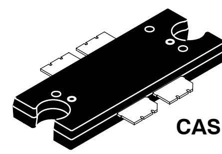
Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Input Matched for Ease of Use
- Qualified Up to a Maximum of 50 V_{DD} Operation
- Integrated ESD Protection
- Excellent Thermal Stability
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- 225°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel. R5 Suffix = 50 Units per 56 mm, 13 inch Reel.

470-860 MHz, 90 W, 50 V
LATERAL N-CHANNEL
SINGLE-ENDED
BROADBAND
RF POWER MOSFETs

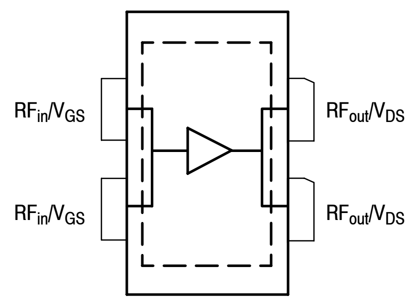
CASE 1486-03, STYLE 1
TO-270 WB-4
PLASTIC
MRF6V3090NR1(NR5)





CASE 1484-04, STYLE 1
TO-272 WB-4
PLASTIC
MRF6V3090NBR1(NBR5)

PARTS ARE SINGLE-ENDED



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +110	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
Case Temperature 76°C, 18 W CW, 50 Vdc, I_{DQ} = 350 mA		0.79	
Case Temperature 80°C, 90 W CW, 50 Vdc, I_{DQ} = 350 mA		0.82	

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2 (Minimum)
Machine Model (per EIA/JESD22-A115)	B (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

freescale™ semiconductor

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

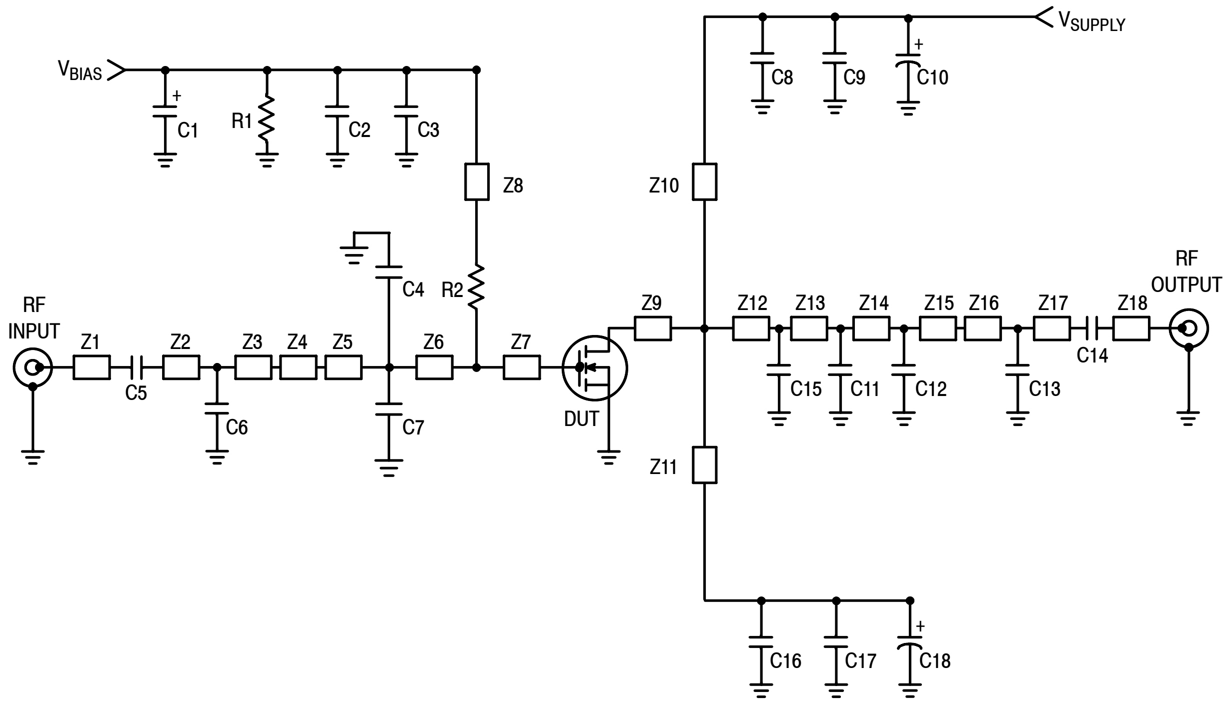
Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	0.5	μAdc
Drain-Source Breakdown Voltage (I_D = 50 mA, V_{GS} = 0 Vdc)	$V_{(BR)DSS}$	115	—	—	Vdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 100 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	20	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 200 μAdc)	$V_{GS(th)}$	0.9	1.6	2.4	Vdc
Gate Quiescent Voltage (V_{DD} = 50 Vdc, I_D = 350 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2	2.7	3.5	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 0.5 Adc)	$V_{DS(on)}$	—	0.2	—	Vdc
Dynamic Characteristics					
Reverse Transfer Capacitance (V_{DS} = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	41	—	pF
Output Capacitance (V_{DS} = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	65.4	—	pF
Input Capacitance (1) (V_{DS} = 50 Vdc, V_{GS} = 0 Vdc ± 30 mV(rms)ac @ 1 MHz)	C_{iss}	—	591	—	pF

Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 50 Vdc, I_{DQ} = 350 mA, P_{out} = 18 W Avg., f = 860 MHz, DVB-T OFDM Single Channel. ACPR measured in 7.61 MHz Channel Bandwidth @ ±4 MHz Offset @ 4 kHz Bandwidth.

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain	G_{ps}	21.0	22.0	24.0	dB
Drain Efficiency	η_D	27.5	28.5	—	%
Adjacent Channel Power Ratio	ACPR	—	-62.0	-60.0	dBc
Input Return Loss	IRL	—	-14	-9	dB

1. Part internally input matched.



Z1	0.266″ x 0.067″ Microstrip	Z10, Z11	1.292″ x 0.079″ Microstrip
Z2	0.331″ x 0.067″ Microstrip	Z12	0.680″ x 0.571″ Microstrip
Z3	0.598″ x 0.067″ Microstrip	Z13	0.132″ x 0.117″ Microstrip
Z4	0.315″ x 0.276″ Microstrip	Z14	0.705″ x 0.117″ Microstrip
Z5	0.054″ x 0.669″ Microstrip	Z15	0.159″ x 0.117″ Microstrip
Z6	0.419″ x 0.669″ Microstrip	Z16	0.140″ x 0.067″ Microstrip
Z7	0.256″ x 0.669″ Microstrip	Z17	0.077″ x 0.067″ Microstrip
Z8	0.986″ x 0.071″ Microstrip	Z18	0.163″ x 0.067″ Microstrip
Z9	0.201″ x 0.571″ Microstrip		

Figure 2. MRF6V3090NR1(NBR1) Test Circuit Schematic

Table 6. MRF6V3090NR1(NBR1) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	22 μF, 35 V Tantalum Capacitor	T491X226K035AT	Kermet
C2, C9, C17	10 μF, 50 V Chip Capacitors	GRM55DR61H106KA88L	Murata
C3, C5, C8, C14, C16	43 pF Chip Capacitors	ATC100B430JT500XT	ATC
C4	6.2 pF Chip Capacitor	ATC100B6R2BT500XT	ATC
C6	2.2 pF Chip Capacitor	ATC100B2R2JT500XT	ATC
C7	9.1 pF Chip Capacitor	ATC100B9R1CT500XT	ATC
C10, C18	220 μF, 100 V Electrolytic Capacitors	EEVFK2A221M	Panasonic-ECG
C11, C15	7.5 pF Chip Capacitors	ATC100B7R5CT500XT	ATC
C12	3.0 pF Chip Capacitor	ATC100B3R0CT500XT	ATC
C13	0.7 pF Chip Capacitor	ATC100B0R7BT500XT	ATC
R1	10 KΩ, 1/4 W Chip Resistor	CRCW120610KOJNEA	Vishay
R2	10 Ω, 1/4 W Chip Resistor	CRCW120610ROJNEA	Vishay
PCB	0.030″, ε_r = 3.5	RF-35	Taconic

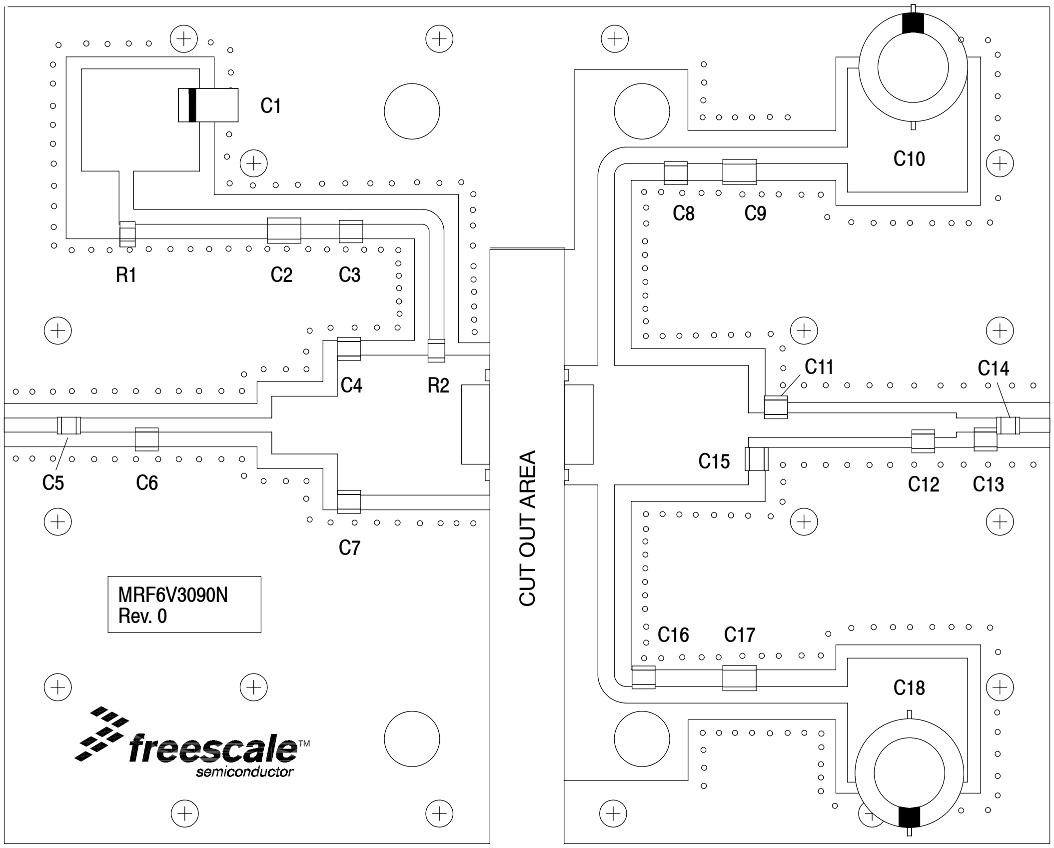


Figure 3. MRF6V3090NR1(NBR1) Test Circuit Component Layout

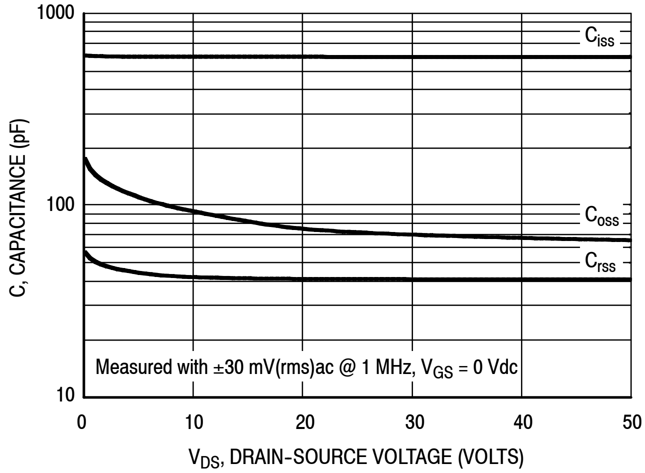


Figure 4. Capacitance versus Drain-Source Voltage

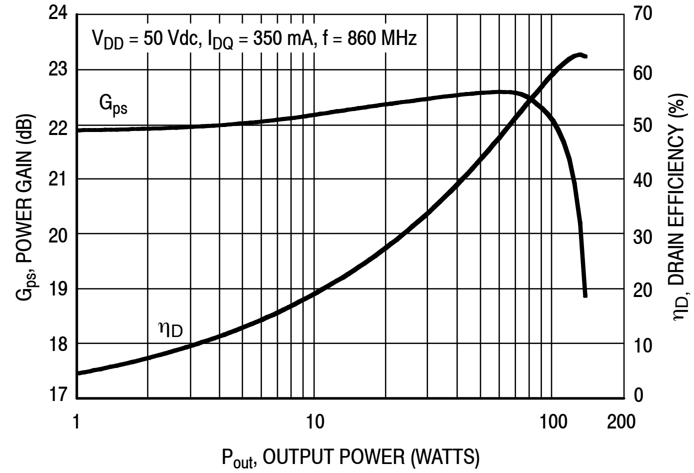


Figure 5. CW Power Gain and Drain Efficiency versus Output Power

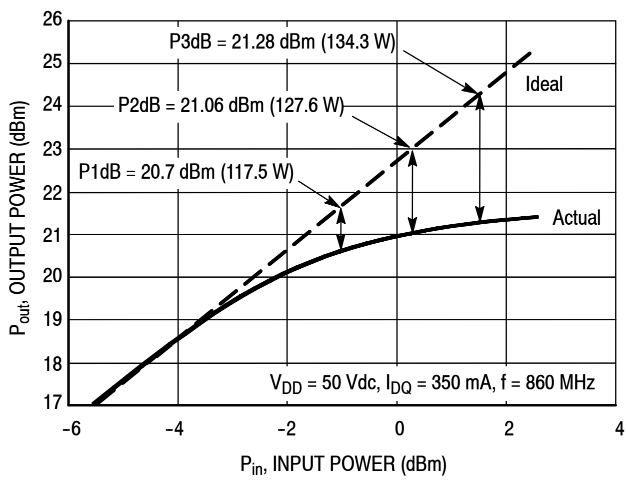


Figure 6. CW Output Power versus Input Power

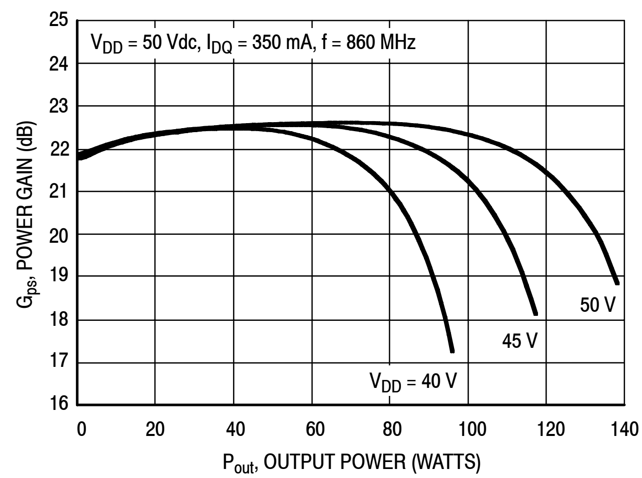


Figure 7. CW Power Gain versus Output Power

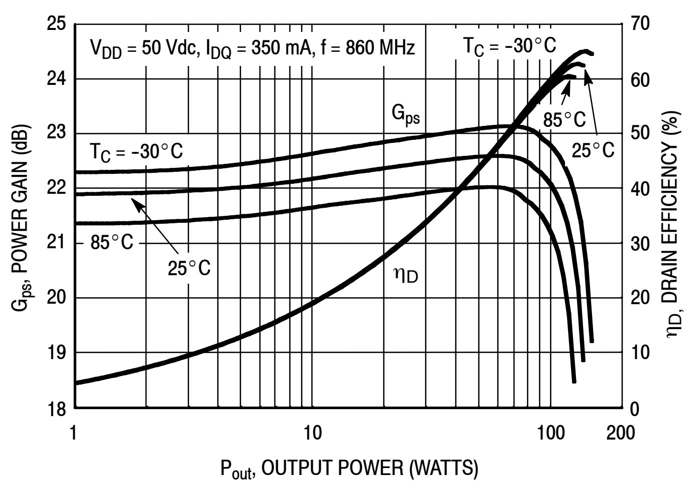


Figure 8. CW Power Gain and Drain Efficiency versus Output Power

TYPICAL CHARACTERISTICS — TWO-TONE

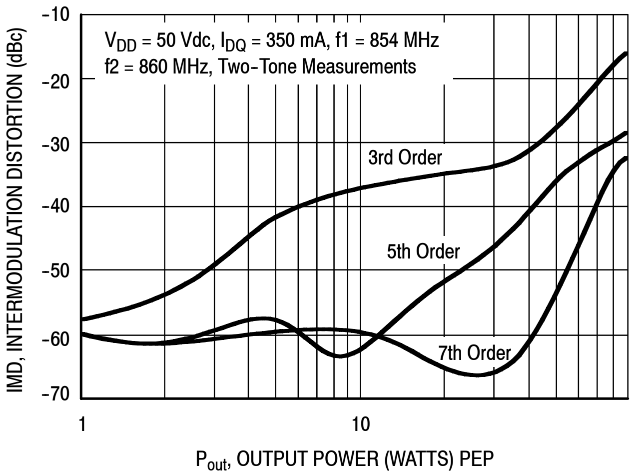


Figure 9. Intermodulation Distortion Products versus Output Power

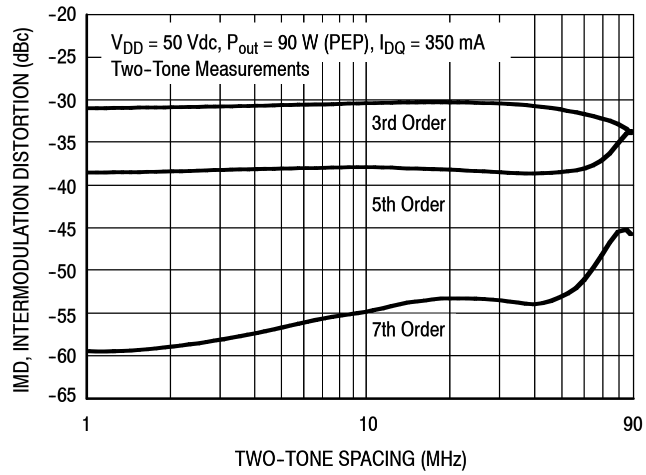


Figure 10. Intermodulation Distortion Products versus Tone Spacing

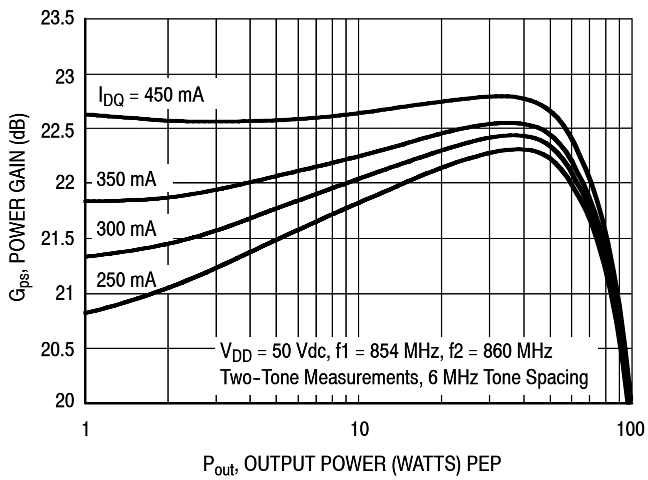


Figure 11. Two-Tone Power Gain versus Output Power

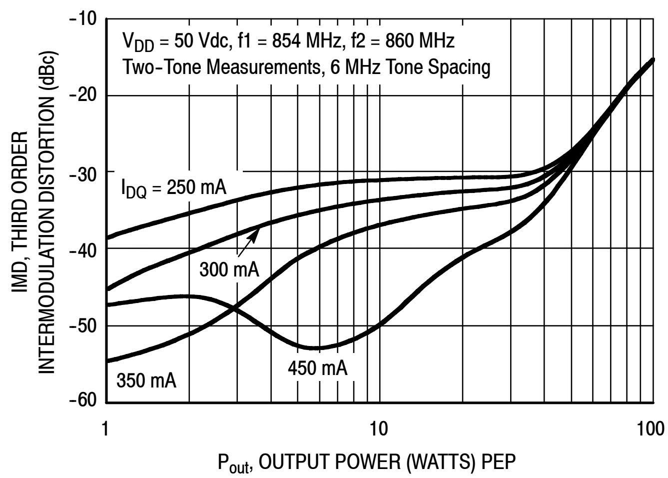


Figure 12. Third Order Intermodulation Distortion versus Output Power

TYPICAL CHARACTERISTICS — OFDM

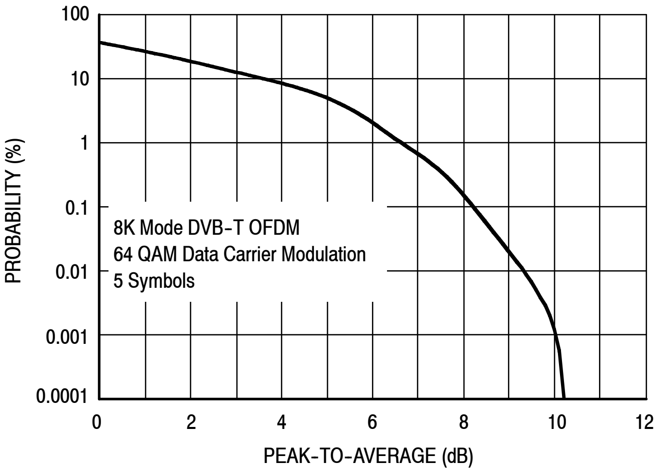


Figure 13. Single-Carrier DVB-T OFDM

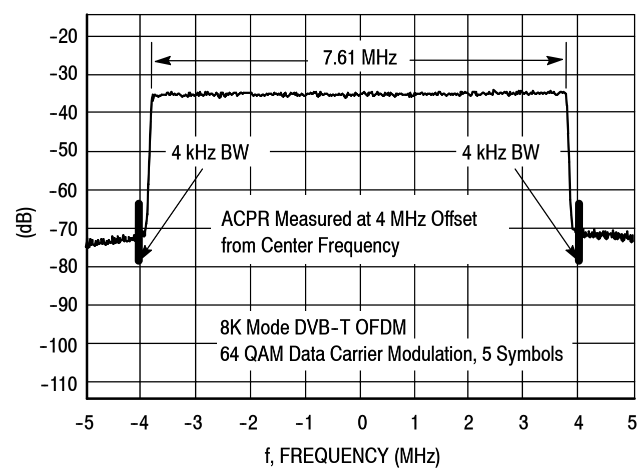


Figure 14. 8K Mode DVB-T OFDM Spectrum

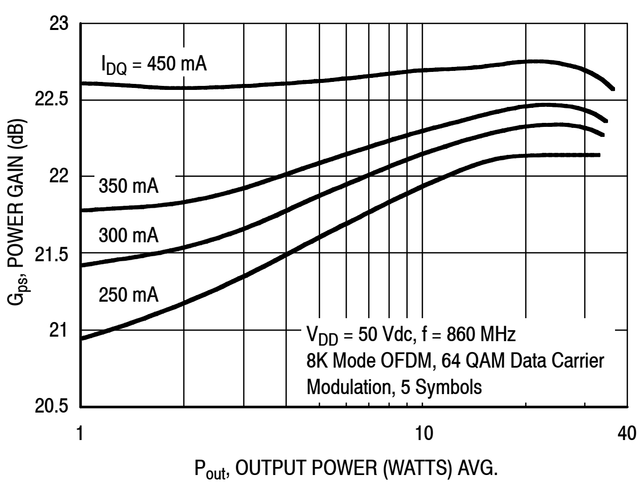


Figure 15. Single-Carrier DVB-T OFDM Power Gain versus Output Power

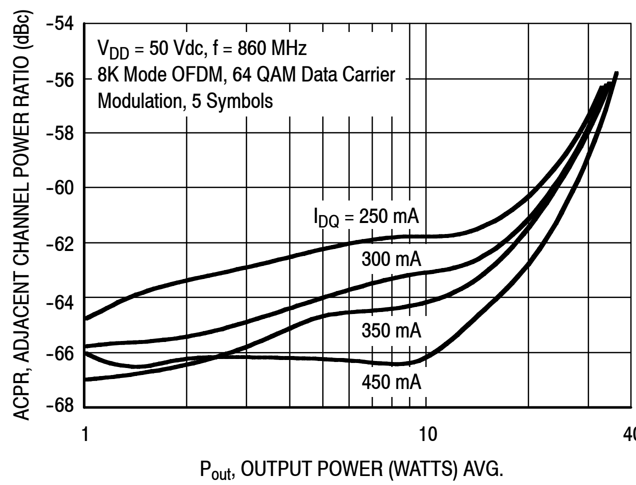


Figure 16. Single-Carrier DVB-T OFDM ACPR versus Output Power

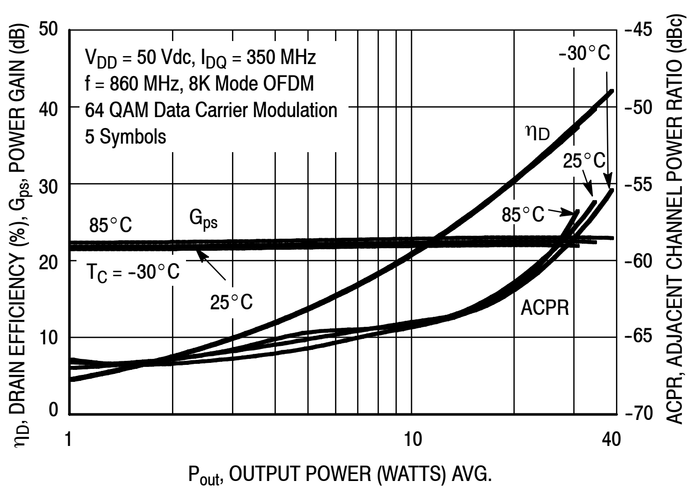
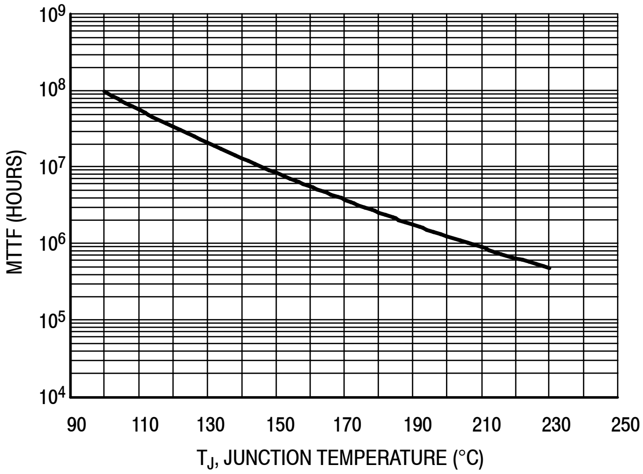


Figure 17. Single-Carrier DVB-T OFDM ACPR Power Gain and Drain Efficiency versus Output Power

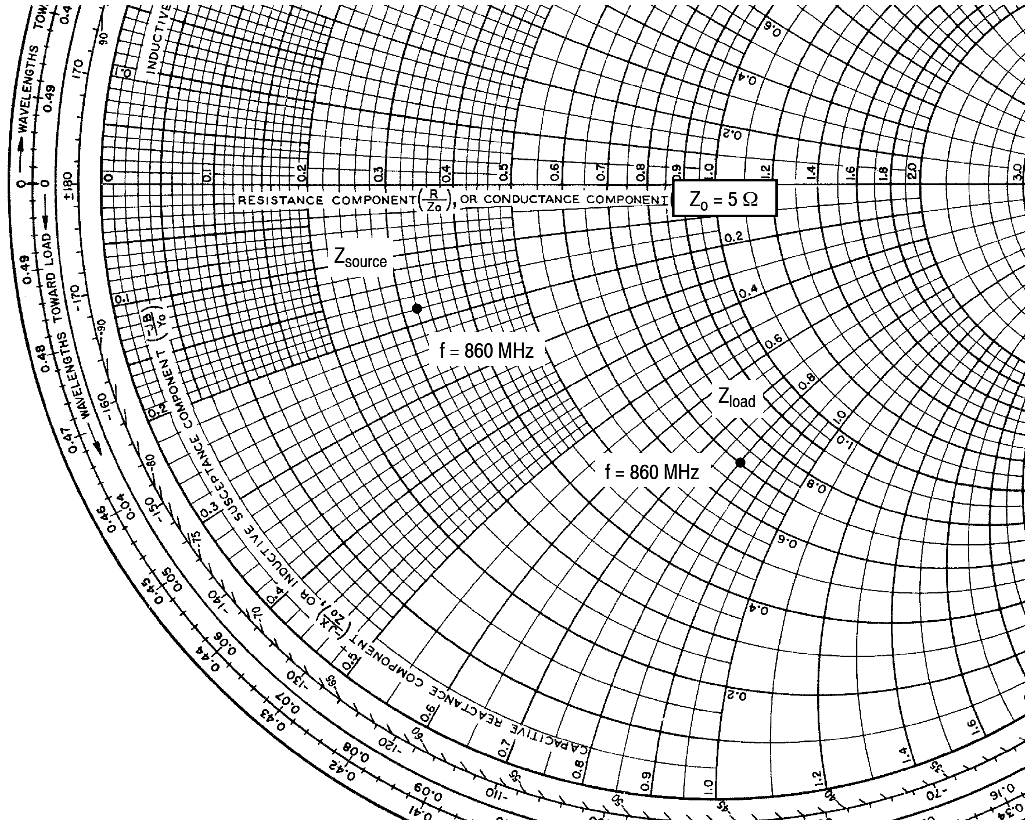
TYPICAL CHARACTERISTICS



This above graph displays calculated MTTF in hours when the device is operated at V_{DD} = 50 Vdc, P_{out} = 18 W Avg., and η_D = 28.5 %.

MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 18. MTTF versus Junction Temperature - CW



V_{DD} = 50 Vdc, I_{DQ} = 350 mA, P_{out} = 18 W Average

f MHz	Z_{source} Ω	Z_{load} Ω
860	1.58 – j0.89	3.51 – j3.98

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

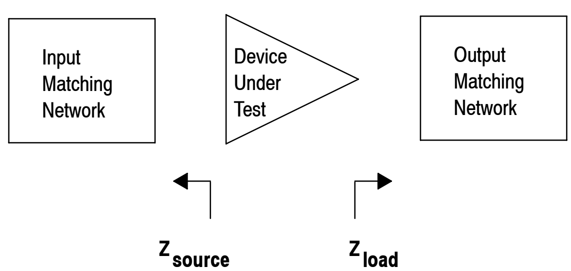
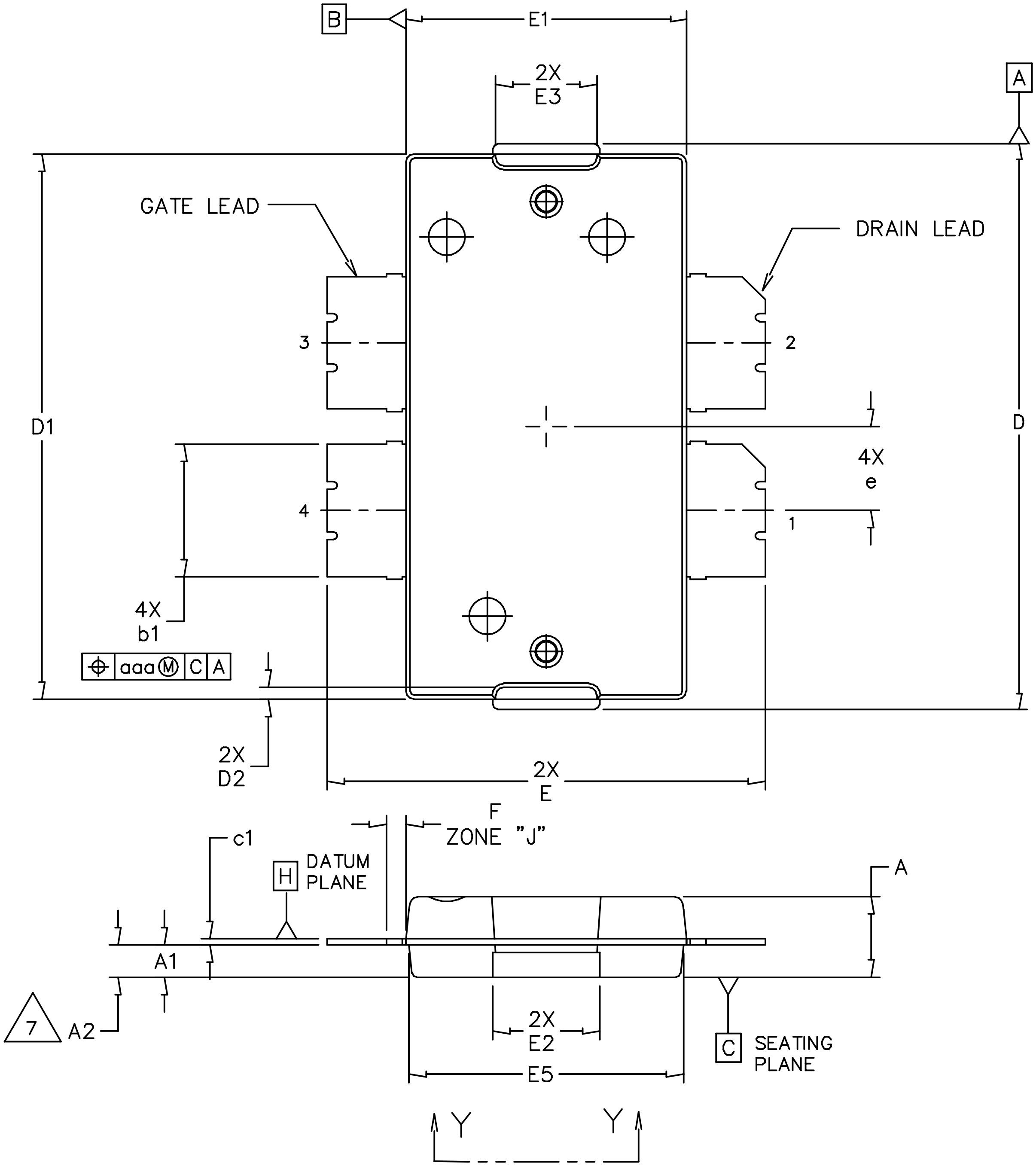


Figure 19. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS



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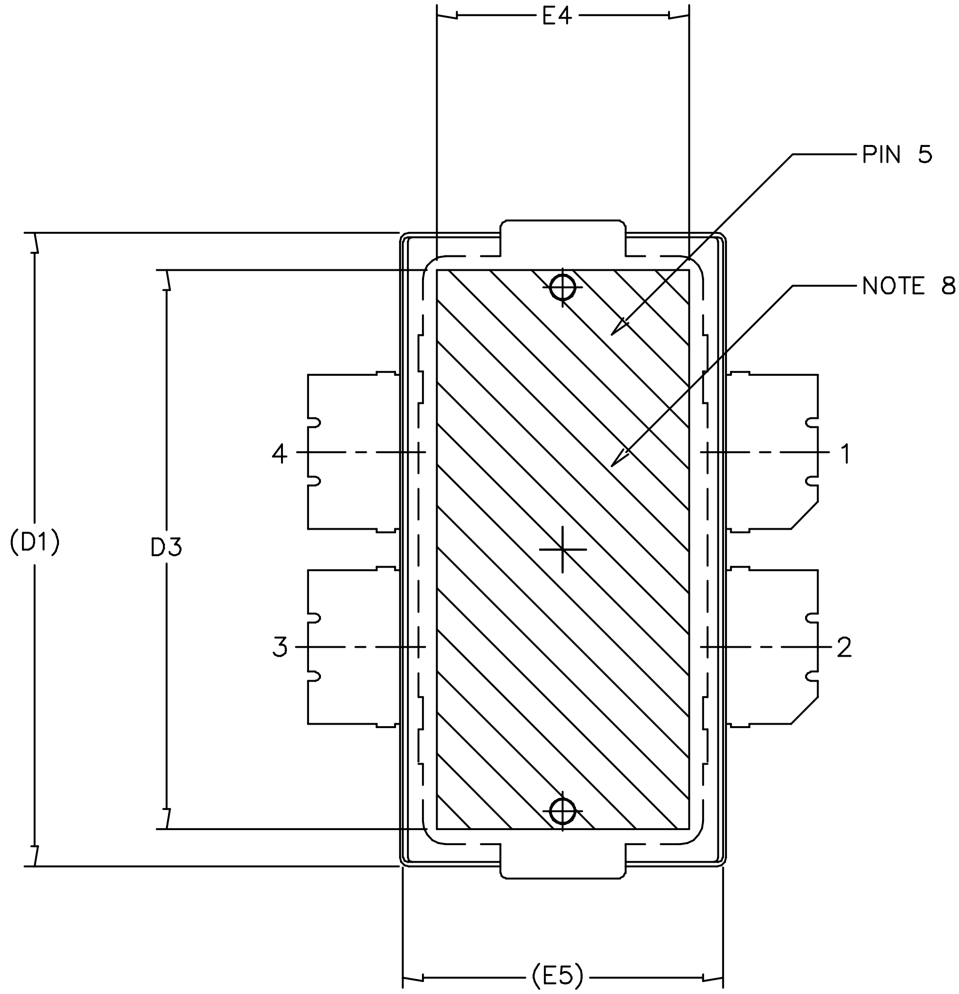
	CASE NUMBER: 1486−03	13 AUG 2007
	STANDARD: NON−JEDEC	



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	STANDARD: NON–JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

STYLE 1:
PIN 1 - DRAIN PIN 2 - DRAIN
PIN 3 - GATE PIN 4 - GATE
PIN 5 - SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b1	.164	.170	4.17	4.32
A2	.040	.042	1.02	1.07	c1	.007	.011	.18	.28
D	.712	.720	18.08	18.29	e	.106 BSC		2.69 BSC	
D1	.688	.692	17.48	17.58	aaa	.004		.10	
D2	.011	.019	0.28	0.48					
D3	.600	---	15.24	---					
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					

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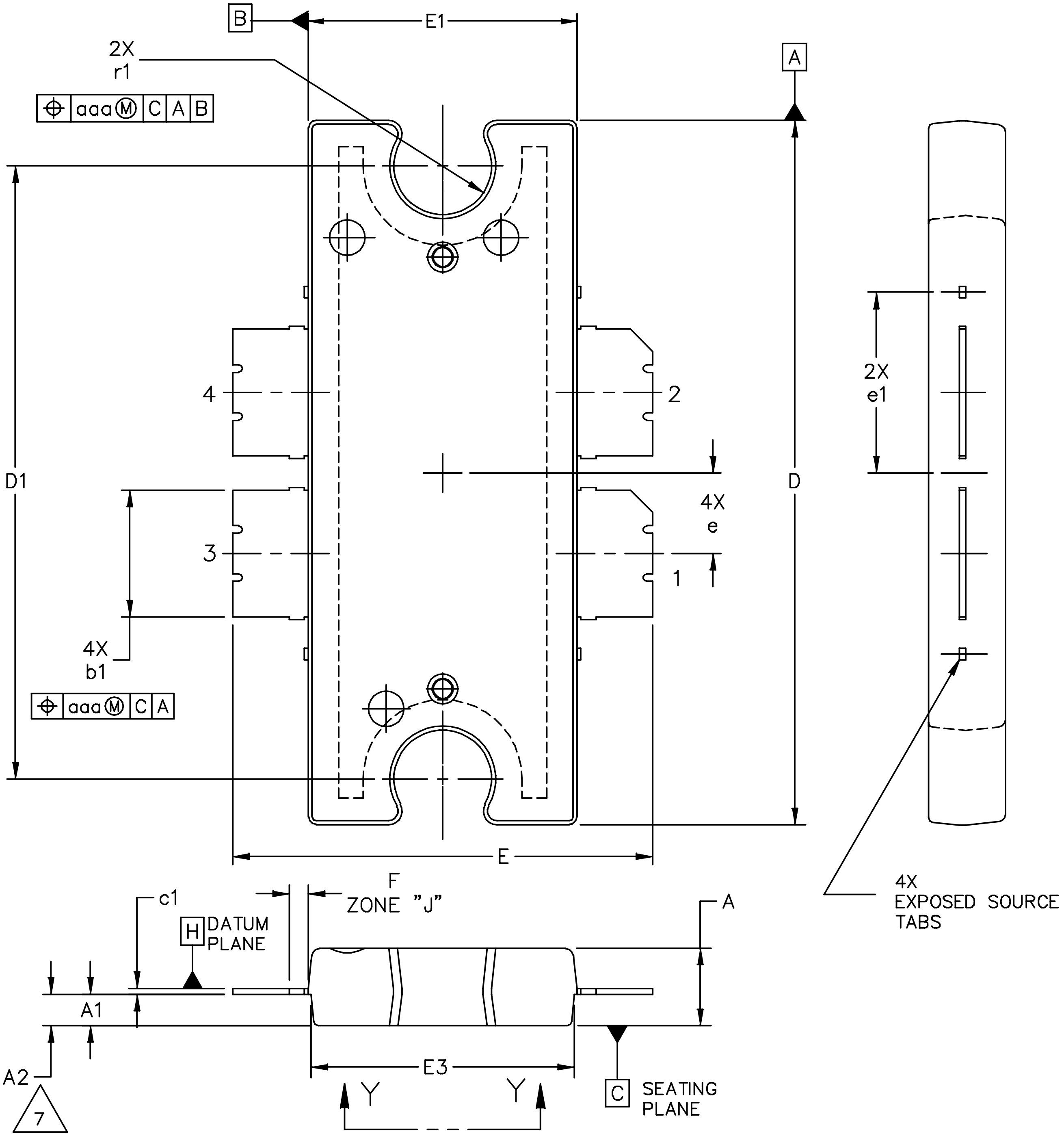

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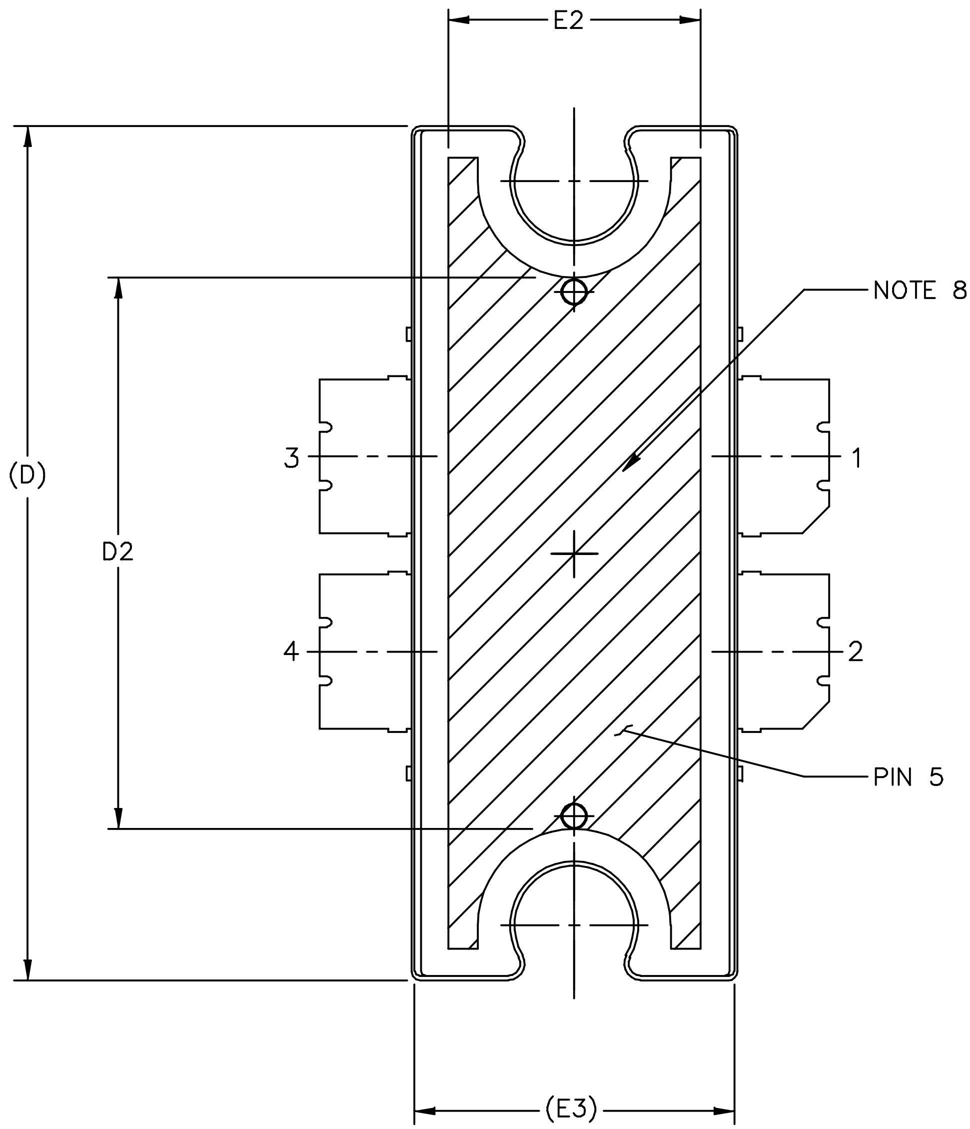
	STANDARD: NON–JEDEC	



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	CASE NUMBER: 1484–04	31 AUG 2007
	STANDARD: NON–JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M—1994.
3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

STYLE 1:
PIN 1 — DRAIN   PIN 2 — DRAIN
PIN 3 — GATE   PIN 4 — GATE
PIN 5 — SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b1	.164	.170	4.17	4.32
A1	.039	.043	0.99	1.09	c1	.007	.011	.18	.28
A2	.040	.042	1.02	1.07	r1	.063	.068	1.60	1.73
D	.928	.932	23.57	23.67	e	.106 BSC		2.69 BSC	
D1	.810 BSC		20.57 BSC		e1	.239 INFO ONLY		6.07 INFO ONLY	
D2	.600	---	15.24	---	aaa	.004		.10	
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.270	---	6.86	---					
E3	.346	.350	8.79	8.89					
F	.025 BSC		0.64 BSC						

MECHANICAL OUTLINE

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	CASE NUMBER: 1484—04	31 AUG 2007
	STANDARD: NON—JEDEC	

PRODUCT DOCUMENTATION, TOOLS AND SOFTWARE

Refer to the following documents, tools and software to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages
- AN3789: Clamping of High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Apr. 2010	• Initial Release of Data Sheet

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