SD4933

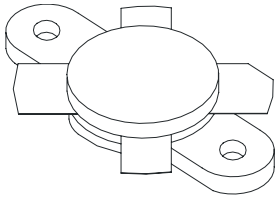
RF power transistor HF/VHF/UHF N-channel MOSFET

Features

- Improved ruggedness $V_{(BR)DSS}$ > 200 V
- Excellent thermal stability
- 20:1 all phases load mismatch capability
- P_{OUT} = 300 W min. with 24 dB gain @ 30 MHz
- In compliance with the 2002/95/EEC european directive

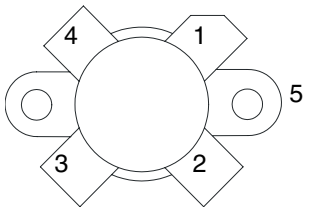
Description

The SD4933 is a N-channel MOS field-effect RF power transistor. It is intended for use in 50 V ISM applications up to 100 MHz.



M177
Epoxy sealed

Figure 1. Pin connection



1. Drain
2. Source
3. Gate
4. Source
5. Source

Table 1. Device summary

Order code	Marking	Package	Packaging
SD4933	SD4933(1)	M177	Plastic tray

1. For more details please refer to *Chapter 9: Marking, packing and shipping specifications.*.

Contents

1 Electrical data

1.1 Maximum ratings

Table 2. Absolute maximum ratings (T_{CASE} = 25 °C)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain source voltage	200	V
V_{DGR}	Drain-gate voltage (R_{GS} = 1 MΩ)	200	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current	40	A
P_{DISS}	Power dissipation	648	W
T_J	Max. operating junction temperature	200	°C
T_{STG}	Storage temperature	-65 to +150	°C

1.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Junction - case thermal resistance	0.27	°C/W

2 Electrical characteristics

T_{CASE} = +25 °C

2.1 Static

Table 4. Static

Symbol	Test conditions			Min	Typ	Max	Unit
$V_{(BR)DSS}$	V_{GS} = 0 V	I_{DS} = 100 mA		200	240		V
I_{DSS}	V_{GS} = 0 V	V_{DS} = 100 V				2	mA
I_{GSS}	V_{GS} = 20 V	V_{DS} = 0 V				500	nA
V_{TH}	I_D = 250 mA			1.5	2.5	4.0	V
$V_{DS(ON)}$	V_{GS} = 10 V	I_D = 20 A			3.5	4.0	V
G_{FS}	V_{DS} = 10 V	I_D = 5 A		5	8		S
C_{ISS}	V_{GS} = 0 V	V_{DS} = 50 V	f = 1 MHz		1000		pF
C_{OSS}	V_{GS} = 0 V	V_{DS} = 50 V	f = 1 MHz		400		pF
C_{RSS}	V_{GS} = 0 V	V_{DS} = 50 V	f = 1 MHz		16		pF

2.2 Dynamic

Table 5. Dynamic

Symbol	Test conditions	Min	Typ	Max	Unit
P_{OUT}	V_{DD} = 50 V I_{DQ} = 250 mA f = 30 MHz	300		-	W
G_{PS}	V_{DD} = 50 V I_{DQ} = 250 mA P_{OUT} = 300 W f = 30 MHz	20	24	-	dB
h_D	V_{DD} = 50 V I_{DQ} = 250 mA P_{OUT} = 300 W f = 30 MHz	50	58	-	%
Load mismatch	V_{DD} = 50 V I_{DQ} = 250 mA P_{OUT} = 300 W f = 30 MHz All phase angles	10:1	20:1	-	VSWR

3 Impedance data

Figure 2. Impedance data

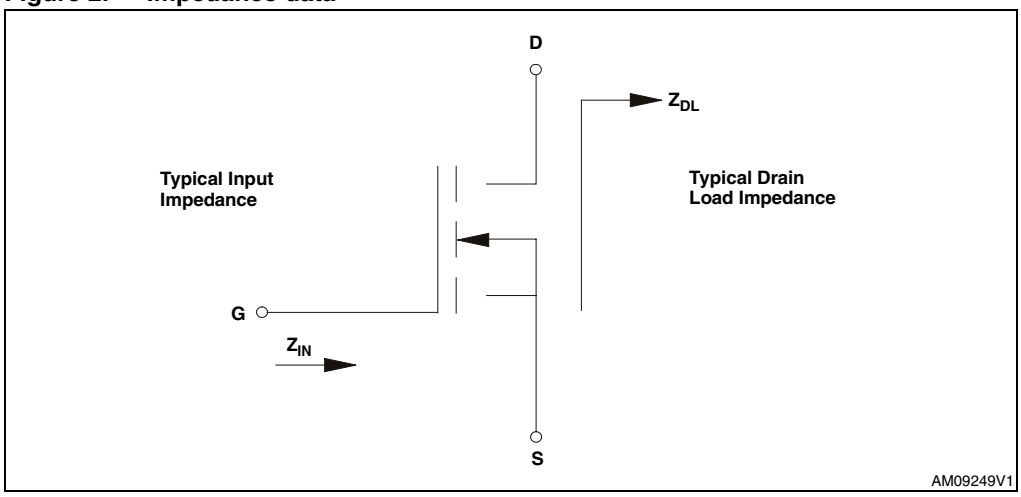


Table 6. Impedance values

Z_{in}	Z_{dl}
1.6 - j 5.0	3.3 + j 1.0

4 Typical performance

Figure 3. Capacitance vs drain voltage

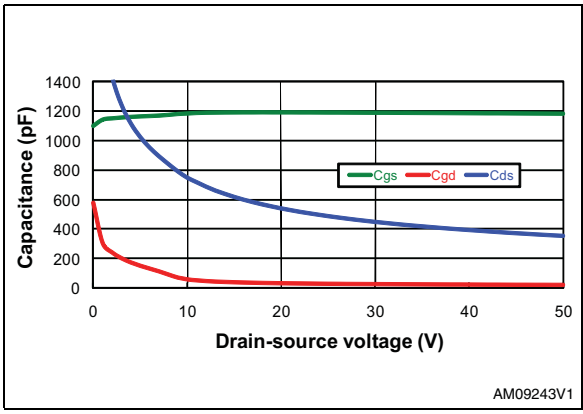


Figure 4. Drain current vs drain-source voltage

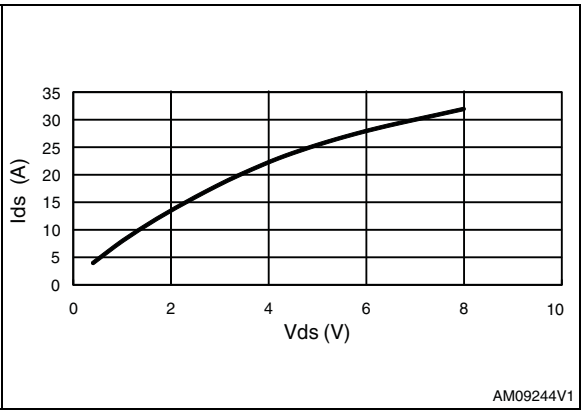
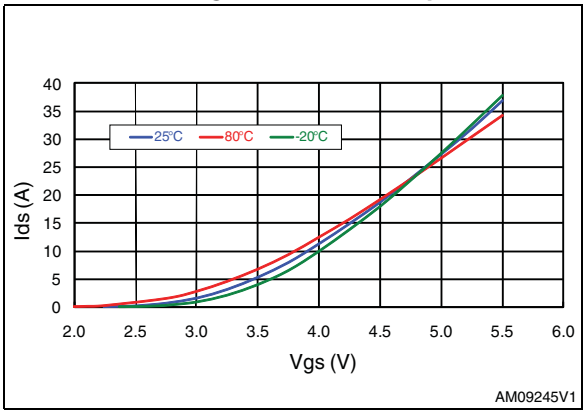


Figure 5. Drain current vs drain-source voltage at different temperatures



5 Typical performance (30 MHz)

Figure 6. Gain and efficiency vs output power_Vdd = 50 V, Idq = 250 mA, freq = 30 MHz

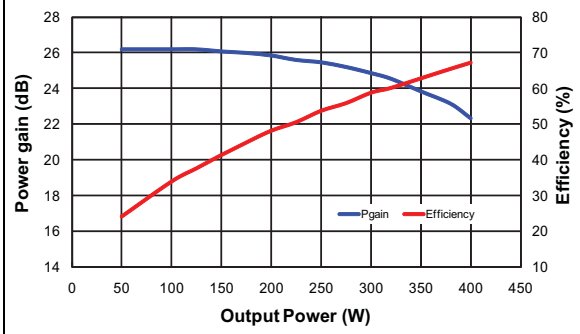


Figure 7. Output power vs input power

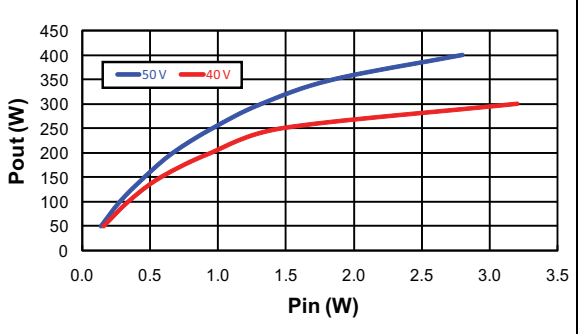


Figure 8. Output power vs supply voltage

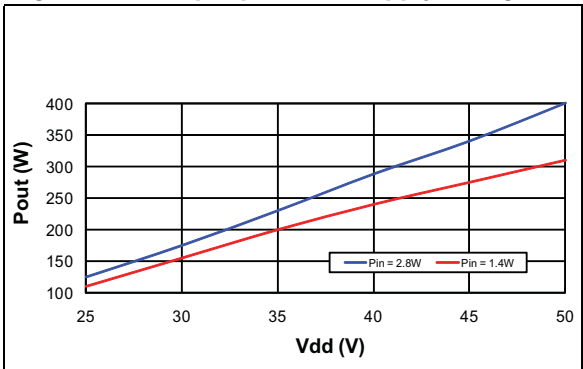
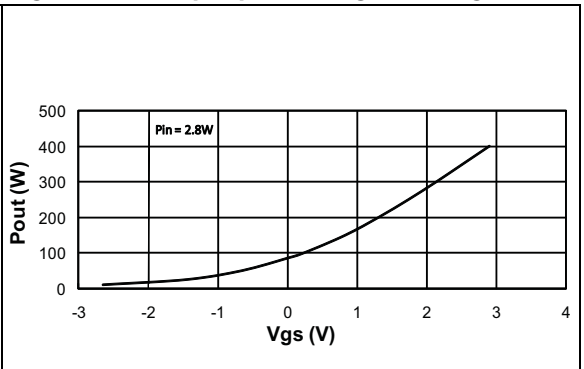


Figure 9. Output power vs gate voltage



5.1 Test circuit (30 MHz)

Figure 10. 30 MHz test circuit schematic

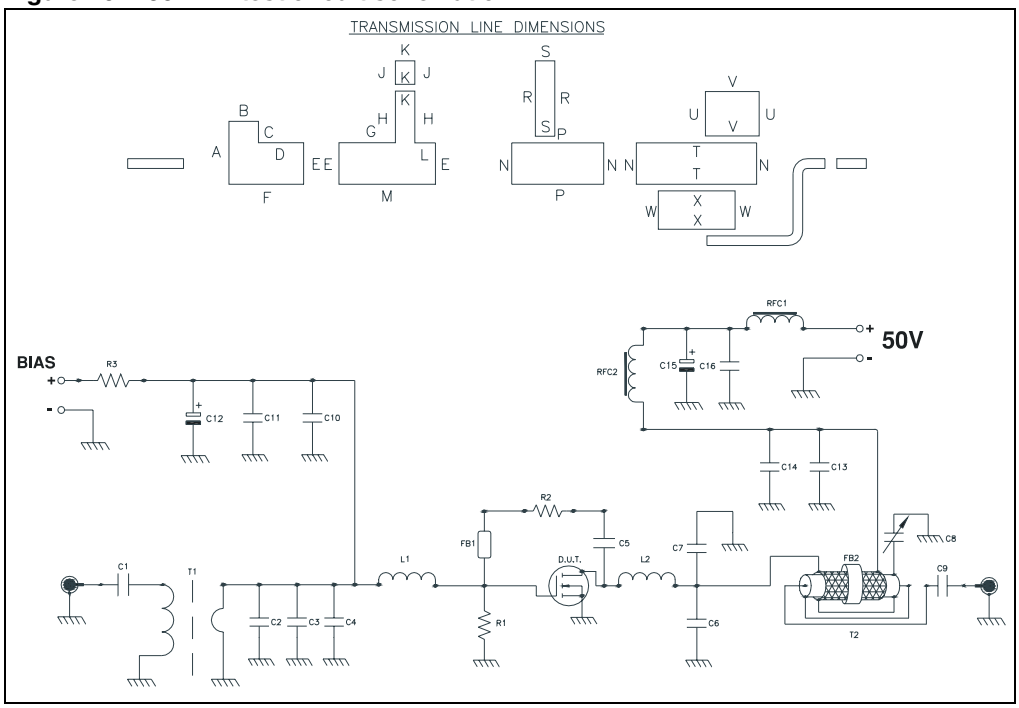


Table 7. Transmission line dimensions

Dim.	Inch	mm
A	0.532	13.51
B	0.250	6.35
C	0.181	4.59
D	0.383	9.37
E	0.351	8.91
F	0.633	16.08
G	0.477	12.12
H	0.438	11.12
J	0.200	5.08
K	0.164	4.16
L	0.174	4.42
M	0.817	20.75
N	0.350	8.89
P	0.779	19.79
R	0.639	16.23

Table 7. Transmission line dimensions (continued)

Dim.	Inch	mm
S	0.165	4.19
T	1.017	25.84
U	0.375	9.52
V	0.456	11.58
W	0.325	8.24
X	0.650	16.50

Table 8. 30 MHz test circuit component part list

Component	Description
C1,C9	0.01 µF / 500 V surface mount ceramic chip capacitor
C2, C3	750 pF ATC 700B surface mount ceramic chip capacitor
C4	300 pF ATC 700B surface mount ceramic chip capacitor
C5,C10,C11,C14,C16	10000 pF ATC 200B surface mount ceramic chip capacitor
C6	510 pF ATC 700B surface mount ceramic chip capacitor
C7	300 pF ATC 700B surface mount ceramic chip capacitor
C8	175-680 pF type 46 standard trimmer capacitor
C12	47 µF / 63 V aluminum electrolytic radial lead capacitor
C13	1200 pF ATC 700B surface mount ceramic chip capacitor
C15	100 µF / 63 V aluminum electrolytic radial lead capacitor
R1,R3	1 K OHM 1 W surface mount chip resistor
R2	560 OHM 2 W wire-wound axils lead resistor
T1	HF 2-30 MHz surface mount 9:1 transformer
T2	RG - 142B/U 50 OHM coaxial cable OD = 0.165[4.18] L 15”[381.00] covered with 15”[381.00] tinned copper tubular brand 13/65” [5.1] width
L1	1 3/4 turn air-wound 16 AWG ID = 0.219 [5.56] poly-coated magnet wire
L2	1 3/4 turn air-wound 12 AWG ID = 0.250 [6.34] bus bar wire
RFC1,RFC2	3 turns 14 AWG wire through fair rite toroid
FB1	Surface mount emi shield bead
FB2	Toroid
PCB	ULTRALAM 2000. 0.030” THK, εr = 2.55, 2 Oz ED CU both sides

6 Circuit layout

Figure 11. Test fixture component layout

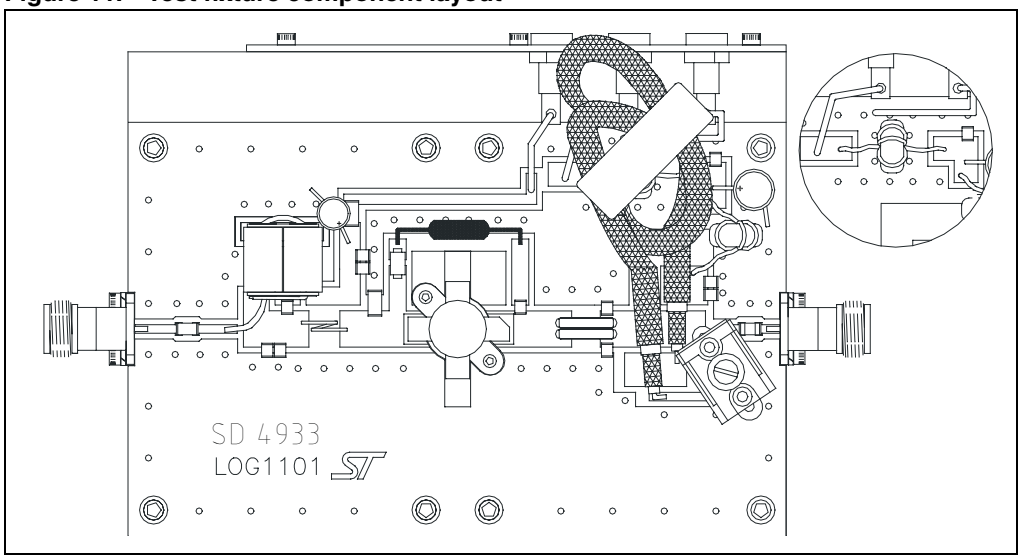
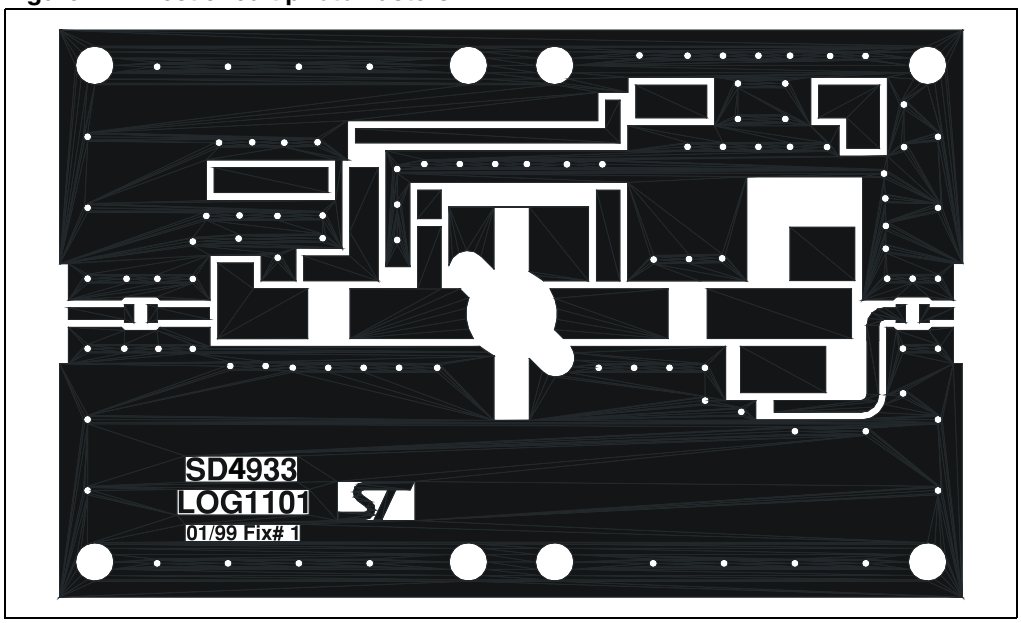


Figure 12. Test circuit photomasters



7 V_{GS}/G_{FS} sorts

Table 9. VGS/GFS sorts

Marking	Vgs(min)	Vgs(max)	Gfs(min)	Gfs(max)
A1	1.50	1.75	5	6
A2	1.50	1.75	6	7
A3	1.50	1.75	7	8
A4	1.50	1.75	8	9
A5	1.50	1.75	9	10
A6	1.50	1.75	10	11
A7	1.50	1.75	11	12
A8	1.50	1.75	12	13
A9	1.50	1.75	13	14
B1	1.75	2.00	5	6
B2	1.75	2.00	6	7
B3	1.75	2.00	7	8
B4	1.75	2.00	8	9
B5	1.75	2.00	9	10
B6	1.75	2.00	10	11
B7	1.75	2.00	11	12
B8	1.75	2.00	12	13
B9	1.75	2.00	13	14
C1	2.00	2.25	5	6
C2	2.00	2.25	6	7
C3	2.00	2.25	7	8
C4	2.00	2.25	8	9
C5	2.00	2.25	9	10
C6	2.00	2.25	10	11
C7	2.00	2.25	11	12
C8	2.00	2.25	12	13
C9	2.00	2.25	13	14
D1	2.25	2.50	5	6
D2	2.25	2.50	6	7
D3	2.25	2.50	7	8
D4	2.25	2.50	8	9
D5	2.25	2.50	9	10

Table 9. VGS/GFS sorts (continued)

Marking	Vgs(min)	Vgs(max)	Gfs(min)	Gfs(max)
D6	2.25	2.50	10	11
D7	2.25	2.50	11	12
D8	2.25	2.50	12	13
D9	2.25	2.50	13	14
E1	2.50	2.75	5	6
E2	2.50	2.75	6	7
E3	2.50	2.75	7	8
E4	2.50	2.75	8	9
E5	2.50	2.75	9	10
E6	2.50	2.75	10	11
E7	2.50	2.75	11	12
E8	2.50	2.75	12	13
E9	2.50	2.75	13	14
F1	2.75	3.00	5	6
F2	2.75	3.00	6	7
F3	2.75	3.00	7	8
F4	2.75	3.00	8	9
F5	2.75	3.00	9	10
F6	2.75	3.00	10	11
F7	2.75	3.00	11	12
F8	2.75	3.00	12	13
F9	2.75	3.00	13	14
G1	3.00	3.25	5	6
G2	3.00	3.25	6	7
G3	3.00	3.25	7	8
G4	3.00	3.25	8	9
G5	3.00	3.25	9	10
G6	3.00	3.25	10	11
G7	3.00	3.25	11	12
G8	3.00	3.25	12	13
G9	3.00	3.25	13	14
H1	3.25	3.50	5	6
H2	3.25	3.50	6	7
H3	3.25	3.50	7	8
H4	3.25	3.50	8	9

Table 9. VGS/GFS sorts (continued)

Marking	Vgs(min)	Vgs(max)	Gfs(min)	Gfs(max)
H5	3.25	3.50	9	10
H6	3.25	3.50	10	11
H7	3.25	3.50	11	12
H8	3.25	3.50	12	13
H9	3.25	3.50	13	14
I1	3.50	3.75	5	6
I2	3.50	3.75	6	7
I3	3.50	3.75	7	8
I4	3.50	3.75	8	9
I5	3.50	3.75	9	10
I6	3.50	3.75	10	11
I7	3.50	3.75	11	12
I8	3.50	3.75	12	13
I9	3.50	3.75	13	14
J1	3.75	4.00	5	6
J2	3.75	4.00	6	7
J3	3.75	4.00	7	8
J4	3.75	4.00	8	9
J5	3.75	4.00	9	10
J6	3.75	4.00	10	11
J7	3.75	4.00	11	12
J8	3.75	4.00	12	13
J9	3.75	4.00	13	14

8 Package mechanical data

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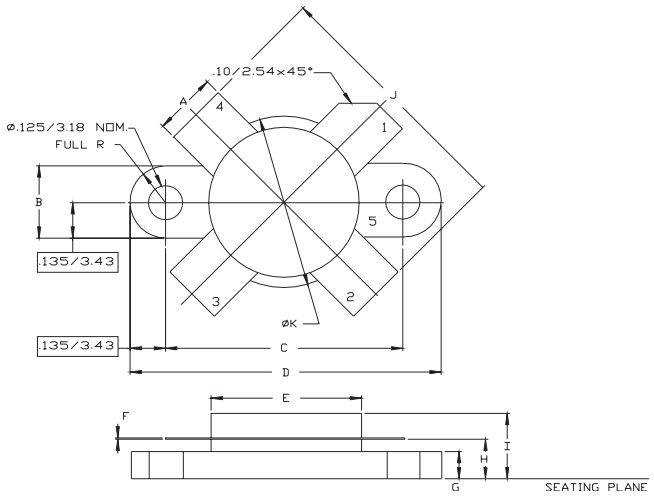
Table 10. M177 (.550 DIA 4/L N/HERM W/FLG) mechanical data

Dim.	mm.			Inch		
	Min	Typ	Max	Min	Typ	Max
A	5.72		5.97	0.225		0.235
B	6.73		6.96	0.265		0.275
C	21.84		22.10	0.860		0.870
D	28.70		28.96	1.130		1.140
E	13.84		14.10	0.545		0.555
F	0.08		0.18	0.003		0.007
G	2.49		2.74	0.098		0.108
H	3.81		4.32	0.150		0.170
I			7.11			0.280
J	27.43		28.45	1.080		1.120
K	15.88		16.13	0.625		0.635

Figure 13. Package dimensions



9 Marking, packing and shipping specifications

Table 11. Packing and shipping specifications

Order code	Packaging	Pcs per tray	Dry pack humidity	VGS and GFS code	Lot code
SD4933	Plastic tray	25	< 10 %	Not mixed	Not mixed

Figure 14. Marking layout

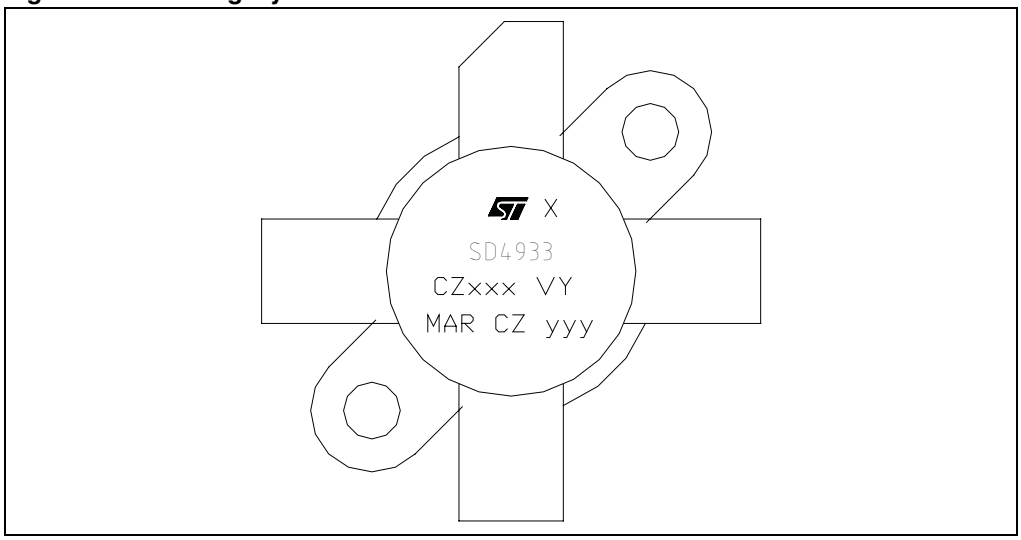


Table 12. Marking specifications

Symbol	Description
X	V_{GS} and G_{FS} sort
CZ	Assy plant
xxx	Last 3 digit of diffusion lot
VY	Diffusion plant
MAR	Country of origin
CZ	Test and finishing plant
y	Assy year
yy	Assy week

10 Revision history

Table 13. Document revision history

Date	Revision	Changes
11-Mar-2009	1	Initial release
24-Feb-2010	2	Updated *Table 9: VGS/GFS sorts on page 11*.
29-Sep-2010	3	Document status promoted from preliminary to datasheet.
06-Apr-2011	4	Inserted *Section 3: Impedance data*, *Section 4: Typical performance*, *Section 6: Circuit layout* and *Section 9: Marking, packing and shipping specifications*.

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