STB18N55M5, STD18N55M5
STF18N55M5, STP18N55M5

N-channel 550 V, 0.18 Ω, 13 A, MDmesh™ V Power MOSFET in D²PAK, DPAK, TO-220FP and TO-220

Features

Order codes	V_{DSS} @T_{Jmax}	$R_{DS(on)}$ max	I_D
STB18N55M5 STD18N55M5 STF18N55M5 STP18N55M5	550 V	< 0.24 Ω	13 A

- DPAK worldwide best $R_{DS(on)}$
- Higher V_{DSS} rating
- High dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested

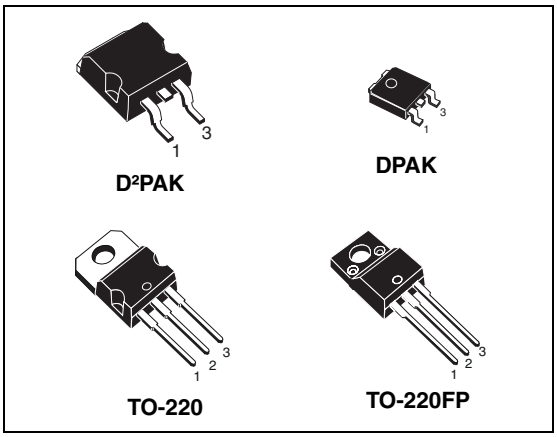
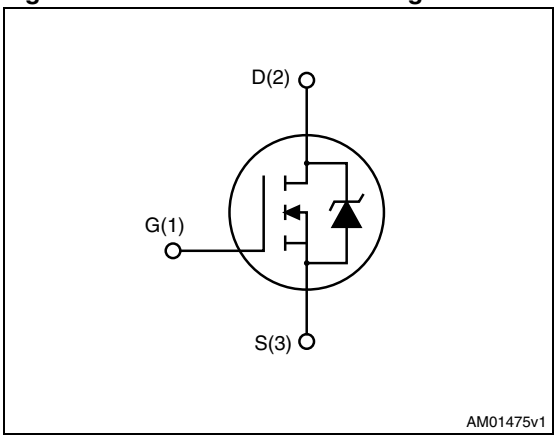


Figure 1. Internal schematic diagram



Application

Switching applications

Description

The devices are N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB18N55M5	18N55M5	D²PAK	Tape and reel
STD18N55M		DPAK	
STF18N55M5		TO-220FP	Tube
STP18N55M5		TO-220	

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220, DPAK, D²PAK	TO-220FP	
V_{GS}	Gate-source voltage	25		V
I_D	Drain current (continuous) at T_C = 25 °C	13	13 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	8.3	8.3 (1)	A
I_{DM} (2)	Drain current (pulsed)	52	52 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	90	25	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	4		A
E_{AS}	Single pulse avalanche energy (starting T_j = 25°C, I_D = I_{AR}, V_{DD} = 50 V)	200		mJ
dv/dt (3)	Peak diode recovery voltage slope	15		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; Tc = 25 °C)		2500	V
T_{stg}	Storage temperature	- 55 to 50		°C
T_j	Max. operating junction temperature	150		°C

1. Limited only by maximum temperature allowed.
2. Pulse width limited by safe operating area.
3. I_{SD} ≤13 A, di/dt ≤400 A/µs, V_{Peak} < $V_{(BR)DSS}$, V_{DD} = 400 V.

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		DPAK	D²PAK	TO-220	TO-220FP	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.39			5	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max			62.5		°C/W
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb max	50	30			°C/W
T_l	Maximum lead temperature for soldering purpose	300				°C

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	550			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 6.5 A		0.18	0.24	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	1352 38 3.7	-	pF pF pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 440 V	-	98	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	35	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	1.7	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 440 V, I_D = 6.5 A, V_{GS} = 10 V (see *Figure 19*)	-	31 6.3 14	-	nC nC nC

1. $C_{oss\ eq.}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. $C_{oss\ eq.}$ energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(off)}$	Turn-off delay time	V_{DD} = 400 V, I_D = 9 A,	-	29	-	ns
t_r	Rise time	R_G = 4.7 Ω, V_{GS} = 10 V		9.5		ns
t_c	Cross time	(see *Figure 18*, *Figure 23*)		23		ns
t_f	Fall time			13		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		13	A
I_{SDM} (1)	Source-drain current (pulsed)				52	A
V_{SD} (2)	Forward on voltage	I_{SD} = 13 A, V_{GS} = 0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 13 A, di/dt = 100 A/µs	-	238		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V (see *Figure 20*)		2.8		µC
I_{RRM}	Reverse recovery current			23.5		A
t_{rr}	Reverse recovery time	I_{SD} = 13 A, di/dt = 100 A/µs	-	278		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V, T_j = 150 °C		3.3		µC
I_{RRM}	Reverse recovery current	(see *Figure 20*)		24		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220, D²PAK

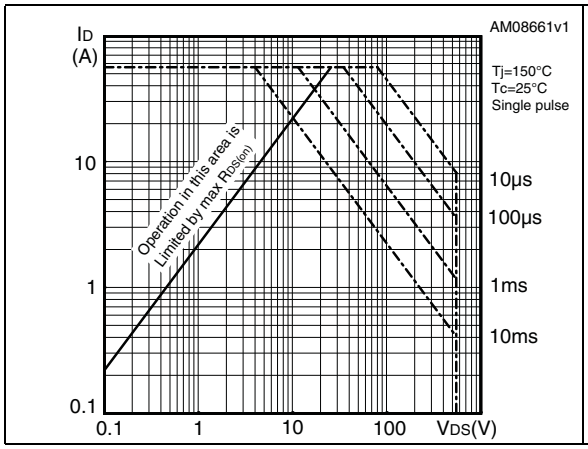


Figure 3. Thermal impedance for TO-220, D²PAK

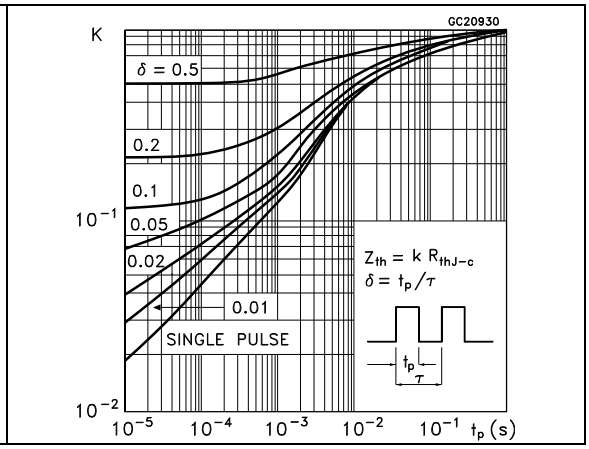


Figure 4. Safe operating area for DPAK

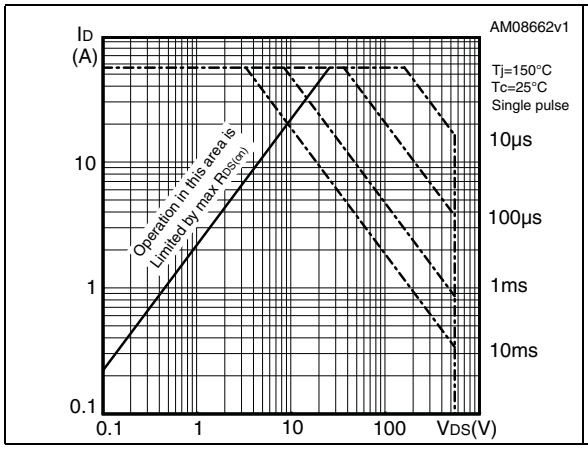


Figure 5. Thermal impedance for DPAK

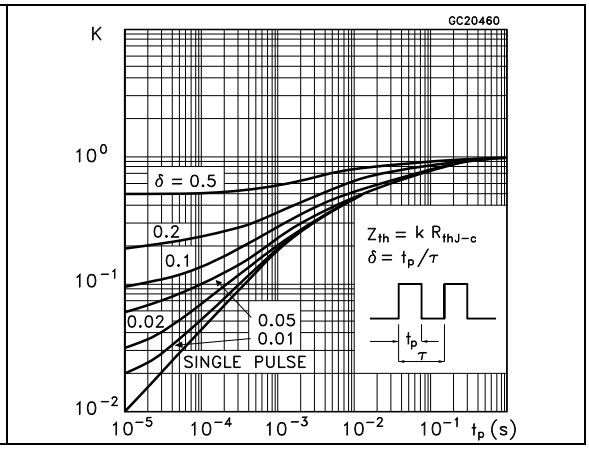


Figure 6. Safe operating area for TO-220FP

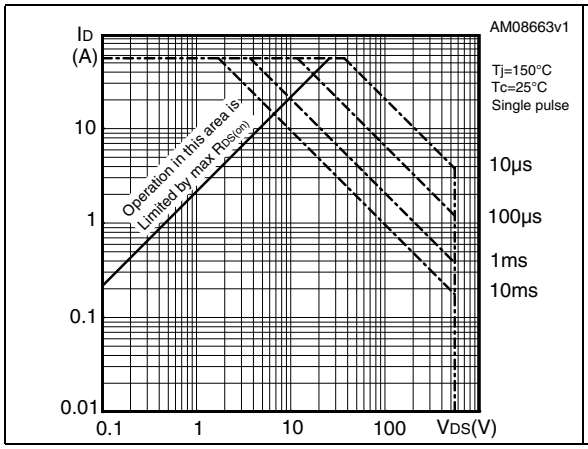


Figure 7. Thermal impedance for TO-220FP

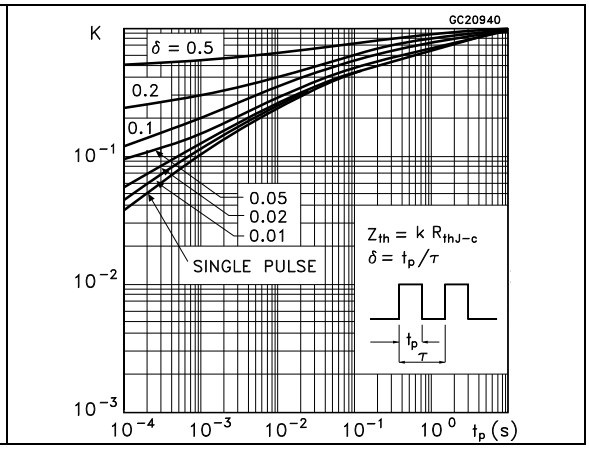


Figure 8. Output characteristics

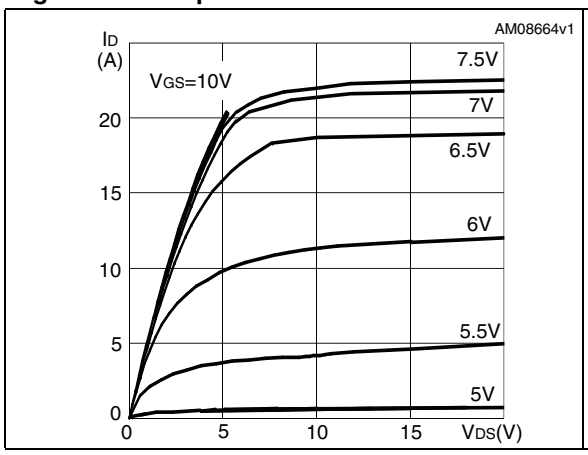


Figure 9. Transfer characteristics

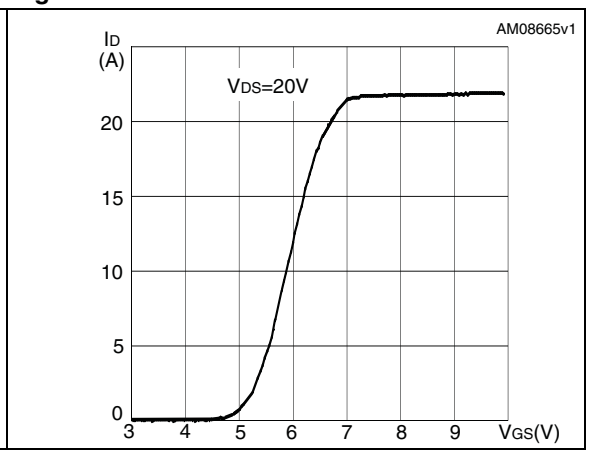


Figure 10. Gate charge vs gate-source voltage

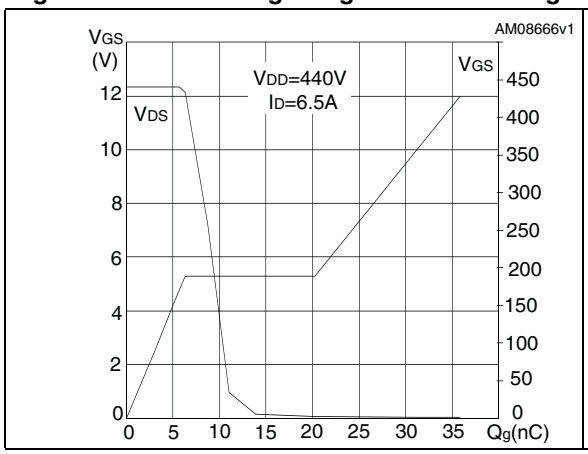


Figure 11. Static drain-source on resistance

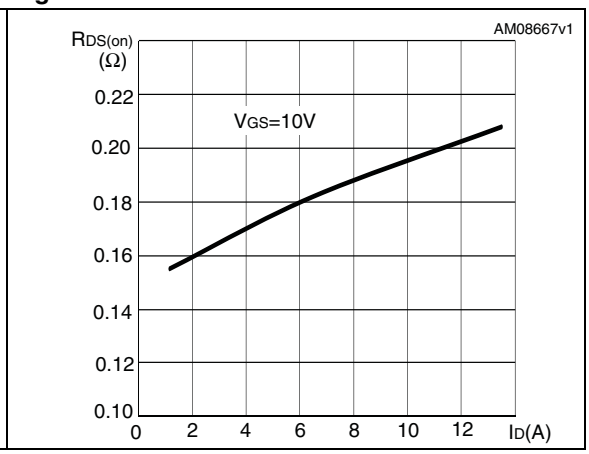


Figure 12. Capacitance variations

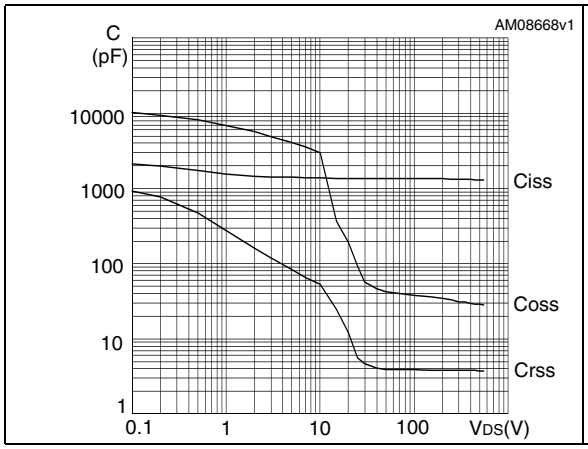


Figure 13. Output capacitance stored energy

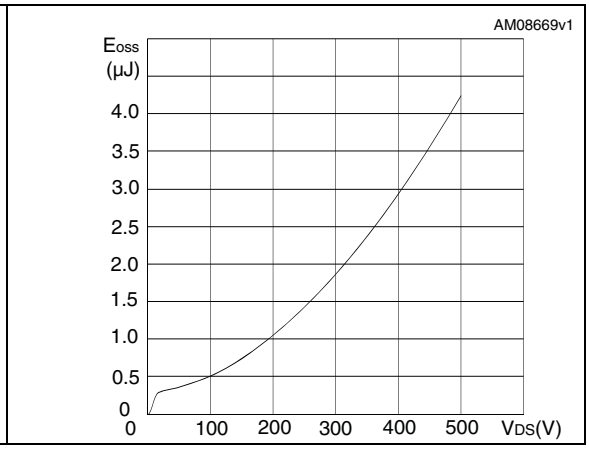


Figure 14. Normalized gate threshold voltage vs temperature

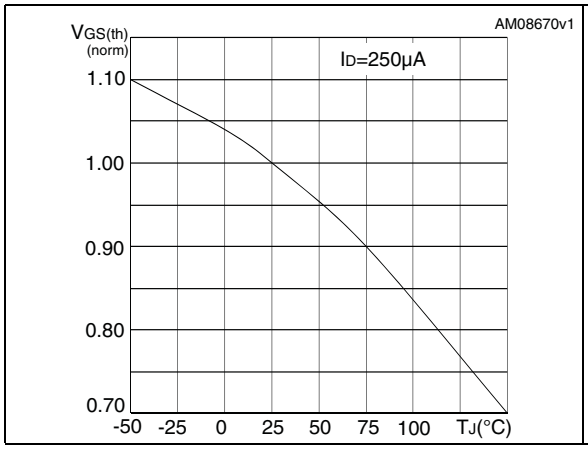


Figure 15. Normalized on resistance vs temperature

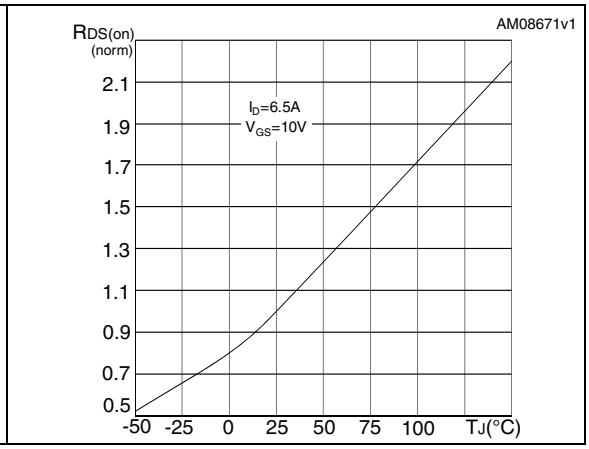


Figure 16. Switching losses vs gate resistance (1)

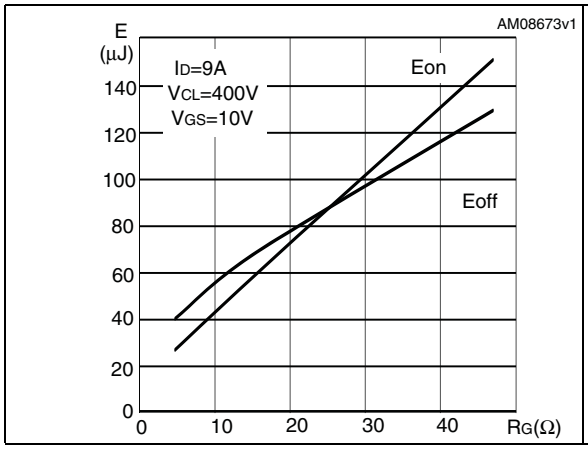
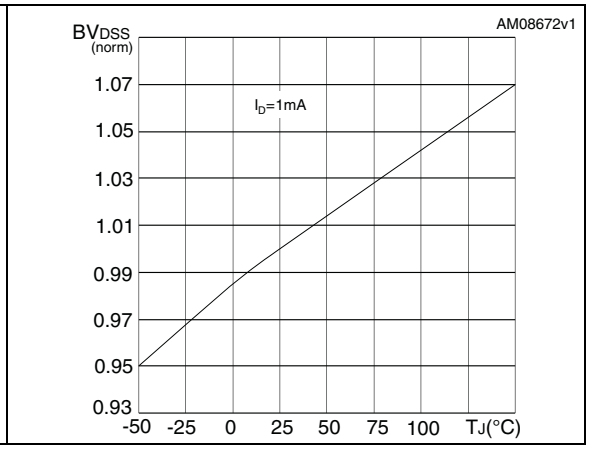


Figure 17. Normalized B_{VDSS} vs temperature



1. Eon including reverse recovery of a SiC diode

3 Test circuits

Figure 18. Switching times test circuit for resistive load

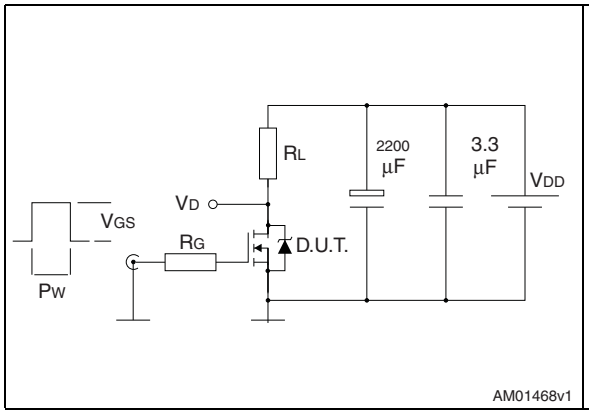


Figure 19. Gate charge test circuit

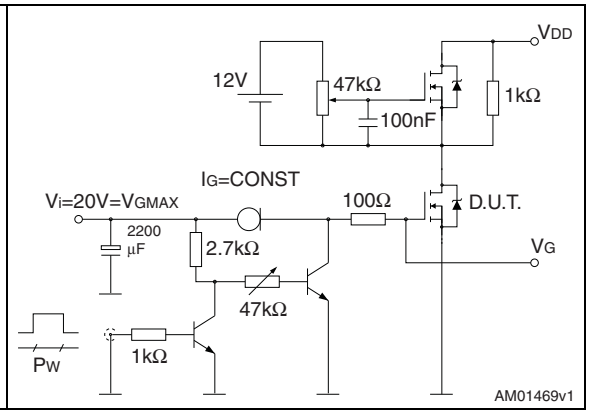


Figure 20. Test circuit for inductive load switching and diode recovery times

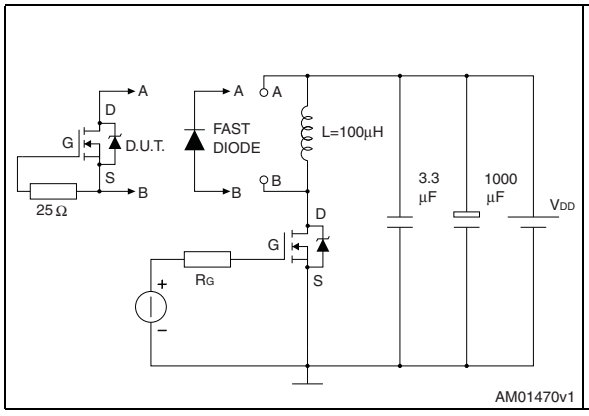


Figure 21. Unclamped inductive load test circuit

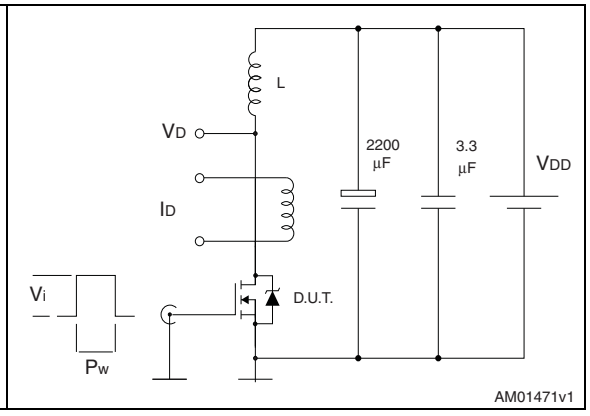


Figure 22. Unclamped inductive waveform

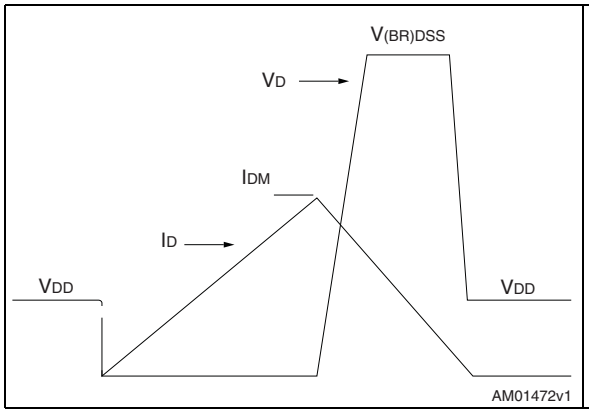
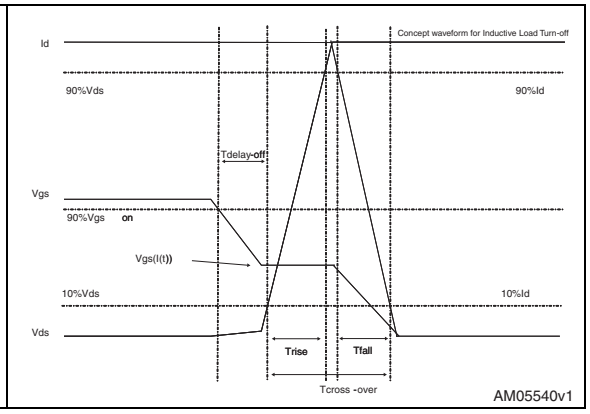


Figure 23. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 24. TO-220FP drawing

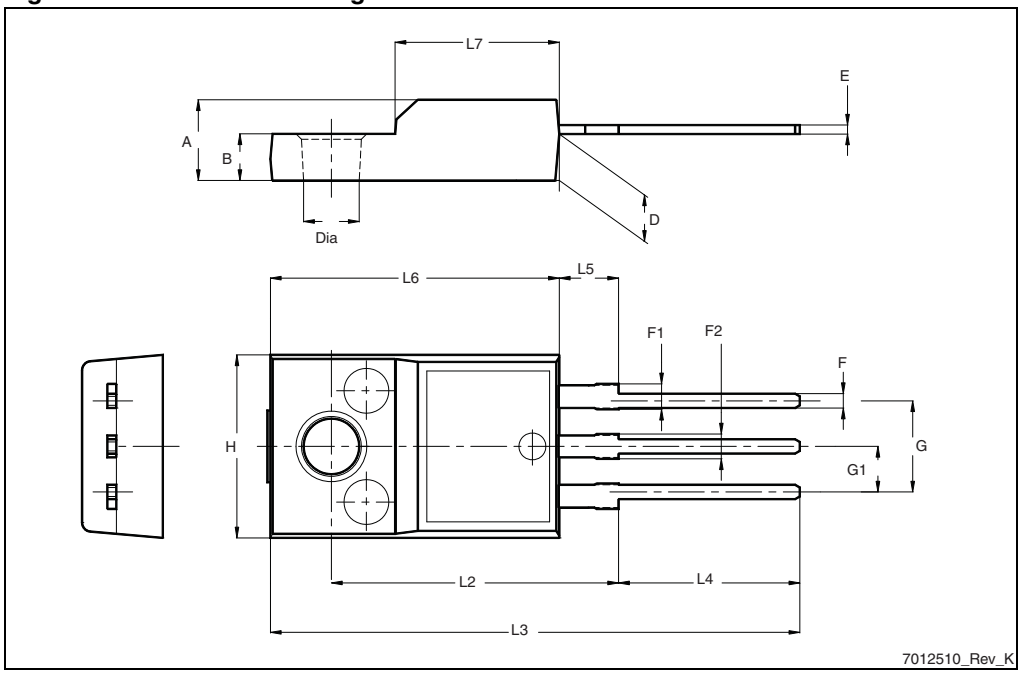
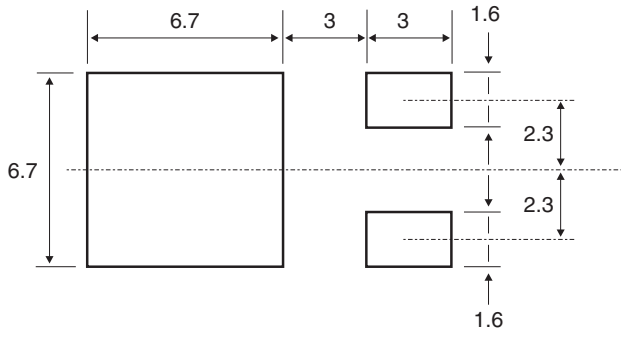


Table 9. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 25. DPAK footprint[a]



a. All dimension are in millimeters

Figure 26. DPAK (TO-252) drawing

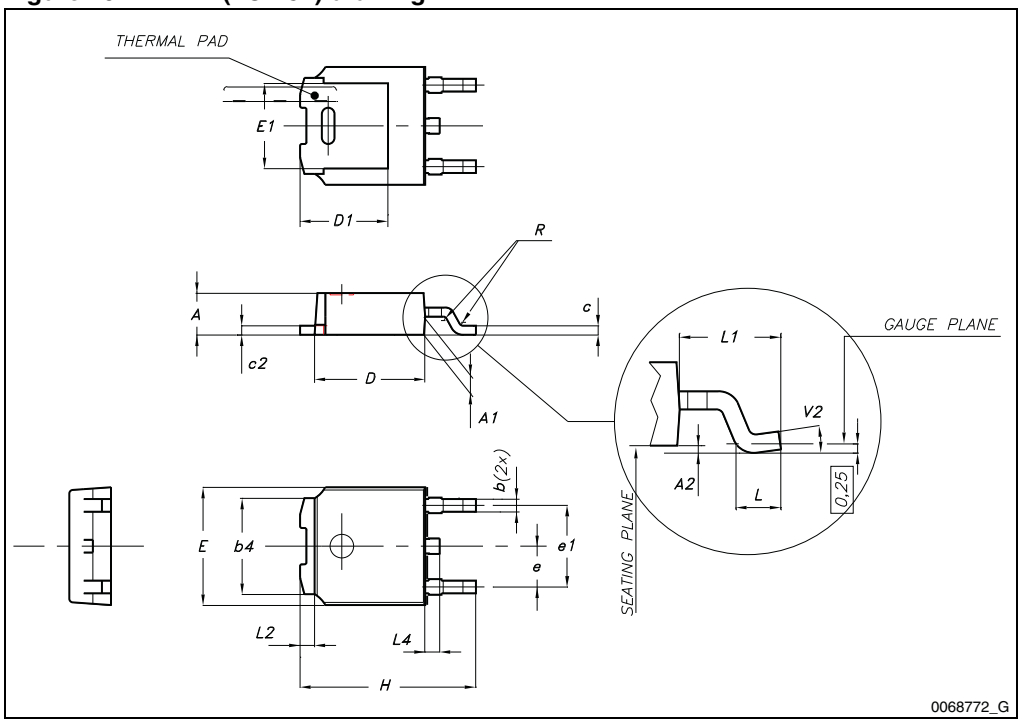


Table 10. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

Figure 27. TO-220 type A drawing

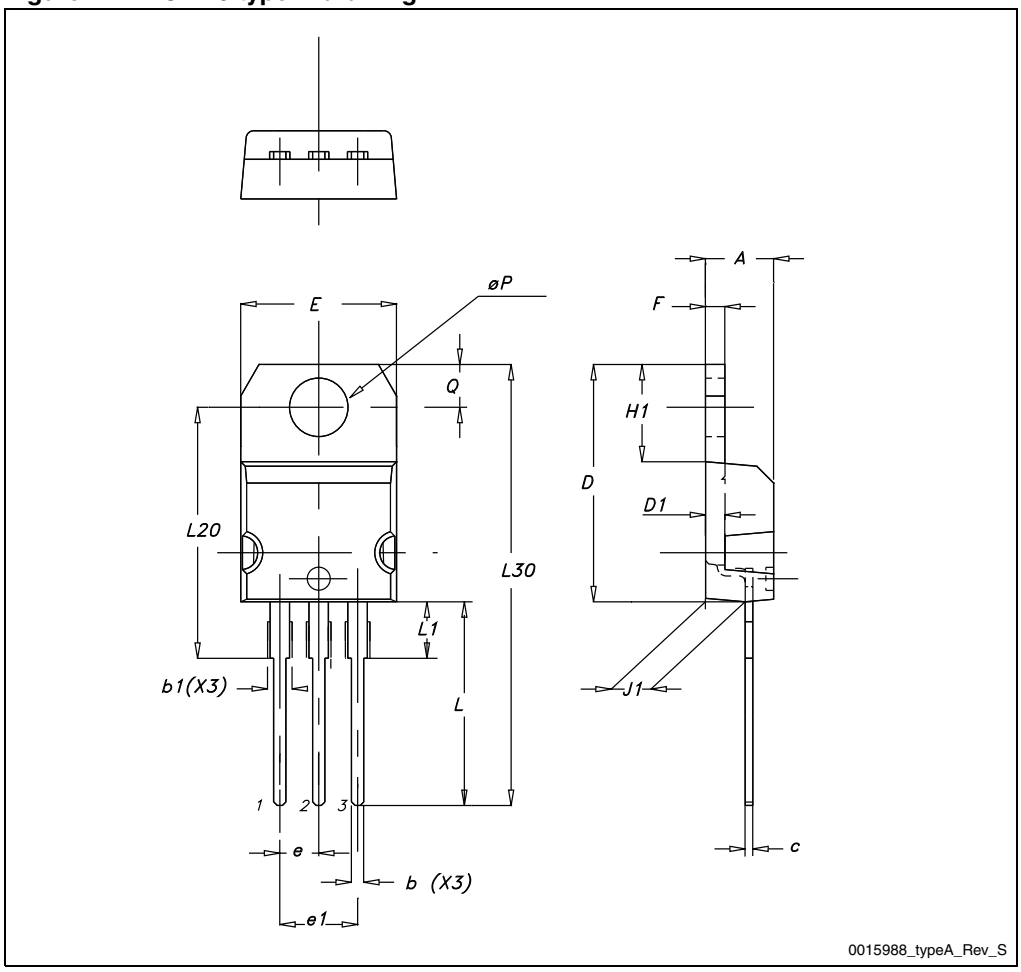


Table 11. D²PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 28. D²PAK (TO-263) drawing

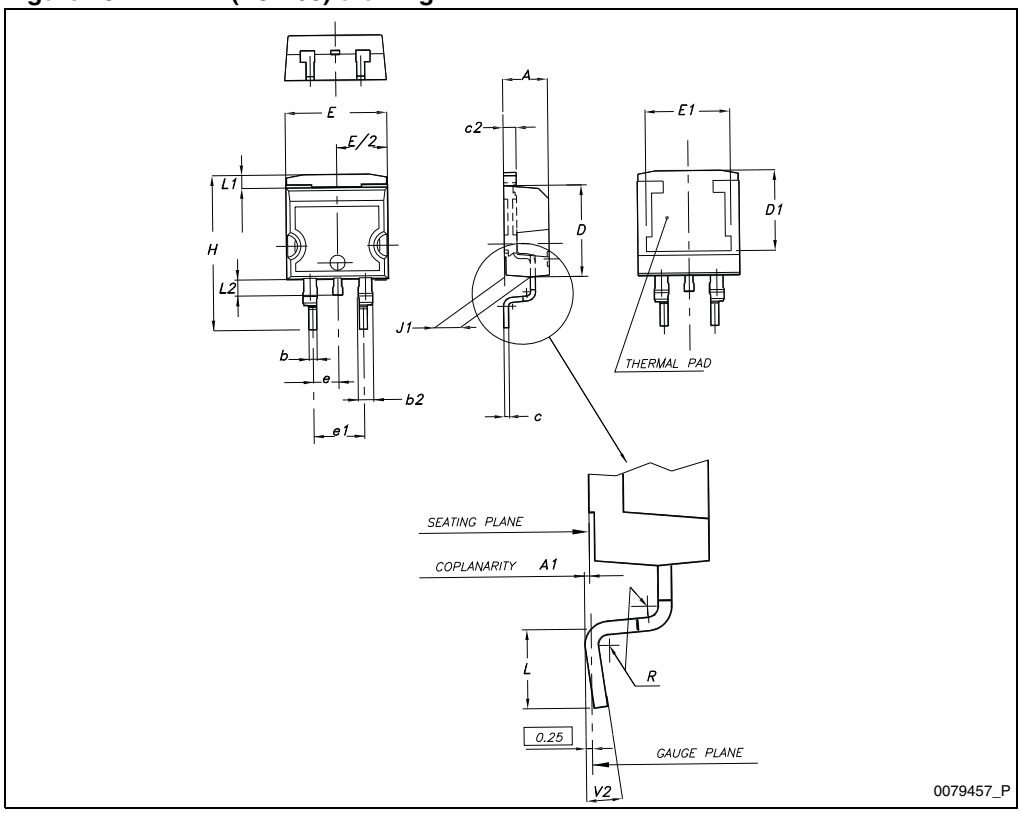
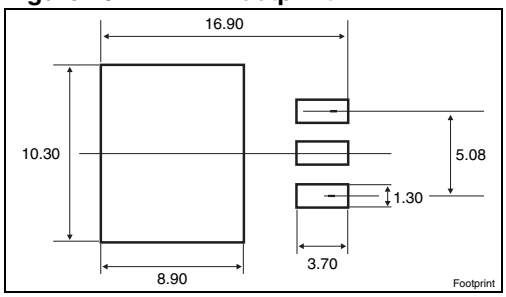


Figure 29. D²PAK footprint[b]



b. All dimension are in millimeters

5 Packaging mechanical data

Table 12. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty.		1000
P2	1.9	2.1	Bulk qty.		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Table 13. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 30. Tape for DPAK and D²PAK

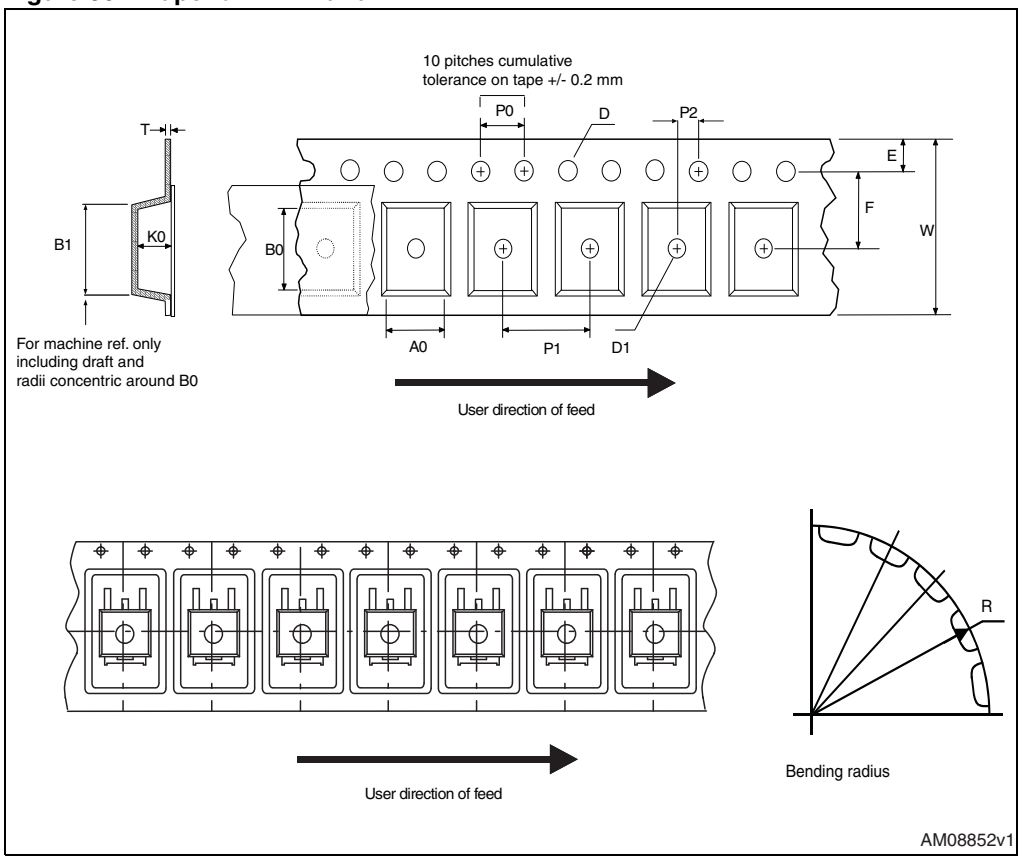
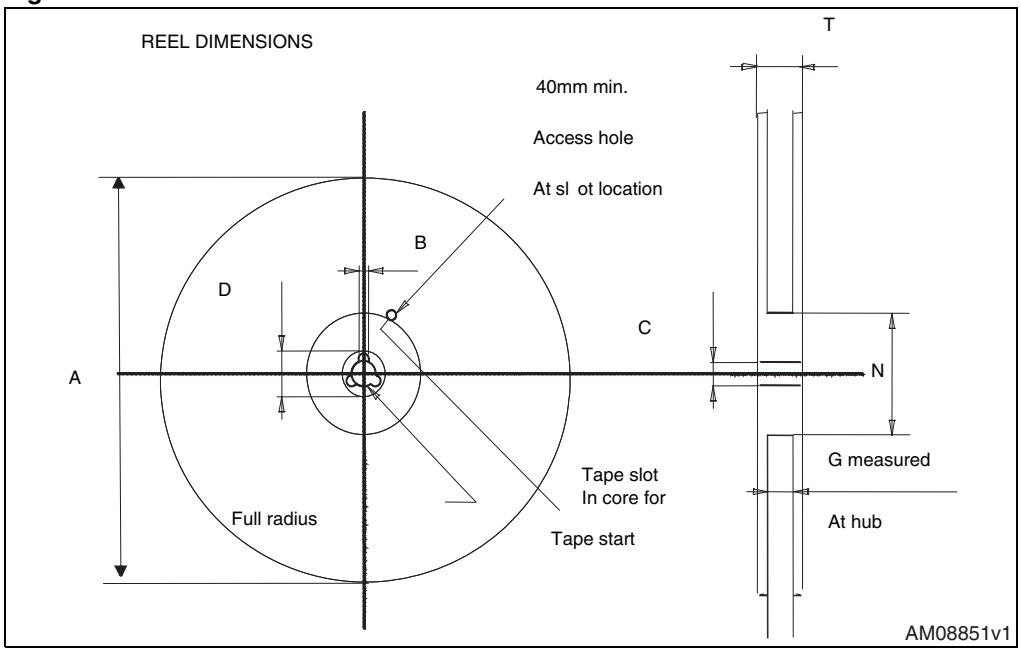


Figure 31. Reel for DPAK and D²PAK



6 Revision history

Table 14. Document revision history

Date	Revision	Changes
09-Feb-2010	1	First release.
04-Mar-2011	2	– Document status promoted from preliminary data to datasheet; – Added new package, mechanical data: D²PAK.