



STD35N3LH5

N-channel 30 V, 14 mΩ, 35 A, DPAK
STripFET™ V Power MOSFET

Preliminary data

Features

Type	V _{DSS}	R _{DS(on) max}	I _D
STD35N3LH5	30 V	< 16 mΩ	35 A

- 100% avalanche tested
- Surface mounting DPAK (TO-252)
- R_{DS(on)} * Q_g industry benchmark
- Low gate drive power losses

Applications

- Switching applications
 - Automotive

Description

This STripFET™V Power MOSFET technology is among the latest improvements, which have been especially tailored to achieve very low on-state resistance providing also one of the best-in-class figure of merit (FOM).

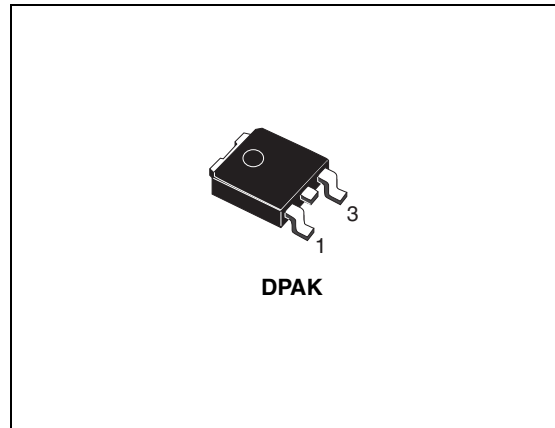


Figure 1. Internal schematic diagram

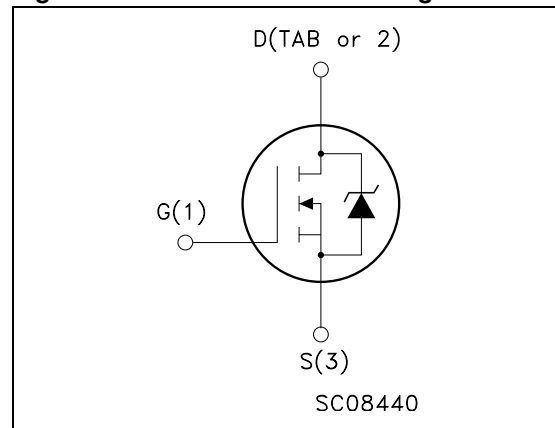


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD35N3LH5	D35N3LH5	DPAK	Tape and reel

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
3	Test circuits	6
4	Package mechanical data	7
5	Packaging mechanical data	9
6	Revision history	10

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS}=0$)	30	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	35	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	22	A
$I_{DM}^{(1)}$	Drain current (pulsed)	140	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	35	W
	Derating factor	0.23	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	TBD	V/ns
E_{AS}	Single pulse avalanche energy	TBD	mJ
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 175	$^\circ\text{C}$

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 30\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS} \leq V_{(BR)DSS}$, $T_j \leq T_{jmax}$

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	4.3	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-ambient max	50	$^\circ\text{C}/\text{W}$

1. When mounted on 1inch² FR-4 2Oz Cu board

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 250 μA, V _{GS} = 0	30			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = Max rating, V _{DS} = Max rating, T _c = 125 °C			1 10	μA μA
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = ±20 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	1		2.5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 15 A V _{GS} = 4.5 V, I _D = 15 A		14 18	16 20	mΩ mΩ

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
g _{fs} ⁽¹⁾	Forward transconductance	V _{DS} = 25 V, I _D = 15 A	-	TBD		S
C _{iSS}	Input capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0	-	725		pF
C _{oSS}	Output capacitance			135		pF
C _{rSS}	Reverse transfer capacitance			20.5		pF
Q _g	Total gate charge	V _{DD} = 15 V, I _D = 11 A	-	6	TBD	nC
Q _{gs}	Gate-source charge	V _{GS} = 4.5 V		2		nC
Q _{gd}	Gate-drain charge	Figure 3		2.1		nC

1. Pulsed: pulse duration = 300 μs, duty cycle 1.5%

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD}=20\text{ V}$, $I_D=15\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=10\text{ V}$ Figure 5	-	TBD TBD	-	ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	$V_{DD}=20\text{ V}$, $I_D=15\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=10\text{ V}$ Figure 5	-	TBD TBD	-	ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		35	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		140	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=35\text{ A}$, $V_{GS}=0$	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=35\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=20\text{ V}$, $T_j=150\text{ }^\circ\text{C}$ Figure 4	-	TBD TBD TBD		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

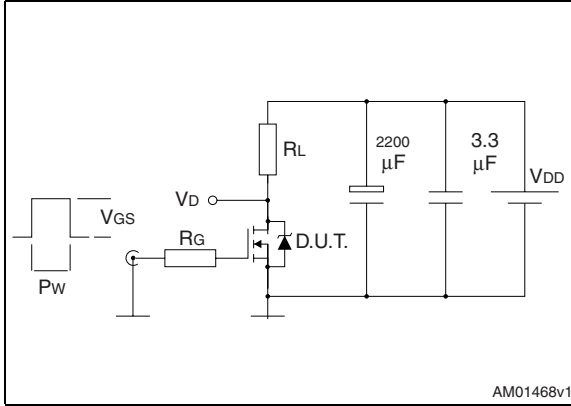


Figure 3. Gate charge test circuit

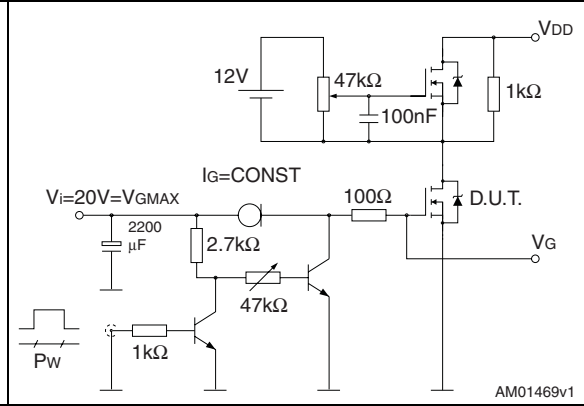


Figure 4. Test circuit for inductive load switching and diode recovery times

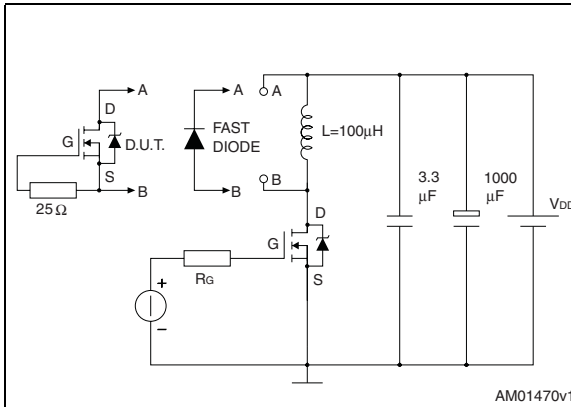


Figure 5. Unclamped inductive load test circuit

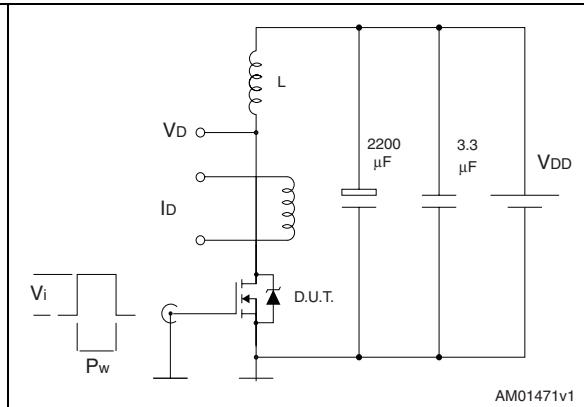


Figure 6. Unclamped inductive waveform

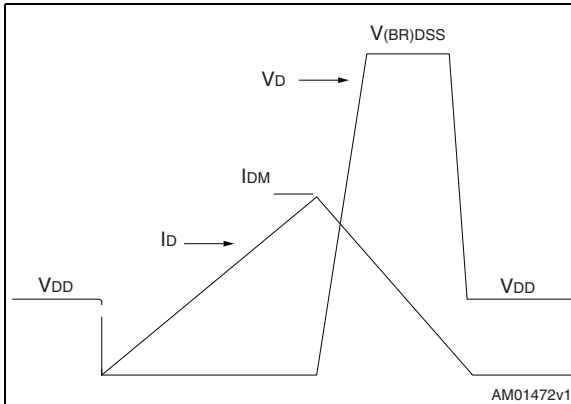
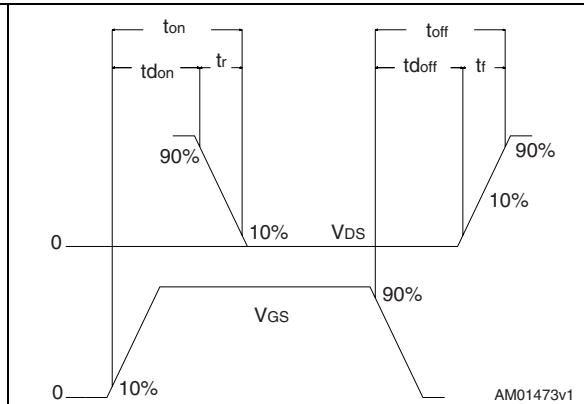


Figure 7. Switching time waveform

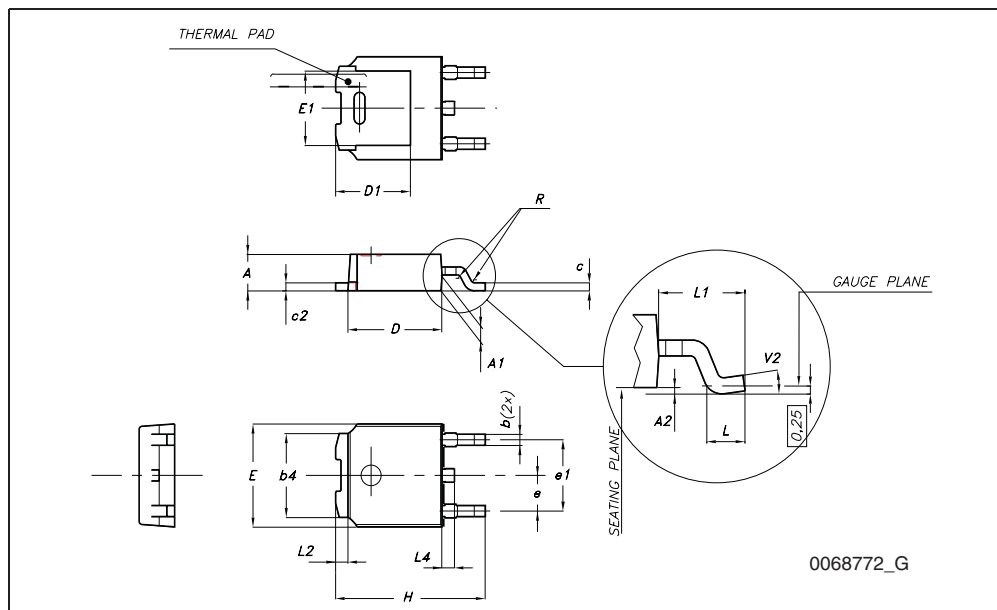


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

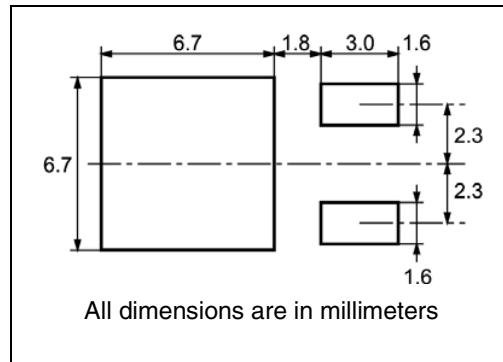
TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°



5 Packaging mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start 2.5mm min. width

G measured at hub

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

10 pitches cumulative tolerance on tape +/- 0.2 mm

Center line of cavity

User Direction of Feed

FEED DIRECTION

Bending radius

R min.

For machine ref. only including draft and radii concentric around B0

6 Revision history

Table 8. Document revision history

Date	Revision	Changes
02-Oct-2009	1	First release.

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