

August 2009
SupreMOS<sup>M</sup>

# FCA16N60N N-Channel MOSFET 600V, 16A, $0.170\Omega$

#### **Features**

- $R_{DS(on)} = 0.17\Omega$  ( Typ.)@  $V_{GS} = 10V$ ,  $I_D = 8A$
- Ultra low gate charge (Typ. Qg = 40.2nC)
- · Low effective output capacitance
- 100% avalanche tested
- · RoHS compliant

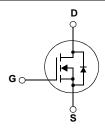


## **Description**

The SupreMOS MOSFET, Fairchild's next generation of high voltage super-junction MOSFETs, employs a deep trench filling process that differentiates it from preceding multi-epi based technologies. By utilizing this advanced technology and precise process control, SupreMOS provides world class Rsp, superior switching performance and ruggedness.

This SupreMOS MOSFET fits the industry's AC-DC SMPS requirements for PFC, server/telecom power, FPD TV power, ATX power, and industrial power applications.





# **MOSFET Maximum Ratings** $T_C = 25^{\circ}C$ unless otherwise noted\*

Symbol	Parameter			FCA16N60N	Units
V <sub>DSS</sub>	Drain to Source Voltage			600	V
V <sub>GSS</sub>	Gate to Source Voltage			±30	V
	Dunin Comment	-Continuous (T <sub>C</sub> = 25°C)		16.0	^
ID	Drain Current	-Continuous (T <sub>C</sub> = 100°C)		10.1	A
I <sub>DM</sub>	Drain Current	- Pulsed (N	Note 1)	48.0	Α
E <sub>AS</sub>	Single Pulsed Avalanche Energ	ngle Pulsed Avalanche Energy (Note 2)		355	mJ
I <sub>AR</sub>	Avalanche Current			5.3	Α
E <sub>AR</sub>	Repetitive Avalanche Energy	nche Energy		1.34	mJ
al. (/alt	MOSFET dv/dt Ruggedness			100	V/ns
dv/dt	Peak Diode Recovery dv/dt	1)	Note 3)	20	V/ns
Б	Daniel Diaglantia	$(T_C = 25^{\circ}C)$		134.4	W
$P_D$	Power Dissipation	- Derate above 25°C		1.08	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temper	ature Range		-55 to +150	°C
T <sub>L</sub>	Maximum Lead Temperature for 1/8" from Case for 5 Seconds	or Soldering Purpose,		300	°C

<sup>\*</sup>Drain current limited by maximum junction temperature

## **Thermal Characteristics**

Symbol	Parameter	FCA16N60N	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.93	
$R_{\theta CS}$	Thermal Resistance, Case to Heat Sink (Typical)	0.24	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	40	

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# **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCA16N60N	FCA16N60N	TO-3PN	-	-	30

# **Electrical Characteristics** $T_C = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
Off Charac	cteristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 1 \text{mA}, V_{GS} = 0 \text{V}, T_C = 25^{\circ} \text{C}$	600	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 1mA, Referenced to 25°C	-	0.73	-	V/°C
Jana Cata Valtana Dunin Current	Zoro Cata Valtaga Prain Current	V <sub>DS</sub> = 480V, V <sub>GS</sub> = 0V	-	-	10	
IDSS	Zero Gate Voltage Drain Current	$V_{DS} = 480V, V_{GS} = 0V, T_{C} = 125^{\circ}C$	-	-	100	μΑ
I <sub>GSS</sub>	Gate to Body Leakage Current	$V_{GS} = \pm 30V, V_{DS} = 0V$	-	-	±100	nA

#### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2.0	-	4.0	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS} = 10V, I_D = 8A$	-	0.170	0.199	Ω
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = 40V, I_{D} = 8A$	-	20	-	S

## **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	1001/1/	-	1630	2170	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V — f = 1MHz		70	95	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 11/11/2	-	5	10	pF
C <sub>oss</sub>	Output Capacitance	$V_{DS} = 380V, V_{GS} = 0V, f = 1MHz$	-	40	60	pF
C <sub>oss</sub> eff.	Effective Output Capacitance	V <sub>DS</sub> = 0V to 480V, V <sub>GS</sub> = 0V		176	-	pF
Q <sub>g(tot)</sub>	Total Gate Charge at 10V		-	40.2	52.3	nC
Q <sub>gs</sub>	Gate to Source Gate Charge	$V_{DS} = 380V, I_{D} = 8A,$		6.7	-	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge	V <sub>GS</sub> = 10V (Note 4)	-	12.9	-	nC
ESR	Equivalent Series Resistance (G-S)	Drain Open		2.9		Ω

## **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time			-	15.8	41.6	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{DD} = 380V, I_{D} = 8A$		-	15.5	41.0	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$R_G = 4.7\Omega$		-	60.3	130.6	ns
t <sub>f</sub>	Turn-Off Fall Time		(Note 4)	-	20.2	50.4	ns

#### **Drain-Source Diode Characteristics**

$I_S$	Maximum Continuous Drain to Source Diode Forward Current			-	16	Α
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current			-	48	Α
$V_{SD}$	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 8A	-	-	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 8A	-	319	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	$dI_F/dt = 100A/\mu s$	-	4.4	-	μС

#### Notes

- 1. Repetitive Rating: Pulse width limited by maximum junction temperature
- 2.  $I_{AS}$  = 5.3A,  $R_G$  = 25 $\Omega$ , Starting  $T_J$  = 25 $^{\circ}$ C
- 3. I  $_{SD} \leq$  16A, di/dt  $\leq$  200A/µs, V  $_{DD}$  = 380V, Starting T  $_{J}$  = 25°C
- 4. Essentially Independent of Operating Temperature Typical Characteristics

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# **Typical Performance Characteristics**

Figure 1. On-Region Characteristics

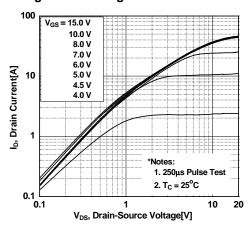


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

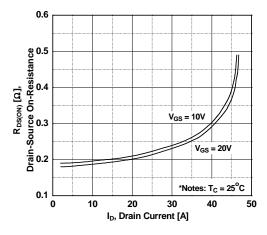


Figure 5. Capacitance Characteristics

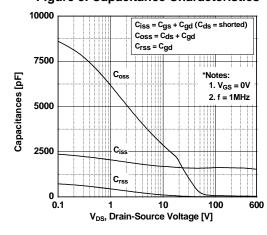


Figure 2. Transfer Characteristics

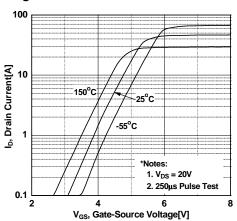


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

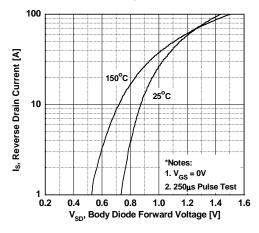
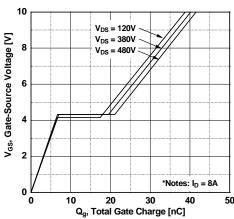


Figure 6. Gate Charge Characteristics



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# **Typical Performance Characteristics (Continued)**

Figure 7. Breakdown Voltage Variation vs. Temperature

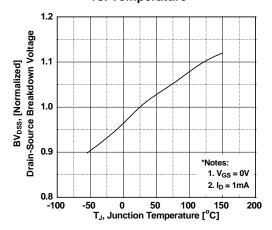


Figure 8. On-Resistance Variation vs. Temperature

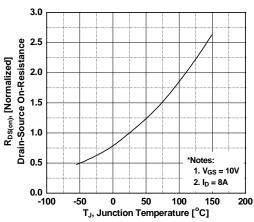


Figure 9. Maximum Safe Operating Area

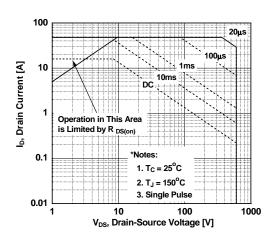


Figure 10. Maximum Drain Current vs. Case Temperature

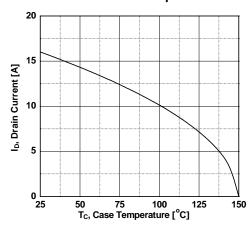
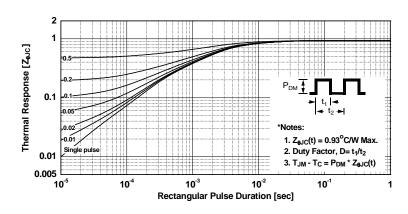
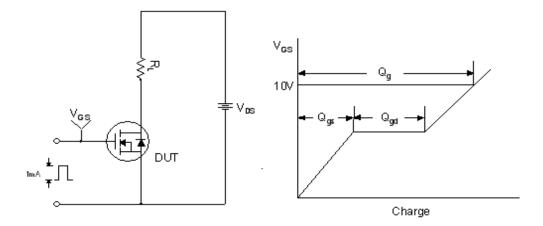


Figure 11. Transient Thermal Response Curve

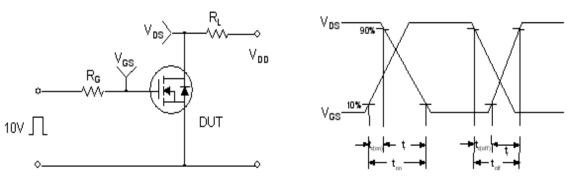


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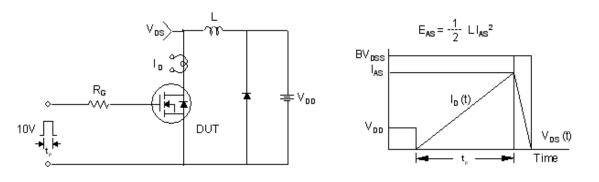
## **Gate Charge Test Circuit & Waveform**



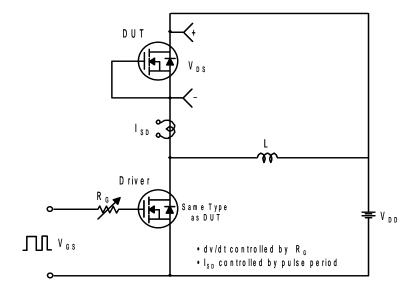
### **Resistive Switching Test Circuit & Waveforms**

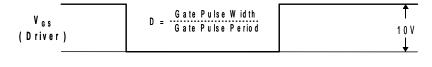


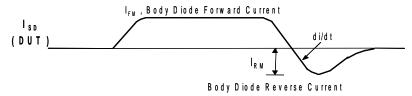
# **Unclamped Inductive Switching Test Circuit & Waveforms**

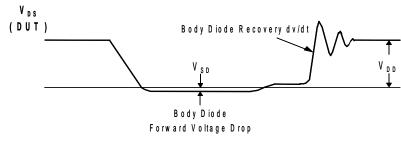


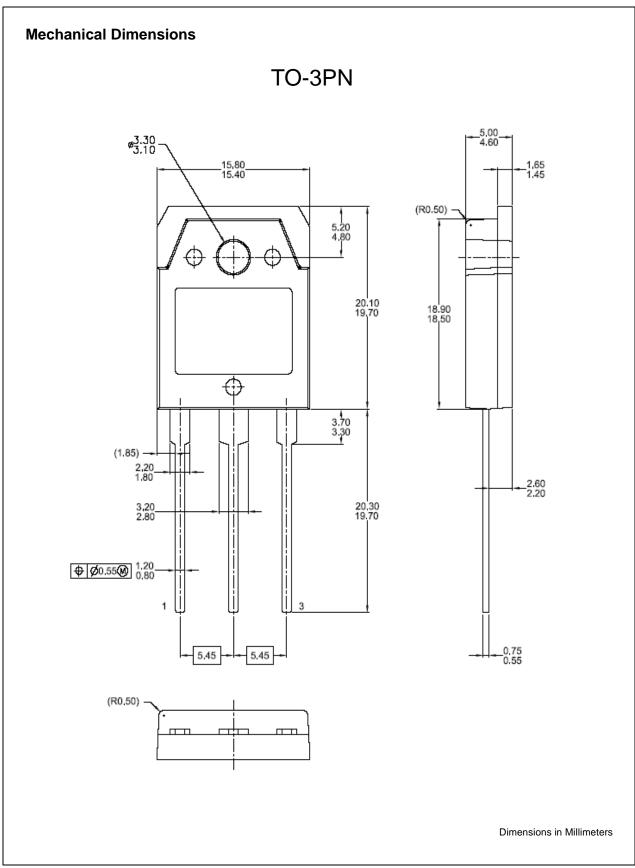
# Peak Diode Recovery dv/dt Test Circuit & Waveforms















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