

FDP6N60ZU / FDPF6N60ZUT N-Channel MOSFET, FRFET 600V, 4.5A, 2Ω

Features

- $R_{DS(on)} = 1.7\Omega$ (Typ.) @ $V_{GS} = 10V$, $I_D = 2.25A$
- Low gate charge (Typ. 14.5nC)
- Low C_{rss} (Typ. 5pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

GDS

RoHS compliant

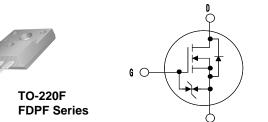


GDS

Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies and active power factor correction.



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted*

TO-220

FDP Series

Symbol		FDP6N60ZU	FDPF6N60ZUT	Units			
V _{DSS}	Drain to Source Voltage			600		V	
V _{GSS}	Gate to Source Voltage			±30		V	
ID	Drain Current	-Continuous ($T_C = 25^{\circ}C$)		4.5	4.5*		
		-Continuous ($T_c = 100^{\circ}C$)		2.7	2.7*	A	
I _{DM}	Drain Current	- Pulsed (Note 1)		18	18*	А	
E _{AS}	Single Pulsed Avalanche Energy		(Note 2)	150		mJ	
I _{AR}	Avalanche Current		(Note 1)	4.5		А	
E _{AR}	Repetitive Avalanche Energy		(Note 1)	10.5		mJ	
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	20		V/ns	
P _D	Deven Dissingtion	$(T_{\rm C} = 25^{\rm o}{\rm C})$		105	33.8	W	
	Power Dissipation	- Derate above 25°C		0.85	0.27	W/ºC	
T _J , T _{STG}	Operating and Storage Temperature Range			-55 to +150		°C	
TL	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds			300		°C	

Symbol	Parameter	FDP6N60ZU	FDPF6N60ZUT	Units
$R_{ ext{ heta}JC}$	Thermal Resistance, Junction to Case	1.2	3.7	
R_{\thetaCS}	Thermal Resistance, Case to Sink Typ.	0.5	-	°C/W
R_{\thetaJA}	Thermal Resistance, Junction to Ambient	62.5	62.5	

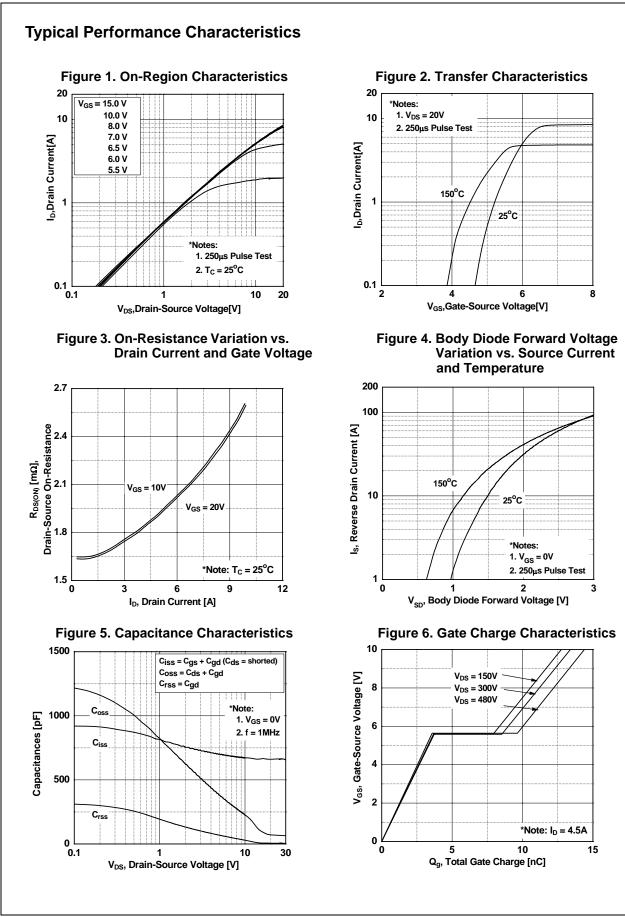
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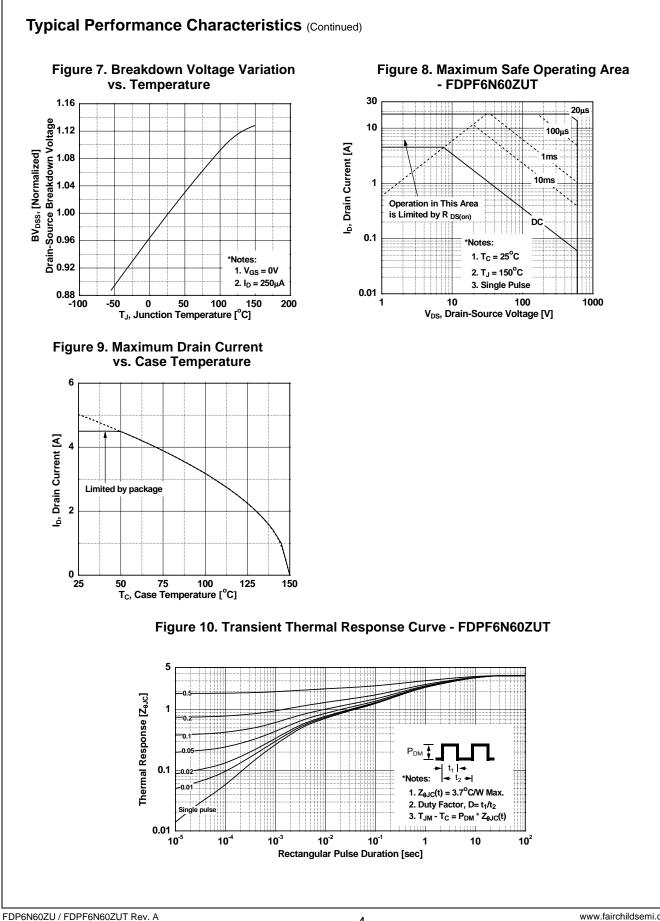
Device Marking		Device	Package	e	Reel Size	Таре	e Width		Quantit	у
FDP6N6	0ZU	FDP6N60ZU	TO-220		-		-		50	
FDPF6N60ZUT FDPF6N60ZUT TO-2		TO-220F	=	-		-		50		
Electrica	l Char	acteristics T _c =	25°C unless o	otherwise r	noted					
Symbol		Parameter		Test Conditions		Min.	Тур.	Max.	Units	
Off Charac	teristic	s								
BV _{DSS}	Drain to	o Source Breakdown Vo	oltage	I _D = 250μA, V _{GS} = 0V, T _J = 25 ^o C		600	-	-	V	
$\frac{\Delta BV_{DSS}}{\Delta T_{,l}}$	Breakdown Voltage Temperature Coefficient		Iro	$I_D = 250 \mu$ A, Referenced to 25°C		-	0.75	-	V/°C	
<u> </u>			$V_{DS} = 600$	0V, V _{GS} = 0V		-	-	25		
IDSS	∠ero G	ate Voltage Drain Curre	nt L	$V_{DS} = 480V, T_{C} = 125^{\circ}C$			-	-	250	μA
I _{GSS}	Gate to	Body Leakage Current			$VV, V_{DS} = 0V$		-	-	±10	μΑ
On Charac	teristic	S								
V _{GS(th)}	Gate Threshold Voltage			$V_{GS} = V_{DS}, I_{D} = 250 \mu A$			3.0	-	5.0	V
R _{DS(on)}	Static D	c Drain to Source On Resistance		$V_{GS} = 10V, I_D = 2.25A$		-	1.7	2.0	Ω	
9 _{FS}	Forward Transconductance			V _{DS} = 40V, I _D = 2.25A		-	3.5	-	S	
Dynamic C _{Ciss}		eristics apacitance					-	650	865	pF
C _{oss}	Output	Capacitance		V _{DS} = 25V, V _{GS} = 0V f = 1MHz		-	75	100	pF	
C _{rss}	Revers	e Transfer Capacitance				-	5	10	pF	
Q _g	Total G	Total Gate Charge at 10V Gate to Source Gate Charge Gate to Drain "Miller" Charge					-	14.5	20	nC
Q _{gs}	Gate to			$V_{DS} = 480V, I_D = 4.5A$ $V_{GS} = 10V$ (Note 4)		-	4	-	nC	
Q _{gd}	Gate to					-	6	-	nC	
Switching	Charac	teristics		<u>.</u>		<u>.</u>	L.			
t _{d(on)}	Turn-On Delay Time					-	19	48	ns	
t _r		n-On Rise Time		V _{DD} = 300V, I _D = 4.5A		-	25	60	ns	
t _{d(off)}		ff Delay Time		$R_{G} = 25\Omega, V_{GS} = 10V$		-	-	25	60	ns
t _f		Furn-Off Fall Time		(Note 4)		(Note 4)	-	45	100	ns
Drain-Sou	ce Dio	de Characteristic	S							
I _S		Im Continuous Drain to	-	Forward (Current		-	-	4.5	Α
I _{SM}	Maximu	Aaximum Pulsed Drain to Source Diode Fo				-	-	18	Α	
V _{SD}	Drain to	Source Diode Forward	l Voltage	$V_{GS} = 0V, I_{SD} = 4.5A$		-	-	1.6	V	
t _{rr}	Reverse	e Recovery Time			, I _{SD} = 4.5A		-	36	-	ns
Q _{rr}	Daviana	e Recovery Charge		$dI_{F}/dt = 100A/\mu s$		-	37	-	nC	

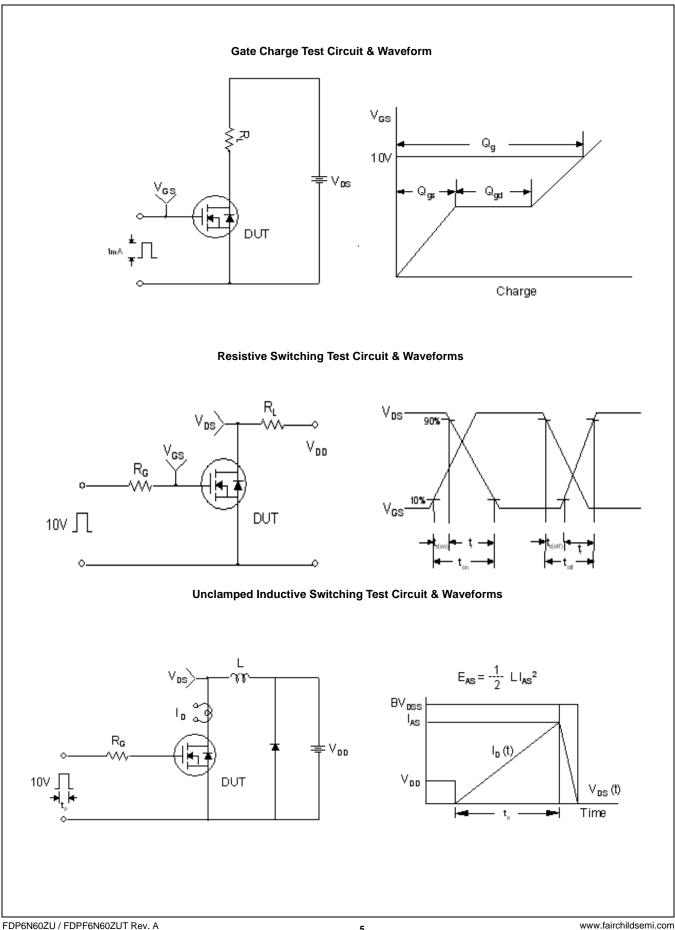
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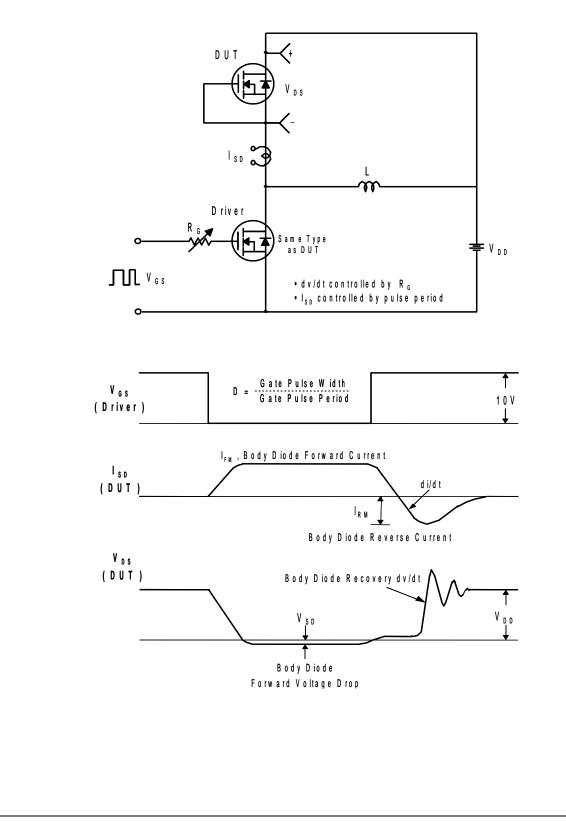


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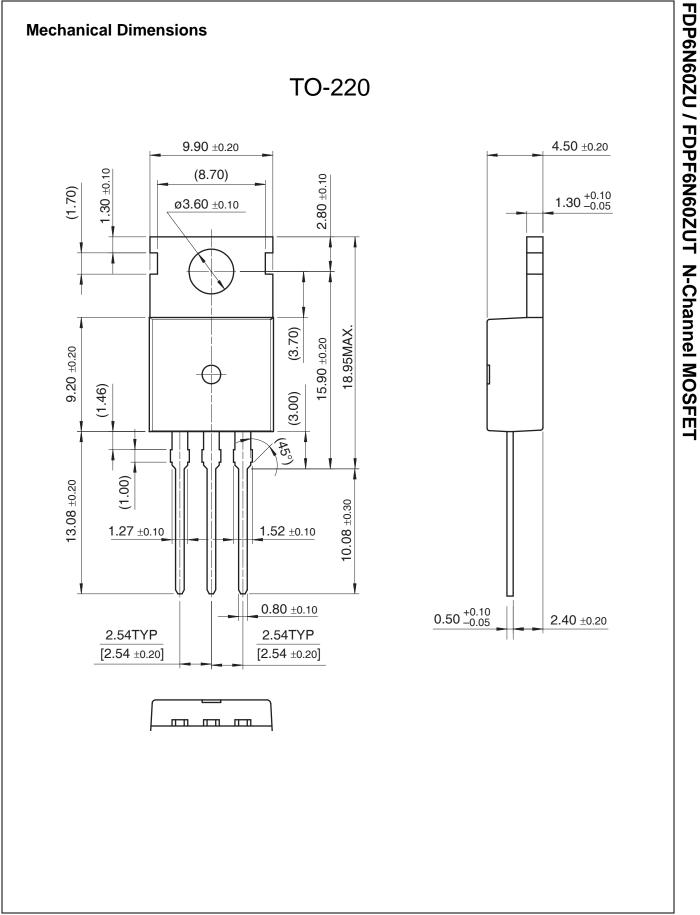




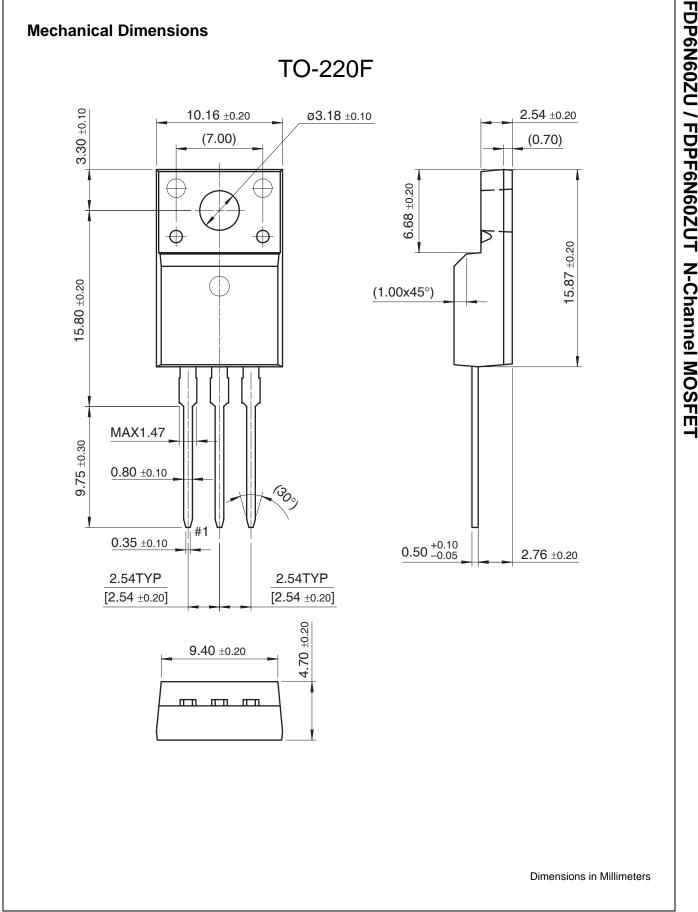
Peak Diode Recovery dv/dt Test Circuit & Waveforms



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