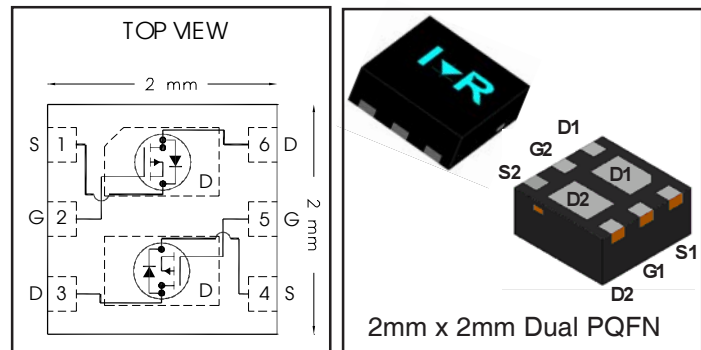


# IRFHS9351PbF

HEXFET® Power MOSFET

$V_{DS}$	<b>-30</b>	<b>V</b>
$V_{GS\ max}$	<b>±20</b>	<b>V</b>
$R_{DS(on)\ max}$ (@ $V_{GS} = -10V$ )	<b>170</b>	<b>mΩ</b>
$I_D$ (@ $T_C = 25^\circ C$ )	<b>-3.4</b> ②	<b>A</b>



## Applications

- Charge and Discharge Switch for Battery Application
- System/load switch

## Features and Benefits

### Features

Low $R_{DSon}$ ( $\leq 170m\Omega$ )
Low Thermal Resistance to PCB ( $\leq 19^\circ C/W$ )
Low Profile ( $\leq 1.0\ mm$ )
Compatible with Existing Surface Mount Techniques
RoHS Compliant Containing no Lead, no Bromide and no Halogen
MSL1, Consumer Qualification

results in

### Benefits

Lower Conduction Losses
Enable better thermal dissipation
Increased Power Density
Easier Manufacturing
Environmentally Friendlier
Increased Reliability

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRFHS9351TRPBF	PQFN 2mm x 2mm	Tape and Reel	4000	
IRFHS9351TR2PBF	PQFN 2mm x 2mm	Tape and Reel	400	

## Absolute Maximum Ratings

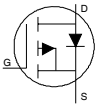
	Parameter	Max.	Units
$V_{DS}$	Drain-to-Source Voltage	-30	V
$V_{GS}$	Gate-to-Source Voltage	± 20	
$I_D$ @ $T_A = 25^\circ C$	Continuous Drain Current, $V_{GS}$ @ -10V	-2.3	A
$I_D$ @ $T_A = 70^\circ C$	Continuous Drain Current, $V_{GS}$ @ -10V	-1.5	
$I_D$ @ $T_C = 25^\circ C$	Continuous Drain Current, $V_{GS}$ @ -10V	-5.1 ②	
$I_D$ @ $T_C = 70^\circ C$	Continuous Drain Current, $V_{GS}$ @ -10V	-4.1 ②	
$I_D$ @ $T_C = 25^\circ C$	Continuous Drain Current, $V_{GS}$ @ 10V (Package Limited)	-3.4 ②	
$I_{DM}$	Pulsed Drain Current ①	-20	
$P_D$ @ $T_A = 25^\circ C$	Power Dissipation ④	1.4	W
$P_D$ @ $T_A = 70^\circ C$	Power Dissipation ④	0.9	
	Linear Derating Factor	0.01	W/°C
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Notes ① through ⑥ are on page 2

## Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	-30	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$V_{DSS}/T_J$	Breakdown Voltage Temp. Coefficient	—	0.02	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = -1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	135	170	m	$V_{GS} = -10V, I_D = -3.1A$ ③
		—	235	290		$V_{GS} = -4.5V, I_D = -2.5A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	-1.3	-1.8	-2.4	V	$V_{DS} = V_{GS}, I_D = -10\mu A$
$V_{GS(th)}$	Gate Threshold Voltage Coefficient	—	-4.6	—	mV/ $^\circ\text{C}$	
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	-1.0	$\mu A$	$V_{DS} = -24V, V_{GS} = 0V$
		—	—	-150		$V_{DS} = -24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -20V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = 20V$
$g_{fs}$	Forward Transconductance	2.4	—	—	S	$V_{DS} = -10V, I_D = -3.1A$
$Q_g$	Total Gate Charge ⑥	—	1.9	—	nC	$V_{DS} = -15V, V_{GS} = -4.5V, I_D = -3.1A$
$Q_g$	Total Gate Charge ⑥	—	3.7	—	nC	$V_{GS} = -10V$ $V_{DS} = -15V$ $I_D = -3.1A$
$Q_{gs}$	Gate-to-Source Charge ⑥	—	0.6	—		
$Q_{gd}$	Gate-to-Drain Charge ⑥	—	1.1	—		
$R_G$	Gate Resistance ⑥	—	17	—		
$t_{d(on)}$	Turn-On Delay Time	—	8.3	—	ns	$V_{DD} = -15V, V_{GS} = -4.5V$ ③ $I_D = -3.1A$ $R_G = 1.8$ See Figs. 19a & 19b
$t_r$	Rise Time	—	30	—		
$t_{d(off)}$	Turn-Off Delay Time	—	6.3	—		
$t_f$	Fall Time	—	7.9	—		
$C_{iss}$	Input Capacitance	—	160	—	pF	$V_{GS} = 0V$ $V_{DS} = -25V$ $f = 1.0\text{KHz}$
$C_{oss}$	Output Capacitance	—	39	—		
$C_{rss}$	Reverse Transfer Capacitance	—	26	—		

## Diode Characteristics

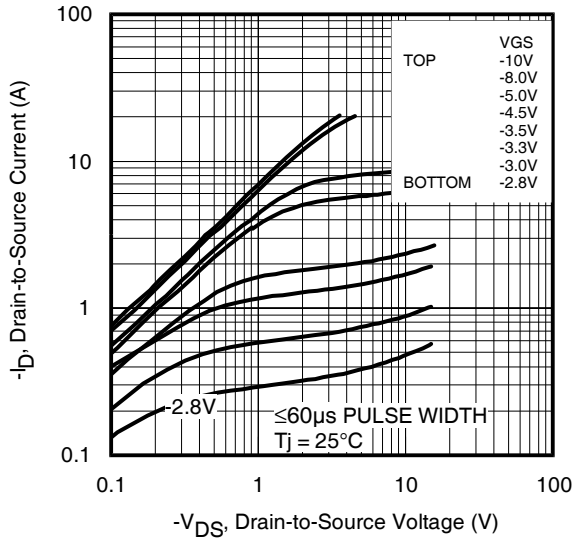
	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	-5.1	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	-20		
$V_{SD}$	Diode Forward Voltage	—	—	-1.2	V	$T_J = 25^\circ\text{C}, I_S = -3.1A, V_{GS} = 0V$ ③
$t_{rr}$	Reverse Recovery Time	—	20	30	ns	$T_J = 25^\circ\text{C}, I_F = -3.1A, V_{DD} = -15V$
$Q_{rr}$	Reverse Recovery Charge	—	42	63	nC	$di/dt = 370/\mu s$ ③

## Thermal Resistance

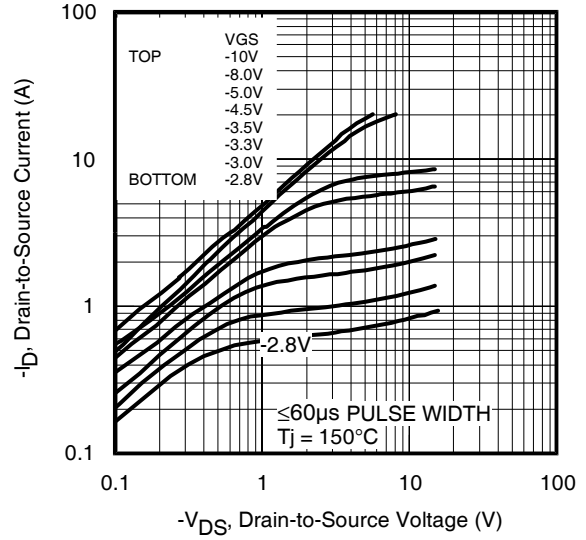
	Parameter	Typ.	Max.	Units
$R_{JC}$ (Bottom)	Junction-to-Case ②	—	19	$^\circ\text{C/W}$
$R_{JC}$ (Top)	Junction-to-Case ②	—	170	
$R_{JA}$	Junction-to-Ambient ④	—	90	
$R_{JA}$	Junction-to-Ambient ( $t < 10s$ ) ④	—	75	

### Notes:

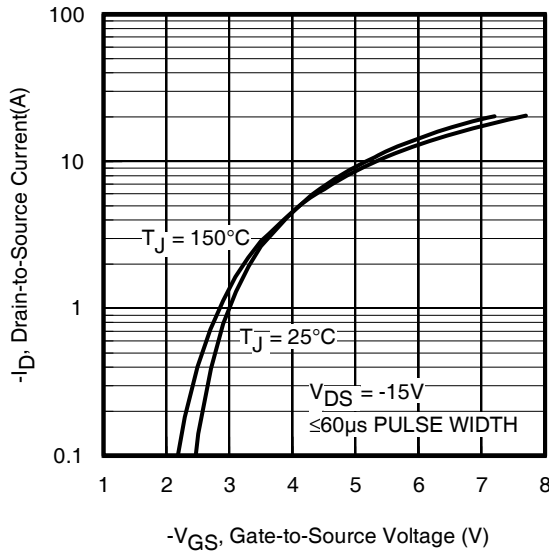
- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Current limited by package. .
- ③ Pulse width  $\leq 400\mu s$ ; duty cycle  $\leq 2\%$ .
- ④ When mounted on 1 inch square copper board.
- ⑤  $R_{\theta}$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .
- ⑥ For DESIGN AID ONLY, not subject to production testing.



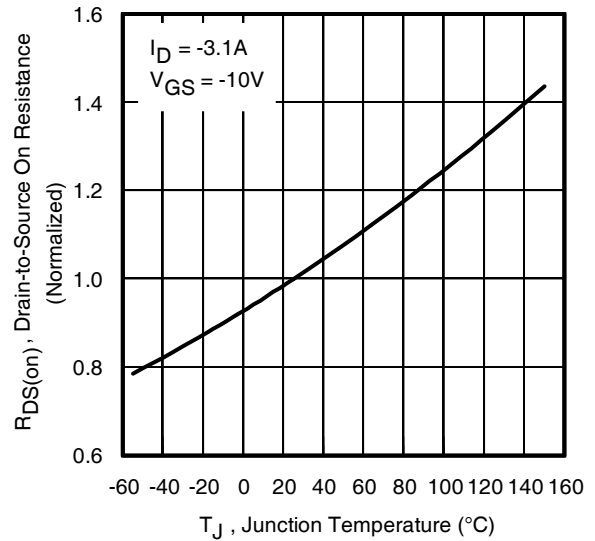
**Fig 1.** Typical Output Characteristics



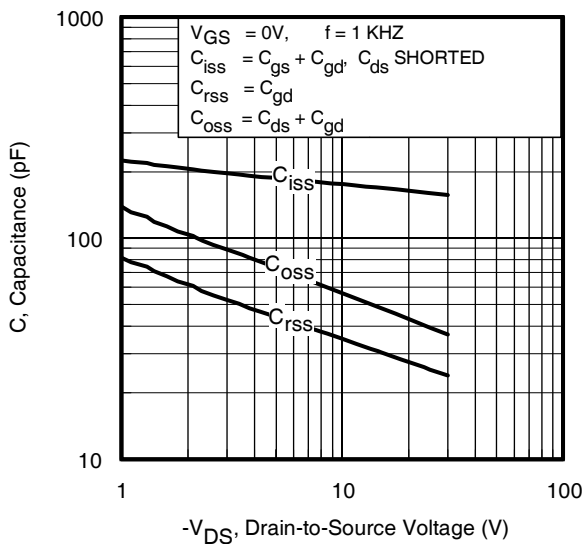
**Fig 2.** Typical Output Characteristics



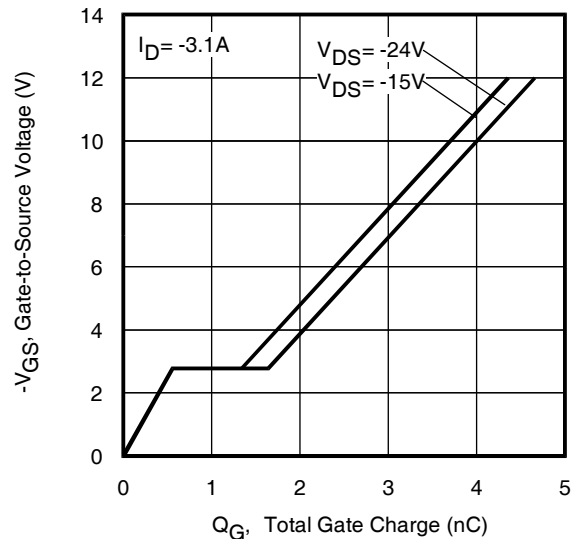
**Fig 3.** Typical Transfer Characteristics



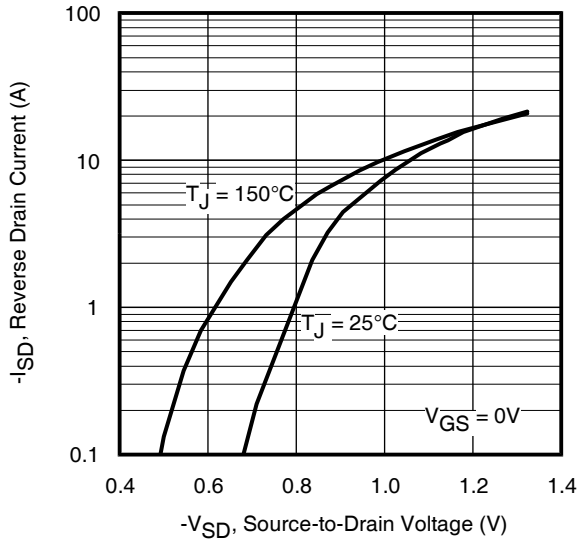
**Fig 4.** Normalized On-Resistance vs. Temperature



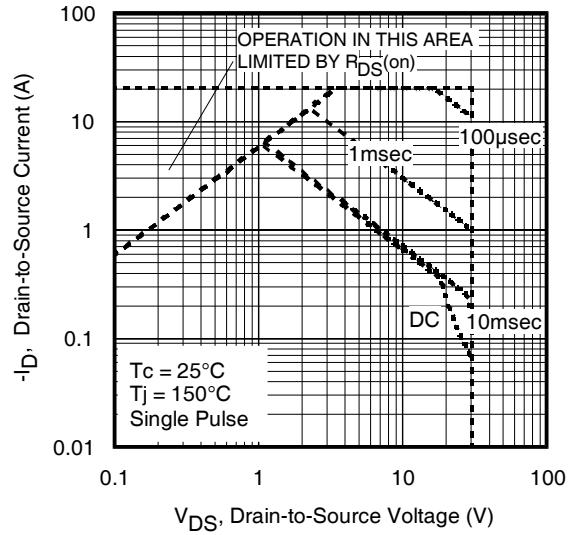
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage  
[www.irf.com](http://www.irf.com)



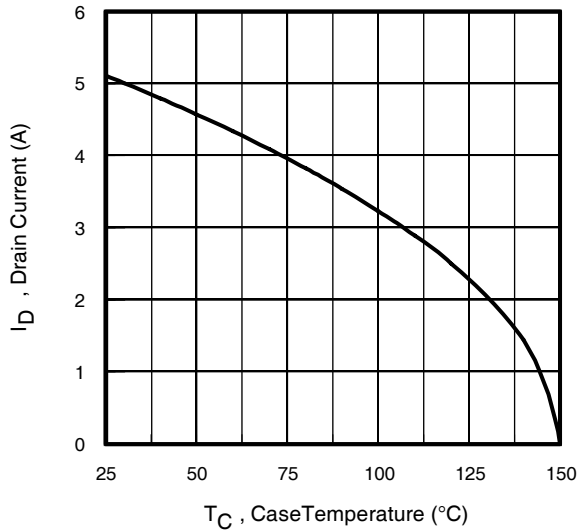
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage



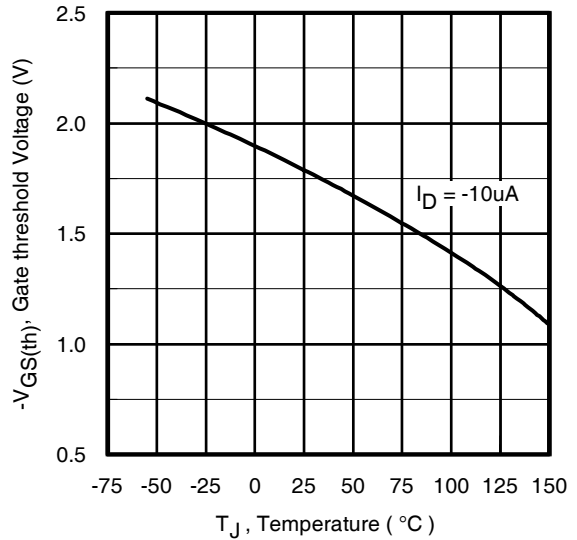
**Fig 7.** Typical Source-Drain Diode Forward Voltage



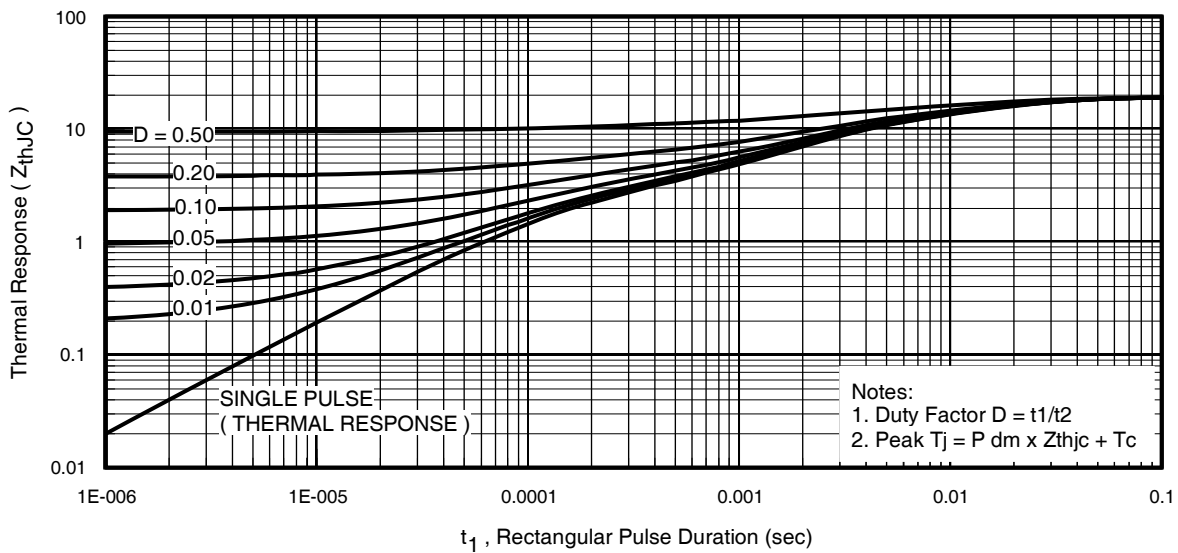
**Fig 8.** Maximum Safe Operating Area



**Fig 9.** Maximum Drain Current vs. Case Temperature



**Fig 10.** Threshold Voltage vs. Temperature



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

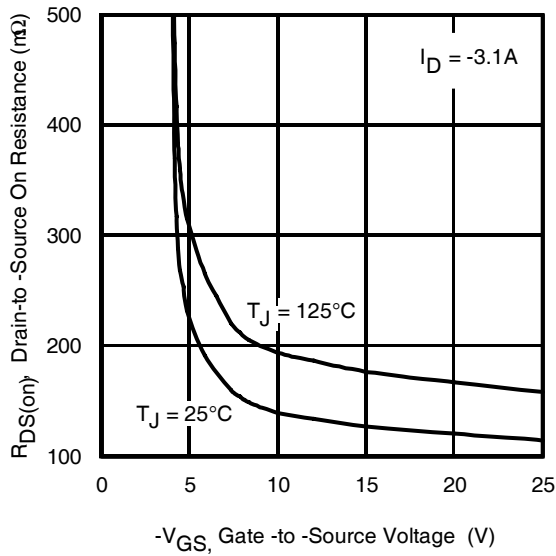


Fig 12. On-Resistance vs. Gate Voltage

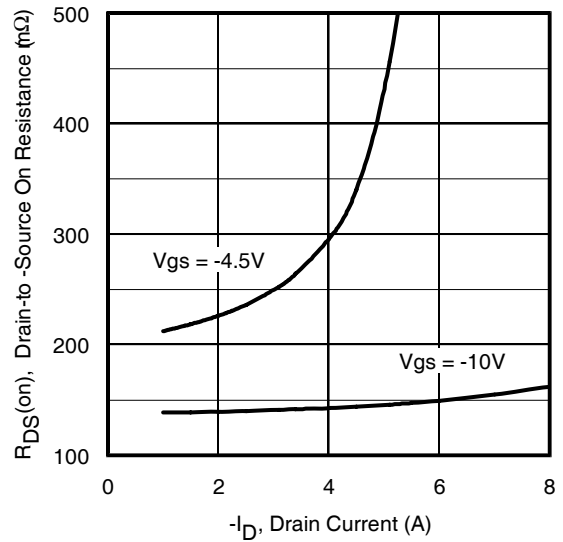


Fig 13. Typical On-Resistance vs. Drain Current

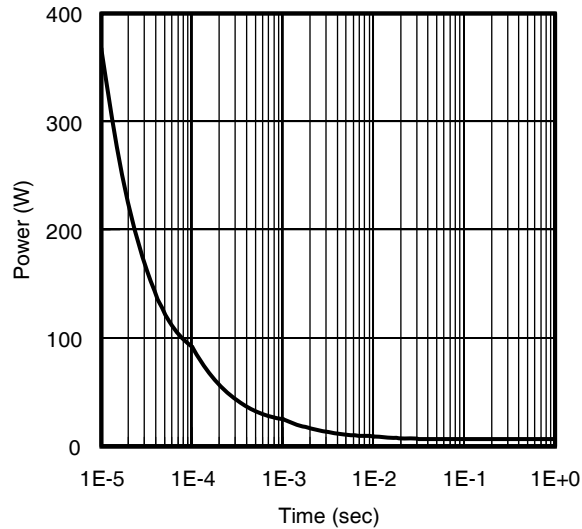
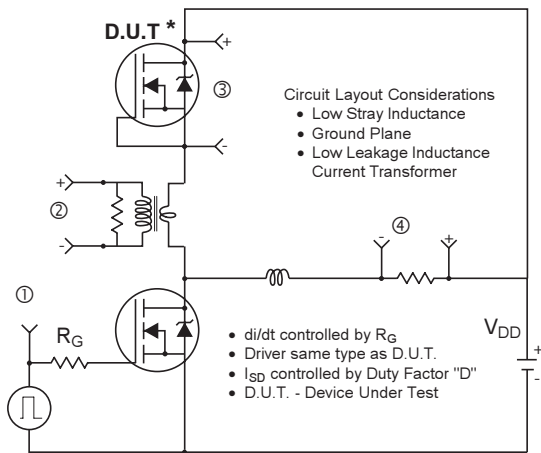
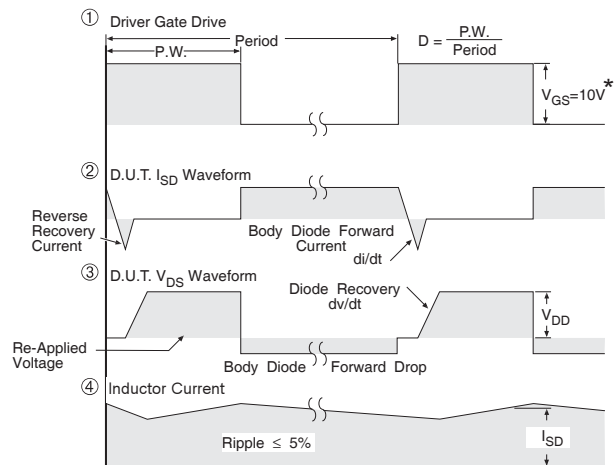


Fig 14. Typical Power vs. Time

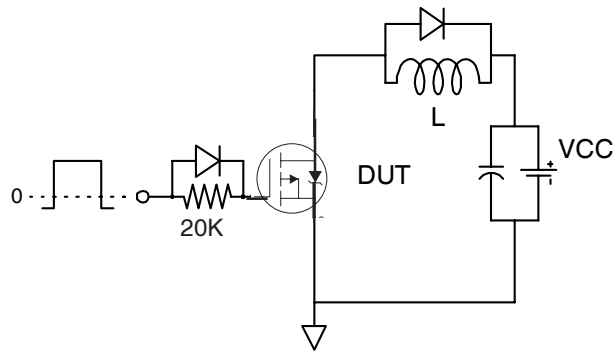


\* Reverse Polarity of D.U.T for P-Channel

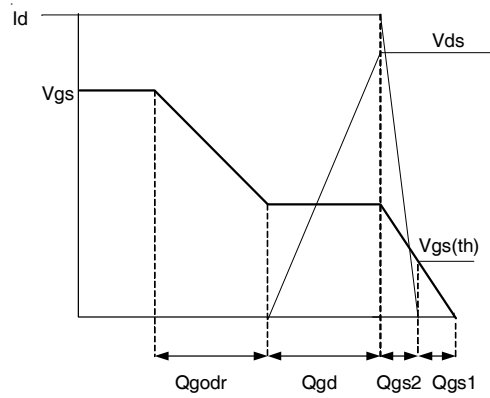


\*  $V_{GS} = 5V$  for Logic Level Devices

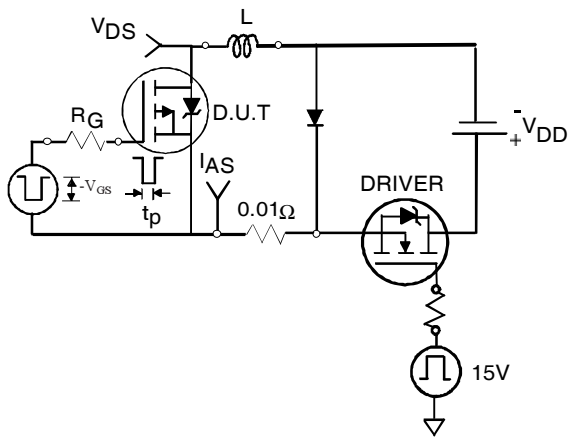
Fig 15. Diode Reverse Recovery Test Circuit for P-Channel HEXFET® Power MOSFETs



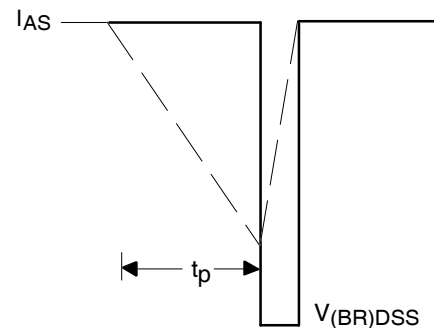
**Fig 16a.** Gate Charge Test Circuit



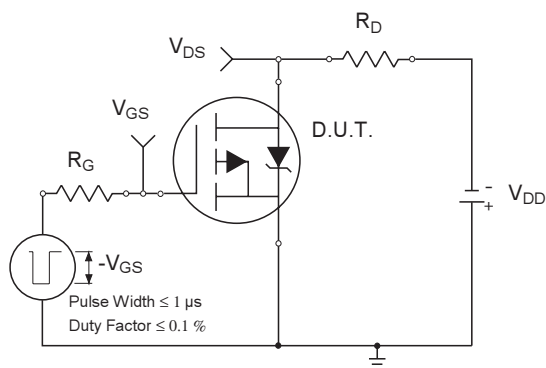
**Fig 16b.** Gate Charge Waveform



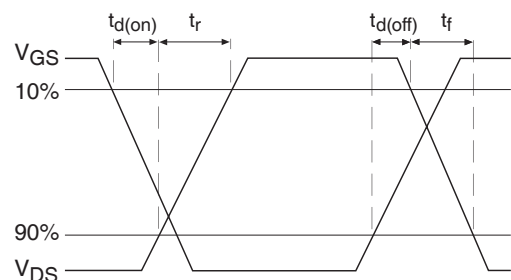
**Fig 17a.** Unclamped Inductive Test Circuit



**Fig 17b.** Unclamped Inductive Waveforms

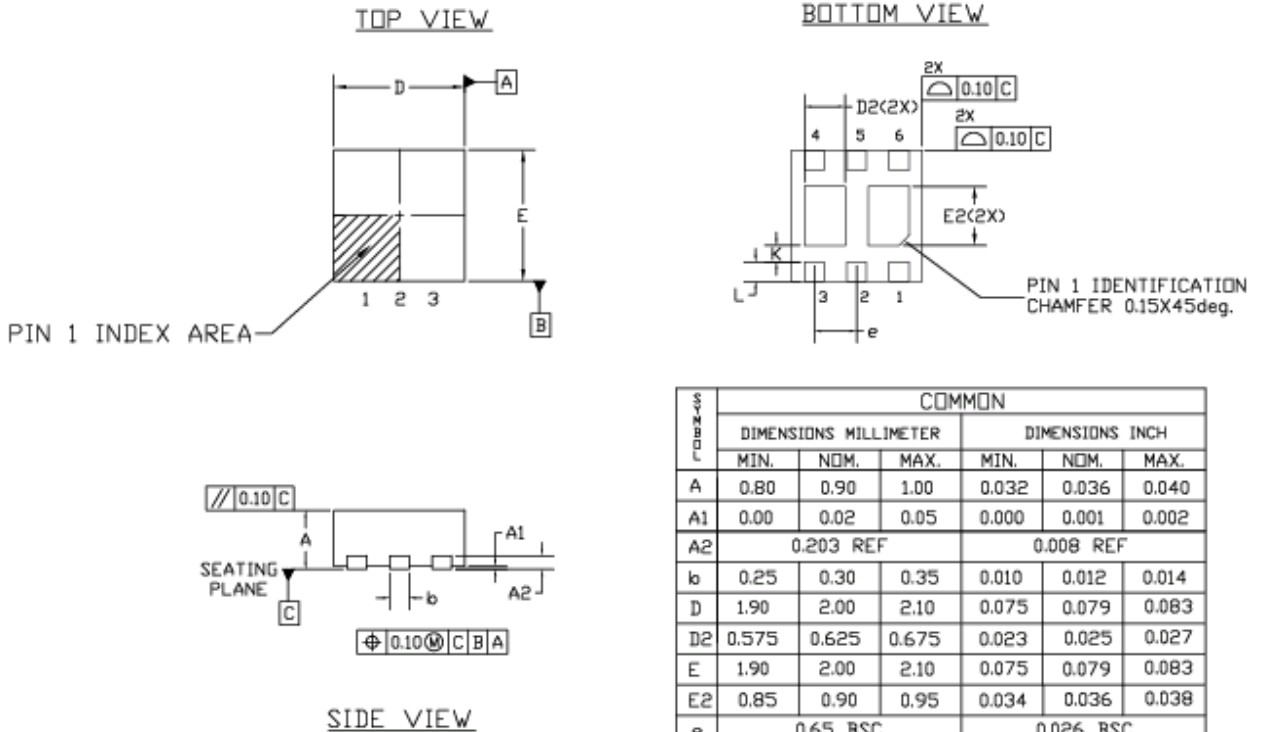


**Fig 18a.** Switching Time Test Circuit



**Fig 18b.** Switching Time Waveforms

### PQFN Package Details

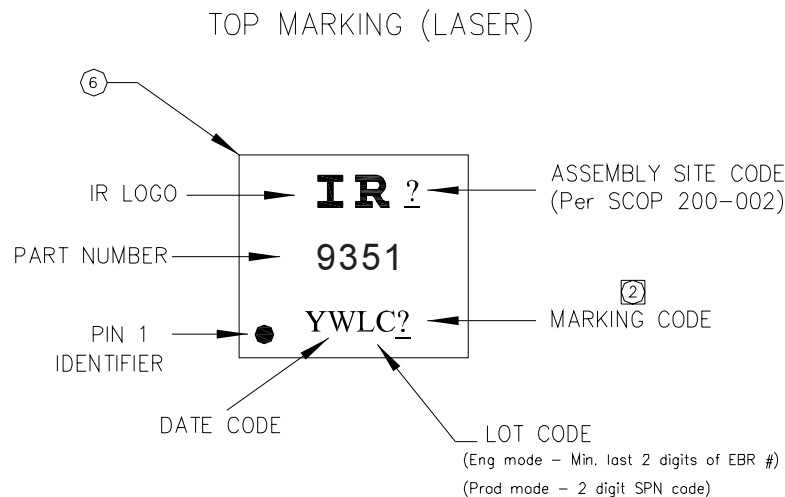


SYMBOL	COMMON					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.032	0.036	0.040
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.203 REF			0.008 REF		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	1.90	2.00	2.10	0.075	0.079	0.083
D2	0.575	0.625	0.675	0.023	0.025	0.027
E	1.90	2.00	2.10	0.075	0.079	0.083
E2	0.85	0.90	0.95	0.034	0.036	0.038
e	0.65 BSC			0.026 BSC		
L	0.25	0.30	0.35	0.010	0.012	0.014
K	0.25	-	-	0.010	-	-

NOTES :

1. DIMENSION AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. CONTROLLING DIMENSIONS : MILLIMETER. CONVERTED INCH DIMENSION ARE NOT NECESSARILY EXACT.

### PQFN Part Marking

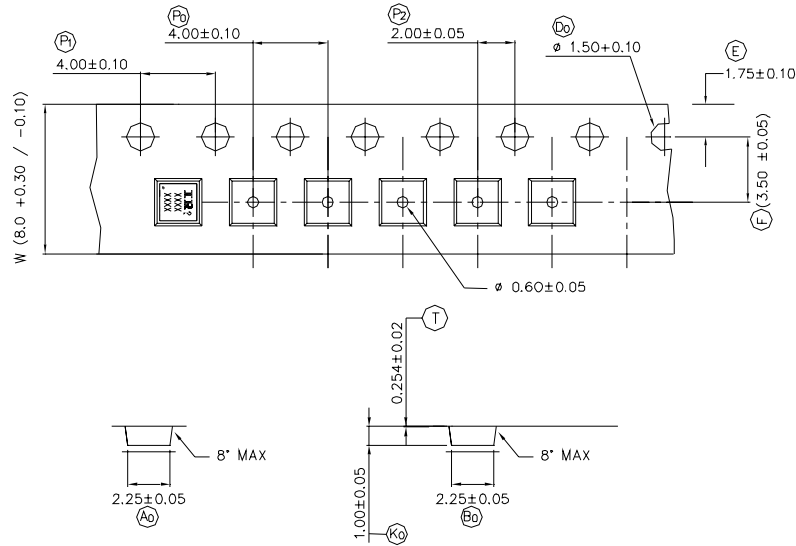


Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

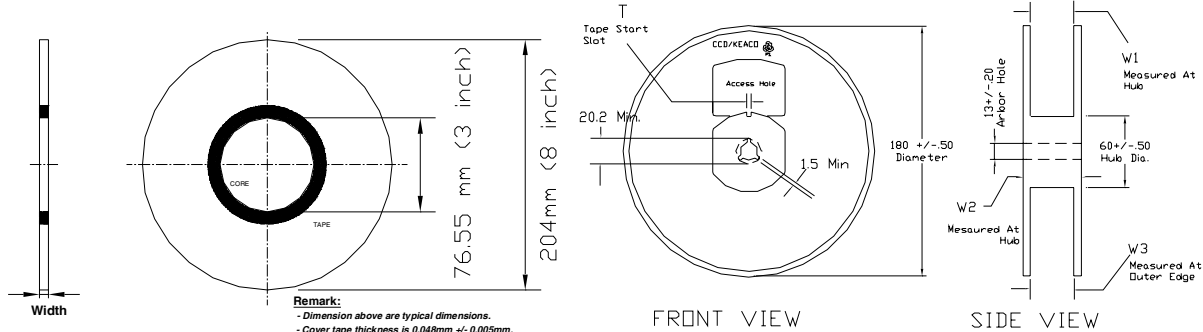
www.irf.com

# IRFHS9351PbF

## PQFN Tape and Reel



NOTE: The Surface Resistivity is  $10^4 - 10^8$  OHM/SQ



COVER TAPE (WIDTH)	TOLERANCE
5.4 mm	±0.1 mm
9.5 mm	±0.1 mm

Remark:  
- Dimension above are typical dimensions.  
- Cover tape thickness is 0.04mm ±0.005mm.  
- Surface resistivity 10ES < Rs < 10ER.

TAPE WIDTH	T	W1	W2	W3	PART NO
8 MM	3 ± 0.50	8.4 <sup>+1.5</sup> <sub>-0.0</sub>	14.4 Max	7.90 Min 10.9 Max	91586-1
12 MM	3 ± 0.50	12.4 <sup>+2.0</sup> <sub>-0.0</sub>	18.4 Max	11.9 Min 15.4 Max	91586-2

Note: Surface resistivity is  $\geq 1 \times 10^5$  but  $< 1 \times 10^{12}$  ohm/sq.

### Qualification information<sup>†</sup>

Qualification level	Consumer <sup>††</sup> (per JEDEC JESD47F <sup>†††</sup> guidelines)	
Moisture Sensitivity Level	PQFN 2mm x 2mm	MSL1 (per IPC/JEDEC J-STD-020D <sup>†††</sup> )
RoHS compliant	Yes	

<sup>†</sup> Qualification standards can be found at International Rectifier's web site

<http://www.irf.com/product-info/reliability>

<sup>††</sup> Higher qualification ratings may be available should the user have such requirements.

Please contact your International Rectifier sales representative for further information:

<http://www.irf.com/whoto-call/salesrep/>

<sup>†††</sup> Applicable version of JEDEC standard at the time of product release.

Data and specifications subject to change without notice.