GENERAL DESCRIPTION

The XRD9836 is a precision 16-bit analog front-end (AFE) for use in 3-channel/1-channel CCD/CIS document imaging applications. Pixel-by-pixel gain and offset for each of the 3 channels are controlled using a time multiplexed parallel input. Offset and Gain are sequentially supplied for red, green, and blue. The outputs from each of the three channels are transmitted time multiplexed with the high order byte first followed by the low order byte for red, blue and green.

FEATURES

- 16-bit resolution ADC, 30MHz Sampling Rate
- 10-bit accurate linear programmable gain range selectable as either 2-to-20 V/V or 1-to-10 V/V per channel
- Fully-differential input pins and internal path
- Sampling rates from 1.0 MSPS to 10.0 MSPS per channel for 3 -Channel mode and up to 15.0 MSPS in single channel mode.
- Pixel-by-Pixel Offset and Gain control through a parallel interface running at a maximum 60 Mbyte/sec. data rate
- A microprocessor serial port to control various modes of operation
- Fixed Gain/Offset Mode (FGOM) or Pixel by Pixel Gain/Offset Mode (PPGOM)
- Alternate Pixel Offset Adjust Mode (APOAM)
- Low Power CMOS=280mW (typ. @ 3V); Power-Down Mode=1mW (typ. @ 3V with static clocks)
- Single Power Supply (3.0 to 3.6 Volts) with Max CCD input signal of 1V and reset pulse up to 0.5V
- High ESD Protection: 2000 Volts Minimum

APPLICATIONS

- Scanners, MFP's

FIGURE 1. BLOCK DIAGRAM

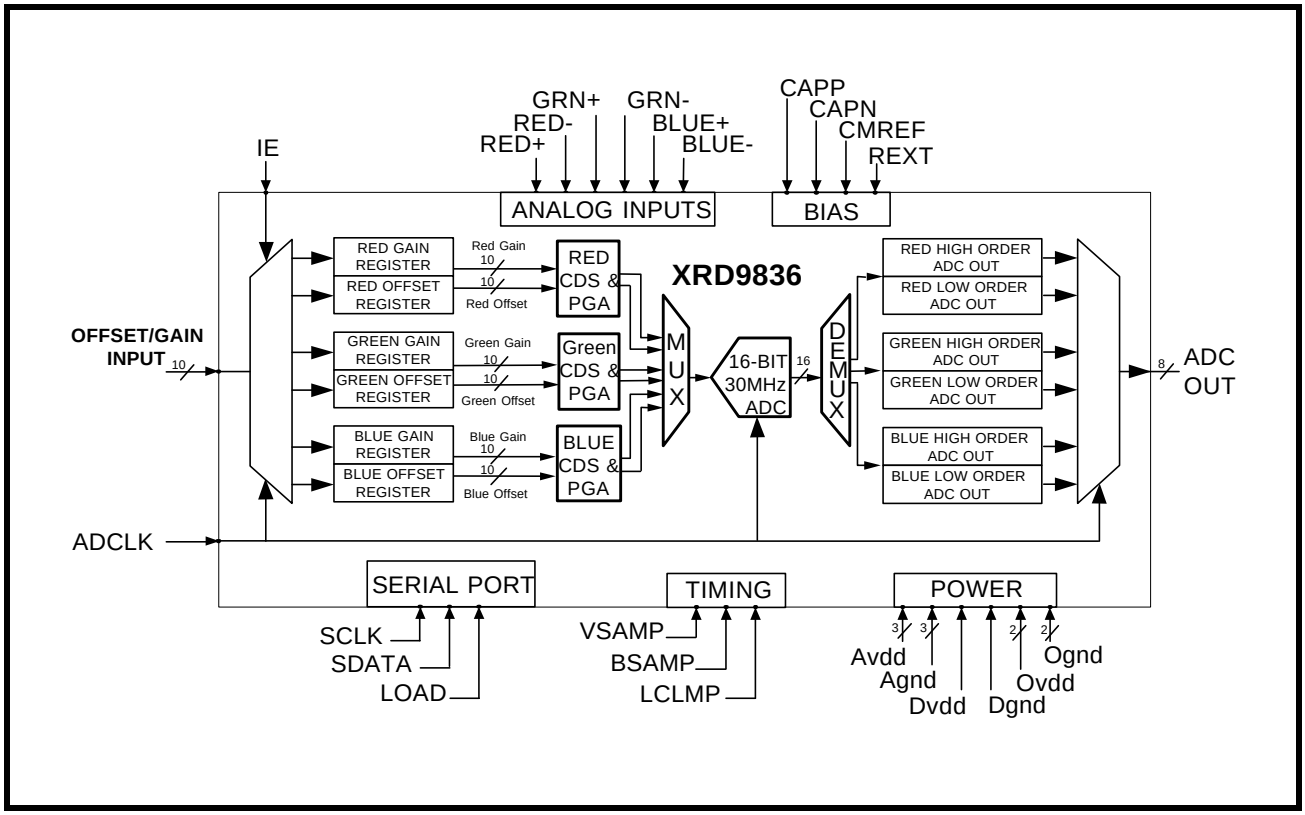
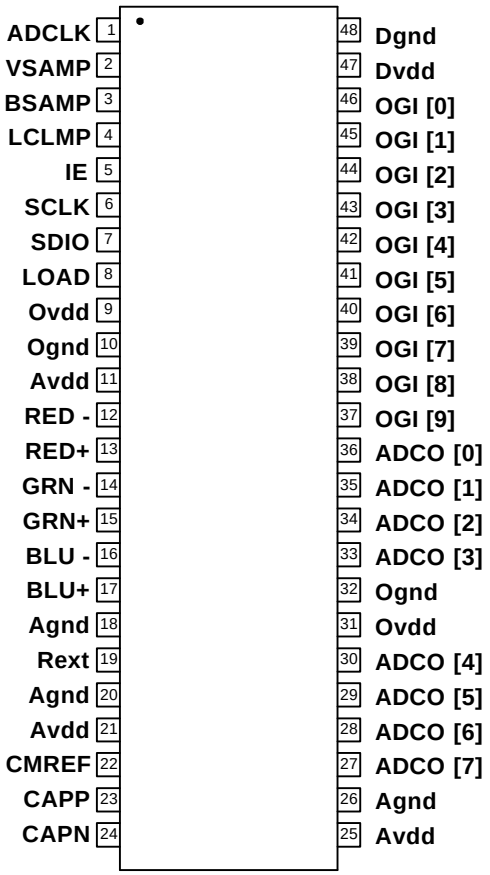


FIGURE 2. PIN OUT OF THE DEVICE



TSSOP

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRD9836ACG	48 - TSSOP	0°C to +70°C

PIN DESCRIPTIONS

PIN #	SYMBOL	TYPE	DESCRIPTION
1	ADCLK	clock	ADC clock - 50Kohm internal pull-down resistor
2	VSAMP	clock	Video Sample clock - 50Kohm internal pull-down resistor
3	BSAMP	clock	Black Sample clock - 50Kohm internal pull-down resistor
4	LCLMP	clock	Line Clamp clock
5	IE	digital	Input Enable - 50Kohm internal pull-down resistor
6	SCLK	clock	Serial Port serial clock - 50Kohm internal pull-down resistor
7	SDIO	digital in/out	Serial Port Data I/O - 50Kohm internal pull-down resistor
8	LOAD	digital in	Serial Port Load - 50Kohm pull-down resistor
9	Ovdd	power	Output driver VDD
10	Ognd	ground	Output driver Ground
11	Avdd	power	ANALOG VDD
12	RED-	analog	RED ANALOG INPUT NEGATIVE
13	RED+	analog	RED ANALOG INPUT POSITIVE
14	GRN-	analog	GREEN ANALOG INPUT NEGATIVE
15	GRN+	analog	GREEN ANALOG INPUT POSITIVE
16	BLU-	analog	BLUE ANALOG INPUT NEGATIVE
17	BLU+	analog	BLUE ANALOG INPUT POSITIVE
18	Agnd	ground	ANALOG GROUND
19	REXT	analog	External Bias Resistor -external 10Kohm resistor to ground
20	Agnd	ground	ANALOG GROUND
21	Avdd	power	ANALOG VDD
22	CMREF	analog	Common Mode Reference for ADC
23	CAPP	analog	ADC Reference By-Pass
24	CAPN	analog	ADC Reference By-Pass
25	Avdd	power	ANALOG VDD
26	Agnd	ground	ANALOG GROUND
27	ADCO[7]	output	ADC parallel out 7 (MSB)
28	ADCO[6]	output	ADC parallel out 6
29	ADCO[5]	output	ADC parallel out 5
30	ADCO[4]	output	ADC parallel out 4
31	Ovdd	power	Output driver VDD
32	Ognd	ground	Output driver Ground
33	ADCO[3]	output	ADC parallel out 3
34	ADCO[2]	output	ADC parallel out 2
35	ADCO[1]	output	ADC parallel out 2
36	ADCO[0]	output	ADC parallel out 1 (LSB)
37	OGI[9]	digital in	OFFSET AND GAIN PARALLEL IN 9 (MSB)
38	OGI[8]	digital in	OFFSET AND GAIN PARALLEL IN 8
39	OGI[7]	digital in	OFFSET AND GAIN PARALLEL IN 7
40	OGI[6]	digital in	OFFSET AND GAIN PARALLEL IN 6
41	OGI[5]	digital in	OFFSET AND GAIN PARALLEL IN 5
42	OGI[4]	digital in	OFFSET AND GAIN PARALLEL IN 4
43	OGI[3]	digital in	OFFSET AND GAIN PARALLEL IN 3
44	OGI[2]	digital in	OFFSET AND GAIN PARALLEL IN 2
45	OGI[1]	digital in	OFFSET AND GAIN PARALLEL IN 1
46	OGI[0]	digital in	OFFSET AND GAIN PARALLEL IN 0 (LSB)
47	Dvdd	power	Digital VDD
48	Dgnd	ground	Digital Ground

ELECTRICAL CHARACTERISTICS - XRD9836

Unless otherwise specified: AVDD=DVDD=3.3V, ADCLK = 30 MHz, REXT=10KW, Ta=25C

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
A/D CONVERTER						
Resolution	R	16			BITS	
Conversion Rate	Fc3	1.0		10	MSPS	PER CHANNEL in 3-CH Mode
	Fc1	1.0		15	MSPS	PER CHANNEL in 1-CH Mode
Differential Non-Linearity	DNL	-0.024	0.002	0.024	% FS	
Input Referred Offset	ZSE		40		mV	
Offset Drift	ZSD		15		uV/C	
Input Referred Gain Error	FSE		+/-2		%FS	
Gain Error Drift	FSD		0.003		%FS/C	
Input Voltage Range	IVR		2		Vpp	

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
VOLTAGE REFERENCES						
Vref+	CAPP	1.475	1.7	1.925	V	
Vref-	CAPN	0.425	0.7	0.875	V	
Vref Common Mode	VCMR	0.970	1.15	1.430	V	
Delta Vref Vref(+) - Vref(-)	ΔVREF	0.85	1.00	1.15	V	

ELECTRICAL CHARACTERISTICS - XRD9836 (con't)
Unless otherwise specified: AVDD=DVDD=3.3V, ADCLK = 30 MHz, REXT=10KW, Ta=25C

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
CDS - S/H						
Input Voltage Range	INVSR			1.0 0.5 1.2	V V V	CCD Mode, Gain = 1 to 10 CCD Mode, Gain = 2 to 20 CIS Mode, Gain = 0.5 to 5
Input Leakage Current	Iin	-40	8	40	nA	
Input Switch On Resistance	Ron		50	150	Ω	At input pins: RED+/-, GRN+/-, BLU+/- when BSAMP is active guaranteed by design
Input Switch Off Resistance	Roff	100			MEGΩ	At input pins: RED+/-, GRN+/-, BLU+/- when BSAMP is inactive guaranteed by design
Internal Voltage Clamp CDS Input (inverting)	Vclampccd	1.1	1.25	1.4	V	CCD MODE
Internal Voltage Clamp S/H Input (Non-inverting)	Vclampsh	-0.2	0.0	0.2	V	CIS MODE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
OFFSET SPECIFICATIONS						
Fine Offset Range	FOFR- FOFR+	-200 80	-128 +127	-80 200	mV mV	
Fine Offset Step	FOFRES		0.25		mV	10bit
Dynamic Offset Range	DOFR- DOFR+	-125 120	-80 +160	-55 250	mV mV	
Dynamic Offset Step	DOFRES		0.25		mV	10bit

ELECTRICAL CHARACTERISTICS - XRD9836 (con't)

Unless otherwise specified: AVDD=DVDD=3.3V, ADCLK = 30 MHz, REXT=10KW, Ta=25C

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
PGA SPECIFICATIONS						
Gain Range Min. (Absolute Value)	GRAN MIN	0.8 1.8	1.0 2.05	1.2 2.2	V/V	Gain range = 1 to 10 Gain range = 2 to 20
Gain Range Max (Absolute Value)	GRAN MAX	7.8 16	9.2 18.5	10.8 21	V/V	Gain range = 1 to 10 Gain range = 2 to 20
Gain Resolution	GRES		0.008 0.016		V/V	Gain range = 1 to 10 Gain range = 2 to 20

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
SYSTEM SPECIFICATIONS (INCLUDES CDS, PGA, AND A/D)						
Differential Non-Linearity	DNL	-0.024	0.002	+0.024	%FS	GAIN =1.5
Integral Non-Linearity	INL	-2.4	+/- 0.1	2.4	%FS	GAIN = 1.5
Input Referred Noise PGA Gain=1	IRNmin		1.7		mVrms	GAIN = 1, inputs shorted together.
Input Referred Noise PGA Gain=20	IRNmax		0.2		mVrms	GAIN = 20, inputs shorted together.

ELECTRICAL CHARACTERISTICS - XRD9836 (con't)

Unless otherwise specified: AVDD=DVDD=3.3V, ADCLK = 30 MHz, REXT=10KW, Ta=25C

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
CLOCK TIMING SPECIFICATIONS						
ADCLK Duty Cycle	tadclk3 tadclk1	49 49		51 51	% %	3-CH, Figure 17 & Figure 19 1-CH, Figure 18 & Figure 20
ADCLK period (1-Ch mode)	tcp1	66.6			ns	Figure 18 & Figure 20
ADCLK period (3-Ch mode)	tcp3	33.3			ns	Figure 17 & Figure 19
Single Channel Conversion period	tcr1	66.6			ns	Figure 18 & Figure 20
Three Channel Conversion period	tcr3	100			ns	Figure 17 & Figure 19
BSAMP Pulse Width	tpwb	20			ns	Figure 17 & Figure 19
VSAMP Pulse Width	tpwv	20			ns	Figure 17 & Figure 19
BSAMP sampling edge to VSAMP sampling edge	tbvf		50		ns	Figure 17 & Figure 19
Min. Time negedge ADCLK to sampling VSAMP	tvfcr	12			ns	Figure 17 & Figure 19
VSAMP/BSAMP Acquisition time (aperture delay)	tap		6		ns	Figure 17 & Figure 19
Settling time	tstl	15			ns	Figure 17 & Figure 19
Latency	tlat		9		cycles	Figure 21 & Figure 22

ELECTRICAL CHARACTERISTICS - XRD9836 (con't)

Unless otherwise specified: AVDD=DVDD=3.3V, ADCLK = 30 MHz, REXT=10KW, Ta=25C

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
USIO TIMING SPECIFICATIONS						
uSIO Data Setup Time	Tuss	10			ns	Figure 15 & Figure 16
uSIO Data Hold Time	Tush	10			ns	Figure 15 & Figure 16
uSIO Load Setup Time	Tusls	10			ns	Figure 15 & Figure 16
uSIO Load Hold Time	Tuslh	10			ns	Figure 15 & Figure 16
uSIO Period	Tusp	40			ns	Figure 15 & Figure 16
uSIO Data Valid Delay	Tusdvd		0			Figure 16

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O TIMING SPECIFICATIONS						
OGI Enable time	Tev	8			ns	Figure 4
VSAMP to ADC setup time	Tva	4			ns	Figure 4 internal time adjustable
ADC to OGI data setup time	Togis	4			ns	Figure 4 internal time adjustable
ADC to OGI data hold time	Togih	4				Figure 4 internal time adjustable
ADCLK to ADCDO data out delay	Tadcdo	4			ns	Figure 5 internal time adjustable
LCLMP Pulse duration	LCLMPd	4	50		pixels	more pixels preferred
BSAMP/LCLMP setup	BLs	1			ns	
BSAMP/LCLMP hold	BLh	1			ns	

ELECTRICAL CHARACTERISTICS - XRD9836 (con't)

Unless otherwise specified: AVDD=DVDD=3.3V, ADCLK = 30 MHz, REXT=10KW, Ta=25C

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
POWER SUPPLIES - 1 CHANNEL MODE						
Analog IDD	IAVDD		47		mA	Tested @ 3.6V
Digital IDD	IDVDD		5		mA	Tested @ 3.6V
Output IDD	IOVDD		5		mA	Tested @ 3.6V
IDD Total	IDD		57		mA	Tested @ 3.6V
Power Dissipation	PDISS		188		mW	Tested @ 3.6V

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
POWER SUPPLIES - 3 CHANNEL MODE						
Analog IDD	IAVDD	60	84	110	mA	Tested @ 3.6V
Digital IDD	IDVDD	1	9	15	mA	Tested @ 3.6V
Output IDD	IOVDD	1	11	15	mA	Tested @ 3.6V
IDD Total	IDD	62	104	140	mA	Tested @ 3.6V
Power Dissipation	PDISS	220	343	500	mW	Tested @ 3.6V
Power Dissipation	PDISS		280		mW	Tested @ 3.0V

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
DIGITAL I/O						
Logic Input Low	Vil			0.5	V	
Logic Input High	Vih	VDD-0.5			V	
OGI Input Current High	Iih	-100		100	nA	
OGI Input Current Low	Iil	-100		100	nA	
Control Inputs Current High	Iinh	50	90	150	uA	50Kohm Pull down
Control Inputs Current Low	Iinl	-5	0.1	5	uA	50Kohm Pull down
Logic Output Low	Vol			0.5	V	Isink=2.0mA
Logic Output High	Voh	VDD-0.5			V	Isrc=2.0ma
Tristate Leakage	IOLeak	-100	0.1	100	nA	

SYSTEM OVERVIEW

The XRD9836 provides a 16-bit Analog Front End functionality for Mid-to-High range, next-generation scanner applications. It has 3 channels of Correlated Double Sampling (CDS), using a 10-bit Dynamic Offset DAC, a 10-bit Programmable Gain Amplifier (PGA) and a 10-bit Fine Offset DAC for Red, Green, and Blue CCD signals. A 16-bit 30MHz ADC is multiplexed among these 3 channels to provide digitized image data for the scanner ASIC chip. In 3-channel mode, the order of channels is R, G, B. In the 1-channel mode, only the selected channel is active. The XRD9836 provides one of the key requirements for the next generation scanner AFE's, the ability to control Pixel-by-Pixel Gain and Offset values. Figure 3 shows the ASIC and AFE interface for the proposed system.

A 10-bit parallel bus Offset Gain Input Port (OGI) is used to transfer 10 bits of Gain and 10 bits of Offset. In the 3-channel mode, the data is received sequentially in the following order: red gain, red offset, green gain, green offset, blue gain, blue offset. In 1-channel mode, the data is received sequentially gain then offset. For an example of both 3-channel and 1-channel OGI timing see Figure 4.

The Input Enable pin (IE) enables OGI port to program internal pixel gain and offset registers. If IE goes low, the gain and offset registers will store the last data while IE was high.

For ADC outputs, the XRD9836 has an 8-bit parallel bus ADC Data Out (ADCDO). The ADC output data is transmitted sequentially in the following order for 3-ch mode red high order byte, red low order byte, green high order byte, green low order byte, blue high order byte, blue low order byte as shown in Figure 5

A three-pin, Micro-controller Serial I/O link (uSIO) is used to write or read from the XRD9836's internal configuration registers. The internal registers control the various modes of operation of the chip.

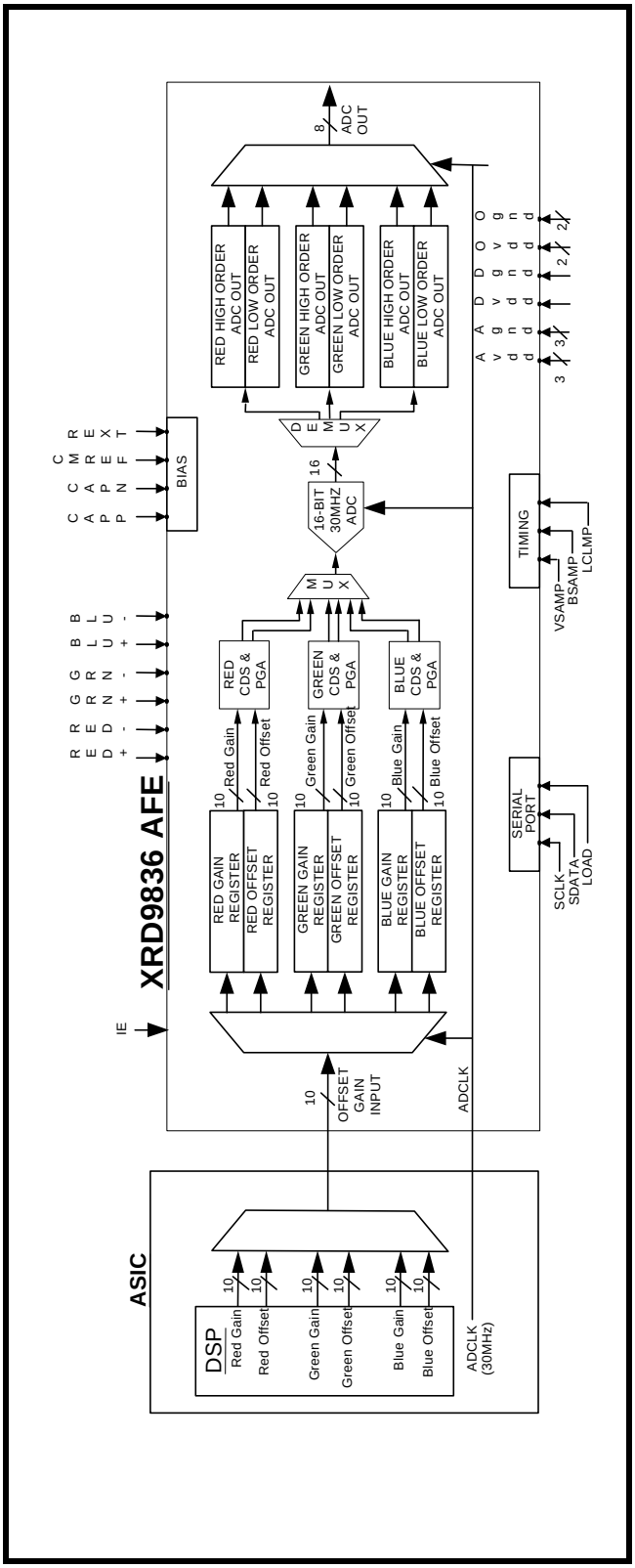


FIGURE 3. SYSTEM BLOCK DIAGRAM

GAIN SELECT:

The XRD9836's Gain range is selectable to either 1 to 10 or 2 to 20 with the Gain Select Bit. If Gain of 1 to 10 is selected (Gain Select bit = 0), the maximum input is 1.0V. If Gain of 2 to 20 is selected (Gain Select bit = 1), the maximum input is 0.5V.

PARALLEL PORT FOR PIXEL OFFSET AND GAIN CONTROL (OGI):

The timing diagram in Figure 4 shows the Offset and Gain Inputs (OGI) and ADCLK in relationship to VSAMP.

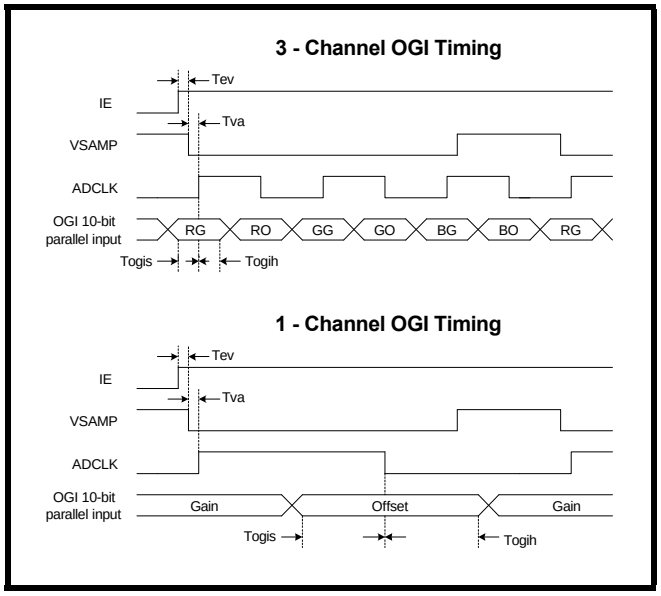


FIGURE 4. OGI TIMING ($ADCLK_{POL}$=0, $VSAMP_{POL}$=0)

The ASIC chip will be clocking OGI data at six times the pixel rate clock in 3-CH mode and two times the pixel rate in 1-CH mode. The gain data is grabbed on the rising edge of ADCLK and the offset data on the falling edge of ADCLK. The OGI port is read into internal pixel gain and offset registers only when Input Enable (IE) is active before the sampling edge of VSAMP as shown above. As noted the RGB gain/offset data is synchronized to sampling edge of VSAMP. Note that ADCLK frequency is 3X the pixel rate in 3-CH mode and 1X the pixel rate in 1-CH mode. The ADCLK's duty cycle is required to be 50%. It is assumed that the OGI port and ADCLK input have matched output drivers inside the ASIC, matched trace lengths on the PCB between the ASIC and the XRD9836, and matched delays at input buffers inside the XRD9836 in order to receive OGI data on both edges of ADCLK error free.

The latency between the input of the parallel inputs and their effective application is 1 pixel. The user is also reminded that data coming out of the ADC outputs will have latency from the gain and offset provided (10 ADC cycles for single color and 12 cycles for 3-color). This latency includes the cycles to put the gain and offset data into the registers and the latency of the ADC itself (9 ADCLK cycles).

Sampling of the OGI parallel input port is defined as the red gain data being the first pulse of ADCLK after VSAMP, therefor VSAMP must occur before a rising edge of ADCLK. It is also recommended that VSAMP__OGI_DLY (DelayD[7:4]) should be smaller than OGI_DLY (DelayA[7:4]) to make sure the correct data is sampled, and that relationship is not reversed internally.

PARALLEL PORT FOR ADC OUTPUT (ADCDO):

The timing diagram, Figure 5, shows the ADC output (ADCDO). The XRD9836 will be clocking ADC high order bytes on the rising edge of ADCLK and clocking ADC low order bytes on the falling edge of ADCLK. As noted the RGB data is synchronized to sampling edge of VSAMP.

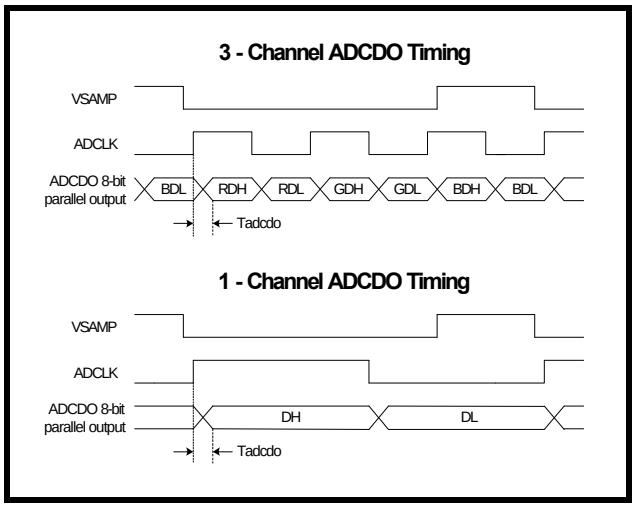


FIGURE 5. ADCDO TIMING ($ADCLK_{POL}$=0, $VSAMP_{POL}$=0)

PIXEL GAIN/OFFSET CONTROL (FGOM OR PGOM):

Figure 6 shows the block diagram of the CDS/PGA/Offset DACs/ADC signal path. The offset for each channel is controlled by a 10-bit Dynamic offset DAC before the CDS amplifier and a 10-bit Fine offset DAC after the PGA amplifier. Thus, the total offset of each channel is controlled by two 10-bit offset DACs. The Dynamic offset DAC will have a range of -80mV to +160mV, with the ability to adjust the CDS stage offset to within +/- 0.25mV. The Fine offset DAC will

have a range of +/- 128mV, with the ability to adjust PGA offsets to within +/- 0.25mV.

There are two modes of operation for Pixel Gain and Offset control. The first is a fixed gain and offset control mode where the gain and offset is adjusted once per line or per scan. The second mode is a pixel to pixel adjustment of gain and offset. This mode allows for gain and offset adjustment for each and every pixel. These modes are controlled by bit D0, GOM (Gain Offset Mode), in the MODE register.

In FGOM (Fixed Gain/Offset Mode, GOM=0), the user can program the PGA gain, Dynamic and Fine Offset registers through the micro-controller serial interface (uSIO).

In PPGOM (pixel-by-pixel gain and offset mode, GOM=1), the user can input 10 bits of Gain and 10 bits of Dynamic offset data through the OGI port.

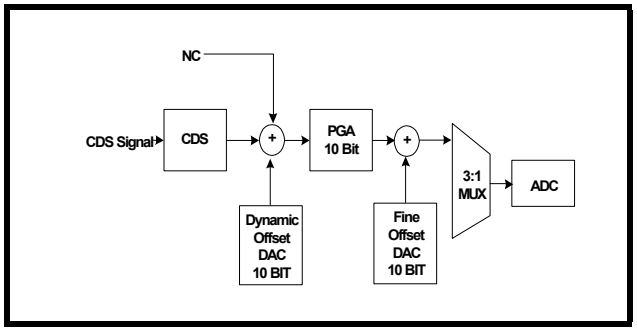


FIGURE 6. CDS TO ADC SIGNAL PATH

CCD MODE(CORRELATED DOUBLE SAMPLING):

Correlated double sampling is a technique used to level shift and acquire CCD output signals whose information is equal to the difference between consecutive reference (V_{Black}) and signal (V_{Video}) samples. The CDS process consists of three steps:

1) Sampling and holding the reference black level (V_{Black}).

2) Sampling the video level (V_{Video}).

3) Subtracting the two samples to extract the video information. (CCD signal information = V_{Black}- V_{Video})

Once the CCD signal information has been extracted, it can be processed further through amplification and/or offset adjustment. Since system noise is also stored and subtracted during the CDS process, signals with bandwidths less than half the sampling frequency will be substantially attenuated.

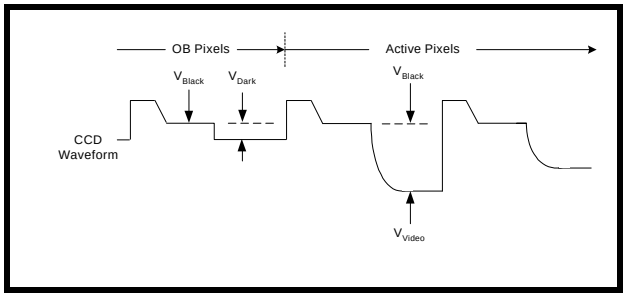


FIGURE 7. CCD WAVEFORM - DEFINITION OF TERMS

CCD OUTPUT INFORMATION = (V_{BLACK}-V_{VIDEO})

LCLMP TIMING:

In order to reject higher frequency power supply noise which is not attenuated near the sampling frequency, the XRD9836 utilizes a fully differential input structure. Since the CDS process uses AC coupled inputs, the coupling capacitor must be charged to the common-mode range of the analog front-end. This can be accomplished by clamping the coupling capacitor to the internal clamp voltage when the CCD is at a reference level at the beginning of each line using LCLMP. This needs to be done for enough clamping time (Tclamp) which is determined by external Capacitor, internal switch resistance, BSAMP pulse width and number of samples during line clamp. The maximum capacitance is

$$C_{MAX} = \frac{N * tpwb}{(Rc + Rs) * \ln\left(\frac{Vr - Vc}{Ve}\right)}$$

where tpwb = clamp pulse width (BSAMP typ 25ns)

N = number of pixels used for clamping

Rc = clamp resistance (typ 50ohms)

Rs = signal source resistance (typ 50ohms)

Vr = black level

Vc = clamp voltage (1.2V)

Ve = error voltage (3.05uV worst case)

The clamp LCLMP should be active for at least 4 pixels during Optical Black (OB) and should be inactive during all of the Active portion of the line. Usually OB lasts for 40 - 50 pixels. It is better if LCLMP remains active during as much of OB as possible. LCLMP should be set Active 1ns before BSAMP leading edge and should be held for at least 1ns after BSAMP trailing edge.

In addition to the above requirement for LCLMP on a line by line basis there is an additional requirement for a one time LCLMP upon power-up to provide the AC coupling capacitor's initial charge. The one time LCLMP pulse width can also be determined from the Cmax equation above. A typical value, using 1 nf cap, with initial charge of 3V (Vr - Vc), and a BSAMP pulse width of 25ns, is estimated to be 1.4us. This is equivalent to one time LCLMP of 56 OB pixels upon power up.

3-CHANNEL CDS MODE:

This mode allows simultaneous CDS of the red, green and blue inputs. Black-level sampling occurs on each pixel and is equal to the width of the BSAMP sampling input. The black level is held on the sampling edge of BSAMP and the PGA will immediately begin to track the signal input until the sampling edge of VSAMP.

At the end of the video sampling phase, the difference between the reference and video levels is inverted, amplified, and offset depending on the contents of the PGA gain and offset registers. The RGB channels are then sequentially converted by a high-speed A/D converter. Converted data appears on the data output bus after 9 ADCLK cycles. The red channel is synchronized on the rising edge of the first ADCLK after the sampling edge of VSAMP. The power-up default mode is for CDS sampling a CCD input.

1-CHANNEL CDS MODE:

The 1-Channel CDS mode allows high-speed acquisition and processing of a single channel. The timing, clamp and buffer configurations are similar to the 3-channel mode described previously. To select a single channel input, the color bits of configuration selected by CHAN[1:0] bits, in the MODE register, must be set to the appropriate value. The A/D input will begin to track the selected color input on the next positive edge of ADCLK. If the configuration is toggled from a single color mode to 3-channel mode, RGB scanning will not occur until the circuit is re-synchronized on the sampling edge of VSAMP.

CIS MODE:

The AFE can be configured for inputs from a CCD or a CIS type device by setting the CCD_CIS bit. For CIS mode, the following interface features are provided:

1. DC Coupled Inputs.

2. Gain Range is 0.5 to 5 with 10 bit resolution.

3. It is assumed that CIS Sample and Hold Outputs and DC offset buffer have low output impedances(~50 ohms).

4. VSAMP should have typ > 25ns pulse width.

5. LCLMP is not needed for CIS Applications. (except for APOAM even and odd selection)

6. Input Voltage Range:

Vcm @ Vin- = 0 to 1.4 V

CIS Signal @ Vin+ = 0 to 1.2 V above Vcm offset

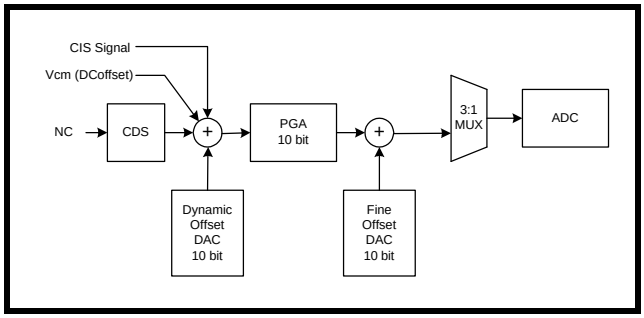


FIGURE 8. CIS SIGNAL PATH

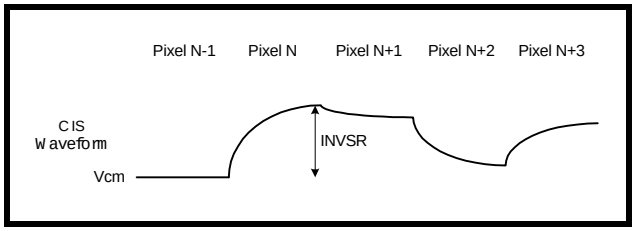


FIGURE 9. CIS WAVEFORM -DEFINITION OF TERMS

3-CHANNEL CIS AND S/H MODE

The XRD9836 also supports operation for Contact Image Sensor (CIS) and S/H applications. The red channel is synchronized on the rising edge of the first ADCLK after the sampling edge of VSAMP.

In this mode of operation, the BSAMP input is connected to DGND, and input sampling occurs on the falling edge of VSAMP(VSAMP_POL=0).

1-CHANNEL CIS AND S/H MODE:

The 1-channel CIS S/H mode allows high-speed acquisition and processing of a single channel. The timing, clamp and buffer configurations are similar to the 3-channel mode. In single channel mode one color channel is selected using CHAN[1:0]. If the configuration is toggled from single color to 3-channel mode, RGB scanning will not occur until the circuit is re-synchronized by the first sampling edge of VSAMP.

TIMING - CLOCK BASICS:

The XRD9836 has 4 clock signals BSAMP, VSAMP, ADCLK and LCLMP. These inputs control the sampling, clamping and synchronization functions of the device.

The pixel rate clocks are BSAMP, VSAMP and ADCLK. BSAMP controls the sampling of the black reference level of a CCD input signal. VSAMP controls the sampling of the video level of a CCD or CIS output signal. The ADCLK controls the internal sampling of the PGA by the ADC and ADC operation.

The line rate clock, LCLMP, performs the clamping and synchronization functions. The clamp function sets the bias point for the external AC coupling capacitor on the inputs. Synchronization defines the odd pixel in the APOAM mode.

CLOCK POLARITY

Each of the 4 timing signals has a separate polarity control bit in the CONTROL register. Figure 10 shows the logic implementation of the polarity control. If the polarity bit is low (default) BSAMP and VSAMP sample on the falling edge, LCLMP is active high and ADCLK must be low during the VSAMP falling edge. See timing examples if Figure 17 and Figure 18

If any of the external timing signals are inverted from the default timing simply write a “1” to the appropriate polarity bit to compensate.

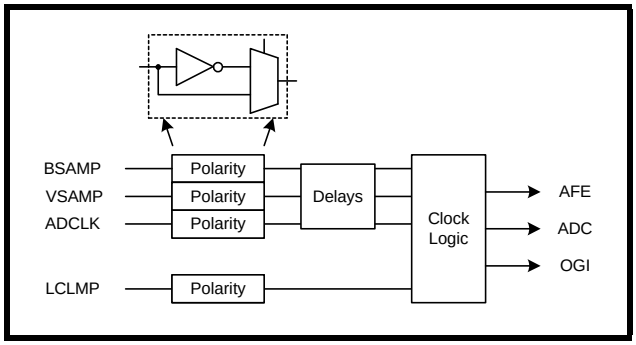


FIGURE 10. CLOCK POLARITY AND DELAYS

DELAY CONTROL

One of the more difficult tasks in designing a scanner is optimizing the pixel and interface (data output & OGI) timing for a CCD, CDS and ADC. The XRD9836 has included a programmable delay function to help simplify this job.

There are four serial interface registers, DelayA, DelayB, DelayC and DelayD, used to program various delays of the pixel timing and Data and OGI bus timing. Each register is divided into 2 delay parameters. Each delay parameter is 4 bits wide.

DelayA[7:4] controls the OGI sampling delay. These bits program the delay of the ADCLK used to sample the OGI input bus. Delay is added in 1ns increments. See Figure 12.

DelayA[3:0] controls the ADCDO delay. These bits are used to program the timing delay added to the ADCDO data bus updates. Delay is added in 1ns increments. See Figure 11.

DelayB[7:4] controls the amount of delay added to the leading edge of BSAMP. Delay to the leading edge will be added in 0.5ns increments. This can help to position the leading edge of the internal BSAMP away from the reset pulse of the CCD input. See Figure 11.

DelayB[3:0] controls the amount of delay added to the trailing edge of BSAMP. Delay to the trailing edge will be added in 0.5ns increments. This will allow for adjustment of the Black Level sampling position by the internal BSAMP. See Figure 11.

DelayC[7:4] controls the amount of delay added to the leading edge of VSAMP. Delay will be added in 0.5ns increments. This can help to position the leading edge of the internal VSAMP to track the video portion of the CCD input. See Figure 11.

DelayC[3:0] controls the amount of delay added to the trailing edge of VSAMP. Delay will be added in 0.5ns increments. This will allow for adjustment of the Video Level sampling position by the internal VSAMP. See Figure 11.

DelayD[7:4] controls the amount of delay added to the VSAMP OGI. The internal VSAMP_OGI is used to transfer the input OGI register data to the PGA and OFFSET control. Delay is added in 1ns increments. **Please note the falling edge of the internal VSAMP_OGI must occur before the rising edge of the OGI sampling clock.** See Figure 12.

DelayD[3:0] controls the amount of delay added to the ADCLK. Delay is added to the internal ADCLK in 0.5ns increments. See Figure 11.

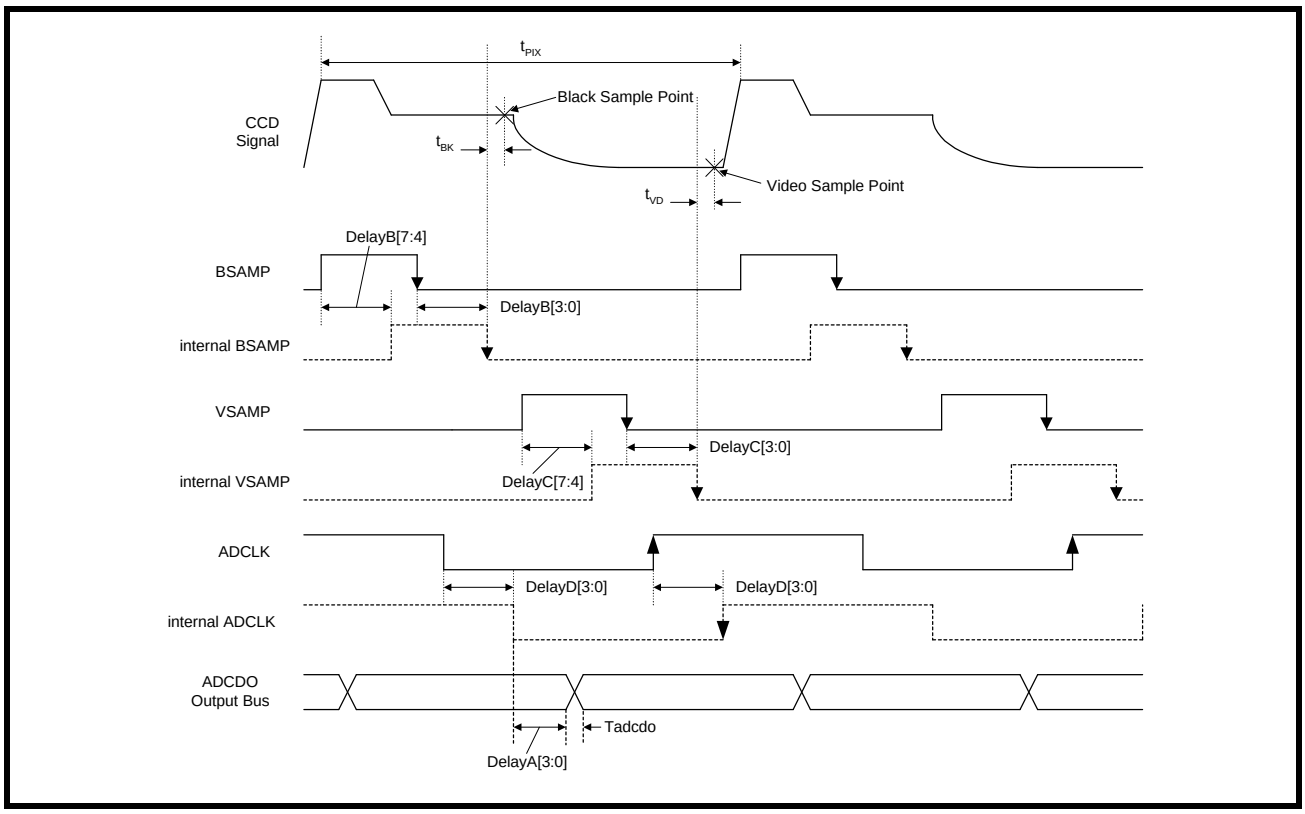


FIGURE 11. PIXEL TIMING & ADCDO (OUTPUT DATA) DELAY ADJUSTMENT

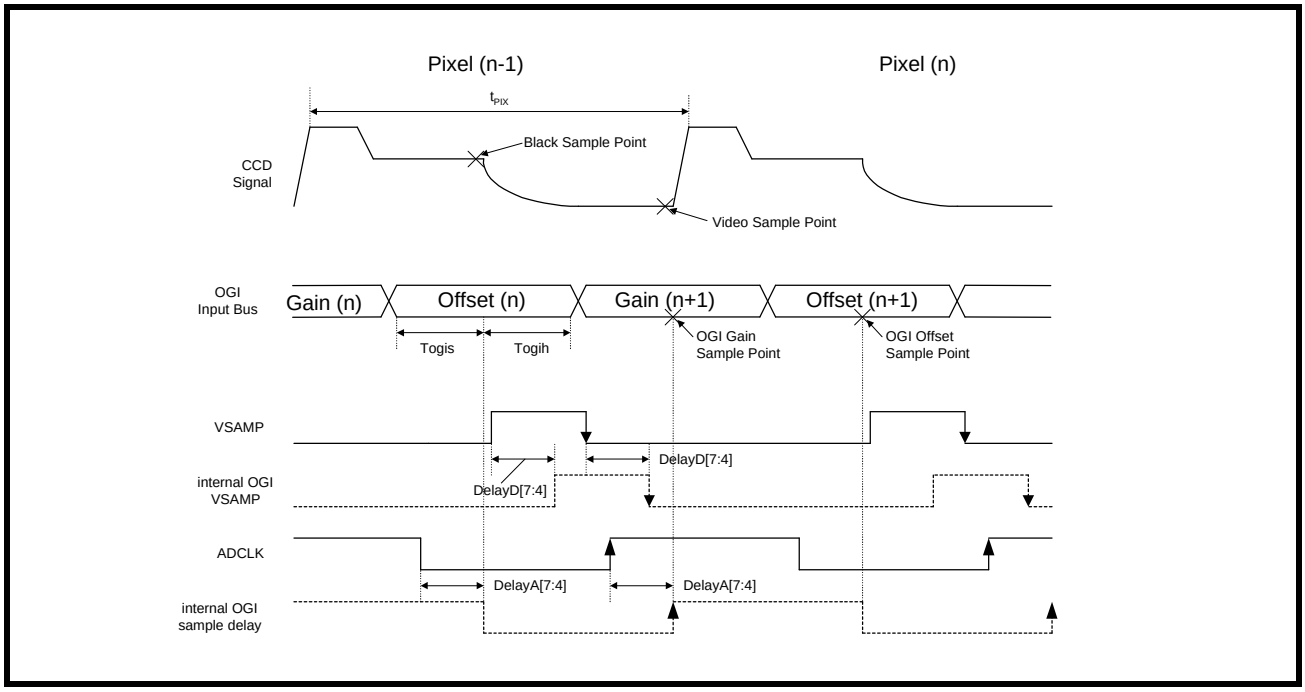


FIGURE 12. OGI TIMING DELAY ADJUSTMENT

ALTERNATE PIXEL OFFSET ADJUST MODE (APOAM):

In some applications, alternate pixels along a scan line come from two different rows of CCD's, causing a systematic offset between alternate pixels. When the XRD9836 is operated in the Fixed Gain Offset Mode (FGOM), it does not have the ability to compensate for this alternating offset phenomenon.

To compensate for these offsets, this chip has an Alternate Pixel Offset Adjust mode (APOAM), which can be enabled by writing a 1 to the APOAM bit (D1of the MODE register) through the serial port. In APOAM mode each channel has four 10-bit offset registers to control offset. Odd pixel offsets are compensated for by the Dynamic Offset Register value and the Fine Offset Register value. The even pixel offsets are compensated for by the APOAM Dynamic Offset Register value and the APOAM Fine Offset Register value. The individual channel pixel gains do not change and are determined by the red, green and blue PGA gain register settings.

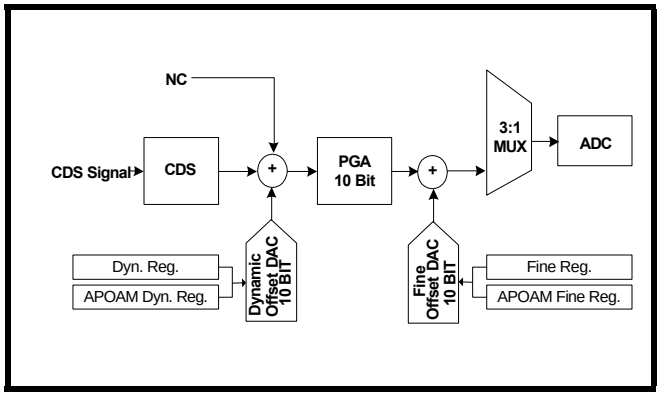


FIGURE 13. APOAM MODE - CONFIGURATION OF OFFSET REGISTERS

The offset alternates every other pixel. The first pixel and all odd pixels in the line use the dynamic offset and fine offset register values. The even pixels use the APOAM dynamic offset and the APOAM fine offset register values. Odd pixels are defined from the first ADCLK after the fall of LCLMP.

In the PPGOM mode, the APOAM can be selected only when Input Enable (IE) is disabled. The last dynamic gain and offset programmed using the OGI port are used for the odd pixels.

The APOAM dynamic offset and the APOAM fine register values, programmed through the USIO port are used for the even pixels. The gain value is fixed as the last received value through the serial port. This is shown in Figure 14.

SUMMARY OF APOAM USABILITY:

MODE	IE	APOAM
FIXED GAIN/OFFSET	OFF	USABLE
FIXED GAIN/OFFSET	ON	USABLE
PIXEL GAIN/OFFSET	OFF	USABLE
PIXEL GAIN/OFFSET	ON	NOT USABLE

TABLE 1: SUMMARY OF APOAM USABILITY

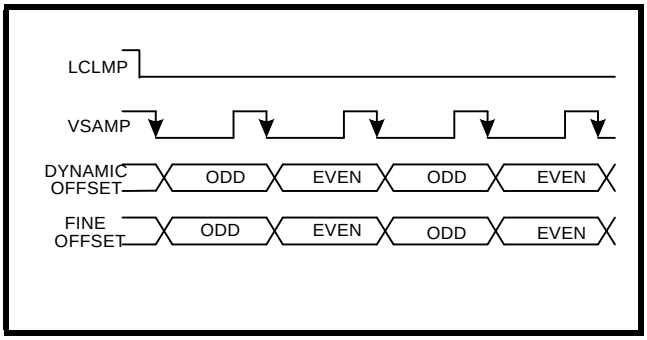


Figure 14. **APOAM SYNCHRONIZATION AND REGISTER ALTERNATION**

Note: LCLMP also defines which pixel is even or odd. The first pixel after LCLMP goes inactive is odd. Position LCLMP so that there are an even number of pixels before start of active pixels.

MICRO-CONTROLLER SERIAL PORT FOR MODE CONTROL (USIO):

The uSIO is a bidirectional I/O port which is used for configuring various operating modes as well as phase aligning internal clocks (delay control). The serial port can be used to program any of the registers listed in the registers table. Note that SDIO is a bidirectional pin used to read or write the XRD9836 internal registers. The R/W bit will define the direction of the bus after Address bits. If R/W = 0, a write to the XRD9836 is performed. If R/W = 1, a read of the XRD9836's internal registers is performed.

During a write operation there must be 18 positive edges of SCLK between the fall of LOAD and the rise of LOAD. If there are more or less than 18, the write operation will not take place. For a write to the XRD9836 the SDIO pin stays configured as an input for entire 18 SCLK's before LOAD goes high. The E0 and E1 bits are dummy (unused) bits.

For a read of the XRD9836 internal registers (R/W=1) the E0 and E1 are used as a transition time for the SDIO pin going from an input to a output. During this time SDIO pin is tri-stated. SDIO is an input while serial port accepts the address of the register to be read and during the E0 and E1 time period transitions to an output for the read operation.

During a read operation the first 18 positive edges are used. If there are less than 18, not all of the data will be output. If there are more than 18, only the first 18 bits will be valid. The data becomes valid after the rising edge of SCLK.

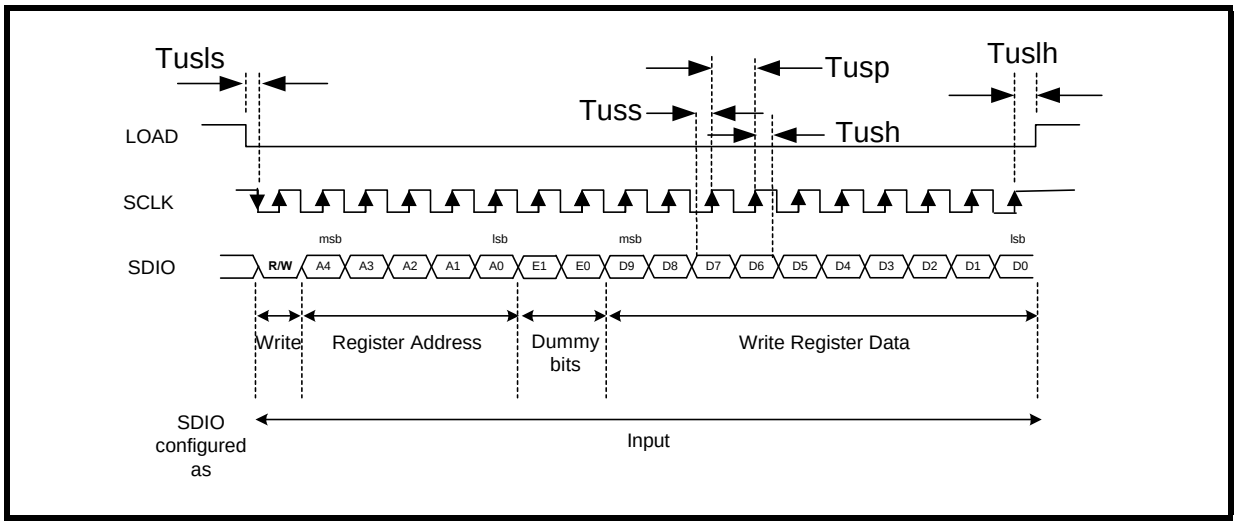


FIGURE 15. SERIAL PORT WRITE TIMING (R/W=0)

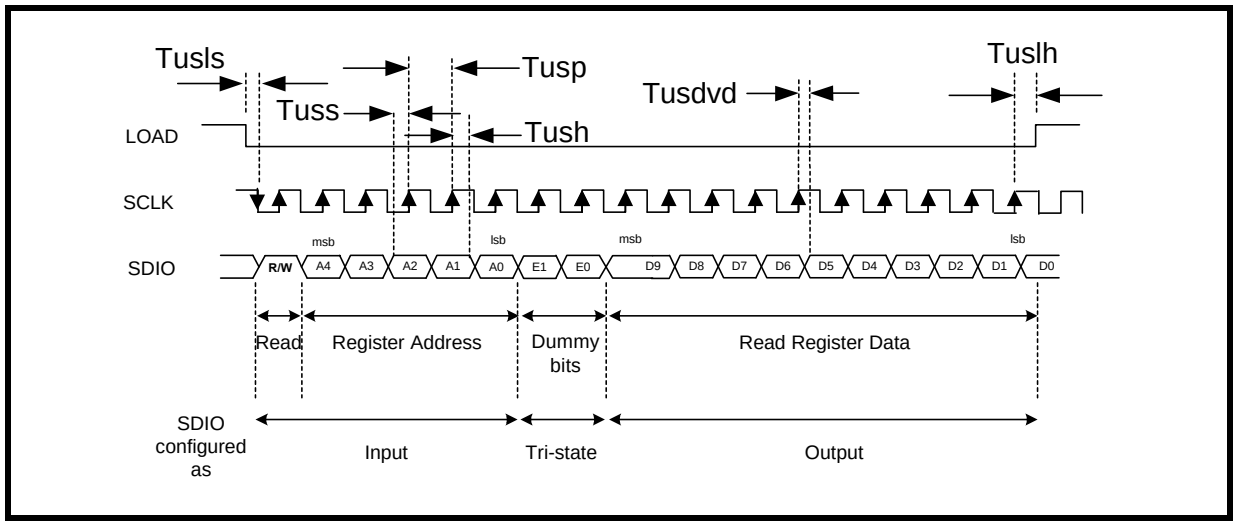


FIGURE 16. SERIAL PORT READ TIMING (R/W=1)

REGISTERS															
	ADDRESS					DATA BITS									
	A4	A3	A2	A1	A0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RED PGA	0	0	0	0	0	RPGA [9]	RPGA [8]	RPGA [7]	RPGA [6]	RPGA [5]	RPGA [4]	RPGA [3]	RPGA [2]	RPGA [1]	RPGA [0]
GREEN PGA	0	0	0	0	1	GPGA [9]	GPGA [8]	GPGA [7]	GPGA [6]	GPGA [5]	GPGA [4]	GPGA [3]	GPGA [2]	GPGA [1]	GPGA [0]
BLUE PGA	0	0	0	1	0	BPGA [9]	BPGA [8]	BPGA [7]	BPGA [6]	BPGA [5]	BPGA [4]	BPGA [3]	BPGA [2]	BPGA [1]	BPGA [0]
RED DYNAMIC OFFSET	0	0	0	1	1	RDOFF [9]	RDOFF [8]	RDOFF [7]	RDOFF [6]	RDOFF [5]	RDOFF [4]	RDOFF [3]	RDOFF [2]	RDOFF [1]	RDOFF [0]
GREEN DYNAMIC OFFSET	0	0	1	0	0	GDOFF [9]	GDOFF [8]	GDOFF [7]	GDOFF [6]	GDOFF [5]	GDOFF [4]	GDOFF [3]	GDOFF [2]	GDOFF [1]	GDOFF [0]
BLUE DYNAMIC OFFSET	0	0	1	0	1	BDOFF [9]	BDOFF [8]	BDOFF [7]	BDOFF [6]	BDOFF [5]	BDOFF [4]	BDOFF [3]	BDOFF [2]	BDOFF [1]	BDOFF [0]
RED FINE OFFSET	0	0	1	1	0	RFOFF [9]	RF0FF [8]	RFOFF [7]	RF0FF [6]	RFOFF [5]	RFOFF [4]	RFOFF [3]	RFOFF [2]	RFOFF [1]	RFOFF [0]
GREEN FINE OFFSET	0	0	1	1	1	GFOFF [9]	GF0FF [8]	GFOFF [7]	GF0FF [6]	GFOFF [5]	GFOFF [4]	GFOFF [3]	GFOFF [2]	GFOFF [1]	GFOFF [0]
BLUE FINE OFFSET	0	1	0	0	0	BFOFF [9]	BF0FF [8]	BFOFF [7]	BF0FF [6]	BFOFF [5]	BFOFF [4]	BFOFF [3]	BFOFF [2]	BFOFF [1]	BFOFF [0]
APOAM RED DYNAMIC OFFSET	0	1	0	0	1	ARDOF [9]	ARDOF [8]	ARDOF [7]	ARDOF [6]	ARDOF [5]	ARDOF [4]	ARDOF [3]	ARDOF [2]	ARDOF [1]	ARDOF [0]
APOAM GREEN DYNAMIC OFFSET	0	1	0	1	0	AGDOF [9]	AGDOF [8]	AGDOF [7]	AGDOF [6]	AGDOF [5]	AGDOF [4]	AGDOF [3]	AGDOF [2]	AGDOF [1]	AGDOF [0]
APOAM BLUE DYNAMIC OFFSET	0	1	0	1	1	ABDOF [9]	ABDOF [8]	ABDOF [7]	ABDOF [6]	ABDOF [5]	ABDOF [4]	ABDOF [3]	ABDOF [2]	ABDOF [1]	ABDOF [0]
APOAM RED FINE OFFSET	0	1	1	0	0	ARFOF [9]	ARFOF [8]	ARFOF [7]	ARFOF [6]	ARFOF [5]	ARFOF [4]	ARFOF [3]	ARFOF [2]	ARFOF [1]	ARFOF [0]
APOAM GREEN FINE OFFSET	0	1	1	0	1	AGFOF [9]	AGFOF [8]	AGFOF [7]	AGFOF [6]	AGFOF [5]	AGFOF [4]	AGFOF [3]	AGFOF [2]	AGFOF [1]	AGFOF [0]
APOAM BLUE FINE OFFSET	0	1	1	1	0	ABFOF [9]	ABFOF [8]	ABFOF [7]	ABFOF [6]	ABFOF [5]	ABFOF [4]	ABFOF [3]	ABFOF [2]	ABFOF [1]	ABFOF [0]
CNTRL/POL	0	1	1	1	1			ADC POL	LCLMP POL	BSAMP POL	VSAMP POL	DLP Disable	PwrDwn	OEB	RESET
DELAY A	1	0	0	0	0			DelayA [7]	DelayA [6]	DelayA [5]	DelayA [4]	DelayA [3]	DelayA [2]	DelayA [1]	DelayA [0]
DELAY B	1	0	0	0	1			DelayB [7]	DelayB [6]	DelayB [5]	DelayB [4]	DelayB [3]	DelayB [2]	DelayB [1]	DelayB [0]
DELAY C	1	0	0	1	0			DelayC [7]	DelayC [6]	DelayC [5]	DelayC [4]	DelayC [3]	DelayC [2]	DelayC [1]	DelayC [0]
DELAY D	1	0	0	1	1			DelayD [7]	DelayD [6]	DelayD [5]	DelayD [4]	DelayD [3]	DelayD [2]	DelayD [1]	DelayD [0]
MODE	1	0	1	0	0			NOFS2	TEST ENABLE	GAIN SELECT	CCD/CIS	CHAN [1]	CHAN [0]	APOAM	GOM
TEST	1	0	1	0	1	do not change	do not change	do not change	do not change	do not change	do not change	do not change	do not change	do not change	do not change

Table 2:

NOTE: *Note: Shaded cells represent unused bits*

Red PGA Register	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RPGA (00000)	RPGA [9]	RPGA [8]	RPGA [7]	RPGA [6]	RPGA [5]	RPGA [4]	RPGA [3]	RPGA [2]	RPGA [1]	RPGA [0]
default	0	0	0	0	0	0	0	0	0	0

RPGA[9:0] is used to set the gain of the Programmable Gain Amplifier (PGA) for the red channel. Code = 0000000000 is minimum gain. Code = 1111111111 is maximum gain.

Green PGA Register	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
GPGA (00001)	GPGA [9]	GPGA [8]	GPGA [7]	GPGA [6]	GPGA [5]	GPGA [4]	GPGA [3]	GPGA [2]	GPGA [1]	GPGA [0]
default	0	0	0	0	0	0	0	0	0	0

GPGA[9:0] is used to set the gain of the Programmable Gain Amplifier (PGA) for the green channel. Code = 0000000000 is minimum gain. Code = 1111111111 is maximum gain.

Blue PGA Register	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BPGA (00010)	BPGA [9]	BPGA [8]	BPGA [7]	BPGA [6]	BPGA [5]	BPGA [4]	BPGA [3]	BPGA [2]	BPGA [1]	BPGA [0]
default	0	0	0	0	0	0	0	0	0	0

BPGA[9:0] sets the gain of the Programmable Gain Amplifier (PGA) for the blue channel. Code = 0000000000 is minimum gain. Code = 1111111111 is maximum gain.

Red Dynamic Offset Register	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RDOFF (00011)	RDOFF [9]	RDOFF [8]	RDOFF [7]	RDOFF [6]	RDOFF [5]	RDOFF [4]	RDOFF [3]	RDOFF [2]	RDOFF [1]	RDOFF [0]
default	0	1	0	1	0	1	0	1	0	1

RDOFF[9:0] sets the course offset level prior to the PGA of the Red channel. Code = 0000000000 is -80mV. Code =1111111111 is +160mV. Default is Code 0101010101 = 0 mV.

Green Dynamic Offset Register	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
GDOFF (00100)	GDOFF [9]	GDOFF [8]	GDOFF [7]	GDOFF [6]	GDOFF [5]	GDOFF [4]	GDOFF [3]	GDOFF [2]	GDOFF [1]	GDOFF [0]
default	0	1	0	1	0	1	0	1	0	1

GDOFF[9:0] sets the course offset level prior to the PGA of the Green channel.
Code = 0000000000 is -80mV. Code =1111111111 is +160mV. Default is Code 0101010101 = 0 mV.

Blue Dynamic Offset Register	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BDOFF (00101)	BDOFF [9]	BDOFF [8]	BDOFF [7]	BDOFF [6]	BDOFF [5]	BDOFF [4]	BDOFF [3]	BDOFF [2]	BDOFF [1]	BDOFF [0]
default	0	1	0	1	0	1	0	1	0	1

BDOFF[9:0] sets the course offset level prior to the PGA of the Blue channel.
Code = 0000000000 is -80mV. Code =1111111111 is +160mV. Default is Code 0101010101 = 0 mV.

Red Fine Offset Register	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RFOFF (00110)	RFOFF [9]	RF0FF [8]	RFOFF [7]	RF0FF [6]	RFOFF [5]	RFOFF [4]	RFOFF [3]	RFOFF [2]	RFOFF [1]	RFOFF [0]
default	1	0	0	0	0	0	0	0	0	0

RFOFF[9:0] sets the fine offset level after the PGA in the Red channel.
Code = 0000000000 is -128mV. Code =1111111111 is +128mV. Default is Code 1000000000 = 0 mV.

Green Fine Offset Register	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
GFOFF (00111)	GFOFF [9]	GFOFF [8]	GFOFF [7]	GFOFF [6]	GFOFF [5]	GFOFF [4]	GFOFF [3]	GFOFF [2]	GFOFF [1]	GFOFF [0]
default	1	0	0	0	0	0	0	0	0	0

GFOFF[9:0] sets the fine offset level after the PGA in the Green channel.
Code = 0000000000 is -128mV. Code =1111111111 is +128mV. Default is Code 1000000000 = 0 mV.

Blue Fine Offset Register	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BFOFF (01000)	BF0FF [9]	BFOFF [8]	BFOFF [7]	BF0FF [6]	BFOFF [5]	BFOFF [4]	BFOFF [3]	BFOFF [2]	BFOFF [1]	BFOFF [0]
default	1	0	0	0	0	0	0	0	0	0

BFOFF[9:0] sets the fine offset level after the PGA in the Blue channel.
Code = 0000000000 is -128mV. Code =1111111111 is +128mV. Default is Code 1000000000 = 0 mV.

APOAM Red Dynamic Offset Register	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ARDOF (01001)	ARDOF [9]	ARDOF [8]	ARDOF [7]	ARDOF [6]	ARDOF [5]	ARDOF [4]	ARDOF [3]	ARDOF [2]	ARDOF [1]	ARDOF [0]
default	0	1	0	1	0	1	0	1	0	1

RDOFF[9:0] sets the course offset level prior to the PGA of the Red channel for even pixels in APOAM Mode.
Code = 0000000000 is -80mV. Code =1111111111 is +160mV. Default is Code 0101010101 = 0 mV.

APOAM Green Dynamic Offset Register	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
AGDOF (01010)	AGDOF [9]	AGDOF [8]	AGDOF [7]	AGDOF [6]	AGDOF [5]	AGDOF [4]	AGDOF [3]	AGDOF [2]	AGDOF [1]	AGDOF [0]
default	0	1	0	1	0	1	0	1	0	1

GDOFF[9:0] sets the course offset level prior to the PGA of the Green channel for even pixels in APOAM Mode.
Code = 0000000000 is -80mV. Code =1111111111 is +160mV. Default is Code 0101010101 = 0 mV.

APOAM Blue Dynamic Offset Register	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ABDOF (01011)	ABDOF [9]	ABDOF [8]	ABDOF [7]	ABDOF [6]	ABDOF [5]	ABDOF [4]	ABDOF [3]	ABDOF [2]	ABDOF [1]	ABDOF [0]
default	0	1	0	1	0	1	0	1	0	1

BDOFF[9:0] sets the course offset level prior to the PGA of the Blue channel for even pixels in APOAM Mode.
Code = 0000000000 is -80mV. Code =1111111111 is +160mV. Default is Code 0101010101 = 0 mV.

APOAM Red Fine Offset Register	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ARFOF (01100)	ARFOF [9]	ARFOF [8]	ARFOF [7]	ARFOF [6]	ARFOF [5]	ARFOF [4]	ARFOF [3]	ARFOF [2]	ARFOF [1]	ARFOF [0]
default	1	0	0	0	0	0	0	0	0	0

RFOFF[9:0] sets the fine offset level after the PGA of the Red channel for even pixels in APOAM Mode. The offset is adjusted in 1mV increments. Code = 0000000000 is -128mV. Code =1111111111 is +128mV. Default is Code 1000000000 = 0 mV.

APOAM Green Fine Offset Register	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
AGFOF (01101)	AGFOF [9]	AGFOF [8]	AGFOF [7]	AGFOF [6]	AGFOF [5]	AGFOF [4]	AGFOF [3]	AGFOF [2]	AGFOF [1]	AGFOF [0]
default	1	0	0	0	0	0	0	0	0	0

GFOFF[9:0] sets the fine offset level after the PGA of the Green channel for even pixels in APOAM Mode. The offset is adjusted in 1mV increments. Code = 0000000000 is -128mV. Code =1111111111 is +128mV. Default is Code 1000000000 = 0 mV.

APOAM Blue Fine Offset Register	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ABFOF (01110)	ABFOF [9]	ABFOF [8]	ABFOF [7]	ABFOF [6]	ABFOF [5]	ABFOF [4]	ABFOF [3]	ABFOF [2]	ABFOF [1]	ABFOF [0]
default	1	0	0	0	0	0	0	0	0	0

BFOFF[9:0] sets the fine offset level after the PGA of the Blue channel for even pixels in APOAM Mode. The offset is adjusted in 1mV increments. Code = 0000000000 is -128mV. Code =1111111111 is +128mV. Default is Code 1000000000 = 0 mV.

Control / Polarity Register	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CNTRL / POL (01111)			ADC POL	LCLMP POL	BSAMP POL	VSAMP POL	DLP DISABLE	PWRDWN	OEB	RESET
default			0	0	0	0	0	0	0	0

The CNTRL / POL register is used to program various options including: input timing polarity control, dynamic low power disable, power down for the chip, output enable, and reset. Reset will reset ALL registers including reset.

All the clock inputs (except the serial interface SCLK) can be programmed to be active high or active low. See the “Timing” section for more information. ADCpol, LCLMPpol, BSAMPpol, and VSAMPpol set the polarity of ADCLK, LCLMP, BSAMP, and VSAMP respectively.

ADCpol - Sets the polarity of the ADCLK input. ADCpol = 0, ADCLK low during VSAMP. ADCpol = 0, ADCLK inverted so that it is high during VSAMP.

LCLMPpol - Sets the polarity of the LCLMP input. LCLMPpol = 0, LCMLP is active high during clamping operation and odd pixel determined from falling edge.

BSAMPpol - Sets the polarity of the BSAMP input. BSAMPpol = 0, BSAMP is active high. The CCD black level is sample by the falling edge. BSAMPpol = 1, BSAMP is active low. The CCD black level is sample by the rising edge.

VSAMPpol - Sets the polarity of the VSAMP input. VSAMPpol = 0, VSAMP is active high. The CCD video level is sample by the falling edge. VSAMPpol = 1, VSAMP is active low. The CCD video level is sample by the rising edge.

DLP DISABLE (ADC Dynamic Low Power Disable)

PWRDWN - Puts the XRD9836 into power down state. PWRDWN = 0, normal operation. PWRDWN = 1, low power state.

OEB - Enables the ADCDO bus. OEB = 0, data valid on ADCDO bus. OEB = 1, ADCDO bus high impedance.

RESET - Will reset the XRD9836 to default (power up) conditions. RESET = 0, normal operation. RESET = 1, all internal registers set to default values and clears itself after ~ 10ns.

Delay Registers	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DelayA (10000)			DelayA [7]	DelayA [6]	DelayA [5]	DelayA [4]	DelayA [3]	DelayA [2]	DelayA [1]	DelayA [0]
default			1	0	0	0	0	0	0	0
DelayB (10001)			DelayB [7]	DelayB [6]	DelayB [5]	DelayB [4]	DelayB [3]	DelayB [2]	DelayB [1]	DelayB [0]
default			0	0	0	0	0	0	0	0
DelayC (10010)			DelayC [7]	DelayC [6]	DelayC [5]	DelayC [4]	DelayC [3]	DelayC [2]	DelayC [1]	DelayC [0]
default			0	0	0	0	0	0	0	0
DelayD (10011)			DelayD [7]	DelayD [6]	DelayD [5]	DelayD [4]	DelayD [3]	DelayD [2]	DelayD [1]	DelayD [0]
default			0	0	0	0	0	0	0	0

DelayA[7:4] - Controls the OGI_DLY. These bits are used to program the timing delay of the ADCLK used to sample the Offset-Gain-Inputs (OGI). Code 0000 is delay of 0ns, and code 1111 is 15ns. Default is 1000 = 7 ns. **OGI_DLY should be larger than VSAMP_OGI_DLY.**

DelayA[3:0] - Controls the ADCO_DLY. These bits are used to program the timing delay of ADCO outputs in relation to ADCLK. Code 0000 is delay of 0ns, and code 1111 is 15ns. Default is 0000 = 0ns. This is used to adjust setup and hold times of the output, for the ASIC chip.

DelayB[7:4] - Controls the BSAMP_LEADING_EDGE_DLY. These bits set the delay for the leading edge of the internal BSAMP pulse. Code 0000 is no delay. The delay increases by 0.5 ns per step to a total of 7.5 ns. Default is 0000 = 0ns.

DelayB[3:0] - Controls the BSAMP_TRAILING_EDGE_DLY. These bits set the delay for the trailing edge of the internal BSAMP pulse. Code 0000 is no delay. The delay increases by 0.5 ns per step to a total of 7.5 ns. Default is 0000 = 0ns.

DelayC[7:4] - Controls the VSAMP_LEADING_EDGE_DLY. These bits set the delay for the leading edge of the internal VSAMP pulse. Code 0000 is no delay. The delay increases by 0.5 ns per step to a total of 7.5 ns. Default is 0000 = 0ns.

DelayC[3:0] - Controls the VSAMP_TRAILING_EDGE_DLY. These bits set the delay for the trailing edge of the internal VSAMP pulse. Code 0000 is no delay. The delay increases by 0.5 ns per step to a total of 7.5 ns. Default is 0000 = 0ns.

DelayD[7:4] - Controls the VSAMP_OGI_DLY. These bits set the delay for the internal VSAMP that is used to transfer the OGI register data to the PGA & OFFSET control registers.

DelayD[3:0] - Controls the ADC_DLY. These bits set the delay of the internal clock used for ADC operation. Code 0000 is no delay. The delay increases by 0.5 ns per step to a total of 7.5 ns. Default is 0000 = 0ns.

Mode Register	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MODES of operation (10100)			NOFS2	TEST ENABLE	GAIN SELECT	CCD/CIS	CHAN [1]	CHAN [0]	APOAM	GOM
default			0	0	0	0	0	0	0	1

NOFS2 - No full scale divided by 2.

Test Enable - Do not modify.

Gain Select - Gain range is 1-10 for Gain Select = 0, and 2-20 for Gain Select = 1.

CCD mode is selected if CCD/CIS is 0, CIS mode is selected if CCD/CIS is 1.

Three channel is selected if CHAN[1] = 0 and CHAN[0] = 0.
One channel red is selected if CHAN[1] = 0 and CHAN[0] = 1.
One channel green is selected if CHAN[1] = 1 and CHAN[0] = 0.
One channel blue is selected if CHAN[1] = 1 and CHAN[0] = 1.

The Alternate Pixel Adjust Mode is selected by setting APOAM to 1. It is used only in Fixed Gain mode i.e. with GOM=0.

The GOM (gain offset mode) bit is used to select either Fixed Gain Offset Mode (GOM=0) or Pixel by Pixel Gain Offset Mode (GOM=1).

TEST	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TEST (10101)										
default	0	0	0	0	0	0	0	0	0	0

Test register used for factory test only. Do not modify

TIMING DIAGRAMS

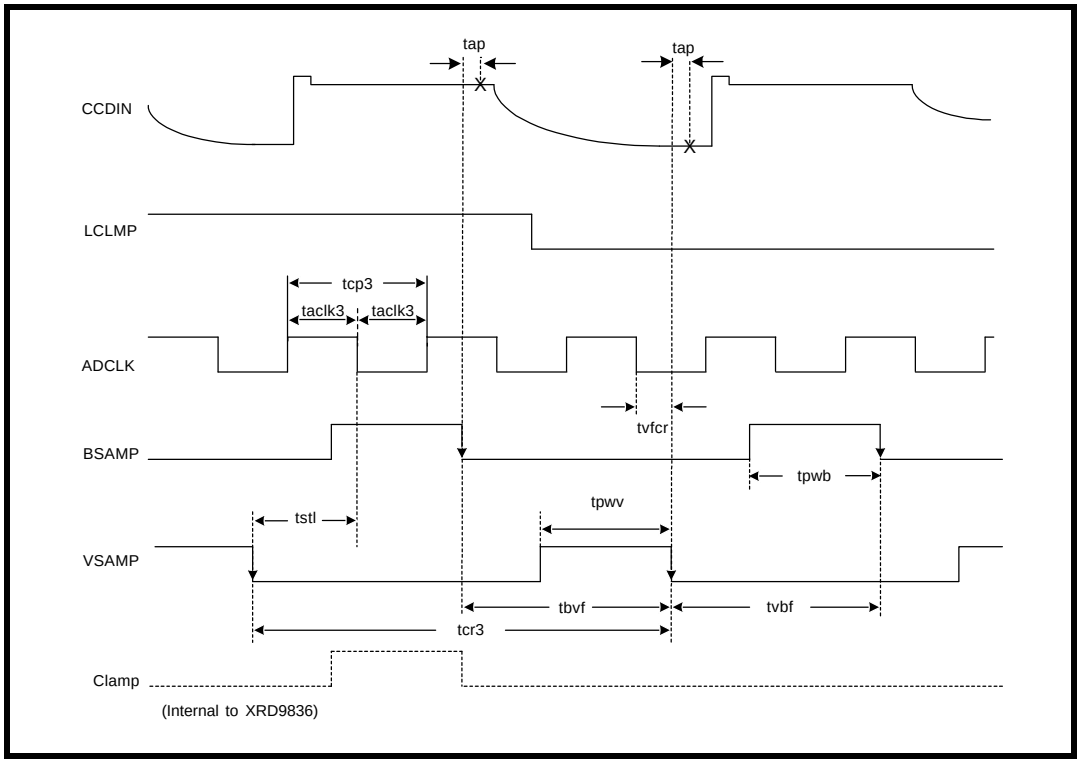


FIGURE 17. 3-CHANNEL CDS MODE (ALL POLARITY BITS =0)

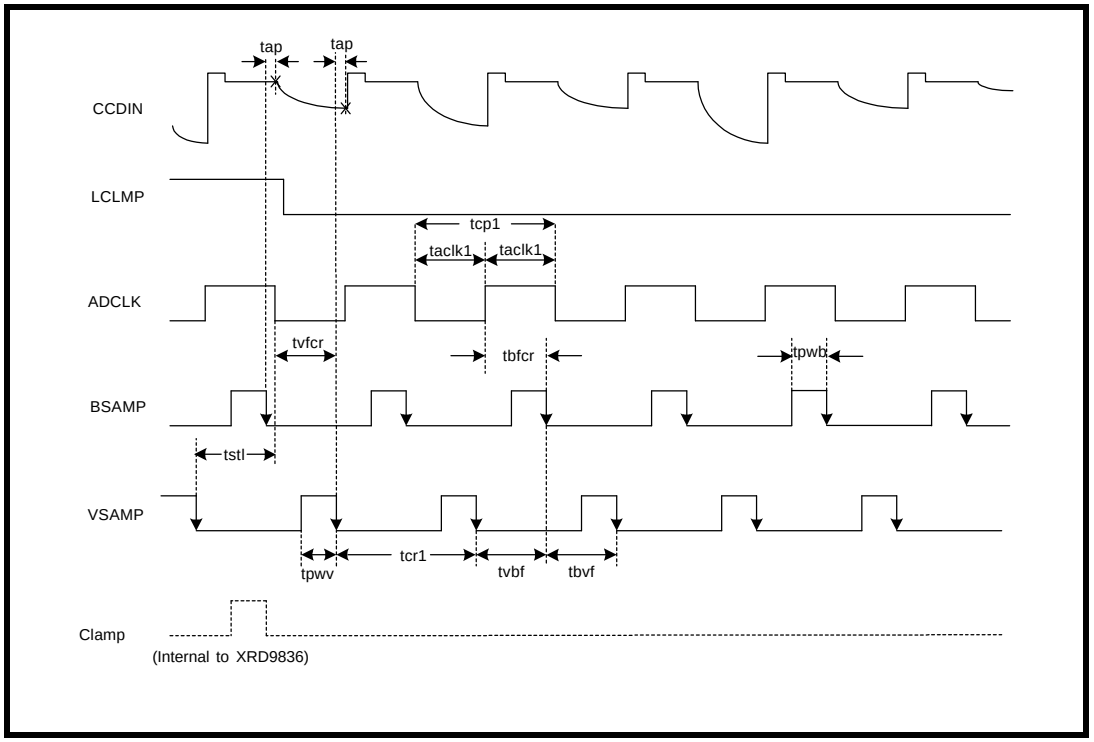


FIGURE 18. 1-CHANNEL CDS MODE (ALL POLARITY BITS=0)

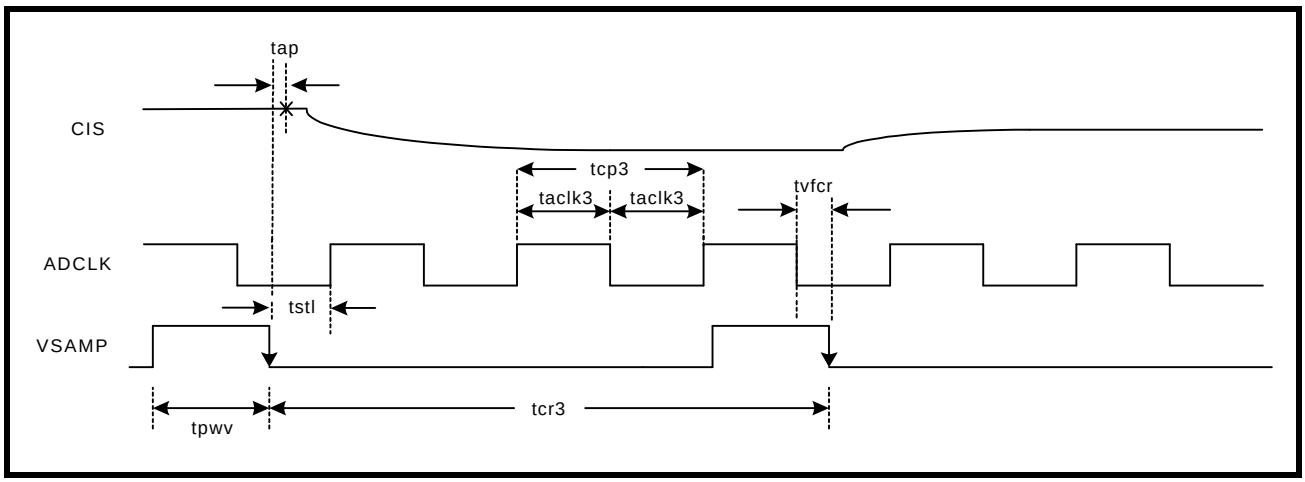


FIGURE 19. 3-CHANNEL CIS MODE (ALL POLARITY BITS = 0, CCD/CIS BIT = 1)

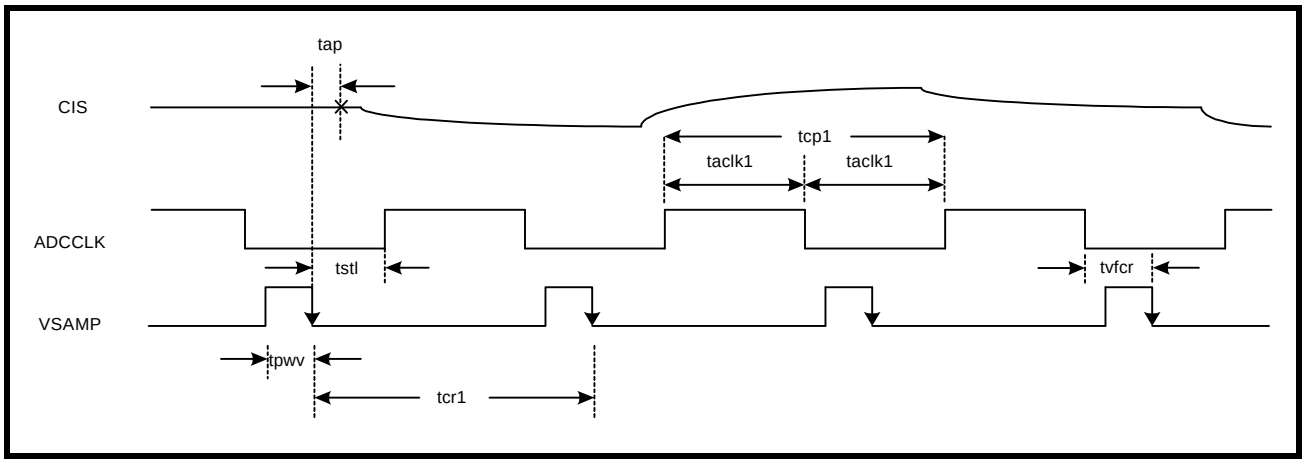


FIGURE 20. 1-CHANNEL CIS MODE (ALL POLARITY BITS = 0, CCD/CIS BIT = 1)

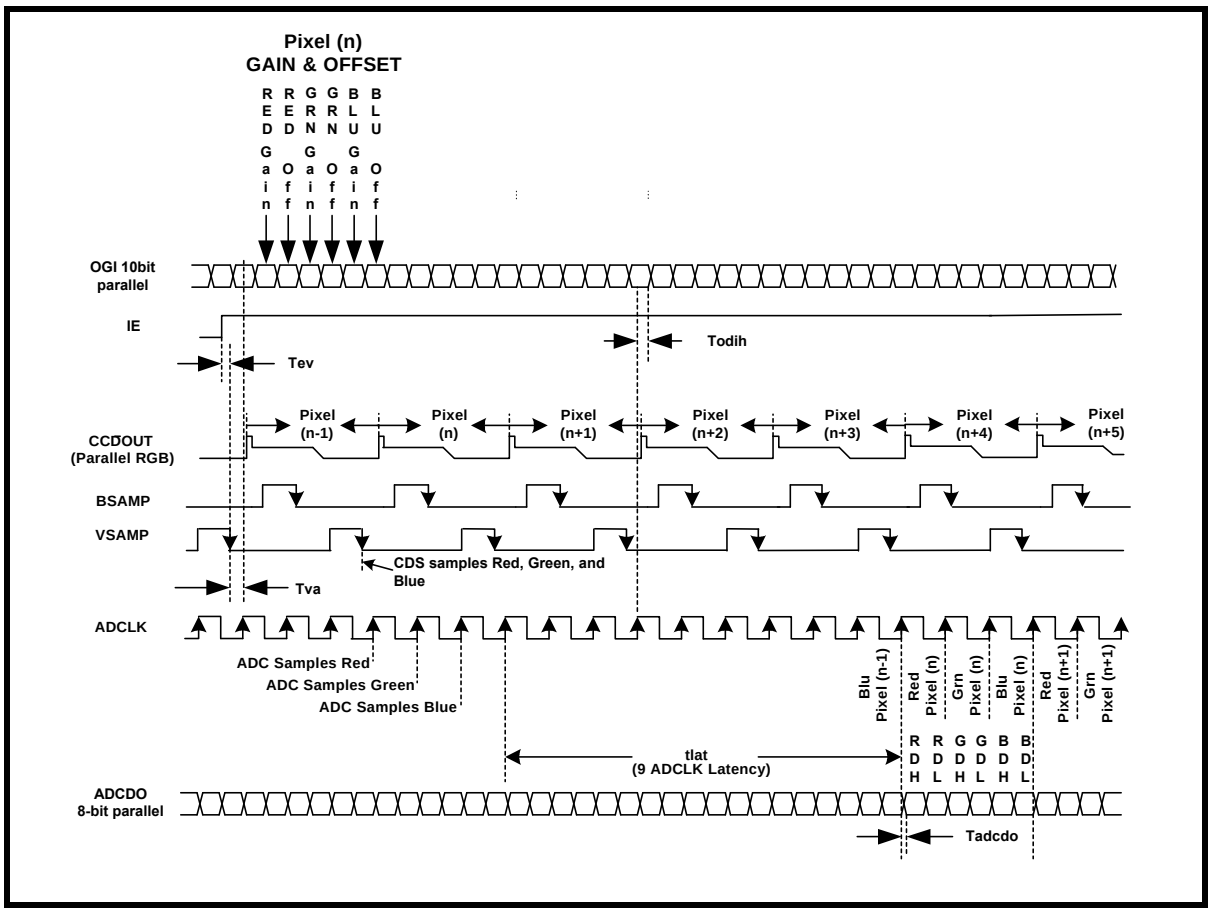


FIGURE 21. 3-CHANNEL LATENCY FOR PARALLEL ADCDO (OUTPUT DATA BUS) & OGI (INPUT BUS)

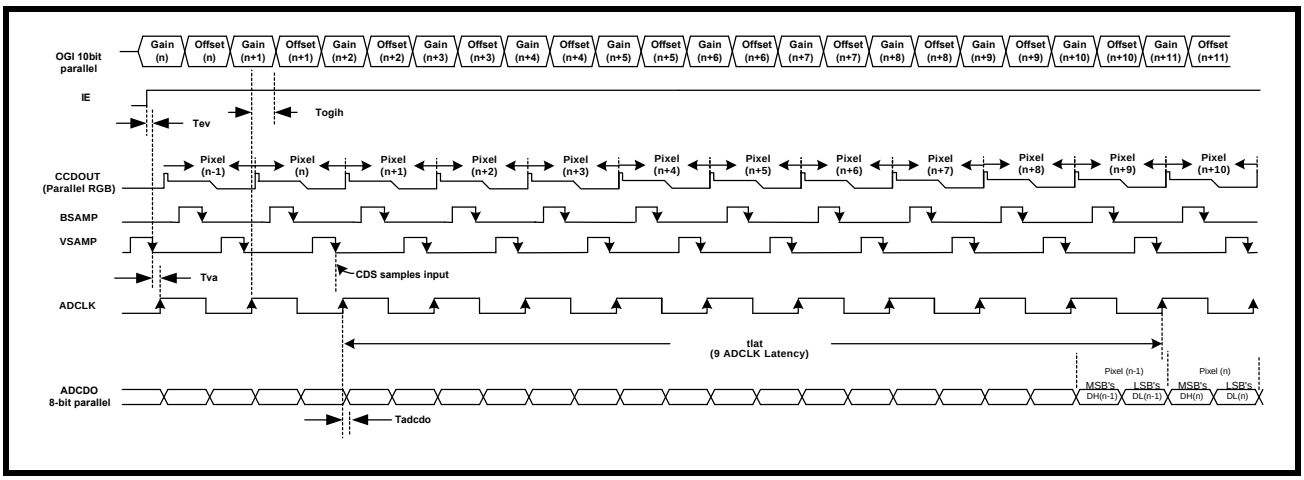


FIGURE 22. 1-CHANNEL LATENCY FOR PARALLEL ADCDO (OUTPUT DATA BUS) & OGI (INPUT BUS)

APPLICATION NOTES AND SCHEMATICS

See Figure 23 for a typical CCD application hookup. The diagram shows an interface to a standard 3 channel output CCD. Both the ADC Output and OGI Control are parallel interfaces to the system ASIC controller. The timing inputs are provided by the system ASIC or timing generator (TG). The serial port control is typically sourced from a micro processor or the system ASIC.

It is recommended that all AGND, DGND and OGND pins, be connected to the analog ground plane under the XRD9836. All VDD's should be supplied from a low noise, well filtered regulator which derives the power supply voltage from the CCD power supply. All of the AVDD pins are analog power supplies and should be decoupled locally to the nearest ground pin with at 0.1uF, high frequency capacitor. The DVDD and OVDD power pins should be locally decoupled to the nearest ground pin also. DVDD and OVDD should be connected to the same power supply network as the digital ASCI which receives data from the XRD9836.

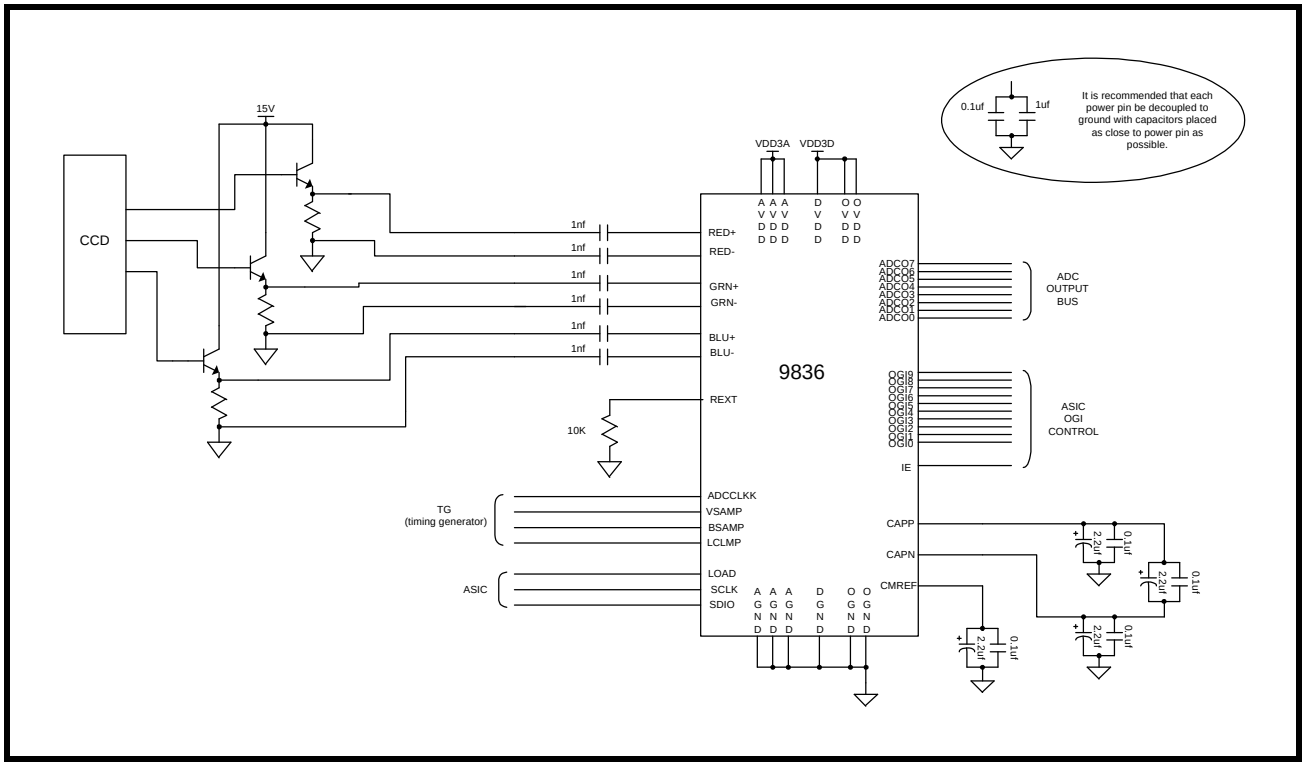


FIGURE 23. TYPICAL CCD APPLICATION DIAGRAM FOR THE XRD9836

The XRD9836 has an input range limitation of 1V maximum for a CCD input. If the maximum CCD output signal swing is greater than 1V, a resisitive divider network on the inputs can be used to reduce the CCD output to meet the 1V input max requirement of the XRD9836 inputs. See Figure 24 for a typical implementation of a resistor divider. Each input channel will require a matching divider network.

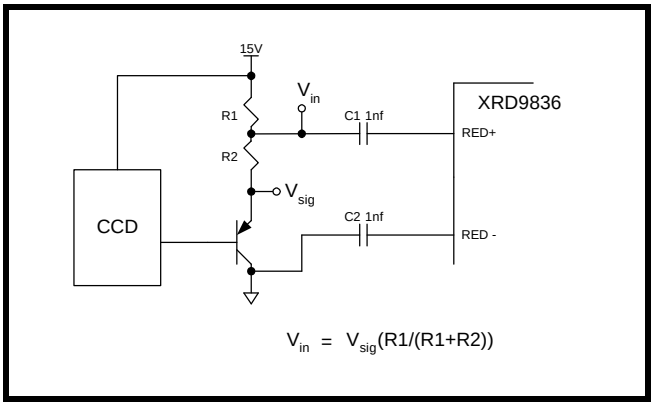


FIGURE 24. INPUT RESISTIVE DIVIDER NETWORK

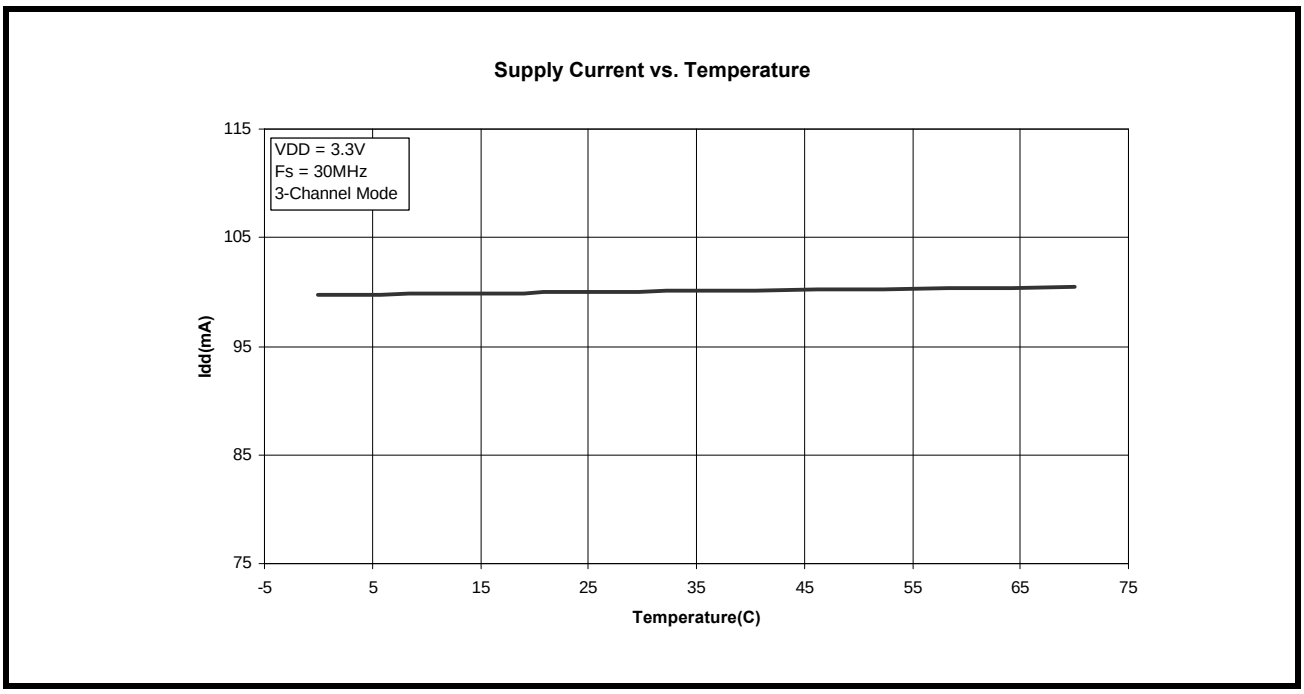


FIGURE 25. XRD9836 TYPICAL IDD VS TEMPERTURE

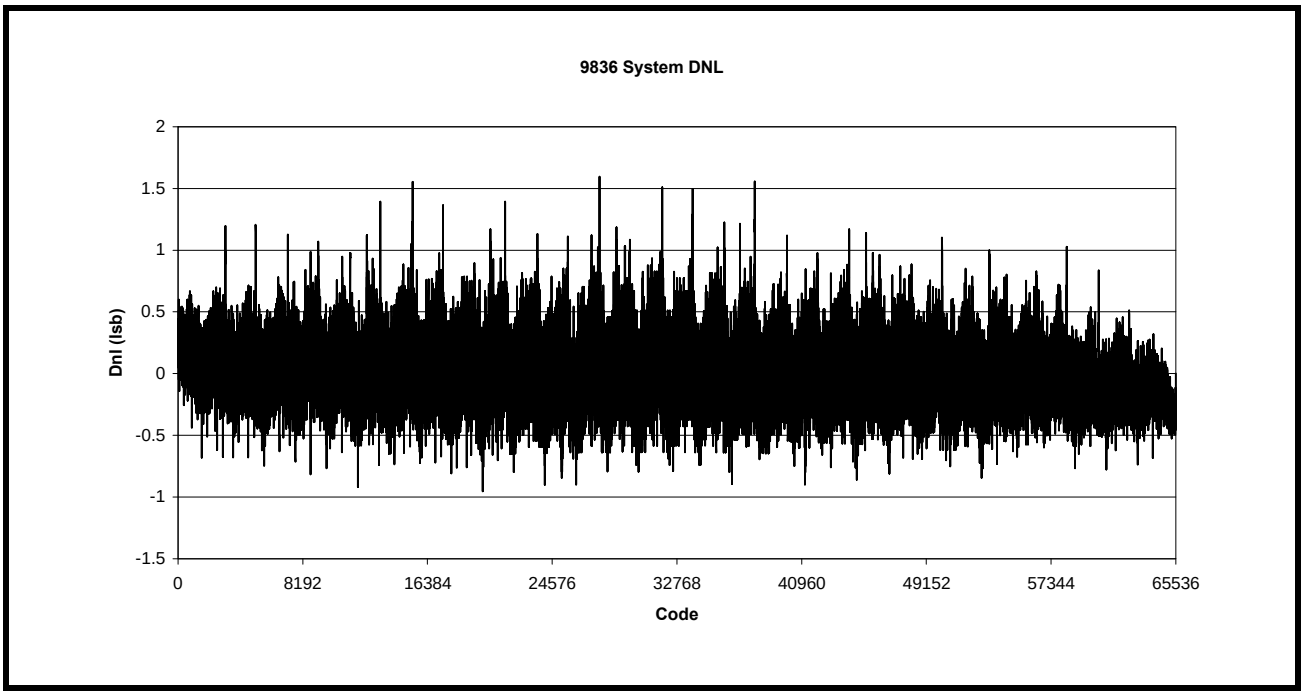
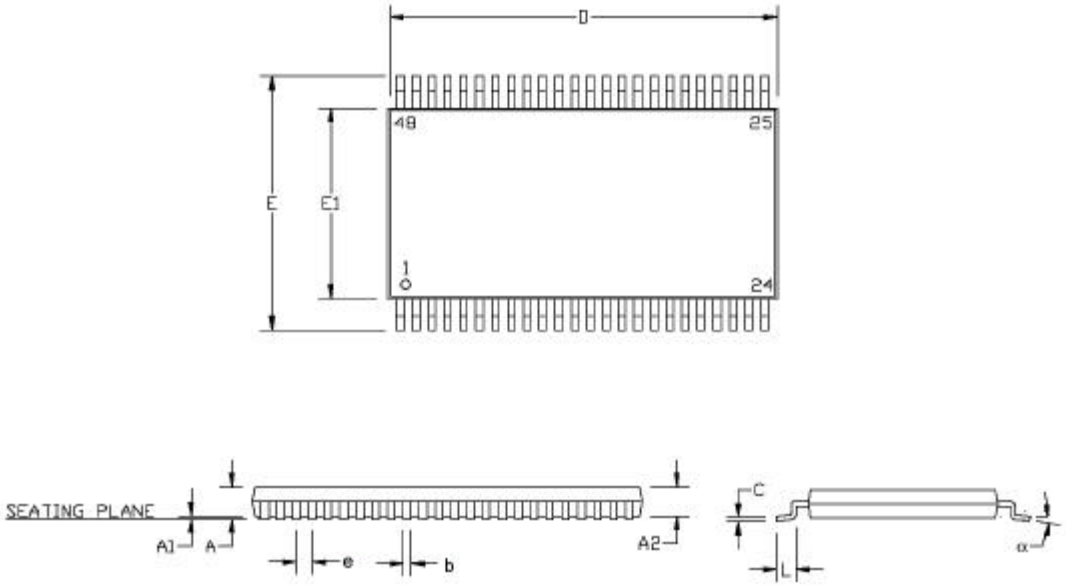


FIGURE 26. TYPICAL XRD9836 DNL FOR RED CHANNEL IN 3-CH MODE

PACKAGE DRAWING:

48 LEAD THIN SHRINK SMALL OUTLINE
(6.1mm TSSOP)
Rev. 2.01



Note: The control dimension is in millimeters.

	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.033	0.047	0.85	1.20
A1	0.002	0.006	0.05	0.15
A2	0.031	0.041	0.80	1.05
b	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.488	0.496	12.40	12.60
E	0.311	0.327	7.90	8.30
E1	0.236	0.244	6.00	6.20
e	0.0197 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
α	0°	8°	0°	8°

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