

STE48NM50

N-CHANNEL 550V @ Tjmax - 0.08Ω - 48A ISOTOP MDmesh™ MOSFET

Table 1: General Features

TYPE	V _{DSS} (@Tjmax)	R _{DS(on)}	Ι _D
STE48NM50	550V	< 0.1Ω	48 A

- TYPICAL $R_{DS}(on) = 0.08\Omega$
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- 100% AVALANCHE TESTED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE
- TIGHT PROCESS CONTROL AND HIGH MANUFACTURING YIELDS

DESCRIPTION

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

APPLICATIONS

The MDmesh[™] family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.

Figure 1: Package

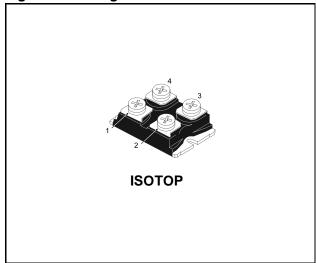


Figure 2: Internal Schematic Diagram

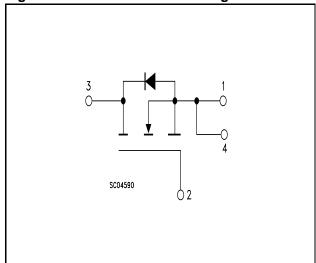


Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING	
STE48NM50	E48NM50	ISOTOP	TUBE	

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Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V _{GS}	Gate- source Voltage	±30	V
ΙD	Drain Current (continuous) at T _C = 25°C	48	А
I _D	Drain Current (continuous) at T _C = 100°C	30	А
I _{DM} (•)	Drain Current (pulsed)	192	А
P _{TOT}	Total Dissipation at T _C = 25°C	450	W
	Derating Factor	3.6	W/°C
dv/dt (*)	Peak Diode Recovery voltage slope	15	V/ns
V_{ISO}	Insulation Winthstand Voltage (AC-RMS)	2500	V
T _{stg}	Storage Temperature	-65 to 150	°C
Tj	Max. Operating Junction Temperature	150	°C

^(•)Pulse width limited by safe operating area

Table 4: Thermal Data

Rthj-case	Thermal Resistance Junction-case	Max	0.28	°C/W
Rthc-sink (**)	Thermal Resistance Case-sink	Тур	0.05	°C/W

^(**) with conductive GREASE Applies

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	15	Α
Eas	Single Pulse Avalanche Energy (starting $T_j = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 50$ V)	810	mJ

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)

Table 6: On/Off

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0$	500			V
I _{DSS}	Zero Gate Voltage	V _{DS} = Max Rating			10	μA
	Drain Current (V _{GS} = 0)	V _{DS} = Max Rating, T _C = 125°C			100	μΑ
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 30V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	3	4	5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 24A		0.08	0.1	Ω

^(*) I_{SD} \leq 48A, di/dt \leq 400 A/ μ s, V_{DD} \leq V(BR)DSS, T_j \leq T_{JMAX}.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Table 7: Dynamic

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
g _{fs} (1)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, $I_D = 24A$		20		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V$, f = 1 MHz, $V_{GS} = 0$		3700 610 80		pF pF pF
R _G	Gate Input Resistance	f=1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		1.7		Ω
$\begin{array}{c} t_{\text{d(on)}} \\ t_{\text{r}} \\ t_{\text{d(off)}} \\ t_{\text{f}} \\ t_{\text{c}} \end{array}$	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time Cross-over Time	$V_{DD}=250$ V, $I_{D}=24$ A $R_{G}=4.7\Omega$ $V_{GS}=10$ V (see Figure 14)		40 35 18 23 44		ns ns ns ns ns
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 400V, I_D = 48 A, V_{GS} = 10V (see Figure 18)		87 23 42	117	nC nC nC

Table 8: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain Current				48	Α
I _{SDM} (2)	Source-drain Current (pulsed)				192	Α
V _{SD} (1)	Forward On Voltage	$I_{SD} = 48 \text{ A}, V_{GS} = 0$			1.5	V
t _{rr} Q _{rr} I _{rrm}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 40 A, di/dt = 100 A/µs, V_{DD} = 100 V, T_{j} = 25°C (see Figure 16)		520 7.8 30		ns µC A
t _{rr} Q _{rr} I _{rrm}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 40 \text{ A, di/dt} = 100 \text{ A/µs,}$ $V_{DD} = 100 \text{ V, T}_j = 150 ^{\circ}\text{C}$ (see Figure 16)		680 11.2 33		ns µC A

Note: 1. Pulsed: Pulse duration = 300 μ s, duty cycle 1.5 %.

2. Pulse width limited by safe operating area.



Figure 3: Safe Operating Area

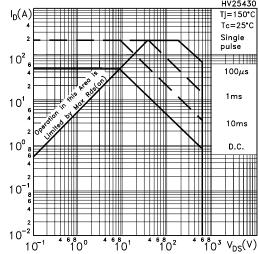


Figure 4: Output Characteristics

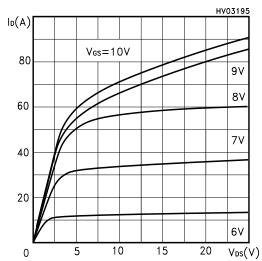


Figure 5: Transconductance

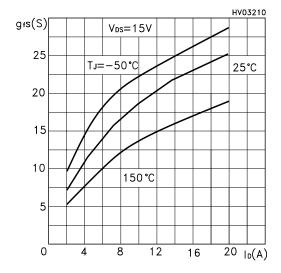


Figure 6: Thermal Impedance

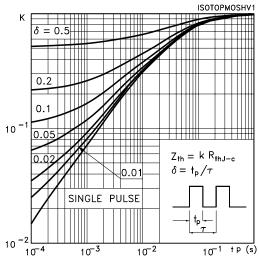


Figure 7: Transfer Characteristics

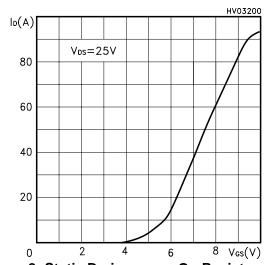


Figure 8: Static Drain-source On Resistance

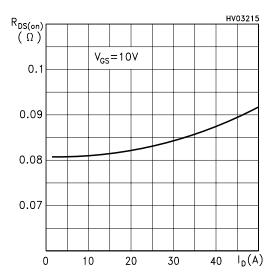


Figure 9: Gate Charge vs Gate-source Voltage

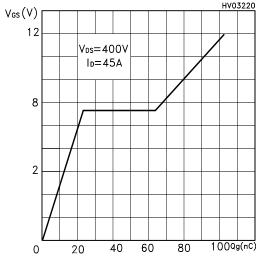


Figure 10: Normalized Gate Thereshold Voltage vs Temperature

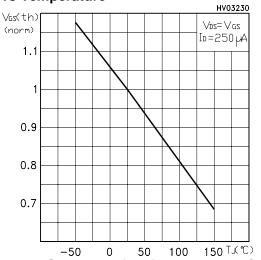


Figure 11: Source-Drain Diode Forward Characteristics

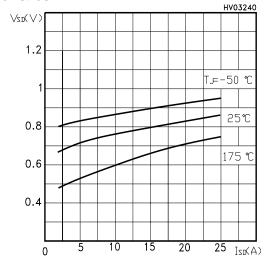


Figure 12: Capacitance Variations

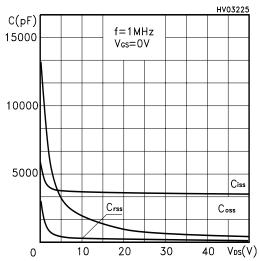


Figure 13: Normalized On Resistance vs Temperature

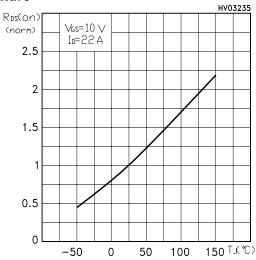


Figure 14: Unclamped Inductive Load Test Circuit

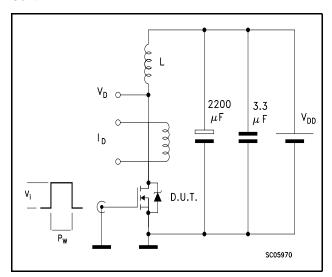


Figure 15: Switching Times Test Circuit For Resistive Load

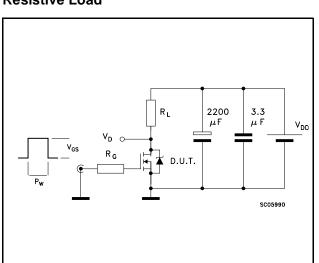


Figure 16: Test Circuit For Inductive Load Switching and Diode Recovery Times

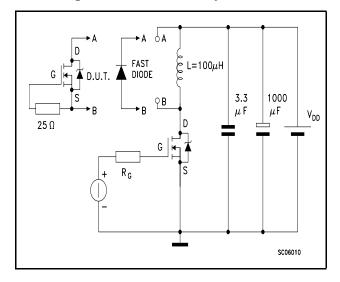


Figure 17: Unclamped Inductive Wafeform

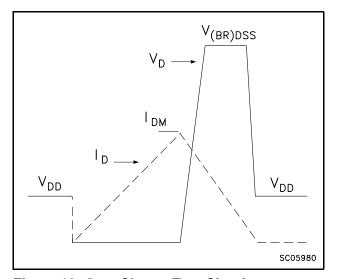
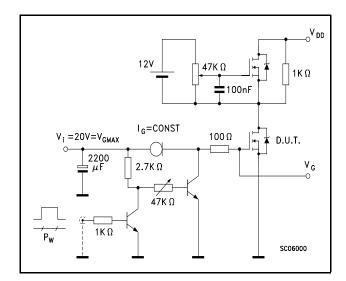


Figure 18: Gate Charge Test Circuit



A7/.

ISOTOP MECHANICAL DATA

DIM.		mm			inch	
Dilvi.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
Α	11.8		12.2	0.466		0.480
В	8.9		9.1	0.350		0.358
С	1.95		2.05	0.076		0.080
D	0.75		0.85	0.029		0.033
E	12.6		12.8	0.496		0.503
F	25.15		25.5	0.990		1.003
G	31.5		31.7	1.240		1.248
Н	4			0.157		
J	4.1		4.3	0.161		0.169
К	14.9		15.1	0.586		0.594
L	30.1		30.3	1.185		1.193
М	37.8		38.2	1.488		1.503
N	4			0.157		
0	7.8		8.2	0.307		0.322

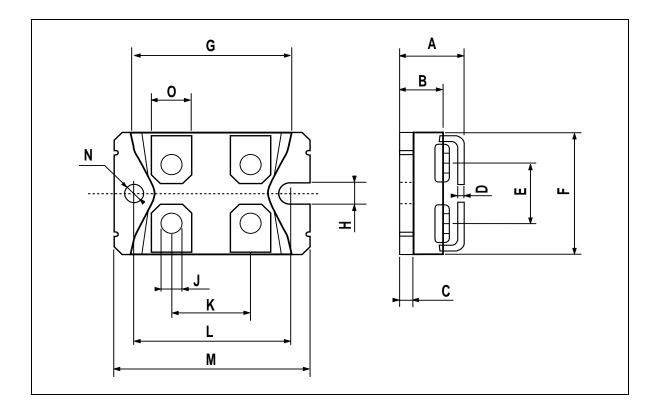




Table 9: Revision History

Date	Revision	Description of Changes
30/Mar/2005	2	Modified value in table 7

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