

IRAM136-0760A

Series

5A, 600V

with Open Emitter Pins

Description

International Rectifier's IRAM136-0760A is a 5A, 600V Integrated Power Hybrid IC with Open Emitter pins for advanced Appliance Motor Drives applications such as energy efficient Washing Machine and Refrigerator Compressor Drivers. IR's technology offers an extremely compact, high performance AC motor-driver in a single isolated package to simplify design.

This advanced HIC is a combination of IR's low $V_{CE(on)}$ Trench IGBT technology and the industry benchmark 3 phase high voltage, high speed driver (3.3V compatible) in a fully isolated thermally enhanced package. A built-in high precision temperature monitor and over-current protection feature, along with the short-circuit rated IGBTs and integrated under-voltage lockout function, deliver high level of protection and fail-safe operation. Using a Single in line package (SIP05) with full transfer mold structure and $CTI > 600$ minimizes PCB space and resolves isolation problems to heatsink.

Features

- Integrated gate drivers and bootstrap diodes
- Temperature monitor
- Protection shutdown pin
- Low $V_{CE(on)}$ Trench IGBT technology
- Undervoltage lockout for all channels
- Matched propagation delay for all channels
- 3.3V Schmitt-triggered input logic
- Cross-conduction prevention logic
- Lower di/dt gate driver for better noise immunity
- Motor Power range 0.1~0.5kW / 85~253 Vac
- Isolation 2000V_{RMS} min and $CTI > 600$



Absolute Maximum Ratings

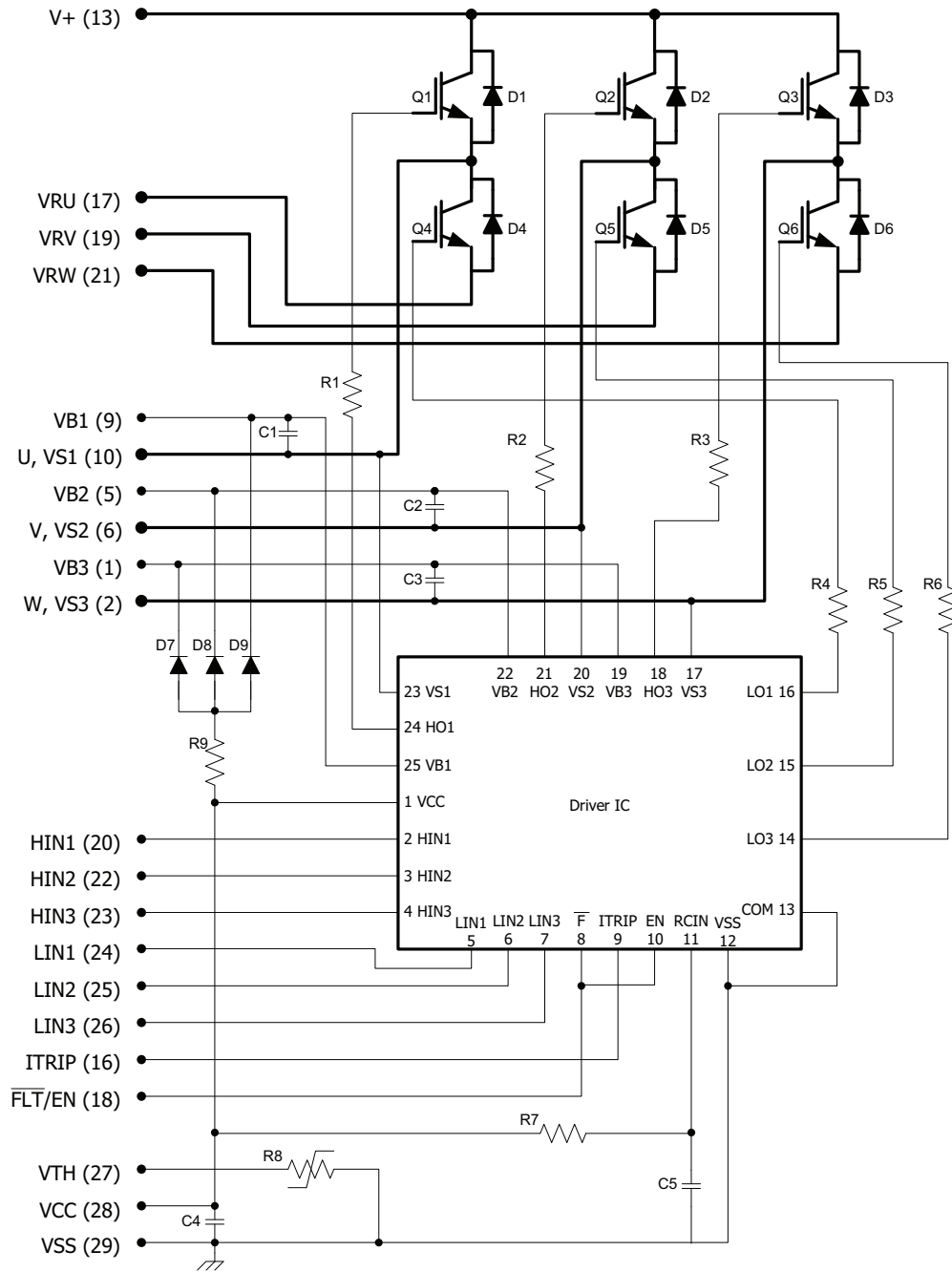
V_{CES} / V_{RRM}	IGBT/ FW Diode Blocking Voltage	600	V
V^+	Positive Bus Input Voltage	450	
$I_o @ T_C=25^\circ\text{C}$	RMS Phase Current (Note 1)	5	A
$I_o @ T_C=100^\circ\text{C}$	RMS Phase Current (Note 1)	3.5	
I_{pk}	Maximum Peak Phase Current (Note 2)	5.5	
F_p	Maximum PWM Carrier Frequency	20	kHz
P_d	Maximum Power dissipation per IGBT @ $T_C = 25^\circ\text{C}$	18	W
V_{ISO}	Isolation Voltage (1min)	2000	V _{RMS}
T_J (IGBT & Diode & IC)	Maximum Operating Junction Temperature	+150	°C
T_C	Operating Case Temperature Range	-20 to +100	
T_{STG}	Storage Temperature Range	-40 to +125	
T	Mounting torque Range (M3 screw)	0.8 to 1.0	Nm

Note 1: Sinusoidal Modulation at $V^+ = 320\text{V}$, $T_J = 150^\circ\text{C}$, $F_{PWM} = 16\text{kHz}$, Modulation Depth=0.8, PF=0.6, See Figure 3.

Note 2: $t_p < 100\text{ms}$, $T_C = 25^\circ\text{C}$, $F_{PWM} = 16\text{kHz}$.

IRAM136-0760A

Internal Electrical Schematic – IRAM136-0760A



Absolute Maximum Ratings (Continued)

Symbol	Parameter	Min	Max	Units	Conditions
$P_{BR \text{ Peak}}$	Bootstrap Resistor Peak Power (Single Pulse)	---	15.0	W	$t_p=100\mu s$, $T_C=100^\circ C$ ESR / ERJ series
$V_{S1,2,3}$	High side floating supply offset voltage	$V_{B1,2,3} - 20$	$V_{B1,2,3} + 0.3$	V	
$V_{B1,2,3}$	High side floating supply voltage	-0.3	600	V	
V_{CC}	Low Side and logic fixed supply voltage	-0.3	20	V	
V_{IN}	Input voltage LIN, HIN, I_{Trip}	-0.3	Lower of ($V_{SS}+15V$) or $V_{CC}+0.3V$	V	

Inverter Section Electrical Characteristics @ $T_J= 25^\circ C$

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	---	---	V	$V_{IN}=0V$, $I_C=250\mu A$
$\Delta V_{(BR)CES} / \Delta T$	Temperature Coeff. Of Breakdown Voltage	---	0.3	---	V/ $^\circ C$	$V_{IN}=0V$, $I_C=250\mu A$ ($25^\circ C - 150^\circ C$)
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	---	1.7	2.0	V	$I_C=3.5A$ $T_J=25^\circ C$, $V_{CC}=15V$
		---	2.1	---		$I_C=3.5A$ $T_J=150^\circ C$
I_{CES}	Zero Gate Voltage Collector Current	---	5	80	μA	$V_{IN}=0V$, $V^+=600V$
		---	80	---		$V_{IN}=0V$, $V^+=600V$, $T_J=150^\circ C$
V_{FM}	Diode Forward Voltage Drop	--	1.6	2.3	V	$I_F=3.5A$
		---	1.4	---		$I_F=3.5A$, $T_J=150^\circ C$
V_{BDFM}	Bootstrap Diode Forward Voltage Drop	--	1.2	---	V	$I_F=1A$
R_{BR}	Bootstrap Resistor Value	---	22	---	Ω	$T_J=25^\circ C$
$\Delta R_{BR}/R_{BR}$	Bootstrap Resistor Tolerance	---	---	± 5	%	$T_J=25^\circ C$

Inverter Section Switching Characteristics @ $T_J = 25^\circ\text{C}$

Symbol	Parameter	Min	Typ	Max	Units	Conditions
E_{ON}	Turn-On Switching Loss	---	210	340	μJ	$I_C=3.5\text{A}$, $V^+=400\text{V}$ $V_{CC}=15\text{V}$, $L=1.2\text{mH}$ Energy losses include "tail" and diode reverse recovery
E_{OFF}	Turn-Off Switching Loss	---	20	30		
E_{TOT}	Total Switching Loss	---	245	370		
E_{REC}	Diode Reverse Recovery energy	---	15	25		
t_{RR}	Diode Reverse Recovery time	---	135	---	ns	See CT1
E_{ON}	Turn-on Switching Loss	---	300	---	μJ	$I_C=3.5\text{A}$, $V^+=400\text{V}$ $V_{CC}=15\text{V}$, $L=1.2\text{mH}$, $T_J=150^\circ\text{C}$ Energy losses include "tail" and diode reverse recovery
E_{OFF}	Turn-off Switching Loss	---	50	---		
E_{TOT}	Total Switching Loss	---	350	---		
E_{REC}	Diode Reverse Recovery energy	---	30	---		
t_{RR}	Diode Reverse Recovery time	---	170	---	ns	See CT1
Q_G	Turn-On IGBT Gate Charge	---	9	13	nC	$I_C=4\text{A}$, $V^+=400\text{V}$, $V_{CC}=15\text{V}$
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE				$T_J=150^\circ\text{C}$, $I_C=3.5\text{A}$, $V_p=600\text{V}$ $V^+=450\text{V}$ $V_{CC}=+15\text{V}$ to 0V See CT3
SCSOA	Short Circuit Safe Operating Area	5	---	---	μs	$T_J=25^\circ\text{C}$, $V_p=600\text{V}$, $V^+=360\text{V}$, $V_{CC}=+15\text{V}$ to 0V See CT2
I_{CSC}	Short Circuit Collector Current	---	30	---	A	$T_J=25^\circ\text{C}$, $V^+=400\text{V}$, $V_{CC}=15\text{V}$ See CT2

Recommended Operating Conditions Driver Function

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. All voltages are absolute referenced to COM. The V_S offset is tested with all supplies biased at 15V differential (Note 3)

Symbol	Definition	Min	Typ	Max	Units
$V_{B1,2,3}$	High side floating supply voltage	V_S+12	V_S+15	V_S+20	V
$V_{S1,2,3}$	High side floating supply offset voltage	Note 4	---	450	
V_{CC}	Low side and logic fixed supply voltage	12	15	20	V
V_{ITRIP}	I_{TRIP} input voltage	V_{SS}	---	$V_{SS}+5$	
V_{IN}	Logic input voltage LIN, HIN, $\overline{\text{FLT/EN}}$	V_{SS}	---	$V_{SS}+5$	V
HIN	High side PWM pulse width	1	---	---	μs
Deadtime	External dead time between HIN and LIN	1	---	---	μs

Note 3: For more details, see IR21364 data sheet

Note 4: Logic operational for V_S from COM-5V to COM+600V. Logic state held for V_S from COM-5V to COM- V_{BS} . (please refer to DT97-3 for more details)

Static Electrical Characteristics Driver Function @ T_j= 25°C

V_{BIAS} (V_{CC}, V_{BS1,2,3})=15V, unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to COM and are applicable to all six channels. (Note 3)

Symbol	Definition	Min	Typ	Max	Units
V _{IN,th+}	Positive going input threshold for LIN, HIN, $\overline{\text{FLT/EN}}$	2.5	---	---	V
V _{IN,th-}	Negative going input threshold for LIN, HIN, $\overline{\text{FLT/EN}}$	---	---	0.8	V
V _{CCUV+} , V _{BSUV+}	V _{CC} and V _{BS} supply undervoltage, Positive going threshold	10.6	11.1	11.6	V
V _{CCUV-} , V _{BSUV-}	V _{CC} and V _{BS} supply undervoltage, Negative going threshold	10.4	10.9	11.4	V
V _{CCUVH} , V _{BSUVH}	V _{CC} and V _{BS} supply undervoltage lock-out hysteresis	---	0.2	---	V
I _{QBS}	Quiescent V _{BS} supply current	---	---	120	μA
I _{QCC}	Quiescent V _{CC} supply current	---	---	4	mA
I _{LK}	Offset Supply Leakage Current	---	---	50	μA
I _{IN+}	Input bias current V _{IN} =3.3V for LIN, HIN, $\overline{\text{FLT/EN}}$	---	100	195	μA
I _{IN-}	Input bias current V _{IN} =0V for LIN, HIN, $\overline{\text{FLT/EN}}$	-1	--	---	μA
I _{TRIP+}	I _{TRIP} bias current V _{T/ITRIP} =3.3V	---	3.3	6	μA
I _{TRIP-}	I _{TRIP} bias current V _{T/ITRIP} =0V	-1	---	---	μA
V(I _{TRIP})	I _{TRIP} threshold Voltage	0.44	0.49	0.54	V
V(I _{TRIP} , HYS)	I _{TRIP} Input Hysteresis	---	0.07	---	V
R _{on_FLT}	Fault low on resistance	---	50	100	Ω

Dynamic Electrical Characteristics @ T_j= 25°C

Driver only timing unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units	Conditions
T _{ON}	Input to Output propagation turn-on delay time (see fig.11)	---	0.7	---	μs	I _C =3.5A, V ⁺ =300V
T _{OFF}	Input to Output propagation turn-off delay time (see fig. 11)	---	0.7	---	μs	
T _{FILIN}	Input filter time (HIN,LIN, $\overline{\text{FLT/EN}}$)	100	200	---	ns	V _{IN} =0 or V _{IN} =5V
T _{EN}	EN to output propagation delay	300	450	600	ns	V _{IN} =0 or V _{IN} =5V, V _{EN} =0
T _{FLT}	I _{TRIP} to Fault propagation delay	400	600	800	ns	V _{IN} =0 or V _{IN} =5V, V _{ITRIP} =5V
T _{BLT-ITRIP}	I _{TRIP} Blanking Time	100	150	---	ns	V _{IN} =0 or V _{IN} =5V, V _{ITRIP} =5V
T _{ITRIP}	I _{TRIP} to six switch turn-off propagation delay (see fig. 2)	---	---	1.75	μs	I _C =3.5A, V ⁺ =300V
D _T	Dead Time	220	290	360	ns	V _{IN} =0 or V _{IN} =5V
M _T	Matching Propagation Delay Time (On & Off) all channels	---	40	75	ns	External dead time > 400ns
T _{FLT-CLR}	FAULT clear time (see fig. 2)	---	1.7	---	ms	T _C = 25°C

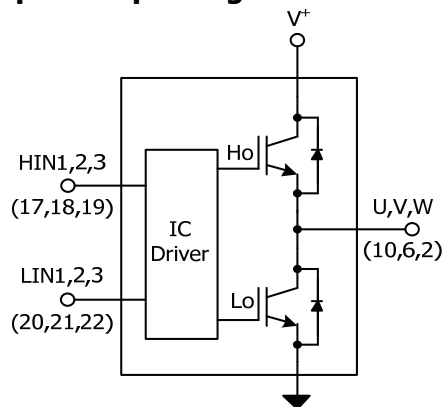
Thermal and Mechanical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$R_{th(J-C)}$	Thermal resistance, per IGBT	---	6.4	7.0	°C/W	Inverter Operating Condition Flat, greased surface. Heatsink compound thermal conductivity 1W/mK
$R_{th(J-C)}$	Thermal resistance, per Diode	---	9.0	9.9		
$R_{th(C-S)}$	Thermal resistance, C-S	---	0.1	---		
C_D	Creepage Distance, from pins to backside of module	3.2	---	---	mm	See outline Drawings
CTI	Comparative Tracking Index	600	---	---	V	

Internal NTC - Thermistor Characteristics

Parameter	Definition	Min	Typ	Max	Units	Conditions
R_{25}	Resistance	97	100	103	k Ω	$T_C = 25^\circ\text{C}$
R_{125}	Resistance	2.25	2.52	2.80	k Ω	$T_C = 125^\circ\text{C}$
B	B-constant (25-50°C)	4165	4250	4335	k	$R_2 = R_1 e^{[B(1/T_2 - 1/T_1)]}$
Temperature Range		-40		125	°C	
Typ. Dissipation constant		---	1	---	mW/°C	$T_C = 25^\circ\text{C}$

Input-Output Logic Level Table



$\overline{\text{FLT/EN}}$	I_{TRIP}	HIN1,2,3	LIN1,2,3	U,V,W
1	0	1	0	V+
1	0	0	1	0
1	0	0	0	Off
1	0	1	1	Off
1	1	X	X	Off
0	X	X	X	Off

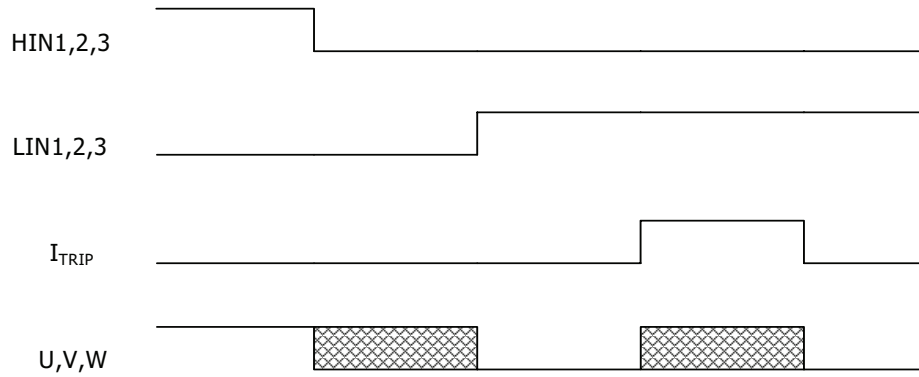


Figure 1. Input/Output Timing Diagram

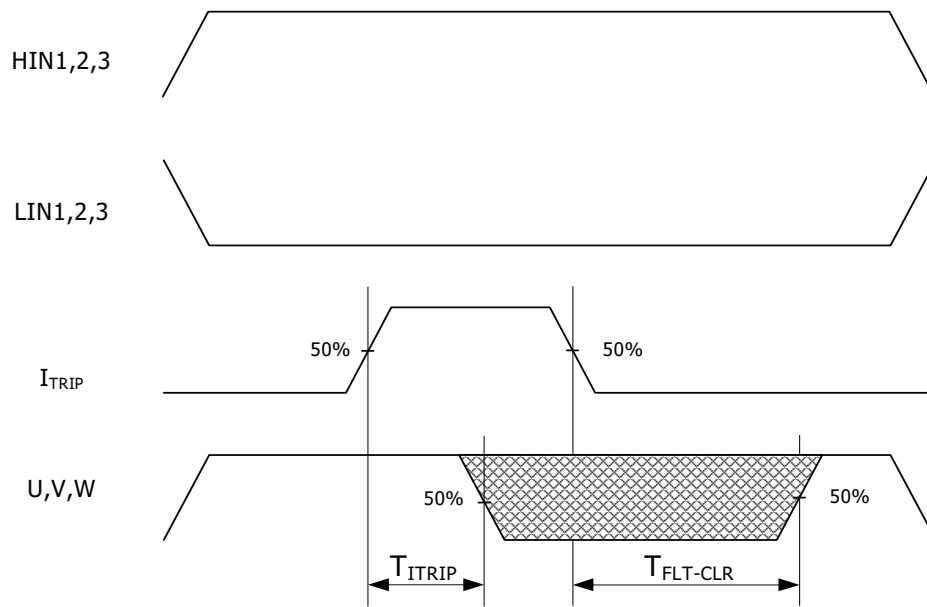


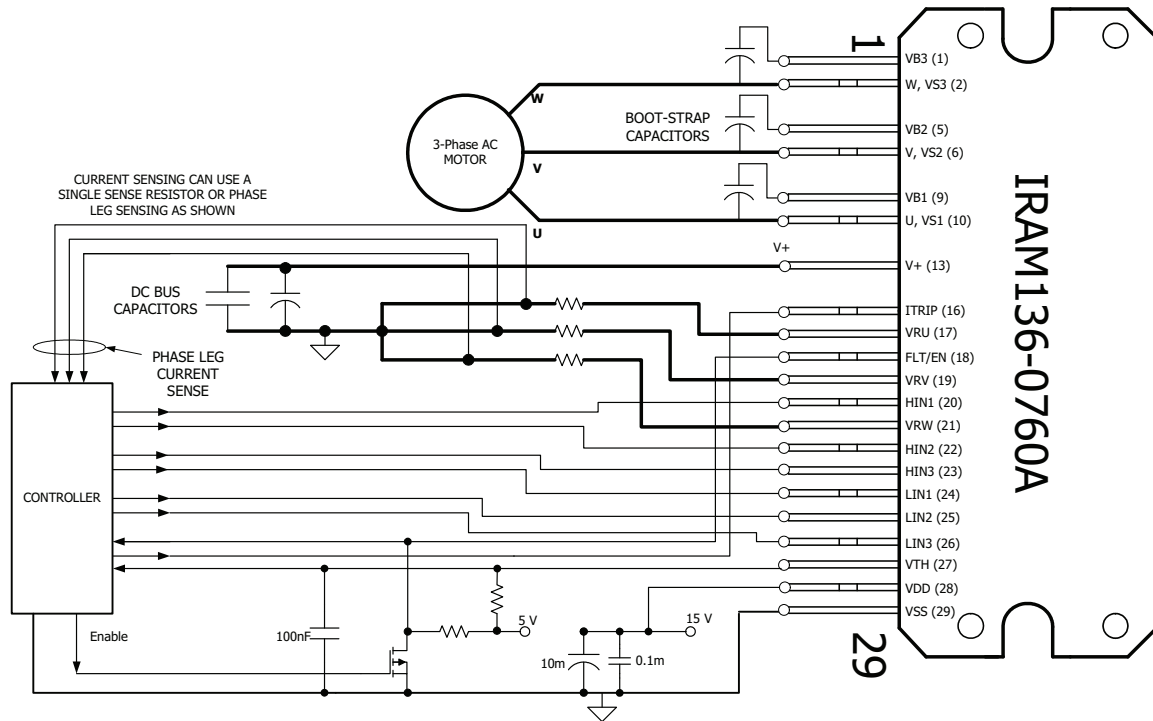
Figure 2. I_{TRIP} Timing Waveform

Note 5: The shaded area indicates that both high-side and low-side switches are off and therefore the half-bridge output voltage would be determined by the direction of current flow in the load.

Module Pin-Out Description

Pin	Name	Description
1	VB3	High Side Floating Supply Voltage 3
2	W,VS3	Output 3 - High Side Floating Supply Offset Voltage
3	na	none
4	na	none
5	VB2	High Side Floating Supply voltage 2
6	V,VS2	Output 2 - High Side Floating Supply Offset Voltage
7	na	none
8	na	none
9	VB1	High Side Floating Supply voltage 1
10	U,VS1	Output 1 - High Side Floating Supply Offset Voltage
11	na	none
12	na	none
13	V ⁺	Positive Bus Input Voltage
14	na	none
15	na	none
16	I _{TRIP}	Current Protection Pin
17	VRU	Low Side Emitter Connection - Phase 1
18	$\overline{\text{FLT}}/\text{EN}$	Fault Output and Enable Pin
19	VRV	Low Side Emitter Connection - Phase 2
20	HIN1	Logic Input High Side Gate Driver - Phase 1
21	VRW	Low Side Emitter Connection - Phase 3
22	HIN2	Logic Input High Side Gate Driver - Phase 2
23	HIN3	Logic Input High Side Gate Driver - Phase 3
24	LIN1	Logic Input Low Side Gate Driver - Phase 1
25	LIN2	Logic Input Low Side Gate Driver - Phase 2
26	LIN3	Logic Input Low Side Gate Driver - Phase 3
27	V _{TH}	Temperature Feedback
28	V _{CC}	+15V Main Supply
29	V _{SS}	Negative Main Supply

Typical Application Connection IRAM136-0760A



1. Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible to reduce ringing and EMI problems. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.
2. In order to provide good decoupling between VCC-VSS and VB1,2,3-VS1,2,3 terminals, the capacitors shown connected between these terminals should be located very close to the module pins. Additional high frequency capacitors, typically $0.1\mu\text{F}$, are strongly recommended.
3. Value of the boot-strap capacitors depends upon the switching frequency. Their selection should be made based on IR design tip DN 98-2a, application note AN-1044 or Figure 9. Bootstrap capacitor value must be selected to limit the power dissipation of the internal resistor in series with the VCC. (see maximum ratings Table on page 3).
4. After approx. 2ms the FAULT is reset. (see Dynamic Characteristics Table on page 5).
5. PWM generator must be disabled within Fault duration to guarantee shutdown of the system, overcurrent condition must be cleared before resuming operation.

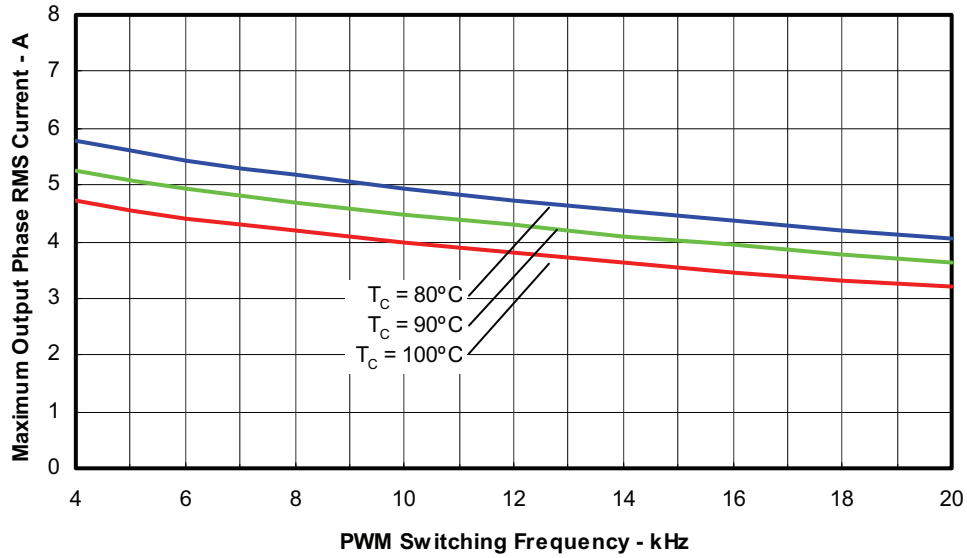


Figure 3. Maximum Sinusoidal Phase Current vs. PWM Switching Frequency Sinusoidal Modulation, $V^+ = 400\text{V}$, $T_J = 150^\circ\text{C}$, $MI = 0.8$, $PF = 0.6$, $f_{\text{mod}} = 100\text{Hz}$

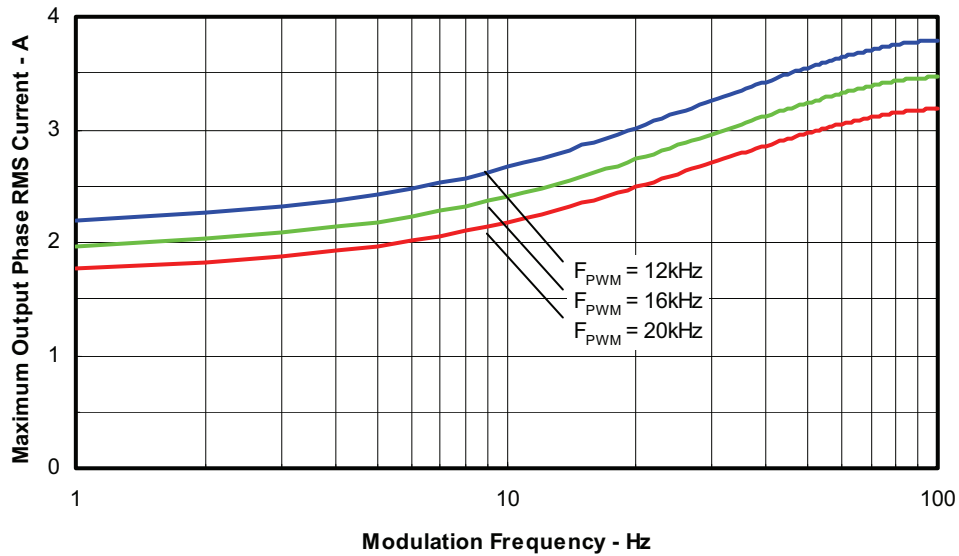


Figure 4. Maximum Sinusoidal Phase Current vs. Modulation Frequency Sinusoidal Modulation, $V^+ = 400\text{V}$, $T_J = 150^\circ\text{C}$, $T_c = 100^\circ\text{C}$, $MI = 0.8$, $PF = 0.6$

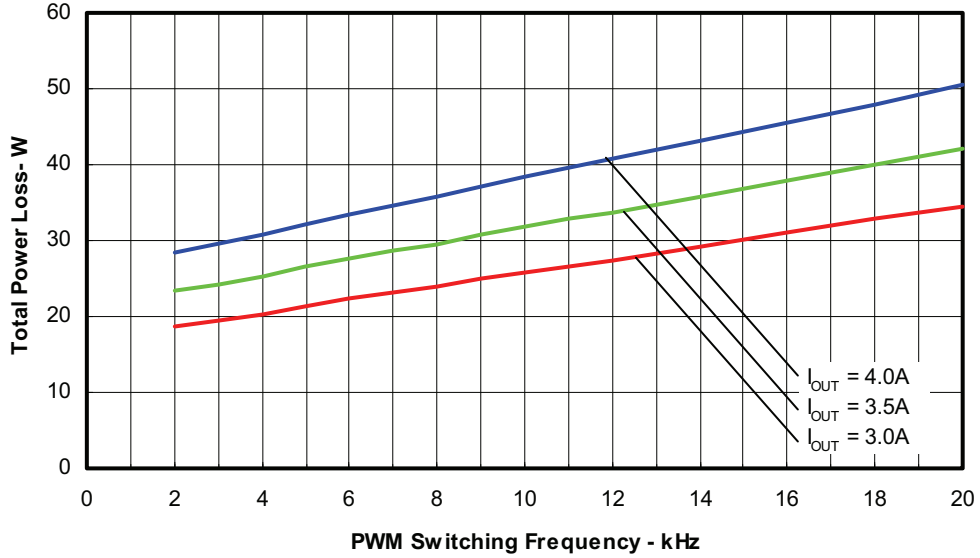


Figure 5. Total Power Losses vs. PWM Switching Frequency
Sinusoidal Modulation, $V^+ = 400V$, $T_J = 150^\circ C$, $MI = 0.8$, $PF = 0.6$, $f_{mod} = 100Hz$

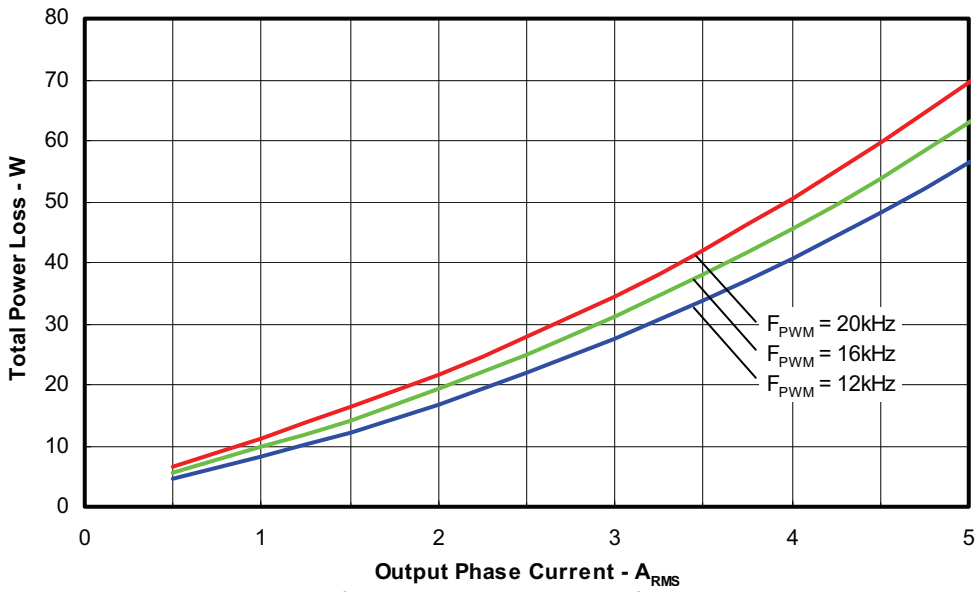


Figure 6. Total Power Losses vs. Output Phase Current
Sinusoidal Modulation, $V^+ = 400V$, $T_J = 150^\circ C$, $MI = 0.8$, $PF = 0.6$, $f_{mod} = 100Hz$

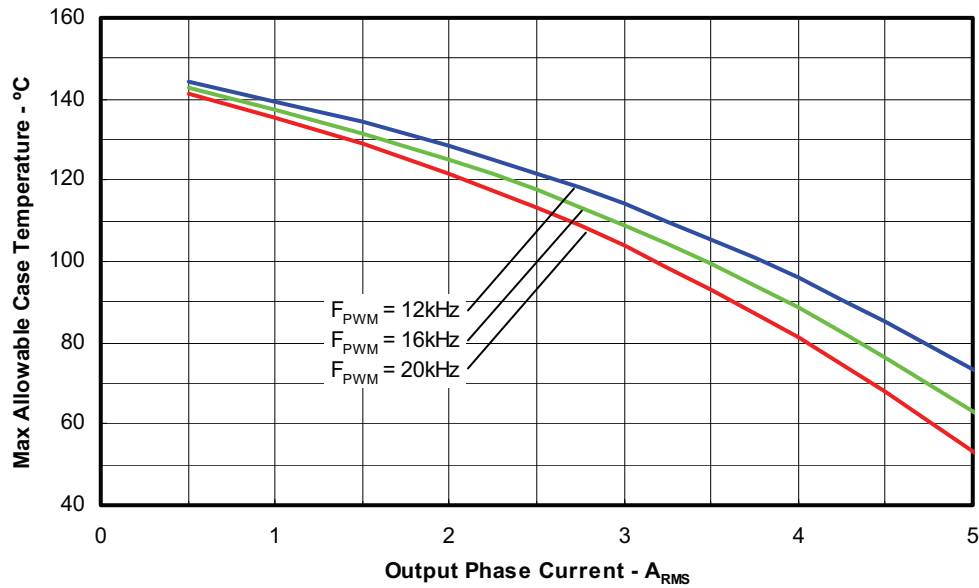


Figure 7. Maximum Allowable Case Temperature vs. Output RMS Current per Phase Sinusoidal Modulation, $V^+ = 400V$, $T_J = 150^\circ C$, $MI = 0.8$, $PF = 0.6$, $f_{mod} = 50Hz$

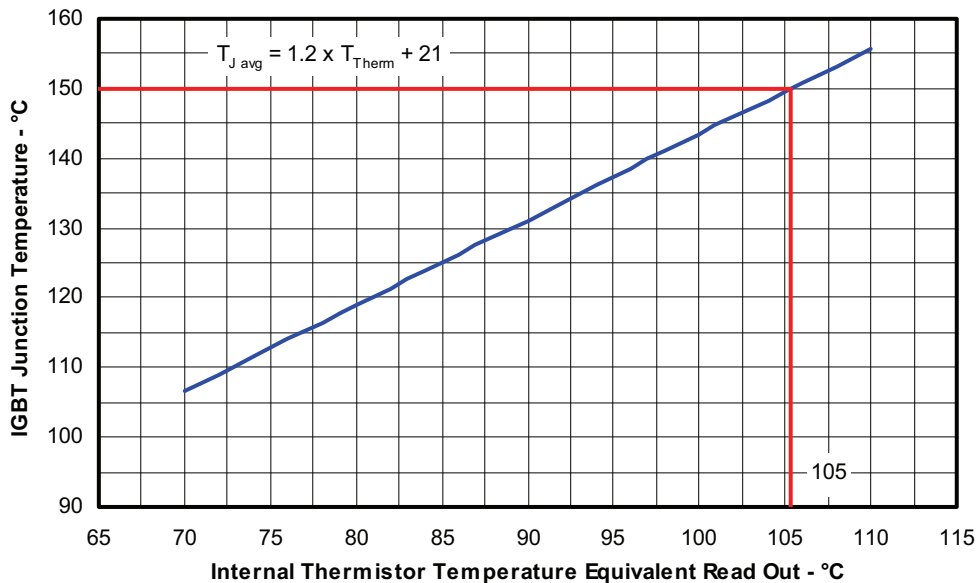


Figure 8. Estimated Maximum IGBT Junction Temperature vs. Thermistor Temperature Sinusoidal Modulation, $V^+ = 400V$, $I_{phase} = 5A_{rms}$, $f_{sw} = 16kHz$, $f_{mod} = 50Hz$, $MI = 0.8$, $PF = 0.6$

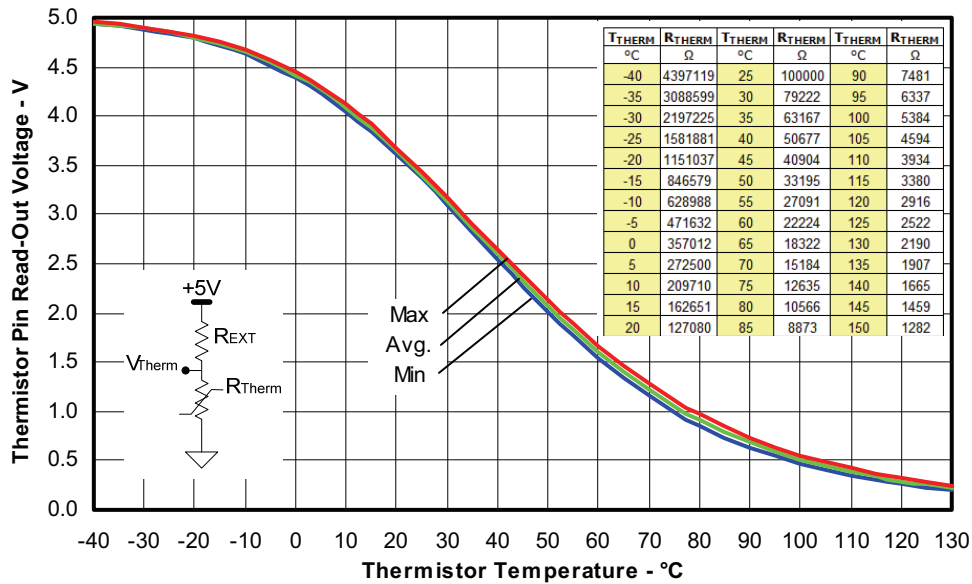


Figure 9. Thermistor Readout vs. Temperature (47kohm pull-up resistor, 5V) and Normal Thermistor Resistance values vs. Temperature Table.

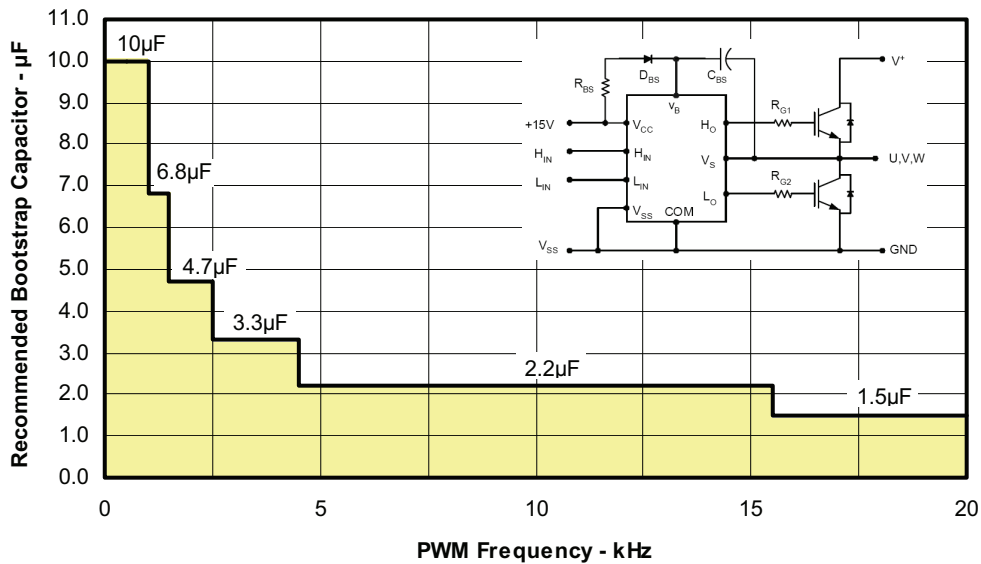


Figure 10. Recommended Bootstrap Capacitor Value vs. Switching Frequency

Figure 11. Switching Parameter Definitions

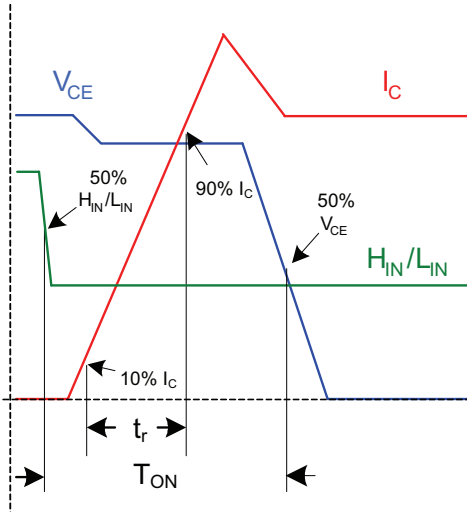


Figure 11a. Input to Output propagation turn-on delay time.

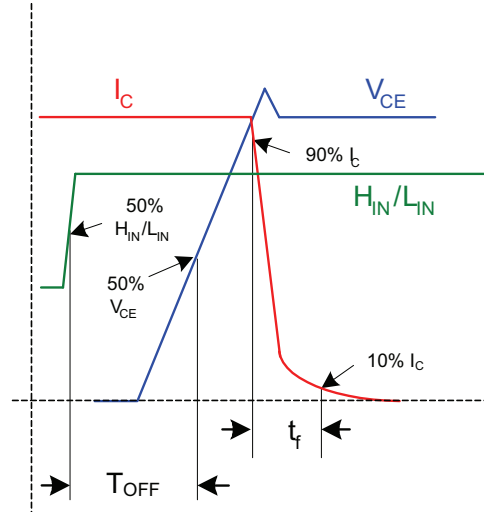


Figure 11b. Input to Output propagation turn-off delay time.

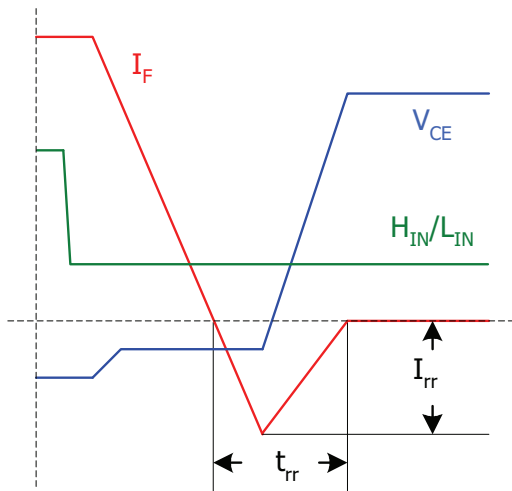


Figure 11c. Diode Reverse Recovery.

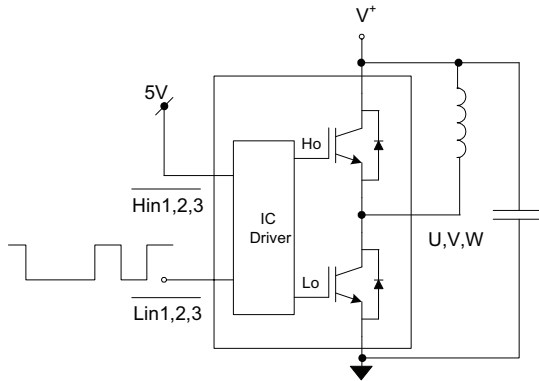


Figure CT1. Switching Loss Circuit

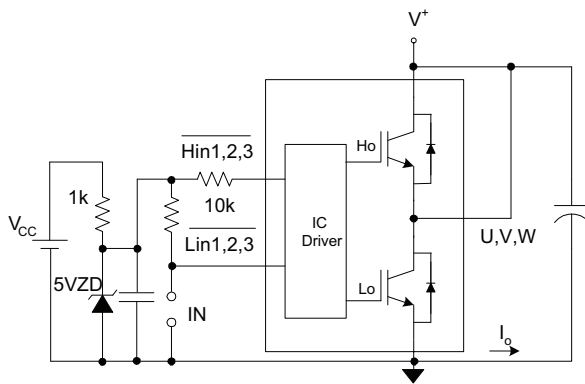
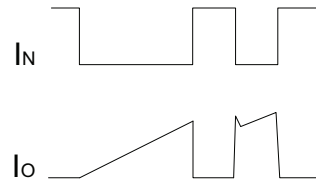


Figure CT2. S.C.SOA Circuit

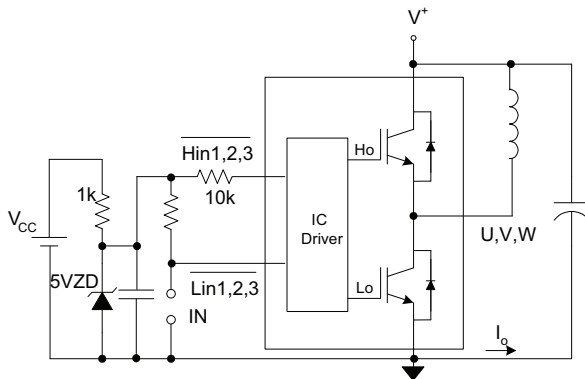
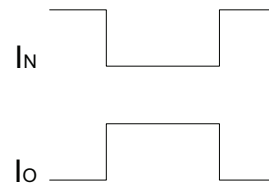
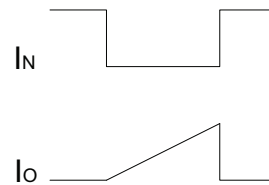
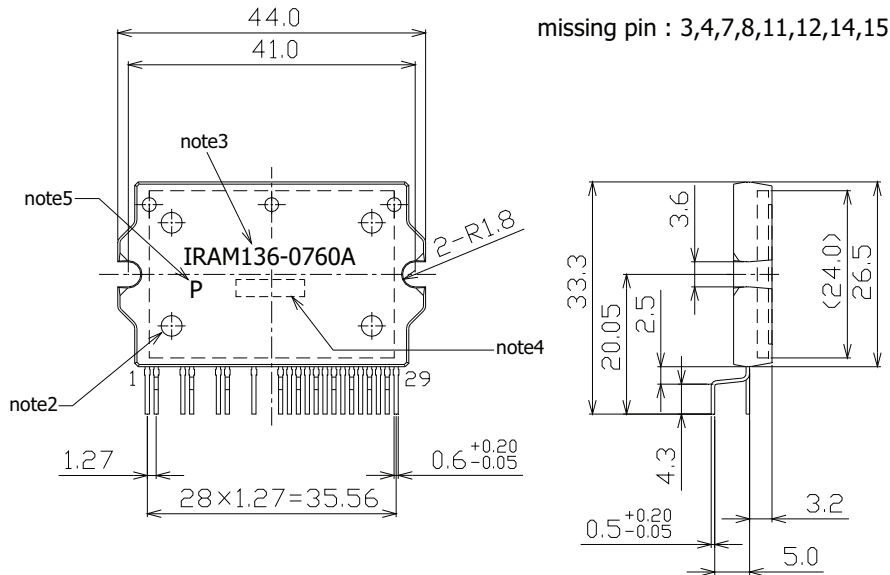


Figure CT3. R.B.SOA Circuit



IRAM136-0760A

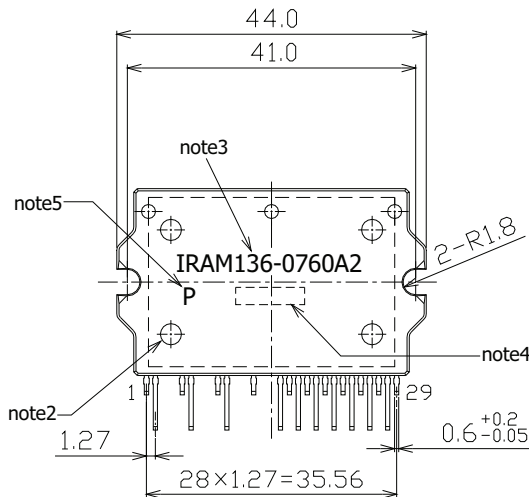
Package Outline IRAM136-0760A



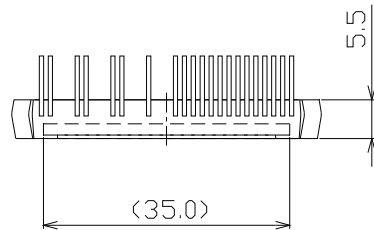
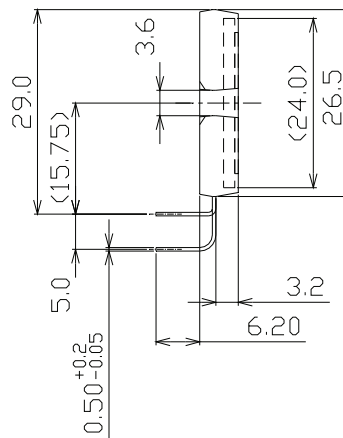
- note1: Unit Tolerance is +0.5mm, Unless Otherwise Specified.
- note2: Mirror Surface Mark indicates Pin1 Identification.
- note3: Part Number Marking. Characters Font in this drawing differs from Font shown on Module.
- note4: Lot Code Marking. Characters Font in this drawing differs from Font shown on Module.
- note5: "P" Character denotes Lead Free. Characters Font in this drawing differs from Font shown on Module.

Dimensions in mm
For mounting instruction see AN-1049

Package Outline IRAM136-0760A2



missing pin : 3,4,7,8,11,12,14,15



- note1: Unit Tolerance is ± 0.5 mm, Unless Otherwise Specified.
- note2: Mirror Surface Mark indicates Pin1 Identification.
- note3: Part Number Marking. Characters Font in this drawing differs from Font shown on Module.
- note4: Lot Code Marking. Characters Font in this drawing differs from Font shown on Module.
- note5: "P" Character denotes Lead Free. Characters Font in this drawing differs from Font shown on Module.

Dimensions in mm
 For mounting instruction see AN-1049