



STE48NM60

N-CHANNEL 650V @ Tjmax - 0.09Ω - 48A ISOTOP MDmesh™ MOSFET

Table 1: General Features

TYPE	V _{DSS} (@T _{jmax})	R _{DS(on)}	I _D
STE48NM60	650V	< 0.11Ω	48 A

- TYPICAL R_{DS(on)} = 0.09Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- 100% AVALANCHE TESTED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE
- TIGHT PROCESS CONTROL AND HIGH MANUFACTURING YIELDS

DESCRIPTION

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

APPLICATIONS

The MDmesh™ family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.

Figure 1: Package



Figure 2: Internal Schematic Diagram

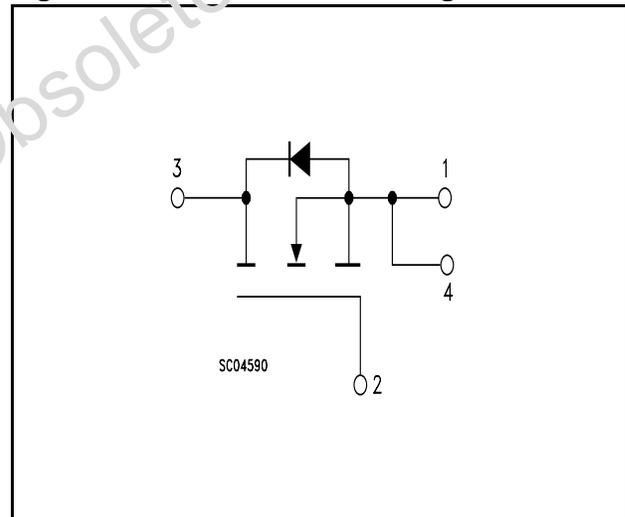


Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STE48NM60	E48NM60	ISOTOP	TUBE

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V _{GS}	Gate- source Voltage	±30	V
I _D	Drain Current (continuous) at T _C = 25°C	48	A
I _D	Drain Current (continuous) at T _C = 100°C	30	A
I _{DM} (•)	Drain Current (pulsed)	192	A
P _{TOT}	Total Dissipation at T _C = 25°C	450	W
	Derating Factor	3.57	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	15	V/ns
V _{ISO}	Insulation Withstand Voltage (AC-RMS)	2500	V
T _{stg}	Storage Temperature	-65 to 150	°C
T _j	Max. Operating Junction Temperature	150	°C

(•)Pulse width limited by safe operating area

(1) I_{SD} ≤ 48A, di/dt ≤ 400 A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}.

Table 4: Thermal Data

R _{thj-case}	Thermal Resistance Junction-case	Max	0.28	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient	Max	30	°C/W
T _I	Maximum Lead Temperature For Soldering Purpose		300	°C

(*) with conductive GREASE Applies

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	15	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 35 V)	850	mJ

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)
Table 6: On/Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	600			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125°C			10 100	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ±30V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	3	4	5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 22.5A		0.09	0.11	Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)

Table 7: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, $I_D = 24A$		20		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V$, $f = 1$ MHz, $V_{GS} = 0$		3800 1250 80		pF pF pF
$C_{oss\ eq.}$ (2)	Equivalent Output Capacitance	$V_{GS} = 0V$, $V_{DS} = 0V$ to 480V		340		pF
R_G	Gate Input Resistance	$f=1$ MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		1.4		Ω
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 250V$, $I_D = 22.5A$ $R_G = 4.7\Omega$ $V_{GS} = 10V$ (see Figure 14)		30 20		ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD} = 400V$, $I_D = 45A$, $R_G = 4.7\Omega$, $V_{GS} = 10V$		16 23 40		ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 400V$, $I_D = 45A$, $V_{GS} = 10V$ (see Figure 18)		96 31 43	134	nC nC nC

Table 8: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				48	A
I_{SDM} (2)	Source-drain Current (pulsed)				192	A
V_{SD} (1)	Forward On Voltage	$I_{SD} = 45A$, $V_{GS} = 0$			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 45A$, $di/dt = 100A/\mu s$, $V_{DD} = 100V$, $T_j = 25^\circ C$ (see Figure 16)		508 10 40		ns μC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 45A$, $di/dt = 100A/\mu s$, $V_{DD} = 100V$, $T_j = 150^\circ C$ (see Figure 16)		650 14 43		ns μC A

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Figure 3: Safe Operating Area

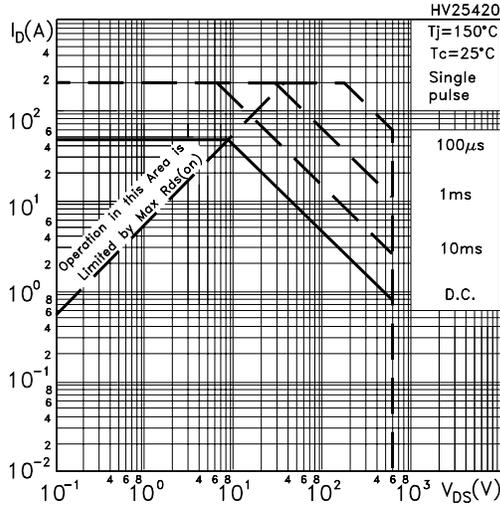


Figure 4: Output Characteristics

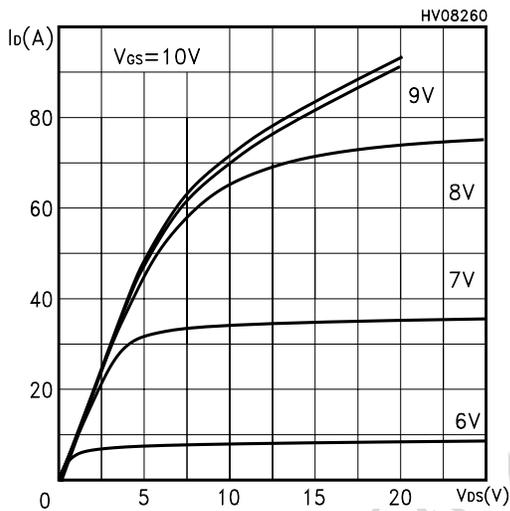


Figure 5: Transconductance

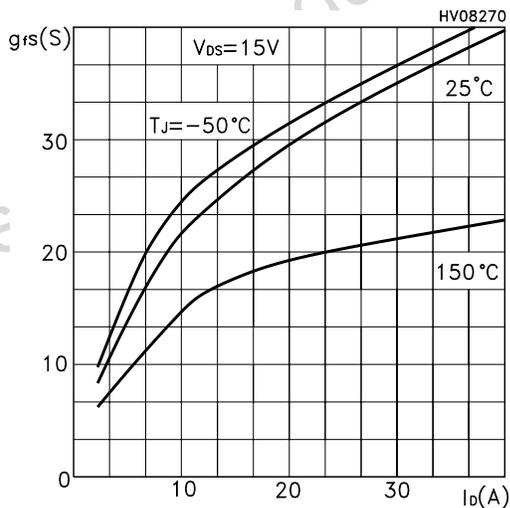


Figure 6: Thermal Impedance

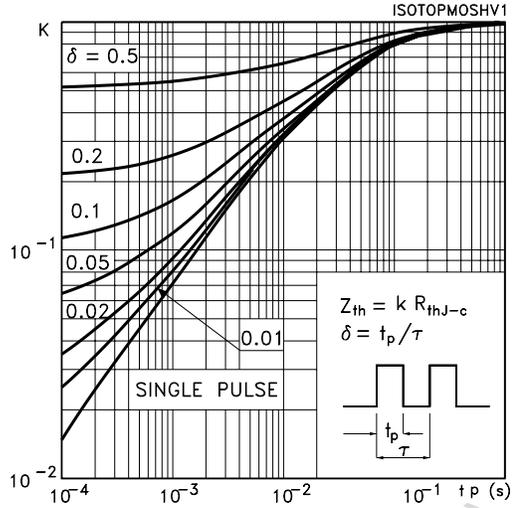


Figure 7: Transfer Characteristics

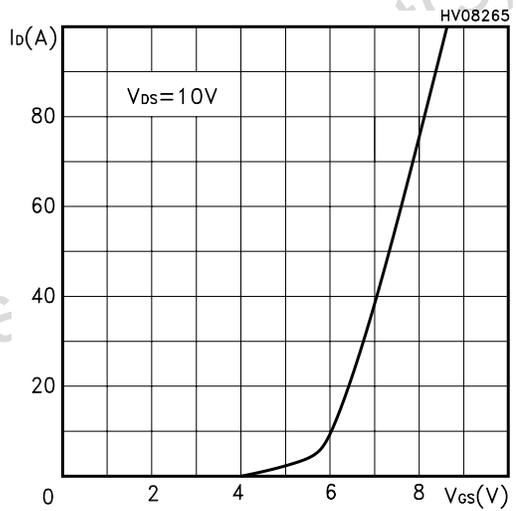


Figure 8: Static Drain-source On Resistance

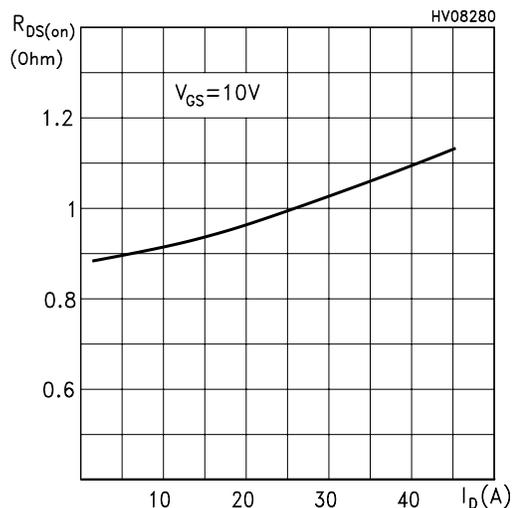


Figure 9: Gate Charge vs Gate-source Voltage

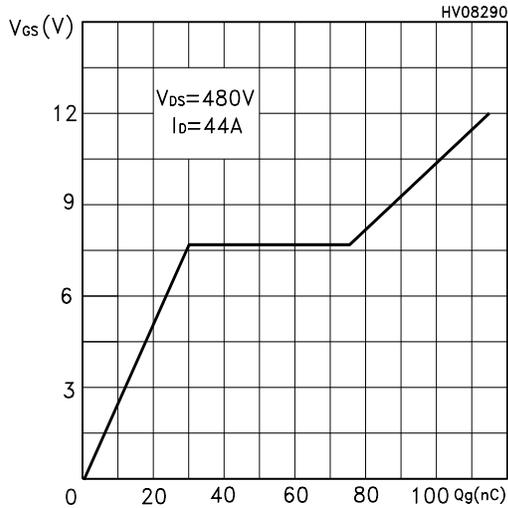


Figure 12: Capacitance Variations

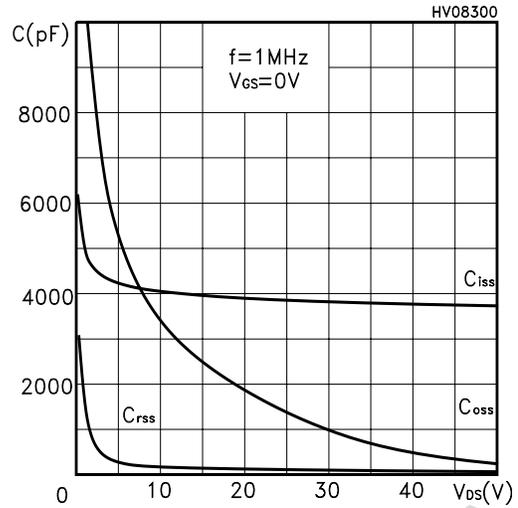


Figure 10: Normalized Gate Threshold Voltage vs Temperature

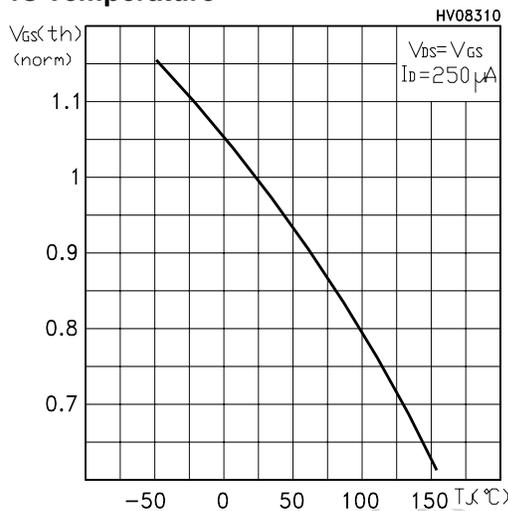


Figure 13: Normalized On Resistance vs Temperature

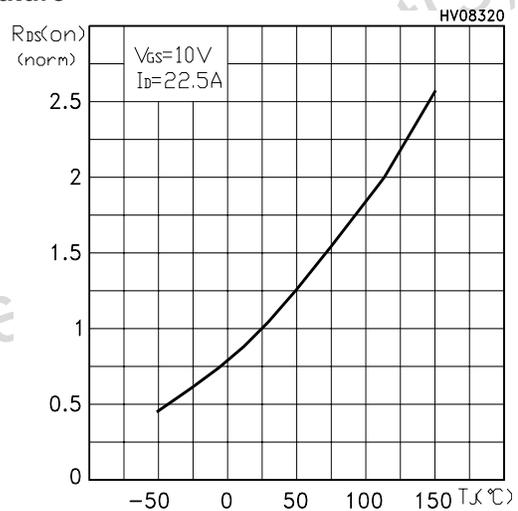


Figure 11: Source-Drain Diode Forward Characteristics

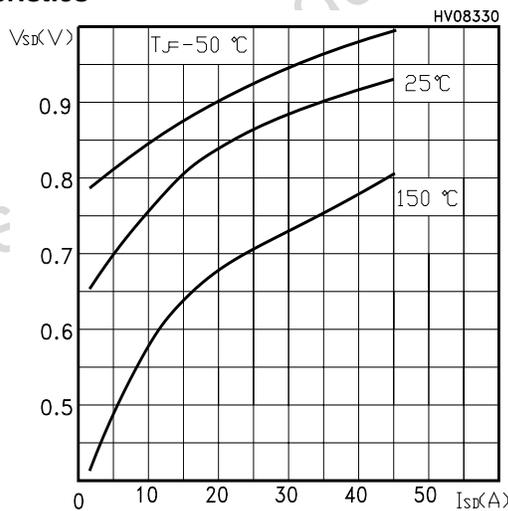


Figure 14: Unclamped Inductive Load Test Circuit

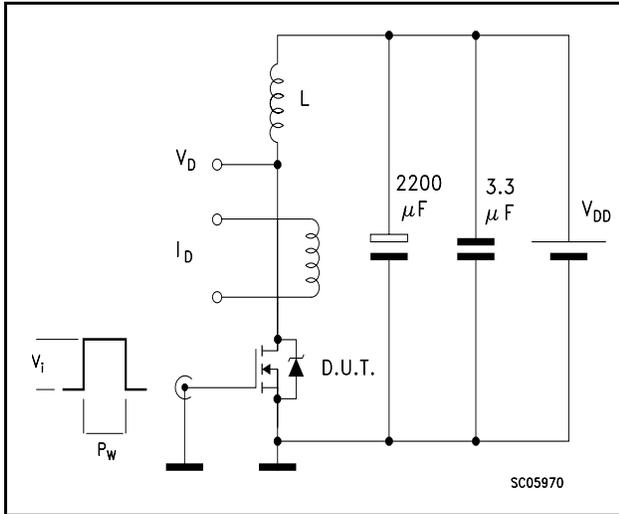


Figure 15: Switching Times Test Circuit For Resistive Load

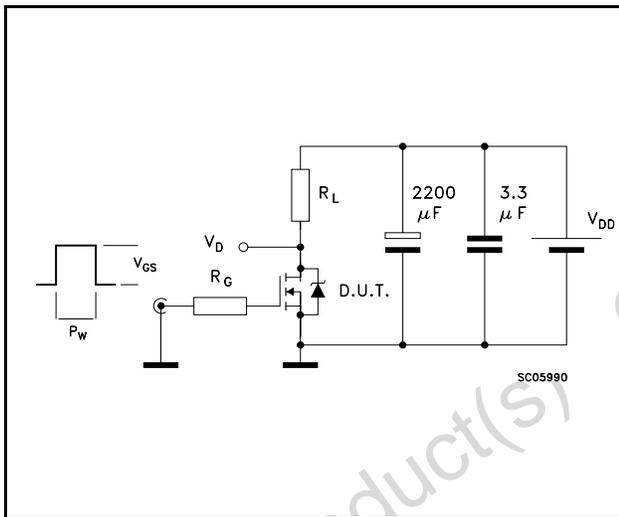


Figure 16: Test Circuit For Inductive Load Switching and Diode Recovery Times

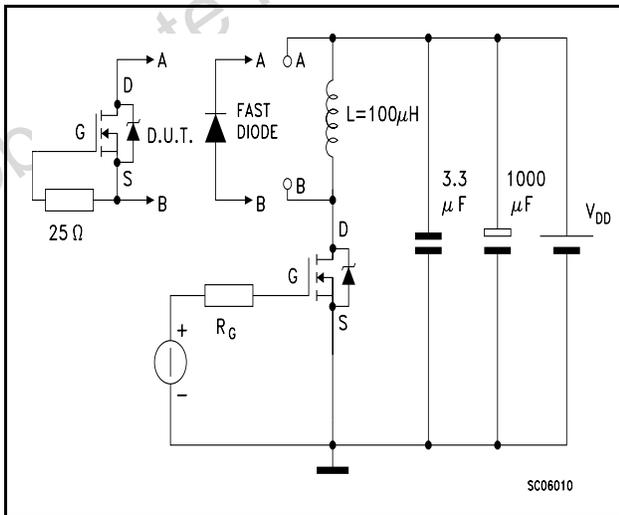


Figure 17: Unclamped Inductive Wavform

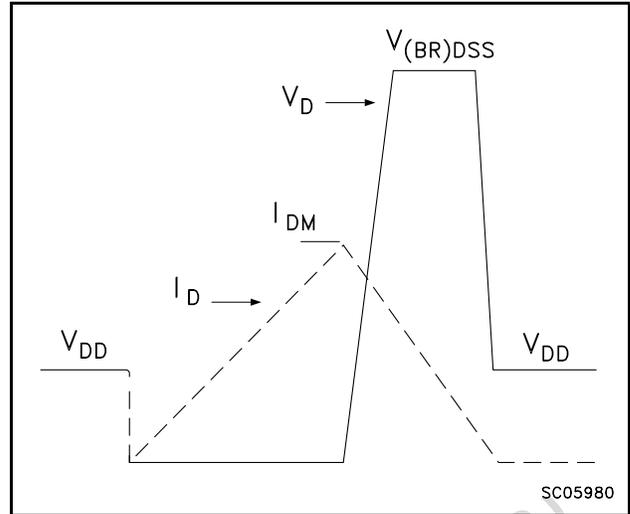
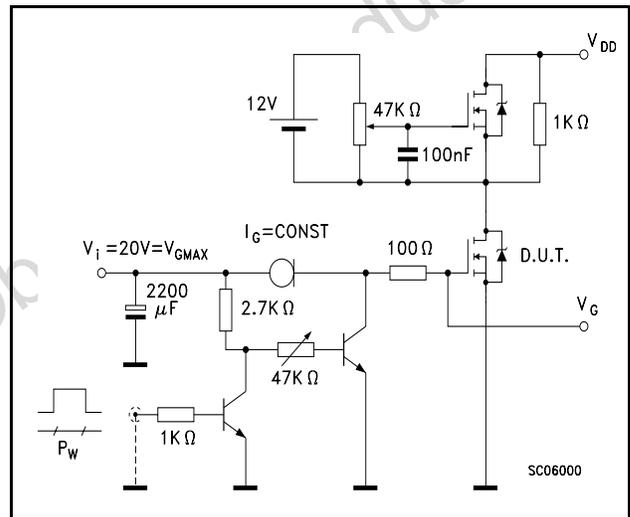


Figure 18: Gate Charge Test Circuit



ISOTOP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	11.8		12.2	0.466		0.480
B	8.9		9.1	0.350		0.358
C	1.95		2.05	0.076		0.080
D	0.75		0.85	0.029		0.033
E	12.6		12.8	0.496		0.503
F	25.15		25.5	0.990		1.003
G	31.5		31.7	1.240		1.248
H	4			0.157		
J	4.1		4.3	0.161		0.169
K	14.9		15.1	0.586		0.594
L	30.1		30.3	1.185		1.193
M	37.8		38.2	1.488		1.503
N	4			0.157		
O	7.8		8.2	0.307		0.322

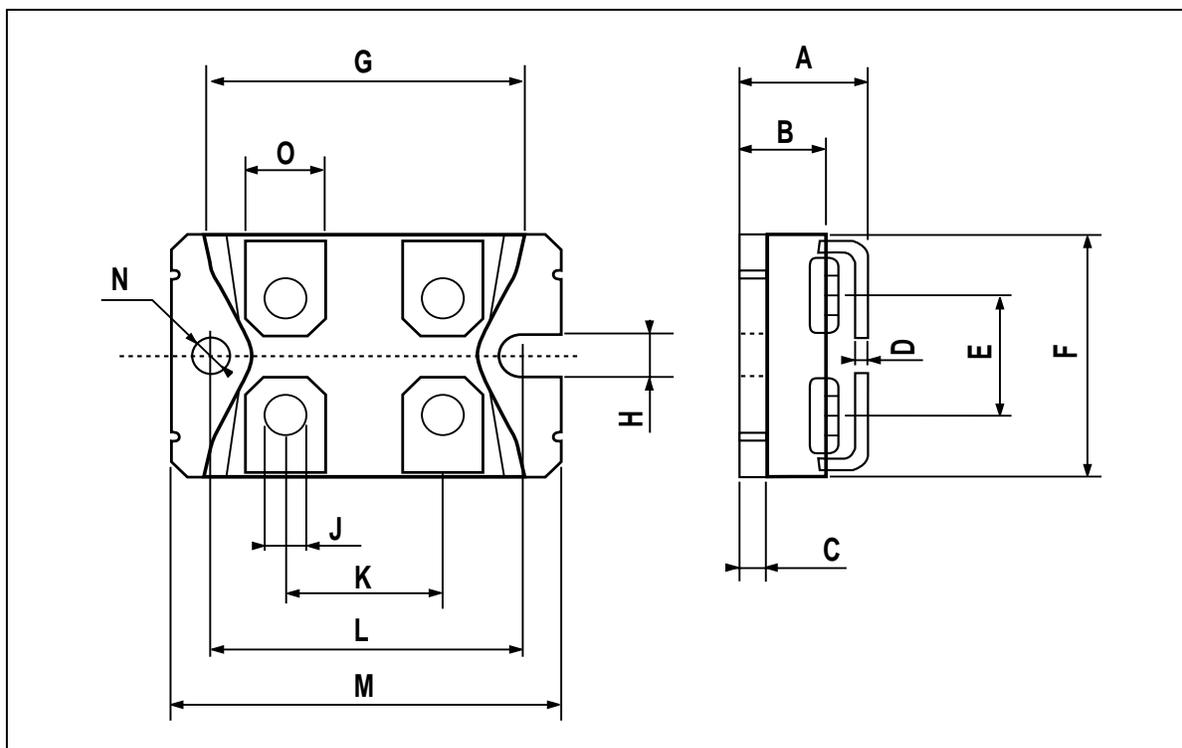


Table 9: Revision History

Date	Revision	Description of Changes
30/Mar/2005	2	Modified value in table 7

Obsolete Product(s) - Obsolete Product(s)

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