



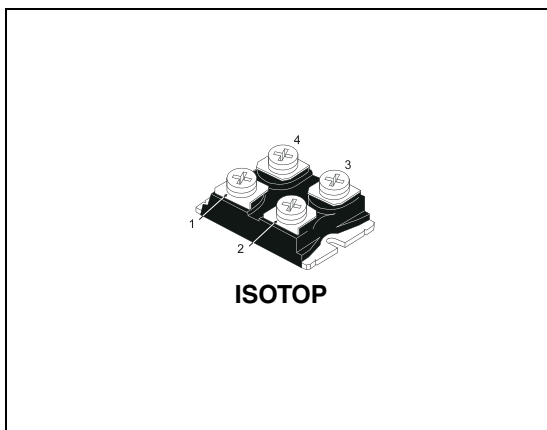
## STGE200NB60S

N-channel 150A - 600V - ISOTOP  
Low drop PowerMESH™ IGBT

### General features

TYPE	V <sub>CES</sub>	V <sub>CE(sat)</sub> (typ.)	I <sub>C</sub>	T <sub>C</sub>
STGE200NB60S	600V	1.2V	150A	100°C
		1.3V	200A	25°C

- High input impedance (voltage driven)
- Low on-voltage drop (V<sub>cesat</sub>)
- Off losses include tail current
- Low gate charge
- High current capability



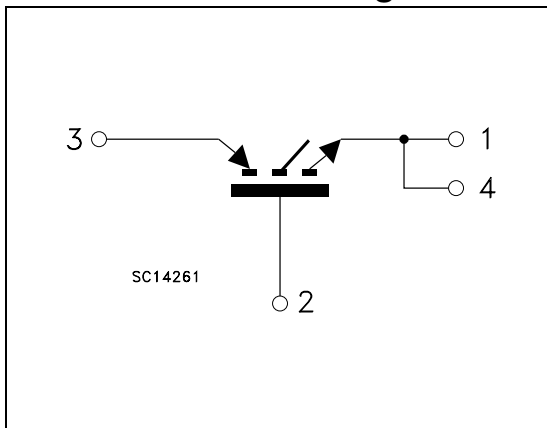
### Description

Using the latest high voltage technology based on a patented strip layout, STMicroelectronics has designed an advanced family of IGBTs, the PowerMESH™ IGBTs, with outstanding performances. The suffix “S” identifies a family optimized to achieve very low V<sub>CE(sat)</sub> (@ max frequency of 1KHz).

### Applications

- Low frequency motor controls
- Aluminum welding equipment

### Internal schematic diagram



### Order codes

Part number	Marking	Package	Packaging
STGE200NB60S	GE200NB60S	ISOTOP	Tube

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CES}$	Collector-emitter voltage ( $V_{GS} = 0$ )	600	V
$V_{GE}$	Gate-emitter voltage	$\pm 20$	V
$I_C$	Collector current (continuous) at $T_C = 25^\circ\text{C}$	200	A
$I_C$	Collector current (continuous) at $T_C = 100^\circ\text{C}$	150	A
$I_{CM}^{(1)}$	Collector current (pulsed)	400	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	600	W
	Derating factor	4.8	W/ $^\circ\text{C}$
$V_{ISO}$	Insulation withstand voltage (DC)	2500	V
$T_{stg}$	Storage temperature	– 55 to 150	$^\circ\text{C}$
$T_j$	Operating junction temperature		

1. Pulse width limited by safe operating area

**Table 2. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.208	$^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	30	$^\circ\text{C}/\text{W}$

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}\text{C}$  unless otherwise specified)

**Table 3. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR(CES)}$	Collector-emitter breakdown voltage	$I_C = 250\mu\text{A}$ , $V_{GE} = 0$	600			V
$I_{CES}$	Collector cut-off ( $V_{GE} = 0$ )	$V_{CE} = \text{Max rating, @ } 25^{\circ}\text{C}$ $V_{CE} = \text{Max rating, @ } 125^{\circ}\text{C}$			500 5	$\mu\text{A}$ mA
$I_{GES}$	Gate-emitterleakage current ( $V_{CE} = 0$ )	$V_{GE} = \pm 20\text{V}$ , $V_{CE} = 0$			$\pm 100$	nA
$V_{GE(th)}$	Gate threshold voltage	$V_{CE} = V_{GE}$ , $I_C = 250\mu\text{A}$	3		5	V
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{GE} = 15\text{V}$ , $I_C = 100\text{A}$ $V_{GE} = 15\text{V}$ , $I_C = 150\text{A}$ , @ $100^{\circ}\text{C}$		1.2 1.2	1.6	V V
$g_{fs}$	Forward transconductance	$V_{CE} = 15\text{V}$ , $I_C = 100\text{A}$		80		S

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{ies}$ $C_{oes}$ $C_{res}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{CE} = 25\text{V}$ , $f = 1\text{MHz}$ , $V_{GE} = 0$		1560 0 1100 95		pF pF pF
$Q_g$ $Q_{ge}$ $Q_{gc}$	Total gate charge Gate-emitter charge Gate-collector charge	$V_{CE} = 480\text{V}$ , $I_C = 100\text{A}$ , $V_{GE} = 15\text{V}$		560 70 170		nC nC nC
$I_{CL}$	Latching current	$V_{clamp} = 480\text{V}$ $T_j = 125^{\circ}\text{C}$ , $R_G = 10\Omega$	300			A

**Table 5. Switching on/off (inductive load)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Delay time	$I_C = 100A$ , $V_{CC} = 480V$		64		ns
$t_r$	Current rise time	$V_{GE} = 15V$ , $R_G = 3\Omega$		112		ns
$(di/dt)_{on}$	Turn-on current slope	$T_j = 25^\circ C$ (see Figure 17)		1840		A/ $\mu s$
$t_{d(on)}$	Dealy time	$I_C = 100A$ , $V_{CC} = 480V$		56		ns
$t_r$	Current rise time	$V_{GE} = 15V$ , $R_G = 3\Omega$		114		ns
$(di/dt)_{on}$	Turn-on current slope	$T_j = 125^\circ C$ (see Figure 17)		1800		A/ $\mu s$
$t_c$	Cross-over time	$I_C = 100A$ , $V_{CC} = 480V$		2.98		$\mu s$
$t_r(V_{off})$	Off voltage rise time	$V_{GE} = 15V$ , $R_G = 3\Omega$		1.7		$\mu s$
$t_{d(off)}$	Delay time	$T_j = 25^\circ C$ (see Figure 17)		2.4		$\mu s$
$t_f$	Current fall time			1.23		$\mu s$
$t_c$	Cross-over time	$I_C = 100A$ , $V_{CC} = 480V$		4.52		$\mu s$
$t_r(V_{off})$	Off voltage rise time	$V_{GE} = 15V$ , $R_G = 3\Omega$		2.6		$\mu s$
$t_{d(off)}$	Delay time	$T_j = 125^\circ C$ (see Figure 17)		2.8		$\mu s$
$t_f$	Current fall time			1.8		$\mu s$

**Table 6. Switching energy (inductive load)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$E_{on}^{(1)}$	Turn-on switching losses	$V_{CC} = 480V$ , $I_C = 100A$		11.7		mJ
$E_{off}^{(2)}$	Turn-off switching loss	$R_G = 3\Omega$ , $V_{GE} = 15V$ , $T_j = 25^\circ C$		59		mJ
$E_{ts}$	Total switching loss	(see Figure 17)		70.7		mJ
$E_{on}^{(1)}$	Turn-on switching losses	$V_{CC} = 480V$ , $I_C = 100A$		12		mJ
$E_{off}^{(2)}$	Turn-off switching loss	$R_G = 3\Omega$ , $V_{GE} = 15V$ ,		92		mJ
$E_{ts}$	Total switching loss	$T_j = 125^\circ C$ (see Figure 17)		104		mJ

1.  $E_{on}$  is the turn-on losses when a typical diode is used in the test circuit in Figure 17

2. Turn-off losses include also the tail of the collector current.

## 2.1 Electrical characteristics (curves)

Figure 1. Output characteristics

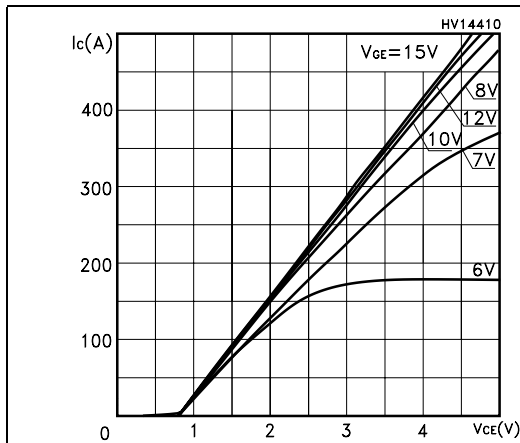


Figure 2. Transfer characteristics

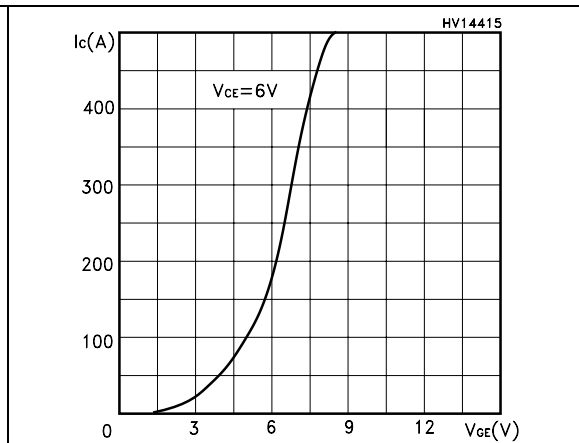


Figure 3. Transconductance

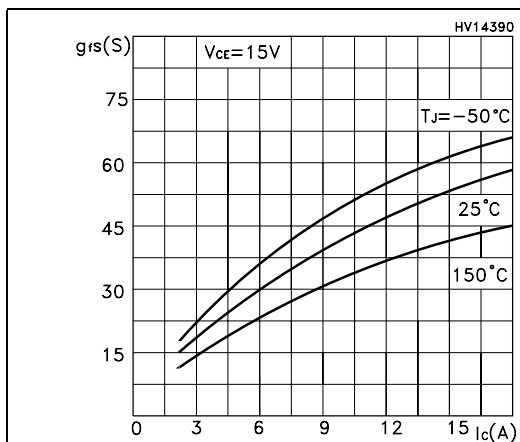


Figure 4. Collector-emitter on voltage vs temperature

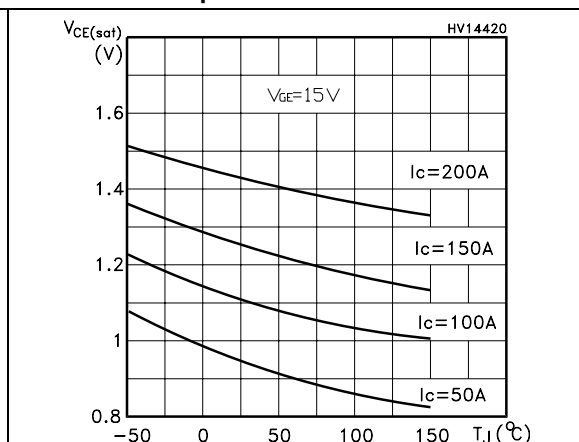


Figure 5. Gate charge vs gate-source voltage

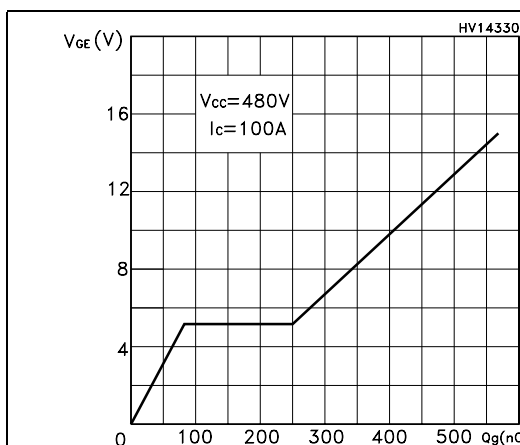
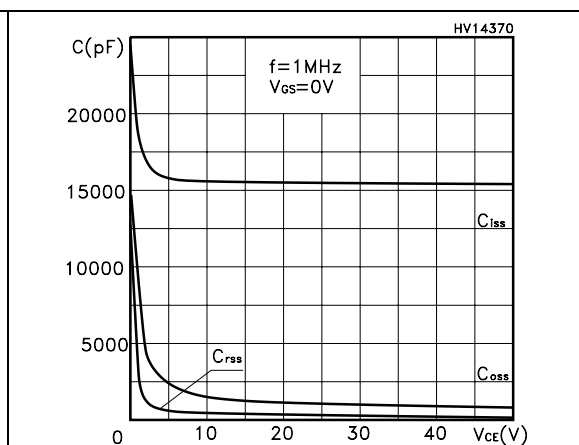


Figure 6. Capacitance variations



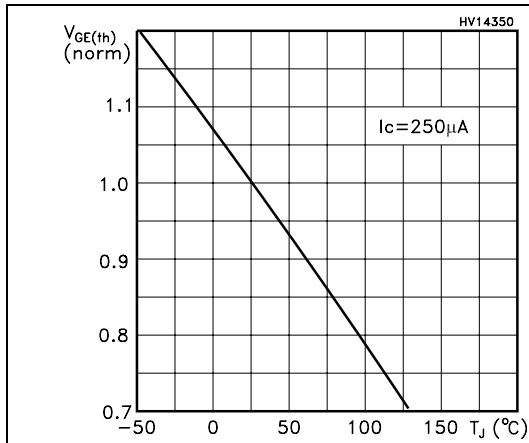
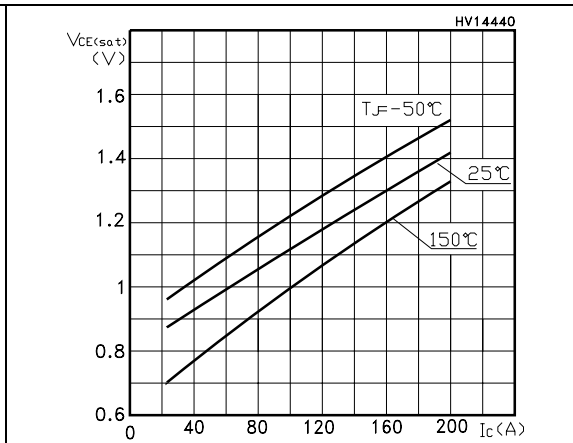
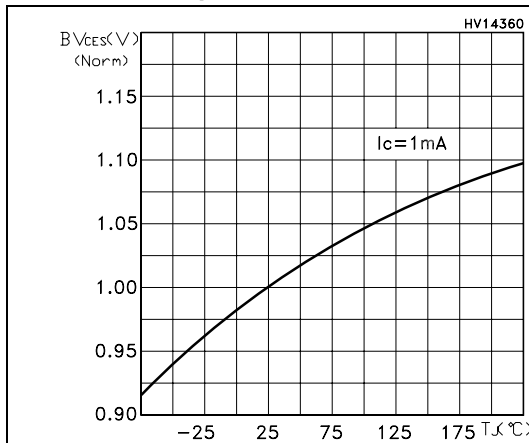
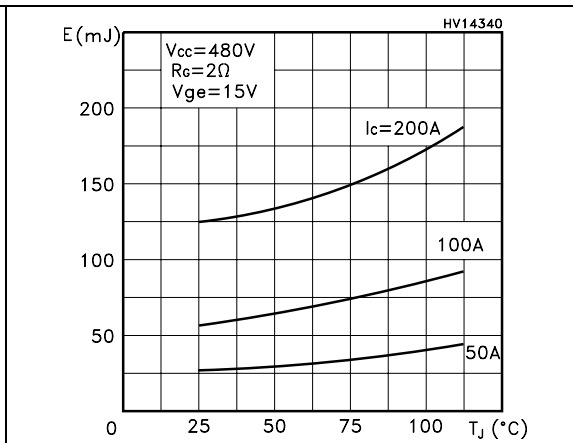
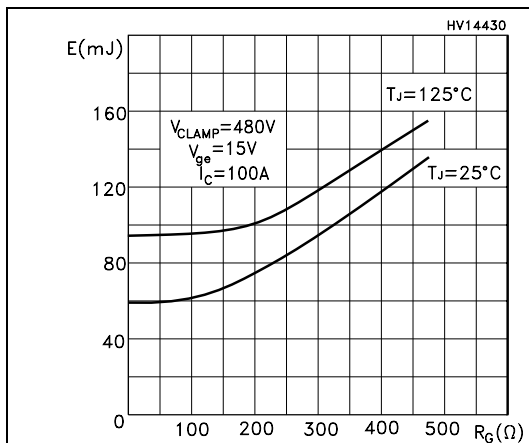
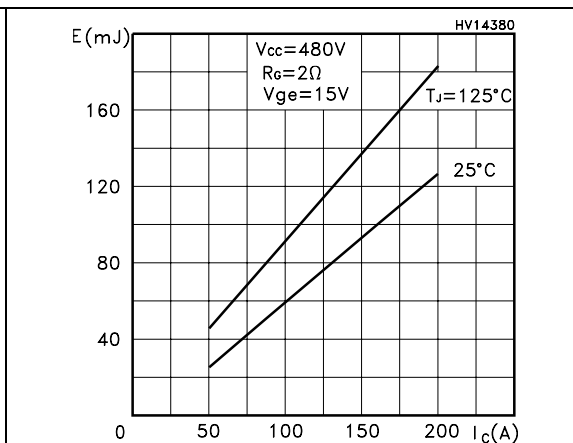
**Figure 7. Normalized gate threshold voltage vs temperature****Figure 8. Collector-emitter on voltage vs collector current****Figure 9. Normalized breakdown voltage vs temperature****Figure 10. Switching losses vs temperature****Figure 11. Switching losses vs gate resistance****Figure 12. Switching losses vs collector current**

Figure 13. Thermal impedance

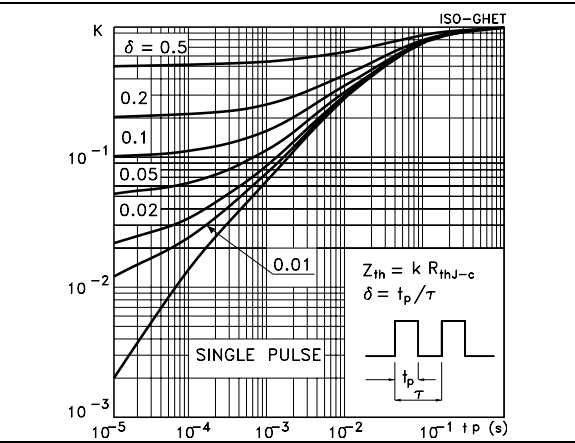
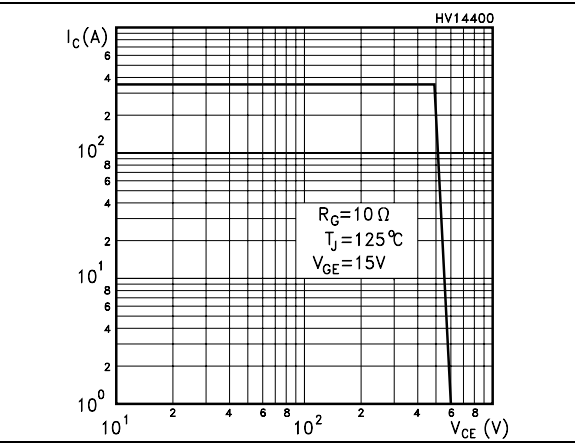


Figure 14. Turn-off SOA





3 Test circuit

Figure 15. Test circuit for inductive load switching

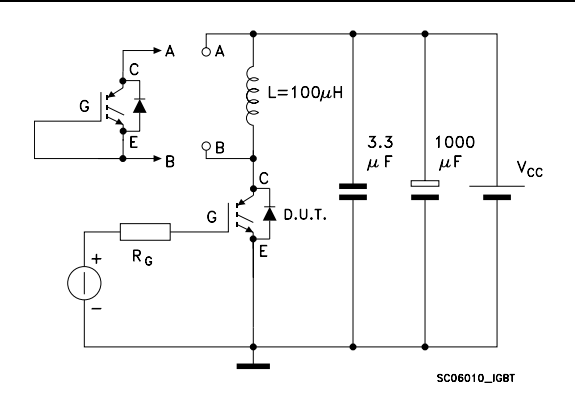


Figure 16. Gate charge test circuit

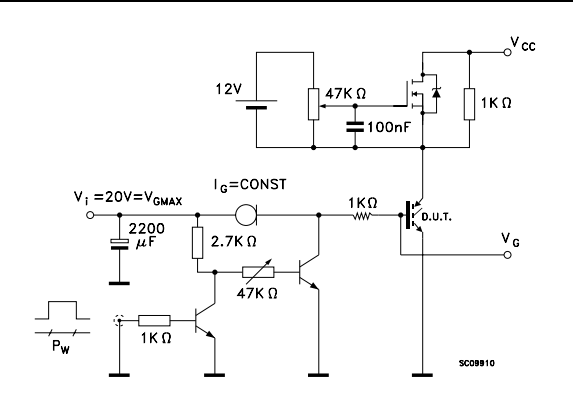


Figure 17. Switching waveform

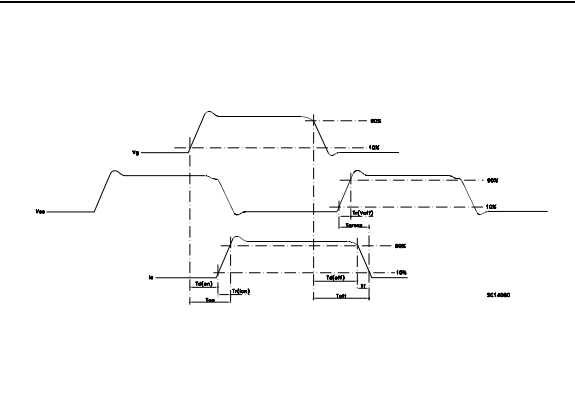
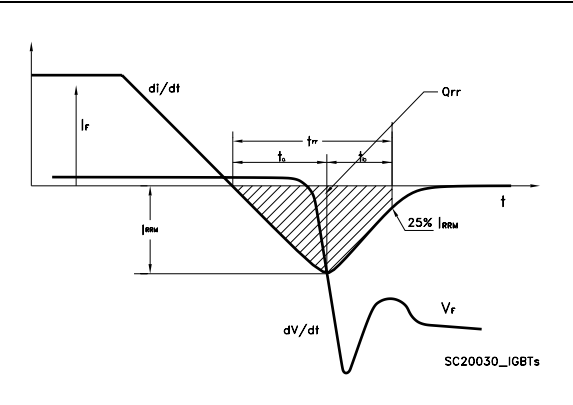


Figure 18. Diode recovery time waveform

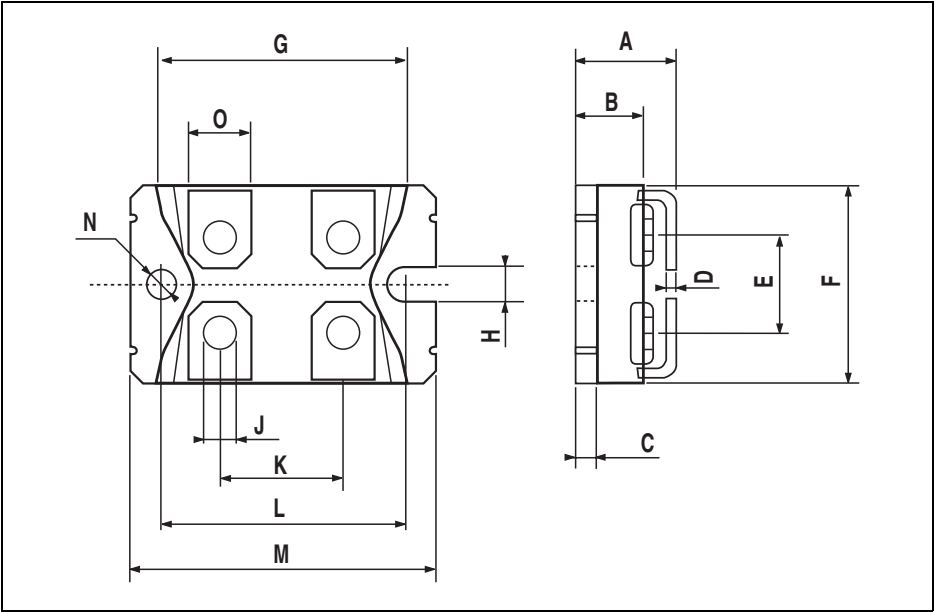


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

ISOTOP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	11.8		12.2	0.466		0.480
B	8.9		9.1	0.350		0.358
C	1.95		2.05	0.076		0.080
D	0.75		0.85	0.029		0.033
E	12.6		12.8	0.496		0.503
F	25.15		25.5	0.990		1.003
G	31.5		31.7	1.240		1.248
H	4			0.157		
J	4.1		4.3	0.161		0.169
K	14.9		15.1	0.586		0.594
L	30.1		30.3	1.185		1.193
M	37.8		38.2	1.488		1.503
N	4			0.157		
O	7.8		8.2	0.307		0.322



## 5 Revision history

Table 7. Revision history

Date	Revision	Changes
28-Feb-2005	6	Complete version
26-Jul-2006	7	New template
03-Nov-2006	8	New value inserted on <a href="#">Table 1.: Absolute maximum ratings</a>

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