Wireless Components

ASK Transmitter 345 MHz

TDA 5103A Version 1.0

Specification March 2001

preliminary

Revision History

Current Version: 1.0, March 2001

Previous Version: 0.1, February 2000

Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
	3-3 ... 3-5	Interface schematics inserted
3-4, 3-5	4-5, 4-6	Hints on the crystal oszillator revised and moved to paragraph applications
3-5, 3-6	3-8, 3-9	Tables adapted, description of power modes revised
	3-10	Timing diagram added
4-1, 4-2	4-1 ... 4-6	new
5-3, 5-4	5-3 ... 5-5	Table corrected for pin1: „V > 1.4 V“ replaced by „pin open“ VCO frequency range added, some limits adapted
	5-6 ... 5-6	Table inserted: AC/DC characteristics over full supply- and temperature range

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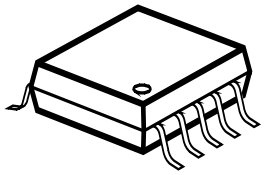
Product Info

General Description

The TDA 5103A is a single chip ASK transmitter for the frequency band 344-347 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a fully integrated PLL synthesizer and a high efficiency power amplifier to drive a loop antenna. A special circuit design and an unique power amplifier design are used to save current consumption and therefore to save battery life. Additionally features like a power down mode, a low power detect and a divided clock output are implemented.

Package



Features

- fully integrated frequency synthesizer
- VCO without external components
- high efficiency power amplifier
- frequency range 344-347 MHz
- ASK modulation
- low supply current (typically 7mA)
- voltage supply range 2.1 - 4 V
- power down mode
- low voltage sensor
- clock output for µC
- low external component count

Applications

- Keyless entry systems
- Remote control systems
- Alarm systems
- Communication systems

Ordering Information

Type	Ordering Code	Package
TDA 5103A	Q67036-A1121	P-TSSOP-10
available on tape and reel		

1 Table of Contents

2 Product Description

Contents of this Chapter

2.1 Overview

The TDA 5103A is a single chip ASK transmitter for the frequency band 344-347 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a fully integrated PLL synthesizer and a high efficiency power amplifier to drive a loop antenna. A special circuit design and an unique power amplifier design are used to save current consumption and therefore to save battery life. Additional features like a power down mode, a low power detect and a divided clock output are implemented.

2.2 Applications

- Keyless entry systems
- Remote control systems
- Alarm systems
- Communication systems

2.3 Features

- fully integrated frequency synthesizer
- VCO without external components
- high efficiency power amplifier
- frequency range 344-347 MHz
- ASK modulation
- low supply current (typically 7 mA)
- voltage supply range 2.1 - 4 V
- power down mode
- low voltage sensor
- clock output for µC
- low external component count

2.4 Package Outlines

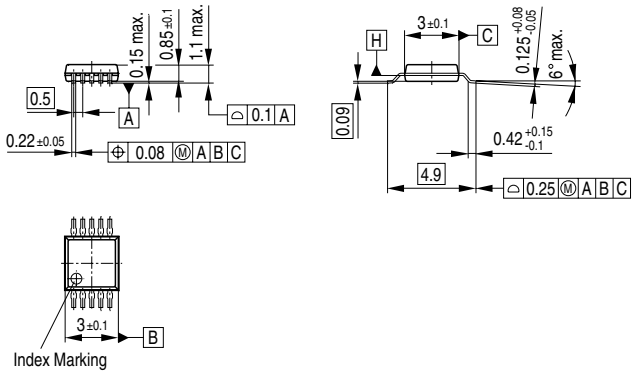
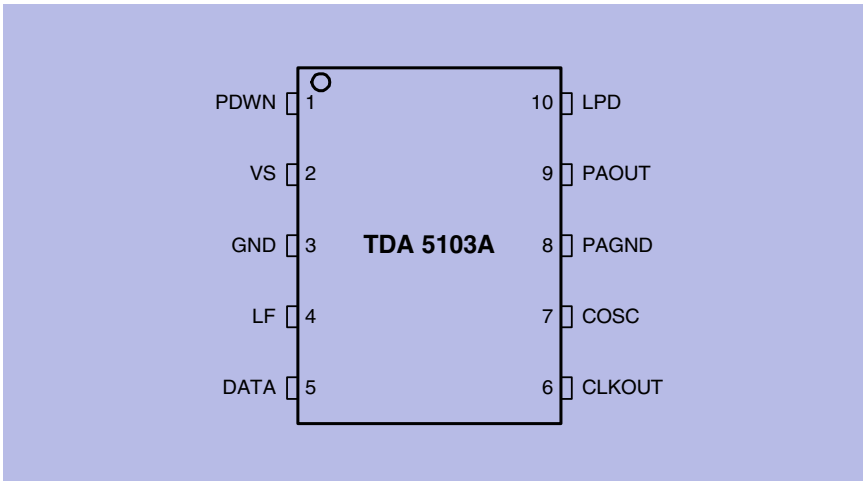


Figure 2-1 P-TSSOP-10

3 Functional Description

Contents of this Chapter

3.1 Pin Configuration



Pin_config.wmf

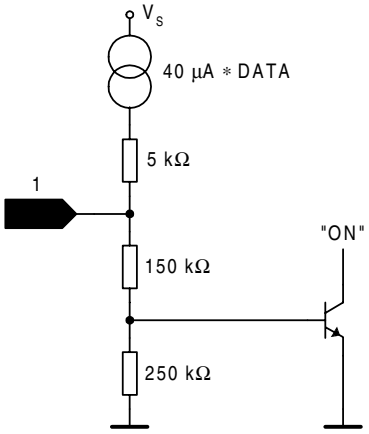
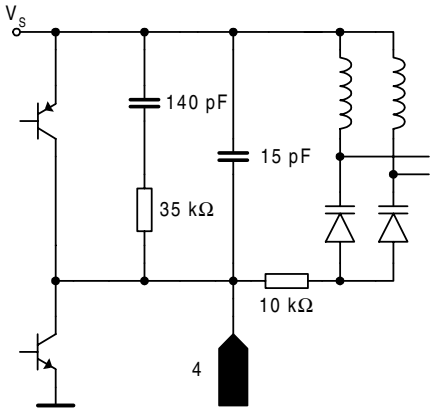
Figure 3-1 IC Pin Configuration

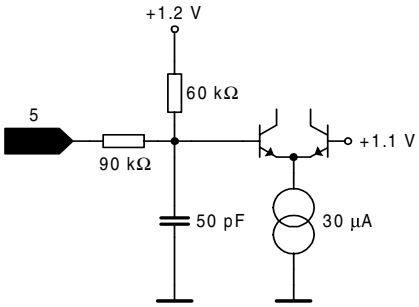
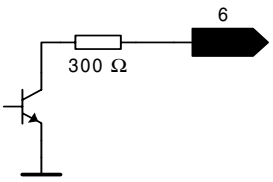
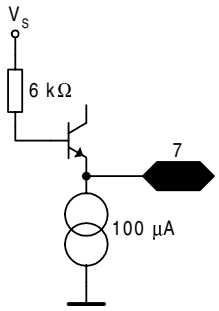
Table 3-1 Pin Configuration

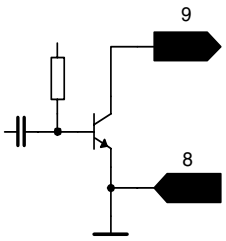
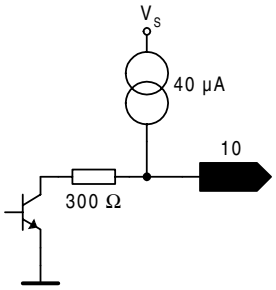
Pin No.	Symbol	Function
1	PDWN	Power Down Mode Control
2	VS	Voltage Supply
3	GND	Ground
4	LF	Loop Filter
5	DATA	Amplitude Shift Keying Data Input
6	CLKOUT	Clock Driver Output
7	COSC	Crystal Oscillator Input
8	PAGND	Power Amplifier Ground
9	PAOUT	Power Amplifier Output
10	LPD	Low Power Detect Output

3.2 Pin Definitions and Functions

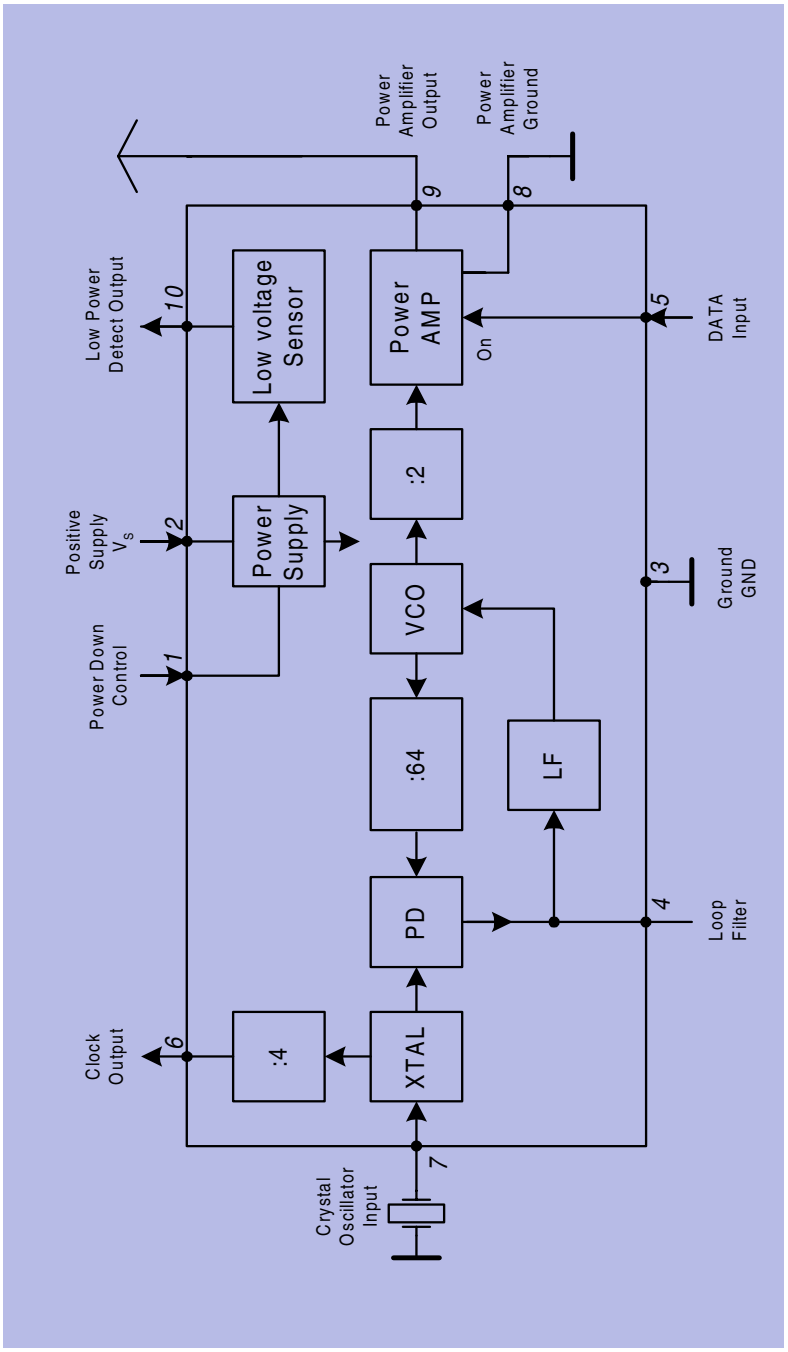
Table 3-2

Pin No.	Symbol	Interface Schematic	Function
1	PDWN		Disable pin for the complete transmitter circuit. A logic low (PDWN < 0.7 V) turns off all transmitter functions. A logic high (PDWN > 1.5 V) gives access to all transmitter functions. PDWN input will be pulled up by 40 µA internally by setting DATA to a logic high-state.
2	VS		This pin is the positive supply of the transmitter electronics. An RF bypass capacitor should be connected directly to this pin and returned to GND (pin 3) as short as possible.
3	GND		General ground connection.
4	LF		Output of the charge pump and input of the VCO control voltage. The loop bandwidth of the PLL is 150 kHz when only the internal loop filter is used. The loop bandwidth may be reduced by applying an external RC network referencing to the positive supply VS (pin 2).

5	DATA		Digital amplitude modulation can be imparted to the Power Amplifier through this pin. A logic high (DATA > 1.5 V or open) enables the Power Amplifier. A logic low (DATA < 0.5 V) disables the Power Amplifier.
6	CLKOUT		Clock output to supply an external device. An external pull-up resistor has to be added in accordance to the driving requirements of the external device. The clock output frequency is 2.7 MHz when a crystal of 10.78 MHz is used.
7	COSC		This pin is connected to the reference oscillator circuit. The reference oscillator is working as a negative impedance converter. It presents a negative resistance in series to an inductance at the COSC pin. The resonance frequency of the crystal should be 10.78 MHz to achieve an output frequency of 345 MHz.

8	PAGND		Ground connection of the power amplifier. The RF ground return path of the power amplifier output PAOUT (pin 9) has to be concentrated to this pin.
9	PAOUT		RF output pin of the transmitter. A DC path to the positive supply VS has to be supplied by the antenna matching network.
10	LPD		This pin provides an output indicating the low-voltage state of the supply voltage VS. VS < 2.15 V will set LPD to the low-state. An internal pull-up current of 40 µA gives the output a high-state at supply voltages above 2.15 V.

3.3 Functional Block diagram



Block_diagram.wmf

Figure 3-2 Functional Block diagram

3.4 Functional Blocks

3.4.1 PLL Synthesizer

The Phase Locked Loop synthesizer consists of a Voltage Controlled Oscillator (VCO), an asynchronous divider chain, a phase detector, a charge pump and a loop filter. It is fully implemented on chip. The tuning circuit of the VCO consisting of spiral inductors and varactor diodes is on chip, too. Therefore no additional external components are necessary. The nominal center frequency of the VCO is 690 MHz. The oscillator signal is fed both, to the synthesizer divider chain and to the power amplifier. The overall division ratio of the asynchronous divider chain is 64, a 10.78 MHz crystal should be used. The phase detector is a Type IV PD with charge pump. The passive loop filter is realized on chip.

3.4.2 Crystal Oscillator

The crystal oscillator operates at 10.78 MHz.

The output frequency at CLKOUT (pin 6) is 2.7 MHz, this is the crystal frequency divided by 4.

3.4.3 Power Amplifier

The VCO frequency 688-694 MHz is divided by 2 and fed to the power amplifier.

The Power Amplifier can be switched on and off
by the signal at DATA (pin 5).

Table 3-3

DATA (pin 5)	Power Amplifier
Low[1)]	OFF
Open[2)], High[3)]	ON

1) Low: Voltage at pin < 0.5 V
2) Open: Pin open
3) High: Voltage at pin > 1.5 V

The Power Amplifier has an Open Collector output at PAOUT (pin 9) and requires an external pull-up coil to provide bias. The coil is part of the tuning and matching LC circuitry to get best performance with the external loop antenna. To achieve the best power amplifier efficiency, the high frequency voltage swing at PAOUT (pin 9) should be twice the supply voltage.

The power amplifier has its own ground pin PAGND (pin 8) in order to reduce the amount of coupling to the other circuits.

3.4.4 Low Power Detect

The supply voltage is sensed by a low power detector. When the supply voltage drops below 2.15 V, the output LPD (pin 10) switches to the low-state. To minimize the external component count, an internal pull-up current of 40 µA gives the output a high-state at supply voltages above 2.15 V.

The output LPD (pin 10) can either be connected to DATA (pin 5) to switch off the PA as soon as the supply voltage drops below 2.15 V or it can be used to inform a micro-controller to stop the transmission after the current data packet.

3.4.5 Power Modes

The IC provides three power modes, the POWER DOWN MODE, the PLL ENABLE MODE and the TRANSMIT MODE.

3.4.5.1 Power Down Mode

In the POWER DOWN MODE the complete chip is switched off.

The current consumption is less than 100nA.

3.4.5.2 PLL Enable Mode

In the PLL ENABLE MODE the PLL is switched on but the power amplifier is turned off to avoid undesired power radiation during the time the PLL needs to settle. The turn on time of the PLL is determined mainly by the turn on time of the crystal oscillator and is typically less than 1 msec, depending on the crystal.

The current consumption is typically 3.5 mA.

3.4.5.3 Transmit Mode

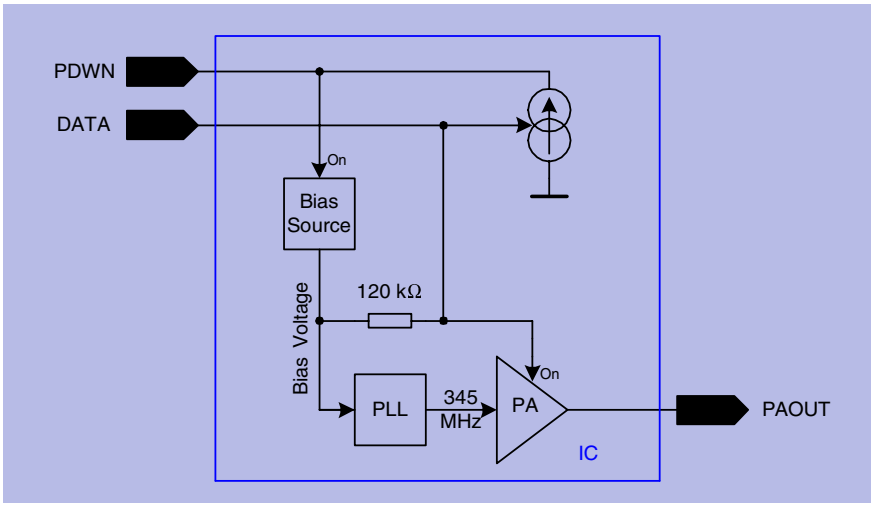
In the TRANSMIT MODE the PLL is switched on and the power amplifier is turned on too.

The current consumption of the IC is typically 7 mA when using a proper transforming network at PAOUT, see Figure 4-1.

3.4.5.4 Power mode control

The bias circuitry is powered up via a voltage V > 1.5 V at the pin PDWN (pin 1). When the bias circuitry is powered up, the pin DATA is pulled up internally. Forcing the voltage at the pin DATA low overrides the internally set state.

The principle schematic of the power mode control circuitry is shown in Figure 3-5.



Power_Mode.wmf

Figure 3-5 Power mode control circuitry

Table 3-4 provides a listing of how to get into the different power modes

Table 3-4

PDWN	DATA	MODE
Low[1)]	Low, Open[2)]	POWER DOWN
High[3)]	Low	PLL ENABLE
High	Open, High	TRANSMIT

1) Low: Voltage at pin < 0.7 V (PDWN)
Voltage at pin < 0.5 V (DATA)
2) Open: Pin open
3) High: Voltage at pin > 1.5 V

Other combinations of the control pins PDWN and DATA are not recommended.

3.4.6 Recommended timing diagram for ASK-Modulation

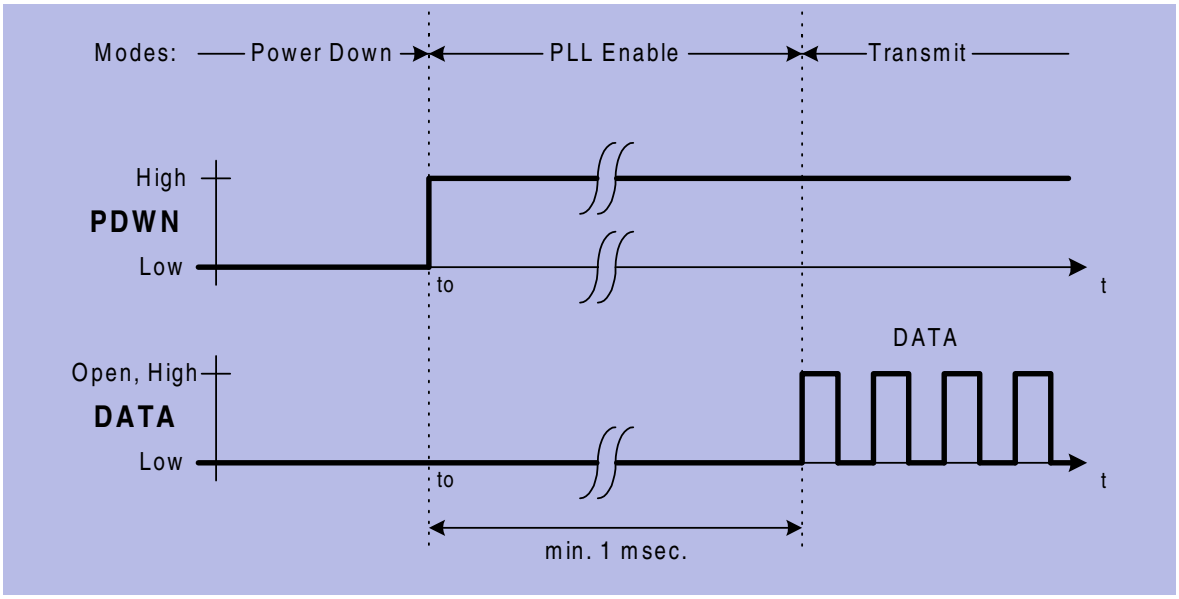


Figure 3-6 Recommended Timing Diagram for ASK Modulation

4 Applications

Contents of this Chapter

4.1 50 Ohm-Output Testboard Schematic

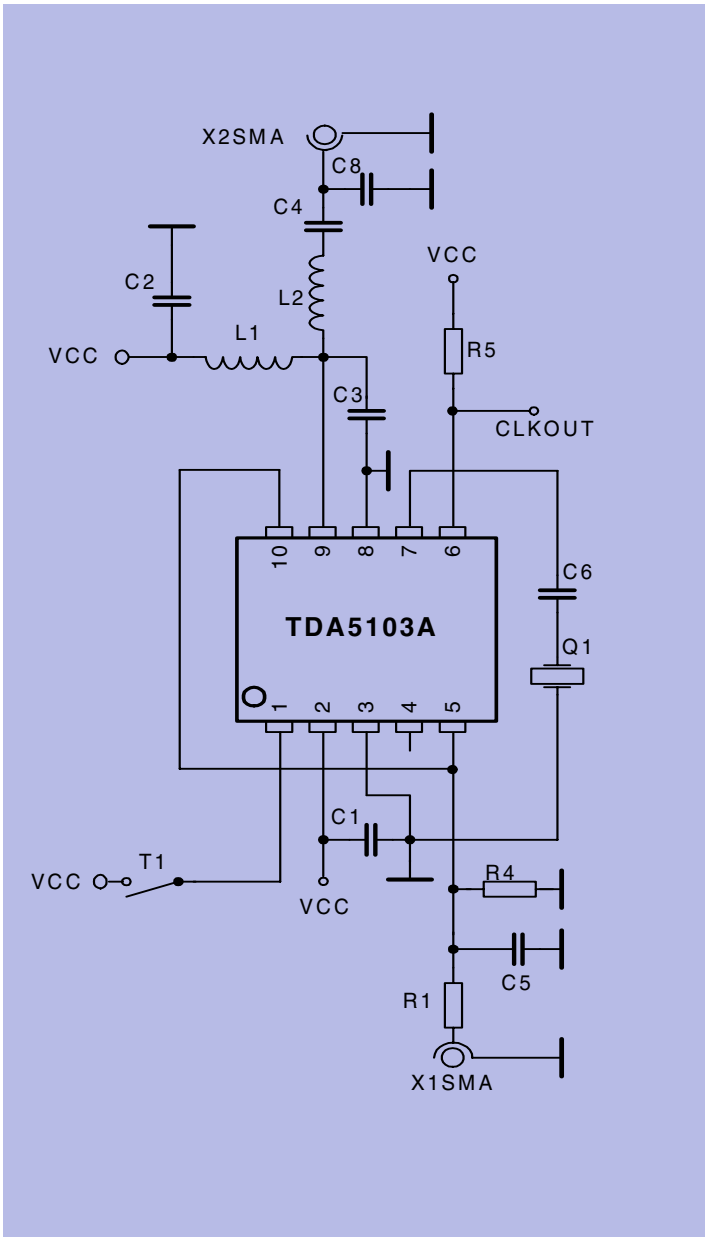


Figure 4-1 50 Ω-Output testboard schematic

4.2 50 Ohm-Output Testboard Layout

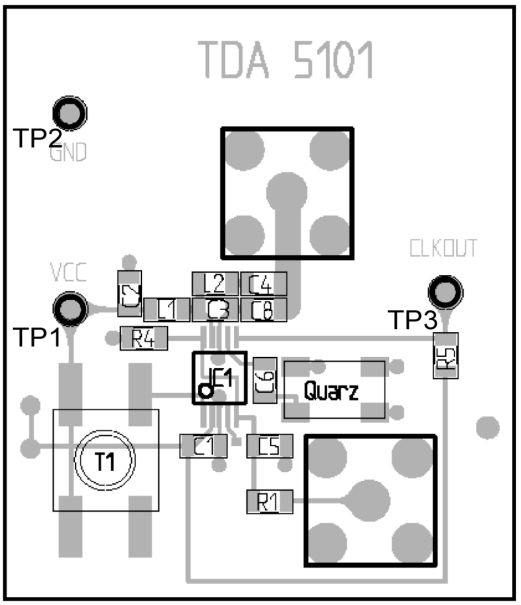


Figure 4-2 Top Side of TDA 5103A-Testboard with 50 Ω-Output
It is the same testboard as for an other product

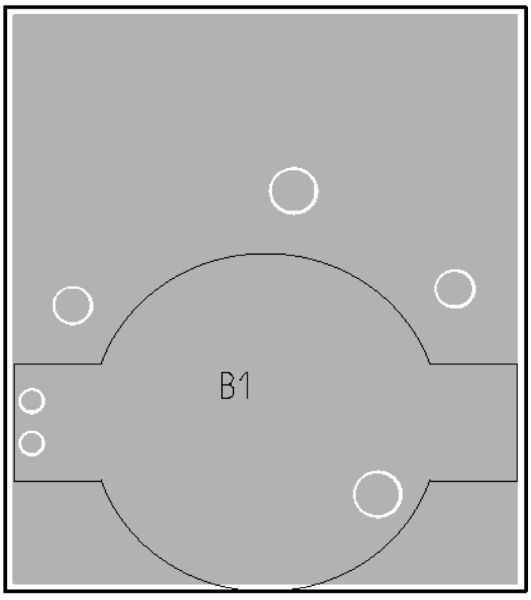


Figure 4-3 Bottom Side of TDA 5103A-Testboard with 50 Ω-Output
It is the same testboard as for an other product

4.3 Bill of material (50 Ohm-Output Testboard)

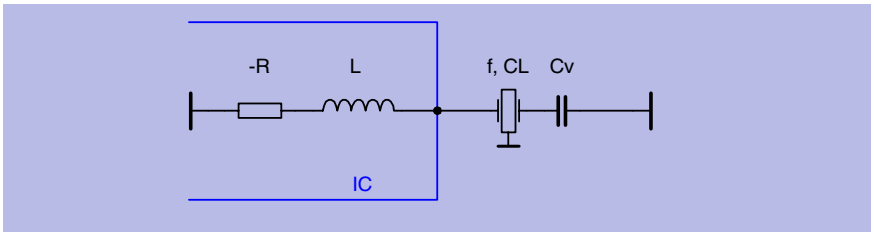
Table 4-1 Bill of material

Part	Value	Specification
R1	4.7 kΩ	0805, ± 5%
R4	open	0805, ± 5%
R5	open	0805, ± 5%
C1	47 nF	0805, X7R, ± 10%
C2	330 pF	0805, COG, ± 5%
C3	3.9 pF	0805, COG, ± 0.1 pF
C4	68 pF	0805, COG, ± 5%
C5	1 nF	0805, X7R, ± 10%
C6	tbd	0805, COG, ± 0.1 pF
C8	10 pF	0805, COG, ± 5%
L1	220 nH	TOKO LL2012-J
L2	56 nH	TOKO LL2012-J
Q1	10.78 MHz	
IC1	TDA 5103A	
T1	Push-button	replaced by a short
B1	Battery clip	HU2031-1,RENATA
X1	SMA-S	SMA standing
X2	SMA-S	SMA standing

4.4 Hints

1. Application Hints on the crystal oscillator

As mentioned before, the crystal oscillator achieves a turn on time less than 1 msec. To achieve this, a NIC oscillator type is implemented in the TDA 5103A. The input impedance of this oscillator is a negative resistance in series to an inductance. Therefore the load capacitance of the crystal CL (specified by the crystal supplier) is transformed to the capacitance Cv.



$$Cv = \frac{1}{\frac{1}{CL} + \omega^2 L}$$ Formula 1)

CL: crystal load capacitance for nominal frequency

ω: angular frequency

L: inductance of the crystal oscillator

Example:

Assume a crystal frequency of 10.78 MHz and a crystal load capacitance of CL = 12 pF. The inductance L is specified within the electrical characteristics at 10.78 MHz to a value of 11 µH. Therefore C6 is calculated to 7.5 pF.

$$Cv = \frac{1}{\frac{1}{CL} + \omega^2 L} = C6$$

2. Design hints on the buffered clock output (CLKOUT)

The CLKOUT pin is an open collector output. An external pull up resistor (RL) should be connected between this pin and the positive supply voltage. The value of RL is depending on the clock frequency and the load capacitance CLD (PCB board plus input capacitance of the microcontroller). RL can be calculated to:

$$RL = \frac{1}{fCLKOUT * 8 * CLD}$$

Table 4-2

fCLKOUT= 2.7 MHz	
CL[pF]	RL[kOhm]
5	8.2
10	4.7
20	2.2

Remark: To achieve a low current consumption and a low spurious radiation, the largest possible RL should be chosen.

5 Reference

Contents of this Chapter

5.1 Absolute Maximum Ratings

The AC / DC characteristic limits are not guaranteed. The maximum ratings must not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC may result.

Table 5-1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		Min	Max		
Junction Temperature	T_J	-40	150	°C	
Storage Temperature	T_s	-40	125	°C	
Thermal Resistance	R_{thJA}		220	K/W	
ESD integrity, all pins	V_{ESD}	-1	+1	kV	100 pF, 1500 Ω

Ambient Temperature under bias: T_A=-25°C to +85°C

5.2 Operating Range

Within the operating range the IC operates as described in the circuit description.

Table 5-2 Operating Range

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min	Max		
Supply voltage	V_S	2.1	4.0	V	
Ambient temperature	T_A	-25	85	°C	

5.3 AC/DC Characteristics

5.3.1 AC/DC Characteristics at 3V, 25°C

Table 5-3 Supply Voltage V_S = 3 V, Ambient temperature T_{amb} = 25°C

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min	Typ	Max		
Current consumption						
Power down mode	$I_{S\ PDWN}$			100	nA	V (Pins 1 and 5) = 0 V
PLL enable mode	$I_{S\ PLL\_EN}$		3.3	4.2	mA	
Transmit mode	$I_{S\ TRANSM}$		7	9	mA	Load tank see Figure 4-1
Power Down Mode Control (Pin 1)						
Power down mode	V_{PDWN}	0		0.7	V	V_{DATA} < 0.2 V
PLL enable mode	V_{PDWN}	1.5		V_S	V	V_{DATA} < 0.5 V
Transmit mode	V_{PDWN}	1.5		V_S	V	V_{DATA} > 1.5 V
Input bias current PDWN	I_{PDWN}			30	µA	$V_{PDWN} = V_S$
Loop Filter (Pin 4)						
VCO tuning voltage	V_{LF}	V_S - 1.3		V_S - 0.8	V	f_{VCO} = 690 MHz
Output frequency range 345 MHz-band	$f_{OUT,\ 345}$	338	345	352	MHz	V_S-V_{LF} = 0.6V...1.6V
ASK Modulation Data Input (Pin 5)						
Transmit disabled	V_{DATA}	0		0.5	V	
Transmit enabled	V_{DATA}	1.5		V_S	V	
Input bias current DATA	I_{DATA}			30	µA	$V_{DATA} = V_S$
Input bias current DATA	I_{DATA}	-20			µA	V_{DATA} = 0 V
ASK data rate	f_{DATA}			20	kHz	

Table 5-3 Supply Voltage V_S = 3 V, Ambient temperature T_{amb} = 25°C

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min	Typ	Max		
Clock Driver Output (Pin 6)						
Output current (Low)	I_{CLKOUT}	1			mA	$V_{CLKOUT} = V_S$
Output current (High)	I_{CLKOUT}			-40	µA	V_{CLKOUT} = 0 V
Saturation Voltage (Low)	V_{SATL}			0.9	V	I_{CLKOUT} = 1 mA
Saturation Voltage (High)	V_{SATH}	V_S - 0.9			V	I_{CLKOUT} = 0 mA
Crystal Oscillator Input (Pin 7)						
Load capacitance	$C_{COSCmax}$			5	pF	
Serial Resistance of the crystal				100	Ω	f = 10.78 MHz
Input inductance of the COSC pin			11		µH	f = 10.78 MHz
Power Amplifier Output (Pin 9)						
Output Power[1] transformed to 50 Ohm	P_{OUT345}	3	5	7	dBm	f_{OUT} = 345 MHz
Low Power Detect Output (Pin 10)						
Internal pull up current	I_{LPD1}	30			µA	V_S = 2.3 V ... V_S
Input current low voltage	I_{LPD2}	1			mA	V_S = 1.9 V ... 2.1 V

1) Power amplifier in overcritical C-operation.
Matching circuitry as used in the 50 Ohm-Output Testboard.

5.3.2 AC/DC Characteristics at 2.1 V ... 4.0 V, -25°C ... +85°C

Table 5-4 Supply Voltage V_S = 2.1 V ... 4.0 V, Ambient temperature T_{amb} = -25°C ... +85°C

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min	Typ	Max		
Current consumption						
Power down mode	$I_{S\ PDWN}$			250	nA	V (Pins 1 and 5) = 0 V
PLL enable mode	$I_{S\ PLL\_EN}$		3.3	4.6	mA	
Transmit mode	$I_{S\ TRANSM}$		7	9.5	mA	Load tank see Figure 4-1
Power Down Mode Control (Pin 1)						
Power down mode	V_{PDWN}	0		0.5	V	V_{DATA} < 0.2 V
PLL enable mode	V_{PDWN}	1.5		V_S	V	V_{DATA} < 0.5 V
Transmit mode	V_{PDWN}	1.5		V_S	V	V_{DATA} > 1.5 V
Input bias current PDWN	I_{PDWN}			30	µA	$V_{PDWN} = V_S$
Loop Filter (Pin 4)						
VCO tuning voltage	V_{LF}	V_S - 1.5		V_S - 0.65	V	f_{VCO} = 690 MHz
Output frequency range 345 MHz-band	$f_{OUT,\ 315}$	343.5	345	347.5	MHz	V_S-V_{LF} = 0.6V...1.6V
ASK Modulation Data Input (Pin 5)						
Transmit disabled	V_{DATA}	0		0.5	V	
Transmit enabled	V_{DATA}	1.5		V_S	V	
Input bias current DATA	I_{DATA}			30	µA	$V_{DATA} = V_S$
Input bias current DATA	I_{DATA}	-20			µA	V_{DATA} = 0 V
ASK data rate	f_{DATA}			20	kHz	

Table 5-4 Supply Voltage V_S = 2.1 V ... 4.0 V, Ambient temperature T_{amb} = -25°C ... +85°C

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min	Typ	Max		
Clock Driver Output (Pin 6)						
Output current (Low)	I_{CLKOUT}	1			mA	$V_{CLKOUT} = V_S$
Output current (High)	I_{CLKOUT}			-40	µA	V_{CLKOUT} = 0 V
Saturation Voltage (Low)	V_{SATL}			0.9	V	I_{CLKOUT} = 1 mA
Saturation Voltage (High)	V_{SATH}	V_S - 0.9			V	I_{CLKOUT} = 0 mA
Crystal Oscillator Input (Pin 7)						
Load capacitance	$C_{COSCmax}$			5	pF	
Serial Resistance of the crystal				100	Ω	f = 10.78 MHz
Input inductance of the COSC pin			11		µH	f = 10.78 MHz
Power Amplifier Output (Pin 9)						
Output Power[1] transformed to 50 Ohm	P_{OUT345}	-2.5	2.5	5.5	dBm	V_s = 2.2 V[2]
	P_{OUT345}	0	5	8	dBm	V_s = 3.0 V
	P_{OUT345}	2	7	10	dBm	V_s = 4.0 V
Low Power Detect Output (Pin 10)						
Internal pull up current	I_{LPD1}	30			µA	V_S = 2.3 V ... V_S
Input current low voltage	I_{LPD2}	1			mA	V_S = 1.9 V ... 2.1 V

1) Power amplifier in overcritical C-operation.
Matching circuitry as used in the 50 Ohm-Output Testboard.
Supply-voltage dependency: 2 dB / V at 3 V with reference to 3 V.
A smaller load impedance reduces the supply-voltage dependency.
Temperature dependency: +1 dB at -25°c and -3 dB at +85°C with reference to +25°C.
A higher load impedance reduces the temperature dependency.

2) Power amplifier is switched off at 2.15 V