National Semiconductor

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LMX9830
Bluetooth® Serial Port Module

1.0 General Description

The National Semiconductor LMX9830 Bluetooth Serial Port module is a highly integrated Bluetooth 2.0 baseband controller and 2.4 GHz radio, combined to form a complete small form factor (6.1 mm x 9.1 mm x 1.2 mm) Bluetooth node.

All hardware and firmware is included to provide a complete solution from antenna through the complete lower and upper layers of the Bluetooth stack, up to the application including the Generic Access Profile (GAP), the Service Discovery Application Profile (SDAP), and the Serial Port Profile (SPP). The module includes a configurable service database to fulfil service requests for additional profiles on the host. Moreover, the LMX9830 is pre-qualified as a Bluetooth Integrated Component. Conformance testing through the Bluetooth qualification program enables a short time to market after system integration by insuring a high probability of compliance and interoperability.

Based on National's CompactRISC® 16-bit processor architecture and Digital Smart Radio technology, the LMX9830 is optimized to handle the data and link management processing requirements of a Bluetooth node.

The firmware supplied in the on-chip ROM memory offers a complete Bluetooth (v2.0) stack including profiles and command interface. This firmware features point-to-point and point-to-multipoint link management supporting data rates up to the theoretical maximum over RFComm of 704 kbps (**Best in Class** in the industry). The internal memory supports up to 7 active Bluetooth data links and one active SCO link.

The on-chip Patch RAM provided for lowest cost and risk, allows the flexibility of firmware upgrade.

The LMX9830 module is lead free and RoHS (Restriction of Hazardous Substances) compliant. For more information on those quality standards, please visit our green compliance website at http://www.national.com/quality/green/

2.0 Features

- Compliant with the Bluetooth 2.0 Core Specification
  - Qualified Design ID (PRD 2.0): B012364
- Better than -80 dBm input sensitivity
- Class 2 operation
- Low power consumption
- High integration:
  - Implemented in 0.18 µm CMOS technology
  - RF includes antenna filter and switch on-chip

3.0 Other Features

3.1 DIGITAL HARDWARE

- Baseband and Link Management processors
- CompactRISC Core
- Embedded ROM and Patch RAM memory
- UART Command/Data Port:
  - Support for up to 921.6k baud rate
- Auxiliary Host Interface Ports:
  - Link Status
  - Transceiver Status (Tx or Rx)
  - Three General Purpose I/Os, available through the API
  - Alternative IO functions:
    - Link Status
    - Transport layer activity
- Advanced Power Management (APM) features:
  - Advanced power management functions
- Advanced Audio Interface for external PCM codec
- ACCESS.bus and SPI/Microwire for interfacing with external non-volatile memory

3.2 FIRMWARE

- Complete Bluetooth Stack including:
  - Baseband and Link Manager
  - L2CAP, RFCOMM, SDP
  - Profiles:
    - GAP
    - SDAP
    - SPP
- Additional Profile support on Host, e.g.:
  - Dial Up Networking (DUN)
  - Facsimile Profile (FAX)
  - File Transfer Protocol (FTP)
  - Object Push Profile (OPP)
  - Synchronization Profile (SYNC)
  - Headset (HSP)
  - Handsfree Profile (HFP)
  - Basic Imaging Profile (BIP)
  - Basic Printing Profile (BPP)
- On-chip application including:
  - Default connections
  - Command Interface:
    - Link setup and configuration (also Multipoint)
    - Configuration of the module
    - Service database modifications
  - UART Transparent mode
  - Optimized cable replacement :
    - Automatic transparent mode

- Event filter

3.3 DIGITAL SMART RADIO

- Accepts external clock or crystal input:
  - 13 MHz Typical
  - Supports 10 - 20 MHz
  - Secondary 32.768 kHz oscillator for low-power modes
  - 20 ppm cumulative clock error required for Bluetooth
- Synthesizer:
  - Integrated VCO
  - Provides all clocking for radio and baseband functions
- Antenna Port (50 Ω nominal impedance):
  - Embedded front-end filter for enhanced out of band performance
- Integrated transmit/receive switch (full duplex operation via antenna port)
- Better than -80 dBm input sensitivity
- 0 dBm typical output power

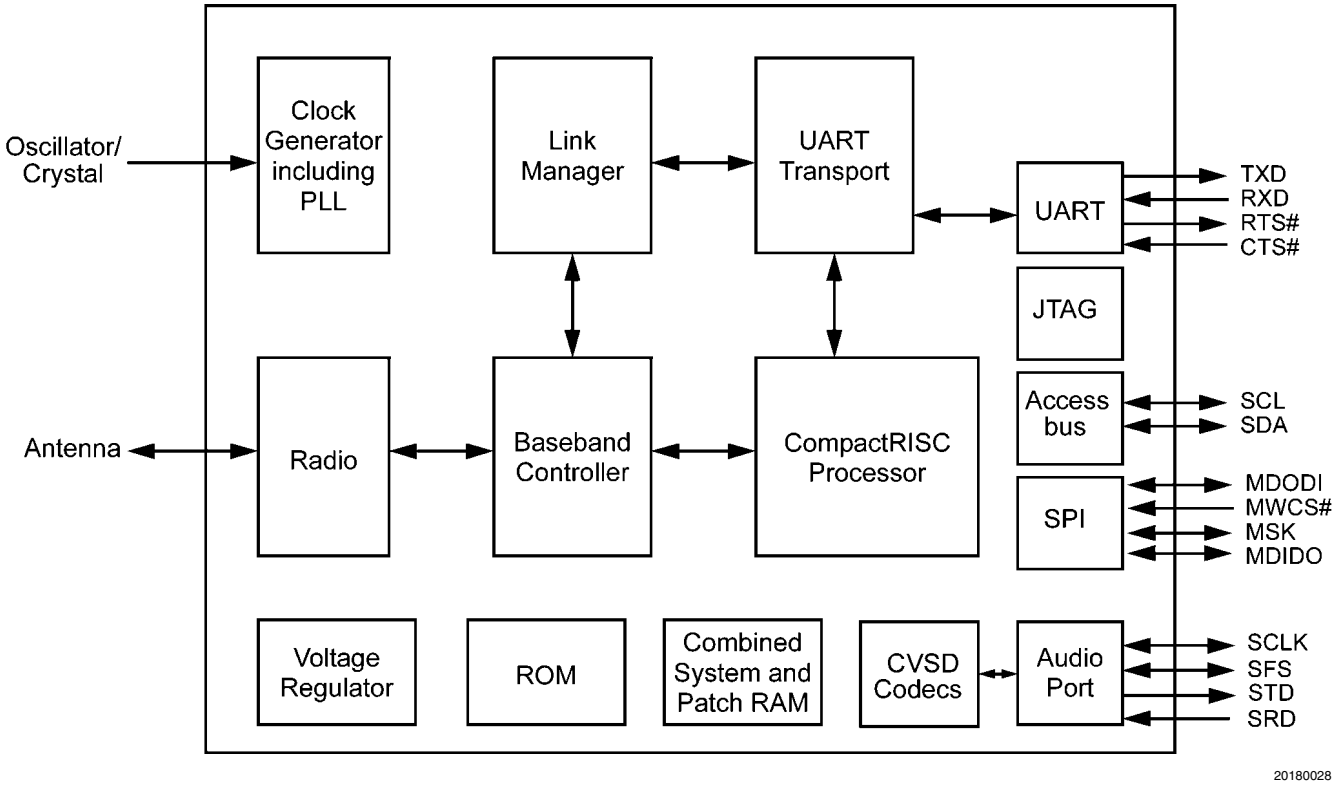
3.4 PHYSICAL

- Compact size - 6.1 mm x 9.1 mm x 1.2 mm
- Complete system interface provided in Ball Grid Array on underside for surface mount assembly

4.0 Applications

- Personal Digital Assistants
- POS Terminals
- Data Logging Systems
- Audio Gateway application
- Telemedicine/Medical, Industrial and Scientific

5.0 Functional Block Diagram



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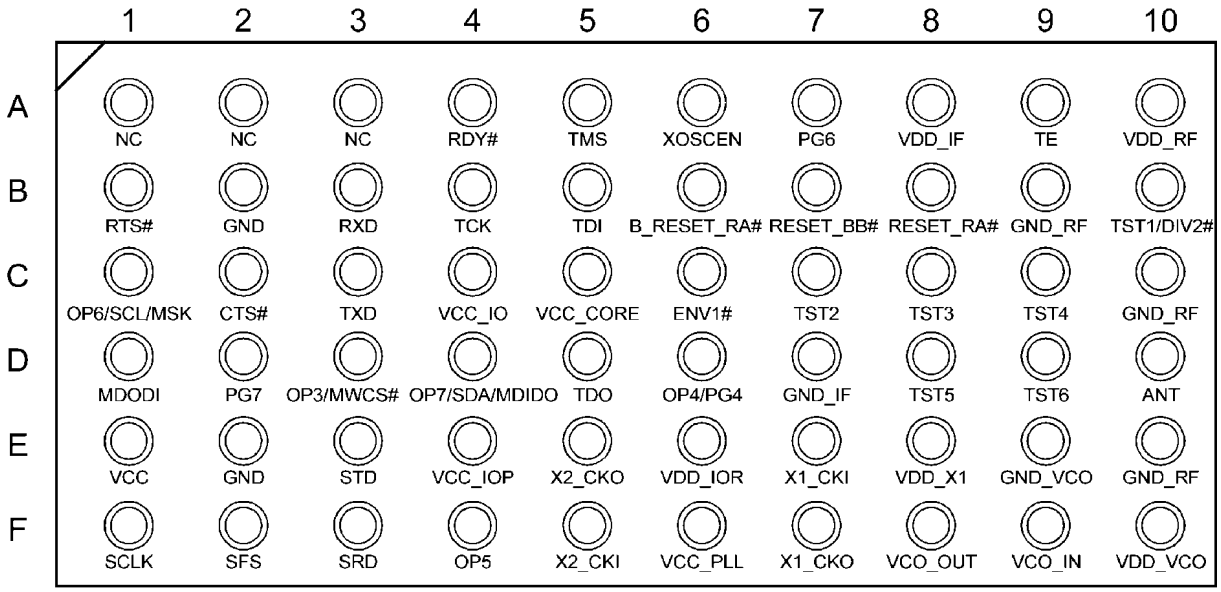
6.0 Ordering Information

Order Number	Spec.	Shipment Method
LMX9830SM	NOPB (Note 1)	388 pcs Tray
LMX9830SMX	NOPB (Note 1)	2500 pcs Tape & Reel

Note 1: NOPB = No Pb (No Lead)

7.0 Connection Diagram

FBGA, Plastic, Laminate, 9x6x1.2mm, 60 Ball, 0.8mm Pitch Package (SLF60A)



X-ray - Top View

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7.1 PAD DESCRIPTIONS

TABLE 1. Pin Descriptions

Pad Name	Pad Location	Type	Default Layout	Description
X1_CKO	F7	O		Crystal 10-20 MHz
X1_CKI	E7	I		Crystal or External Clock 10-20 MHz
X2_CKI	F5	I	GND **(if not used)**	32.768 kHz Crystal Oscillator
X2_CKO	E5	O	NC **(if not used)**	32.768 kHz Crystal Oscillator
RESET_RA#	B8	I		Radio Reset (active low)
B_RESET_RA#	B6	O	NC	Buffered Reset Radio Output (active low)
RESET_BB#	B7	I		Baseband Reset (active low)
ENV1#	C6	I	NC	ENV1: Environment Select (active low) used for manufacturing test only
TE	A9	I	GND	Test Enable - Used for manufacturing test only
TST1/DIV2#	B10	I	NC	**TST1**: Test Mode. Leave not connected to permit use with VTune automatic tuning algorithm **DIV2#**: No longer supported
TST2	C7	I	GND	Test Mode, Connect to GND
TST3	C8	I	GND	Test Mode, Connect to GND
TST4	C9	I	GND	Test Mode, Connect to GND
TST5	D8	I	GND	Test Mode, Connect to GND
TST6	D9	I	VCO_OUT	Test Input, Connect to VCO_OUT via 0 Ω resistor to permit use with VTune automatic tuning algorithm
MDODI (Note 2)	D1	I/O		SPI Master Out Slave In
OP6/SCL/MSK	C1	**OP6:** I **SCL/MSK:** I/O	See *Table 16*	**OP6**: Pin checked during Startup Sequence for configuration option **SCL:** ACCESS.Bus Clock **MSK**: SPI Shift

Pad Name	Pad Location	Type	Default Layout	Description
OP7/SDA/ MDIDO	D4	**OP7**: I **SDA/MDIDO**: I/O	See *Table 16*	**OP7**: Pin checked during Startup Sequence for configuration option **SDA:** ACCESS.Bus Serial Data **MDIDO**: SPI Master In Slave Out
OP3/MWCS#	D3	I	See *Table 16* and *Table 17*	**OP3:** Pin checked during Startup Sequence for configuration option **MWCS#:** SPI Slave Select Input (active low)
OP4/PG4	D6	**OP4:** I **PG4:** I/O	See *Table 16* and *Table 17*	**OP4**: Pin checked during Startup Sequence for configuration option **PG4:** GPIO
OP5	F4	I/O	See *Table 16* and *Table 17*	**OP5:** Pin checked during Startup Sequence for configuration option
SCLK	F1	I/O		Audio PCM Interface Clock
SFS	F2	I/O		Audio PCM Interface Frame Synchronization
SRD	F3	I		Audio PCM Interface Receive Data Input
STD	E3	O		Audio PCM Interface Transmit Data Output
XOSCEN	A6	O		Clock Request. Toggles with X2 (LP0) crystal enable/ disable
PG6	A7	I/O		GPIO
PG7	D2	I/O		GPIO - Default setup RF traffic LED indication
CTS#(Note 3)	C2	I	GND **(if not used)**	Host Serial Port Clear To Send (active low)
RXD	B3	I		Host Serial Port Receive Data
RTS#(Note 4)	B1	O	NC **(if not used)**	Host Serial Port Request To Send (active low)
TXD	C3	O		Host Serial Port Transmit Data
RDY#	A4	O	NC	JTAG Ready Output (active low)
TCK	B4	I	NC	JTAG Test Clock Input
TDI	B5	I	NC	JTAG Test Data Input
TDO	D5	O	NC	JTAG Test Data Output
TMS	A5	I	NC	JTAG Test Mode Select Input
VCO_OUT	F8	O		Charge Pump Output, connect to Loop filter
VCO_IN	F9	I		VCO Tuning Input, feedback from Loop filter
ANT	D10	I/O		RF Antenna 50 Ω Nominal Impedance
VCC_PLL	F6	O		1.8V Core Logic Power Supply Output
VCC_CORE	C5	O		1.8V Voltage Regulator Output
VDD_X1	E8	I		Power Supply Crystal Oscillator
VDD_VCO	F10	I		Power Supply VCO
VDD_RF	A10	I		Power Supply RF
VDD_IOR	E6	I		Power Supply I/O Radio/BB
VDD_IF	A8	I		Power Supply IF
VCC_IOP	E4	I		Power Supply Audio Interface
VCC_IO	C4	I		Power Supply I/O
VCC	E1	I		Voltage Regulator Input
GND_VCO	E9			Ground
GND_RF	B9, C10, E10			Ground
GND_IF	D7			Ground
GND	B2,E2			Ground
NC	A1,A2,A3		NC	Treat as no connect. Place pad for mechanical stability

Note 2: Must use 1k Ω pull up.

Note 3: Connect to GND if CTS is not use.

Note 4: Treat as No Connect if RTS is not used. Pad required for mechanical stability.

8.0 General Specifications

Absolute Maximum Ratings (see *Table 2*) indicate limits beyond which damage to the device may occur. Operating Ratings (see *Table 3*) indicate conditions for which the device is intended to be functional.

This device is a high performance RF integrated circuit and is ESD sensitive. Handling and assembly of this device should be performed at ESD free workstations.

The following conditions are true unless otherwise stated in the tables below:

- T_A = -40°C to +85°C
- V_{CC} = 3.3V
- RF system performance specifications are guaranteed on National Semiconductor Mesa board rev 1.1 reference design platform.

TABLE 2. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{CC}	Digital Voltage Regulator input	-0.2	4	V
V_I	Voltage on any pad with GND = 0V	-0.2	V_{CC} + 0.2	V
VDD_RF	Supply Voltage Radio	0.2	3.3	V
VDD_IF				
VDD_X1				
VDD_VCO				
P_{IN}RF	RF Input Power		0	dBm
V_{ANT}	Applied Voltage to ANT pad		1.95	V
T_S	Storage Temperature Range	-65	+150	°C
T_L	Lead Temperature (Note 5) (solder 4 sec.)		225	°C
T_{LNOPB}	Lead Temperature NOPB (Note 5), (Note 6) (solder 40 sec.)		260	°C
ESD_{HBM}	ESD - Human Body Model		2000	V
ESD_{MM}	ESD - Machine Model		200 (Note 7)	V

Note 5: Reference IPC/JDEC J-STD-20C spec.

Note 6: NOPB = No Pb (No Lead).

Note 7: A 200V ESD rating applies to all pins except OP3, OP6, OP7, MDODI, SCLK, SFS, STD, TDO, and ANT pins = 150V.

TABLE 3. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Digital Voltage Regulator input	2.5	2.75	3.6	V
T_R	Digital Voltage Regulator Rise Time			10	µs
T_A	Ambient Operating Temperature Range Fully Functional Bluetooth Node	-40	+25	+125	°C
VCC_IO	Supply Voltage Digital I/O	1.6	3.3	3.6	V
VCC_PLL	Internally connected to VCC_Core				
VDD_RF	Supply Voltage Radio	2.5	2.75	3	V
VDD_IF					
VDD_X1					
VDD_VCO					
VDD_IOR	Supply Voltage Radio I/O	1.6	2.75	VDD_RF	V
VCC_IOP	Supply Voltage PCM Interface	1.6	3.3	3.6	V
VCC_CORE	Supply Voltage Output		1.8		V
VCC_CORE_{MAX}	Supply Voltage Output Max Load		5		mA
VCC_CORE_{SHORT}	When used as Supply Input (V_{CC} grounded)	1.6	1.8	2	V

TABLE 4. Power Supply Requirements (Notes 8, 9)

Symbol	Parameter	Min	Typ (Note 10)	Max	Unit
I_{CC-TX}	Power supply current for continuous transmit			65	mA
I_{CC-RX}	Power supply current for continuous receive			65	mA
I_{RXSL}	Receive Data in SPP Link, Slave (Note 11)		26		mA
I_{RXM}	Receive Data in SPP Link, Master (Note 11)		23		mA
I_{SnM}	Sniff Mode, Sniff interval 1 second (Note 11)		5.6		mA
$I_{SC-TLDIS}$	Scanning, No Active Link, TL Disabled (Note 11)		0.43		mA
I_{Idle}	Idle, Scanning Disabled, TL Disabled (Note 11)		100		µA

Note 8: Power supply requirements based on Class II output power.

Note 9: Based on UART Baudrate 921.6 kbit/s.

Note 10: V_{CC} = 3.3V, VCC_IO = 3.3V, Ambient Temperature = +25°C.

Note 11: Average values excluding IO.

8.1 DC CHARACTERISTICS

TABLE 5. Digital DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
V_{IH}	Logical 1 Input Voltage high (except oscillator I/O)	1.6V ≤ VCC_IO ≤ 3.0V 3.0V ≤ VCC_IO ≤ 3.6V	0.7 x VCC_IO 2	VCC_IO + 0.2 VCC_IO + 0.2	V
V_{IL}	Logical 0 Input Voltage low	1.6V ≤ VCC_IO ≤ 3.0V	-0.2	0.25 x VCC_IO	V
	(except oscillator I/O)	3.0V ≤ VCC_IO ≤ 3.6V	-0.2	0.8	
V_{HYS}	Hysteresis Loop Width (Note 12)		0.1 x VCC_IO		V
I_{OH}	Logical 1 Output Current	V_{OH} = 2.4V, VCC_IO = 3.0V	-10		mA
I_{OL}	Logical 0 Output Current	V_{OH} = 0.4V, VCC_IO = 3.0V	10		mA

Note 12: Guaranteed by design.

8.2 RF PERFORMANCE CHARACTERISTICS

In the performance characteristics tables the following applies:

- All tests performed are based on Bluetooth Test Specification revision 2.0.
- All tests are measured at antenna port unless otherwise specified
- T_A = -40°C to +85°C
- VDD_RF = 2.8V unless otherwise specified.

RF system performance specifications are guaranteed on National Semiconductor Mesa Board rev 1.1 reference design platform.

TABLE 6. Receiver Performance Characteristics

Symbol	Parameter	Condition		Min	Typ (Note 13)	Max	Unit
RX_{sense}	Receive Sensitivity	BER < 0.001	2.402 GHz		-80	-76	dBm
			2.441 GHz		-80	-76	dBm
			2.480 GHz		-80	-76	dBm
$P_{in}RF$	Maximum Input Level			-10	0		dBm
IMP (Note 14), (Note 15)	Intermodulation Performance	F1= + 3 MHz, F2= + 6 MHz, $P_{in}RF$ = -64 dBm		-38	-36		dBm
RSSI	RSSI Dynamic Range at LNA Input			-72		-52	dBm

Symbol	Parameter	Condition	Min	Typ (Note 13)	Max	Unit
Z_{RFIN} (Note 15)	Input Impedance of RF Port (RF_inout)	Single input impedance F_{in} = 2.5 GHz		32		Ω
Return Loss (Note 15)	Return Loss				-8	dB
OOB (Note 14), (Note 15)	Out Of Band Blocking Performance	P_{in}RF = -10 dBm, 30 MHz < F_{CWI} < 2 GHz, BER < 0.001	-10			dBm
		P_{in}RF = -27 dBm, 2000 MHz < F_{CWI} < 2399 MHz, BER < 0.001	-27			dBm
		P_{in}RF = -27 dBm, 2498 MHz < F_{CWI} < 3000 MHz, BER < 0.001	-27			dBm
		P_{in}RF = -10 dBm, 3000 MHz < F_{CWI} < 12.75 GHz, BER < 0.001	-10			dBm

Note 13: Typical operating conditions are at 2.75V operating voltage and 25°C ambient temperature.

Note 14: The f_0 = -64 dBm Bluetooth modulated signal, f_1 = -39 dbm sine wave, f_2 = -39 dBm Bluetooth modulated signal, $f_0 = 2f_1 - f_2$, and $|f_2 - f_1| = n * 1$ MHz, where n is 3, 4, or 5. For the typical case, n = 3.

Note 15: Not tested in production.

TABLE 7. Transmitter Performance Characteristics

Symbol	Parameter	Condition	Min	Typ (Note 13)	Max	Unit
P_{OUT}RF	Transmit Output Power	2.402 GHz	–4	0	+3	dBm
		2.441 GHz	–4	0	+3	dBm
		2.480 GHz	–4	0	+3	dBm
MOD $\Delta F1_{AVG}$	Modulation Characteristics	Data = 00001111	140	165	175	kHz
MOD $\Delta F2_{MAX}$ (Note 17)	Modulation Characteristics	Data = 10101010	115	125		kHz
$\Delta F2_{AVG}/DF1_{AVG}$ (Note 18)	Modulation Characteristics		0.8			
20 dB Bandwidth					1000	kHz
$P_{OUT}2*f_o$ (Note 19)	PA 2nd Harmonic Suppression	Maximum gain setting: f_0 = 2402 MHz, P_{out} = 4804 MHz			-30	dBm
Z_{RFOUT} (Note 20)	RF Output Impedance/Input Impedance of RF Port (RF_inout)	P_{out} @ 2.5 GHz		47		Ω

Note 16: Typical operating conditions are at 2.75V operating voltage and 25°C ambient temperature.

Note 17: ΔF2max ≥ 115 kHz for at least 99.9% of all Δf2max.

Note 18: Modulation index set between 0.28 and 0.35.

Note 19: Out-of-Band spurs only exist at 2nd and 3rd harmonics of the CW frequency for each channel.

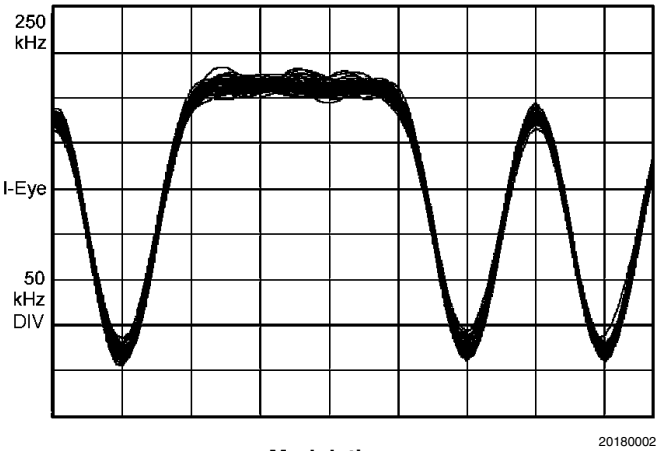
Note 20: Not tested in production.

TABLE 8. Synthesizer Performance Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{VCO}	VCO Frequency Range		2402		2480	MHz
t_{LOCK}	Lock Time	f_0 ± 20 kHz		120		µs
Δf_0offset (Note 21)	Initial Carrier Frequency Tolerance	During preamble	-75	0	75	kHz
Δf_0drift (Note 21)	Initial Carrier Frequency Drift	DH1 data packet	-25	0	25	kHz
		DH3 data packet	-40	0	40	kHz
		DH5 data packet	-40	0	40	kHz
		Drift Rate	-20	0	20	kHz/50µs
t_D - Tx	Transmitter Delay Time	From Tx data to antenna		4		µs

Note 21: Frequency accuracy is dependent on crystal oscillator chosen. The crystal must have a cumulative accuracy of < +/-20ppm to meet Bluetooth specifications.

8.3 PERFORMANCE DATA (typical)



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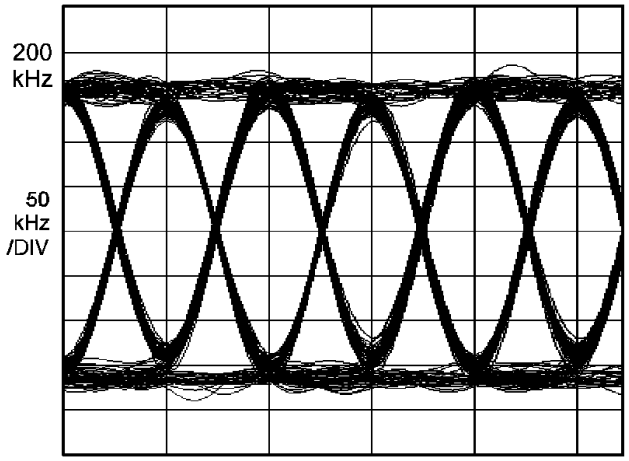
Modulation



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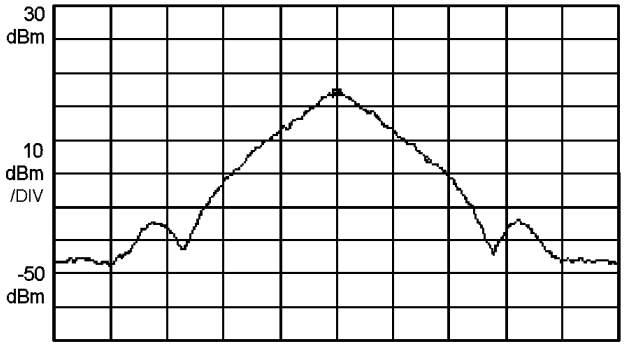
Corresponding Eye Diagram



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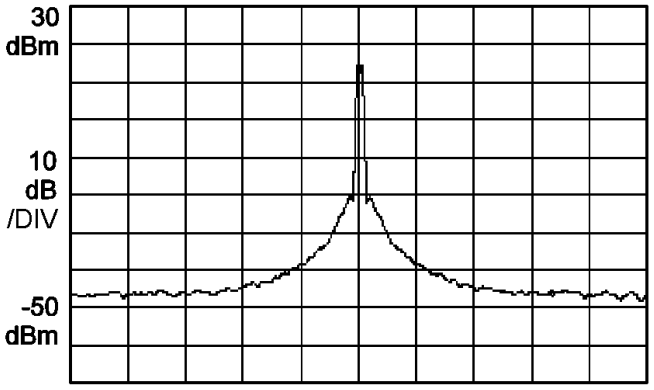
Transmit Spectrum



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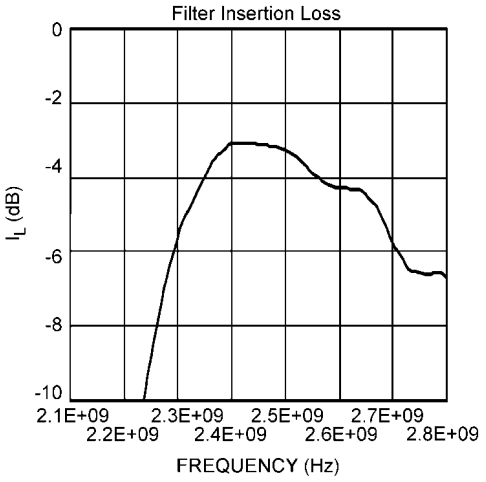
Synthesizer Phase Noise



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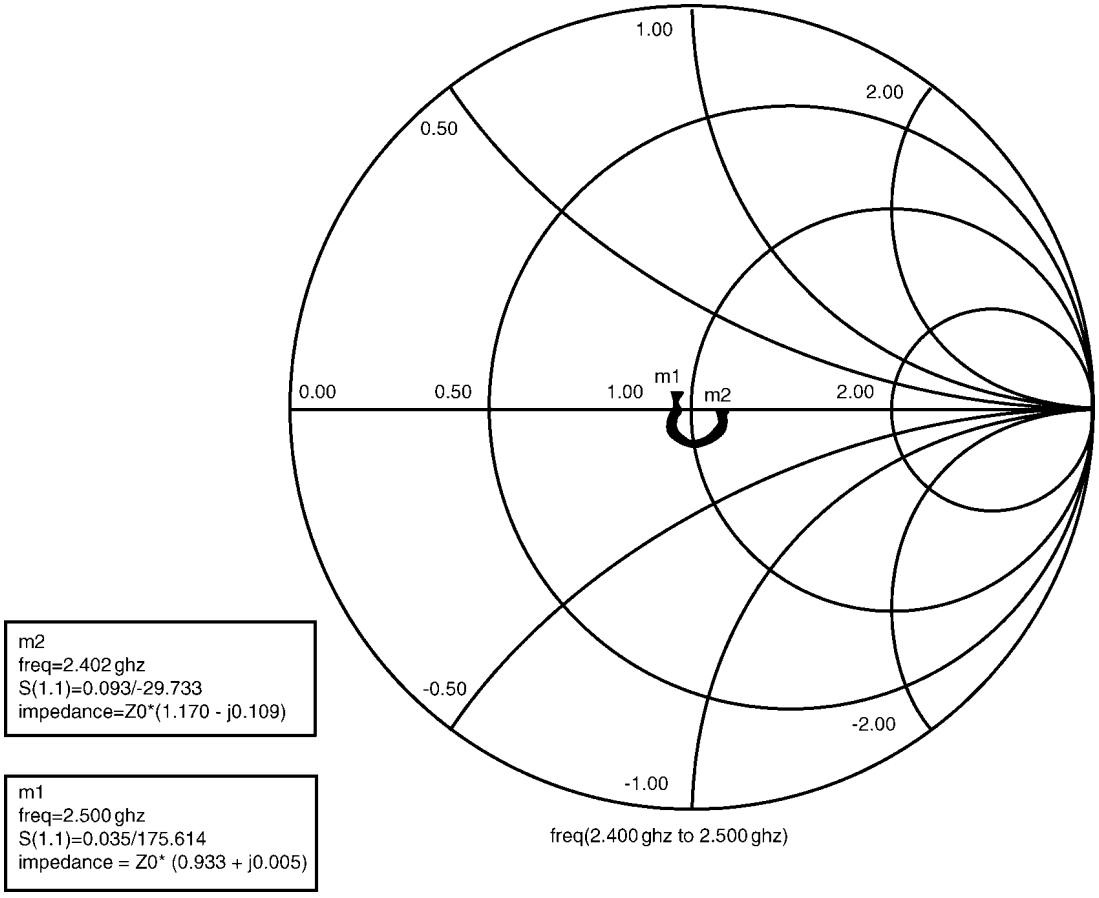
Front-End Bandpass Filter Response



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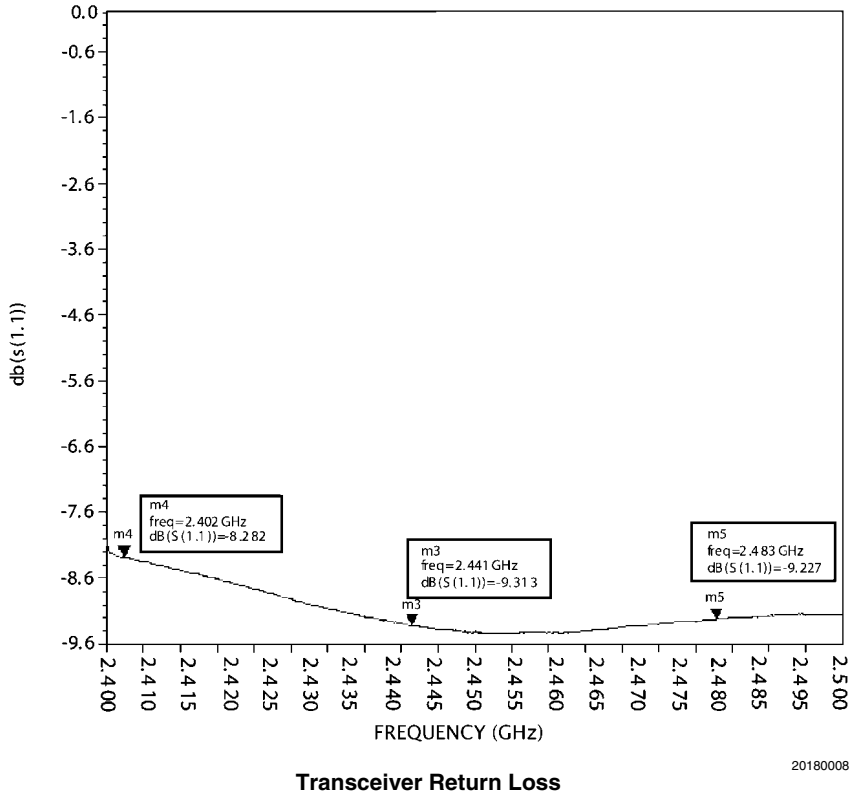
TX and RX Pin 50Ω Impedance Characteristics



Transceiver Return Loss

9.0 Functional Description

9.1 BASEBAND AND LINK MANAGEMENT PROCESSORS

Baseband and Lower Link control functions are implemented using a combination of National's CompactRISC 16-bit processor and the Bluetooth Lower Link Controller. These processors operate from integrated ROM memory and RAM and execute on-board firmware implementing all Bluetooth functions.

9.1.1 Bluetooth Lower Link Controller

The integrated Bluetooth Lower Link Controller (LLC) complies with the Bluetooth Specification version 2.0 and implements the following functions:

- Adaptive Frequency Hopping
- Interlaced Scanning
- Fast Connect
- Support for 1, 3, and 5 slot packet types
- 79 Channel hop frequency generation circuitry
- Fast frequency hopping at 1600 hops per second
- Power management control
- Access code correlation and slot timing recovery

9.1.2 Bluetooth Upper Layer Stack

The integrated upper layer stack is prequalified and includes the following protocol layers:

- L2CAP
- RFComm
- SDP

9.1.3 Profile support

The on-chip application of the LMX9830 allows full standalone operation, without any Bluetooth protocol layer necessary outside the module. It supports the Generic Access Profile (GAP), the Service Discovery Application Profile (SDAP), and the Serial Port Profile (SPP).

The on-chip profiles can be used as interfaces to additional profiles executed on the host. The LMX9830 includes a configurable service database to answer requests with the profiles supported.

9.1.4 Application with command interface

The module supports automatic slave operation eliminating the need for an external control unit. The implemented transparent option enables the chip to handle incoming data raw, without the need for packaging in a special format. The device uses a pin to block unallowed connections. This pincode can be fixed or dynamically set.

Acting as master, the application offers a simple but versatile command interface for standard Bluetooth operation like inquiry, service discovery, or serial port connection. The firmware supports up to seven slaves. Default Link Policy settings and a specific master mode allow optimized configuration for the application specific requirements. See also *Section 11.0 Integrated Firmware*.

9.1.5 Memory

The LMX9830 introduces 16 kB of combined system and Patch RAM memory that can be used for data and/or code upgrades of the ROM based firmware. Due to the flexible startup used for the LMX9830 operating parameters like the Bluetooth Device Address (BD_ADDR) are defined during boot time. This allows reading out the parameters of an external EEPROM or programming them directly over UART.

9.1.6 External memory interfaces

As the LMX9830 is a ROM based device with no on-chip non volatile storage, the operation parameters will be lost after a power cycle or hardware reset. In order to prevent re initializing such parameters, patches or even user data, the LMX9830 offers two interfaces to connect an external EEPROM to the device:

- µ-wire/SPI
- Access.bus (I²C compatible)

The selection of the interface is done during start up based on the option pins. See *Table 16* for the option pin descriptions.

9.1.7 µ-wire/SPI interface

In case the firmware is configured by the option pins to use a µ-wire/SPI EEPROM, the LMX9830 will activate that interface and try to read out data from the EEPROM. The external memory needs to be compatible to the reference listed in *Table 10*. The largest size EEPROM supported is limited by the addressing format of the selected NVM.

The device must have a page size equal to N x 32 bytes.

The firmware requires that the EEPROM supports Page write. Clock must be HIGH when idle.

TABLE 9. M95640-S EEPROM 8k x 8

Parameter	Value
Supplier	ST Microelectronics
Supply Voltage (Note 22)	1.8 - 3.6V
Interface	SPI compatible (positive clock SPI Modes)
Memory Size	8k x 8, 64 kbit
Clock Rate (Note 22)	2 MHz
Access	Byte and Page Write (up to 32 bytes)

Note 22: Parameter range reduced to requirements of National reference design.

9.1.8 Access.bus Interface

In case the firmware is configured by the option pins to use an access.bus or I²C compatible EEPROM, the LMX9830 will activate that interface and try to read out data from the EEPROM. The external memory needs to be compatible to the reference listed in *Table 10*.

The largest size EEPROM supported is limited by the addressing format of the selected NVM. The device must have a page size equal to N x 32 bytes.

The device uses a 16 bit address format. The device address must be “000”.

TABLE 10. 24C64 EEPROM 8kx8

Parameter	Value
Supplier	Atmel
Supply Voltage(Note 23)	2.7 - 5.5 V
Interface	2 wire serial interface
Memory Size	8K x 8, 64 kbit
Clock Rate (Note 23)	100 kHz
Access	32 Byte Page Write Mode

Note 23: Parameter range reduced to requirements of National reference design.

9.2 TRANSPORT PORT - UART

The LMX9830 provides one Universal Asynchronous Receiver Transmitter (UART). The UART interface consists out of Receive (RX), Transmit (TX), Ready-to-Send (RTS) and Clear-to-Send signals. RTS and CTS are used for hardware handshaking between the host and the LMX9830. Since the LMX9830 acts as gateway between the bluetooth and the UART interface, National recommends to use the handshaking signals especially for transparent operation. In case two signals are used CTS needs to be pulled to GND. Please refer also to “LMX9830 Software User’s Guide” for detailed information on 2-wire operation.

The UART interface supports formats of 8-bit data with or without parity, with one or two stop bits. It can operate at standard baud rates from 2400bits/s up to a maximum baud rate of 921.6 kbits/s. DMA transfers are supported to allow for fast processor independent receive and transmit operation.

The UART baudrate is configured during startup by checking option pins OP3, OP4 and OP5 for reference clock and baudrate. In case Auto baud rate detect is chosen, the firmware check the NVS area if a valid UART baudrate has been stored in a previous session. In case, no useful value can be found the device will switch to auto baud rate detection and wait for an incoming reference signal.

The UART offers wakeup from the power save modes via the multi-input wakeup module. When the LMX9830 is in low power mode, RTS# and CTS# can function as Host_WakeUp and Bluetooth_WakeUp respectively. *Table 11* represents the operational modes supported by the firmware for implementing the transport via the UART.

TABLE 11. UART Operation Modes

Item	Range	Default at Power-Up	With Auto-Detect
Baud Rate	2.4 to 921.6 kbits/s	Either configured by option pins, NVS parameter or auto baud rate detection	2.4 to 921.6 kbits/s
Flow Control	RTS#/CTS# or None	RTS#/CTS#	RTS#/CTS#
Parity	Odd, Even, None	None	None
Stop Bits	1,2	1	1
Data Bits	8	8	8

9.3 AUDIO PORT

9.3.1 Advanced Audio Interface

The Advanced Audio Interface (AAI) is an advanced version of the Synchronous Serial Interface (SSI) that provides a full-duplex communications port to a variety of industry-standard 13/14/15/16-bit linear or 8-bit log PCM codecs, DSPs, and other serial audio devices.

The interface allows the support one codec or interface. The firmware selects the desired audio path and interface configuration by a parameter that is located in RAM (imported from non-volatile storage or programmed during boot-up). The audio path options include the Motorola MC145483 codec, the OKI MSM7717 codec, the Winbond W681360/W681310 codecs and the PCM slave through the AAI.

In case an external codec or DSP is used the LMX9830 audio interface generates the necessary bit and frame clock driving the interface.

Table 12 summarizes the audio path selection and the configuration of the audio interface at the specific modes.

The LMX9830 supports one SCO link.

TABLE 12. Audio Path Configuration

Audio setting	Interface	Freq	Format	AAI Bit Clock	AAI Frame Clock	AAI Frame Sync Pulse Length
OKI MSM7717	Advanced audio interface	ANY (Note 24)	8-bit log PCM (a-law only)	480 kHz	8 kHz	14 Bits
Motorola MC145483 (Note 25)	Advanced audio interface		13-bit linear	480 kHz	8 kHz	13 Bits
OKI MSM7717	Advanced audio interface	13 MHz	8-bit log PCM (a-law only)	520 kHz	8 kHz	14 Bits
Motorola MC145483 (Note 26)	Advanced audio interface		13-bit linear	520 kHz	8 kHz	13 Bits
Winbond W681310	Advanced audio interface	13 MHz	8 bit log PCM A-law and µ-law	520 kHz	8 kHz	14 Bits
Winbond W681360	Advanced audio interface	13 MHz	13-bit linear	520 kHz	8 kHz	13 Bits
PCM slave (Note 27)	Advanced audio interface	ANY (Note 24)	8/16 bits	128 - 1024 kHz	8 kHz	8/16 Bits

Note 24: For supported frequencies see *Table 20*.

Note 25: Due to internal clock divider limitations the optimum of 512 kHz, 8 kHz can not be reached. The values are set to the best possible values. The clock mismatch does not result in any discernible loss in audio quality.

Note 26: Due to internal clock divider limitations the optimum of 512 kHz, 8 kHz can not be reached. The values are set to the best possible values. The clock mismatch does not result in any discernible loss in audio quality.

Note 27: In PCM slave mode, parameters are stored in NVS. Bit clock and frame clock must be generated by the host interface.

PCM slave configuration example: PCM slave uses the slot 0, 1 slot per frame, 16 bit linear mode, long frame sync, normal frame sync. In this case, 0x03E0 should be stored in NVS. See “LMX9830 Software Users Guide” for more details.

9.4 AUXILIARY PORTS

9.4.1 RESET#

There are two reset inputs: RESET_RA# for the radio and RESET_BB# for the baseband. Both are active low.

There is also a reset output, B_RESET_RA# (Buffered Radio Reset) active low. This output follows input RESET_RA#.

When RESET_RA# is released, going high, B_RESET_RA# stays low until the clock has started.

Please see *Section 9.5 SYSTEM POWER UP* for details.

9.4.2 General Purpose I/Os

The LMX9830 offers 3 pins which either can be used as indication and configuration pins or can be used for General Purpose functionality. The selection is made out of settings derived out of the power up sequence.

In General Purpose configuration the pins are controlled hardware specific commands giving the ability to set the direction, set them to high or low or enable a weak pull-up.

In alternate function the pins have pre-defined indication functionality. Please see *Table 13* for a description on the alternate indication functionality.

TABLE 13. Alternate GPIO Pin Configuration

Pin	Description
OP4/PG4	Operation Mode pin to configure Transport Layer settings during boot-up
PG6	GPIO
PG7	RF Traffic indication

9.5 SYSTEM POWER UP

In order to correctly power-up the LMX9830 the following sequence is recommended to be performed:

Apply VCC_IO and V_{CC} to the LMX9830.

The RESET_RA# should be driven high. Then RESET_BB# should be driven high at a recommended time of 1ms after the LMX9830 voltage rails are high. The LMX9830 is properly reset.

Please see timing diagram, *Figure 1*.

ESR of the crystal also has impact on the startup time of the crystal oscillator circuit of the LMX9830 (See *Table 14* and *Table 15*).

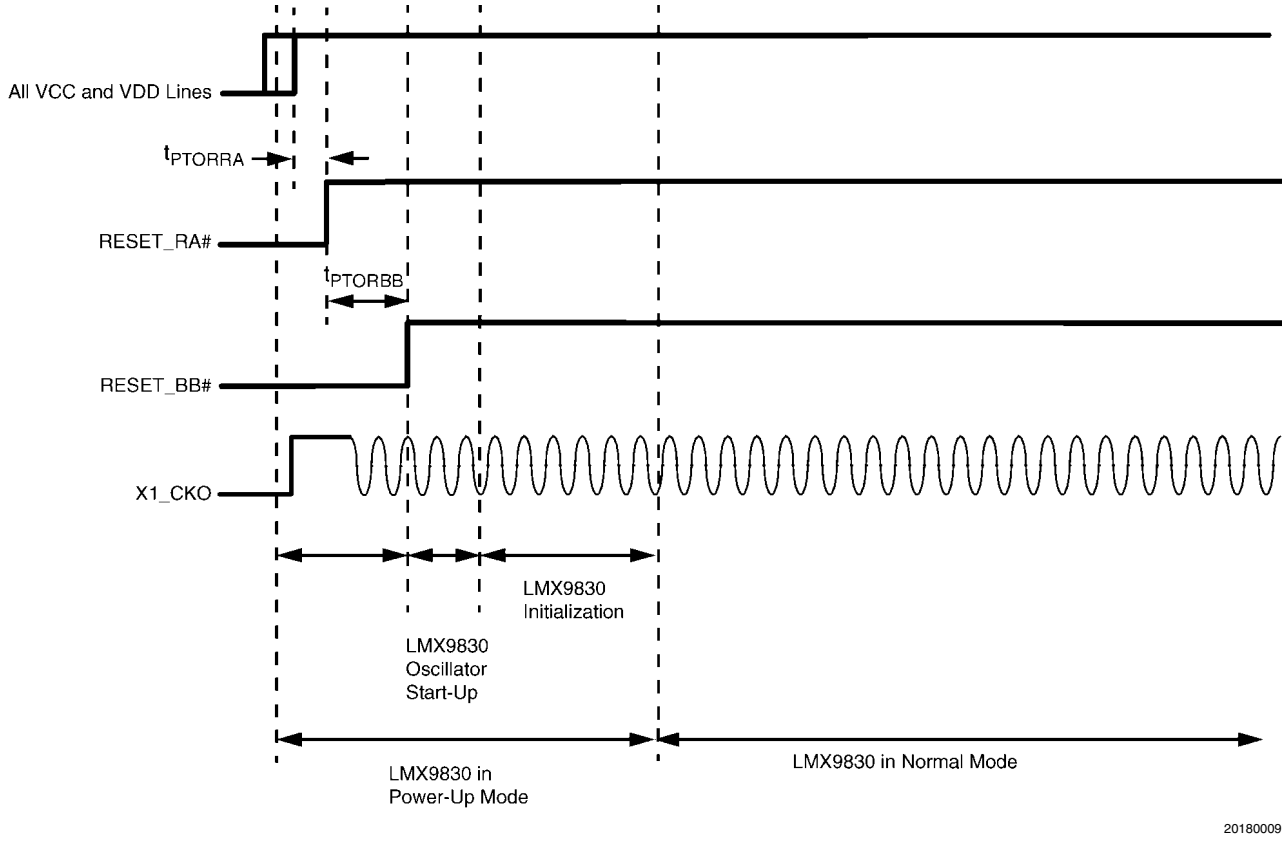


FIGURE 1. LMX9830 Power on Reset Timing

TABLE 14. LMX9830 Power to Reset timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{PTORRA}	Power to Reset _RA#	V_{CC} and VCC_IO at operating voltage level to valid reset	<500 (Note 28)			µs
t_{PTORBB}	Reset_RA# to Reset_BB#	V_{CC} and VCC_IO at operating voltage level to valid reset	1 (Note 29)			ms

Note 28: Rise time on power must switch on fast, rise time <500us.

Note 29: Recommended value.

TABLE 15. ESR vs. Startup Time

ESR (Ω)	**Typical** (Note 30), (Note 31)	Unit
10	12	ms
25	13	ms
40	16	ms
50	24	ms
80	30	ms

Note 30: Frequency, loading caps and ESR all must be considered for determining startup time.

Note 31: For reference only, must be tested on each system to accurately design POR and correctly startup system.

9.6 STARTUP SEQUENCE

During startup the LMX9830 checks the options register pins OP3 to OP7 for configuration on operation mode, external clock source, transport layer and available non volatile storage PROM.

The different options for startup are described in *Table 16*.

9.6.1 Options Register

External pads in *Table 16* are latched in this register at the end of Reset. The Options register can be read by firmware at any time.

All pads are inputs with weak on-chip pull-up/down resistors during Reset. Resistors are disconnected at the end of RESET_BB#.

1 = Pull-up resistor connected in application

0 = Pull-down resistor connected in application

x = Don't care

9.6.2 Startup With External PROM Available

To be able to read out information from an external PROM the option pins have to be set according to *Table 16*.

Startup sequence activities:

1. From the Options registers OP6 and OP7, the LMX9830 checks if a serial PROM is available to use (ACCESS.bus or Microwire).
2. If serial PROM is available, the permanent parameter block, patch block, and non-volatile storage (NVS) are read from it. If the BD Address is not present, enter the BD address to be saved in the NVS. For more information see *Section 9.6.4 Configuring the LMX9830 Through Transport Layer*.
3. From the Options register OP3, OP4 and OP5, the LMX9830 checks for clocking information and transport layer settings. If the NVS information are not sufficient, the LMX9830 will send the "Await Initialization" event on the TL (Transport Layer) and wait for additional information (see *Section 9.6.3 Startup Without External PROM Available*.)
4. The LMX9830 compensates the UART for new BBCLK information from the NVS.
5. The LMX9830 starts up the Bluetooth core.

9.6.3 Startup Without External PROM Available

The following sequence will take place if OP6 and OP7 have been set to "No external memory" as described in *Table 16*.

Startup sequence activities:

1. From the Options registers OP6 and OP7, the LMX9830 checks if a serial PROM is available to use.
2. From the Options register OP3, OP4 and OP5, the LMX9830 checks for clocking mode and transport layer.
3. The LMX9830 sends the "Await Initialization" Event on the TL (Transport Layer) and waits for NVS configuration commands. The configuration is finalized by sending the "Enter Bluetooth Mode" command.
4. The LMX9830 compensates the UART for new BBCLK information from the NVS.
5. The LMX9830 starts up the Bluetooth core.

TABLE 16. Startup Sequence Options (Note 32)

Package Pad						**Comment**
OP3	**OP4**	**OP5**	**OP6** (Note 33)	**OP7** (Note 34)	**ENV1#**	
PD	PD	PD	PD	PD	PU	PD = Internal Pull-down during Reset PU = Internal Pull-up during Reset
x	x	x	Open (0)	Open (0)	Open (1) BBCLK	No serial memory
x	x	x	1	Open (0)	Open (1) BBCLK	Reserved
x	x	x	Open (0)	1	Open (1) BBCLK	Microwire serial memory
x	x	x	1	1	Open (1) BBCLK	ACCESS.bus serial memory
T_SCLK	x	x	T_RFDATA	T_RFCE	0 BBCLK	Test mode

Note 32: 1/0 pull-up/down resistor connected in application.

Note 33: If OP6 is 1, must use 1k Ω pull up, If OP6 is 0, must use 10k Ω pull down.

Note 34: If OP7 is 1, must use 1k Ω pull up.

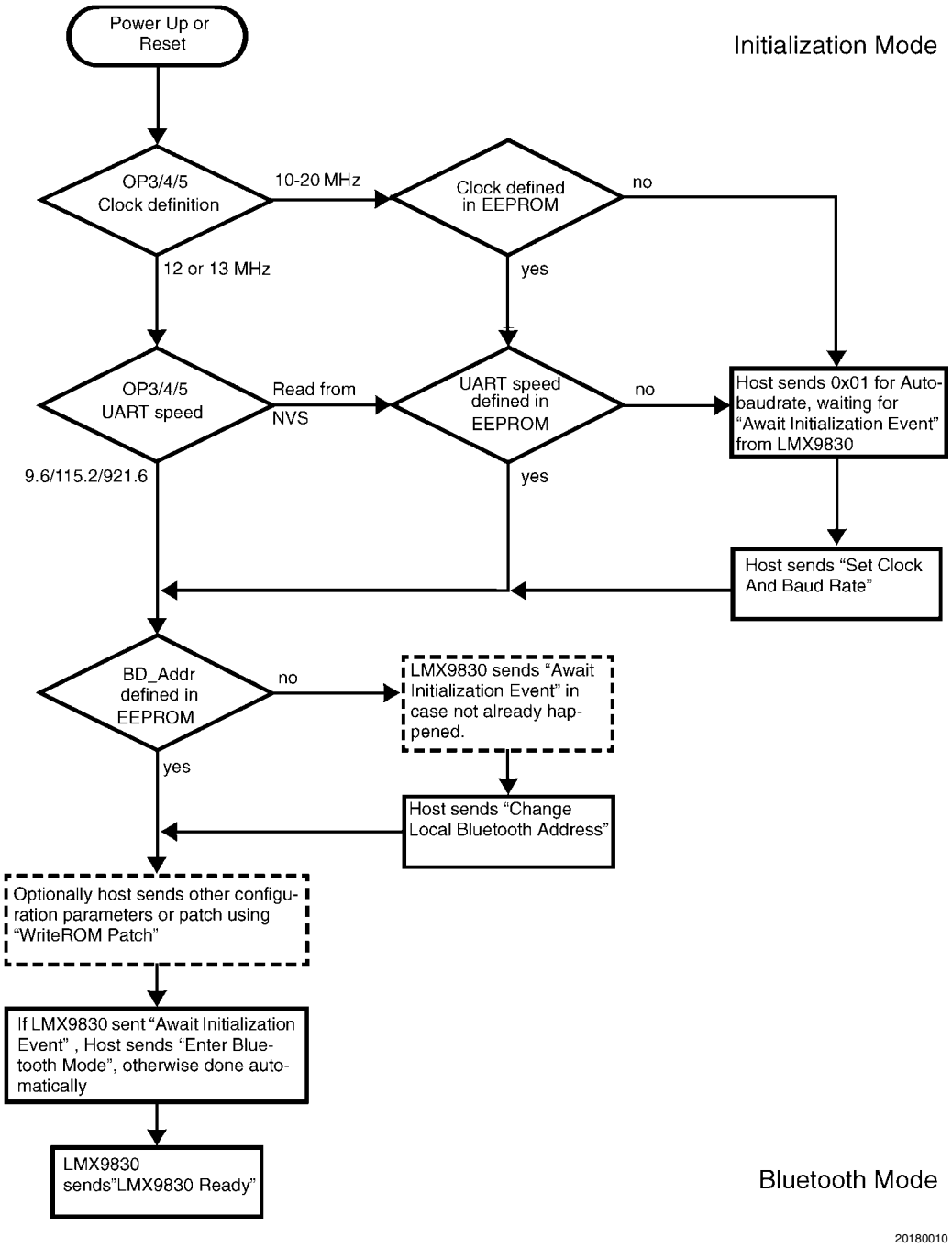


FIGURE 2. Flow Diagram for the Start-up Sequence

TABLE 17. Fixed Frequencies

Osc Freq. (MHz)	BBCLK (MHz)	PLL (48 MHz)	**OP3** (Note 35)	**OP4** (Note 36)	**OP5** (Note 37)	Function
12	12	OFF	0	0	0	UART speed read from NVS
10-20 (Note 38)	10-20 (Note 35)	ON	0	1	0	Clock and UART baudrate detection
13	13	OFF	1	0	0	UART speed read from NVS
13	13	OFF	1	0	1	UART speed 9.6 kbps
13	13	OFF	1	1	0	UART speed 115.2 kbps
13	13	OFF	1	1	1	UART speed 921.6 kbps

Note 35: If OP3 is 1, must use 1k Ω pull up.

Note 36: If OP4 is 1, must use 1k Ω pull up.

Note 37: If OP5 is 1, must use 1k Ω pull up.

Note 38: Supported frequencies see *Table 21*.

9.6.4 Configuring the LMX9830 Through Transport Layer

As described in *Section 9.5 SYSTEM POWER UP*, the LMX9830 will check during startup the Options Registers if an external PROM is available. If the information on the PROM are incomplete or no PROM is installed the LMX9830 will boot into the “initialization Mode”.

The mode is confirmed by the “Await Initialization” Event.

The following information are needed to enter Bluetooth Mode:

- Bluetooth Device Address (BD_Addr)
- External clock source (only if 10 - 20 MHz has been selected)
- UART Baudrate (only if Auto baudrate detection has been selected)

In general the following procedure will initialize the LMX9830:

1. Wait for “Await initialization” Event
   — Event will only appear if transport layer speed is set or after successful baudrate detection.
2. Send “Set Clock and Baudrate” Command only if the clock speed is not known through hardware configuration **(i.e only if OP3, OP4, OP5 = 0 1 0)**.
3. Send “Write BD_Addr” to Configure Local Bluetooth Device Address.
4. Send “Enter Bluetooth Mode”
   — LMX9830 will use configured clock and UART speed and start the command interface.

Note: In case no EEPROM is used, BDAddr, clock source and Baudrate are only valid until the next power-cycle or hardware reset.

9.6.5 Auto Baud Rate Detection

The LMX9830 supports an Automatic Baudrate Detection in case the external clock is different to 12, 13MHz or the range 10-20 MHz or the baudrate is different to 9.6 kbps, 115.2 or 921.6 kbit/s.

The baudrate detection is based on the measurement of a single character. The following issues need to be considered:

- The flow control pin CTS must be low or else the host is in flow stop.
- The Auto Baudrate Detector measures the length of the 0x01 character from the positive edge of bit 0 to the positive edge of stop bit.
- Therefore the very first received character must always be a 0x01.
- The host can restrict itself to send only a 0x01 character or also can send a command.
- The host must flush the TX buffer within 50-100 milliseconds depend on clock frequency on the host controller.
- After 50-100 milliseconds the UART is about to be initialized and short after the host should receive a “Await Initialization” Event or an “Command Status” Event.

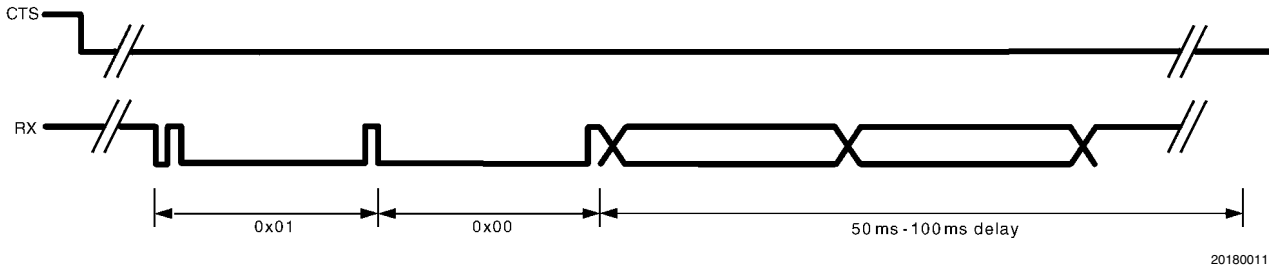


FIGURE 3. Auto Baudrate Detection Timing Diagram

9.7 USING AN EXTERNAL EEPROM FOR NON-VOLATILE DATA

The LMX9830 offers two interfaces to connect to external memory. Depending on the EEPROM used, the interface is activated by setting the correct option pins during start up. See *Table 16* for the option pin settings.

The external memory is used to store mandatory parameters like the BD_Address as well as many optional parameters like Link Keys or even User data.

The NVM is organized with fixed addresses for the parameters. Because of that the EEPROM can be preprogrammed with default parameters in manufacturing. Refer to "Operation Parameters Stored in LMX9830" for the organization of the NVS map.

In case the external memory is empty on first startup the LMX9830 will behave as like no memory is connected. (See *Section 9.6.3 Startup Without External PROM Available*). During the startup process parameters can be written directly to the EEPROM to be available after next bootup. On first bootup, the EEPROM will be automatically programmed to default values, including the UART speed of 9600 BPS. Patches supplied over the TL will be stored automatically into the EEPROM.

10.0 Digital Smart Radio

10.1 FUNCTIONAL DESCRIPTION

The integrated Digital Smart Radio utilizes a heterodyne receiver architecture with a low intermediate frequency (2 MHz) such that the intermediate frequency filters can be integrated on chip. The receiver consists of a low-noise amplifier (LNA) followed by two mixers. The intermediate frequency signal processing blocks consist of a poly-phase bandpass filter (BPF), two hard-limiters (LIM), a frequency discriminator (DET), and a post-detection filter (PDF). The received signal level is detected by a received signal strength indicator (RSSI).

The received frequency equals the local oscillator frequency (fLO) plus the intermediate frequency (fIF):

fRF = fLO + fIF (supradyne).

The radio includes a synthesizer consisting of a phase detector, a charge pump, an (off-chip) loop-filter, an RF-frequency divider, and a voltage controlled oscillator (VCO).

The transmitter utilizes IQ-modulation with bit-stream data that is gaussian filtered. Other blocks included in the transmitter are a VCO buffer and a power amplifier (PA).

10.2 RECEIVER FRONT-END

The receiver front-end consists of a low-noise amplifier (LNA) followed by two mixers and two low-pass filters for the I- and Q-channels.

The intermediate frequency (IF) part of the receiver front-end consists of two IF amplifiers that receive input signals from the mixers, delivering balanced I- and Q-signals to the poly-phase bandpass filter. The poly-phase bandpass filter is directly followed by two hard-limiters that together generate an AD-converted RSSI signal.

10.2.1 Poly-Phase Bandpass Filter

The purpose of the IF bandpass filter is to reject noise and spurious (mainly adjacent channel) interference that would otherwise enter the hard limiting stage. In addition, it takes care of the image rejection.

The bandpass filter uses both the I- and Q-signals from the mixers. The out-of-band suppression should be higher than 40 dB (f<1 MHz, f>3 MHz). The bandpass filter is tuned over process spread and temperature variations by the autotuner circuitry. A 5th order Butterworth filter is used.

10.2.2 Hard-Limiter and RSSI

The I- and Q-outputs of the bandpass filter are each followed by a hard-limiter. The hard-limiter has its own reference current. The RSSI (Received Signal Strength Indicator) measures the level of the RF input signal.

The RSSI is generated by piece-wise linear approximation of the level of the RF signal. The RSSI has a mV/dB scale, and an analog-to-digital converter for processing by the baseband circuit. The input RF power is converted to a 5-bit value. The RSSI value is then proportional to the input power (in dBm).

The digital output from the ADC is sampled on the BPKTCTL signal low-to-high transition.

10.3 RECEIVER BACK-END

The hard-limiters are followed by a two frequency discriminators. The I-frequency discriminator uses the 90× phase-shifted signal from the Q-path, while the Q-discriminator uses the 90× phase-shifted signal from the I-path. A poly-phase bandpass filter performs the required phase shifting. The output signals of the I- and Q-discriminator are substracted and filtered by a low-pass filter. An equalizer is added to improve the eye-pattern for 101010 patterns.

After equalization, a dynamic AFC (automatic frequency offset compensation) circuit and slicer extract the RX_DATA from the analog data pattern. It is expected that the Eb/No of the demodulator is approximately 17 dB.

10.3.1 Frequency Discriminator

The frequency discriminator gets its input signals from the limiter. A defined signal level (independent of the power supply voltage) is needed to obtain the input signal. Both inputs of the frequency discriminator have limiting circuits to optimize performance. The bandpass filter in the frequency discriminator is tuned by the autotuning circuitry.

10.3.2 Post-Detection Filter and Equalizer

The output signals of the FM discriminator first go through a post-detection filter and then through an equalizer. Both the post-detection filter and equalizer are tuned to the proper frequency by the autotuning circuitry. The post-detection filter is a low-pass filter intended to suppress all remaining spurious signals, such as the second harmonic (4 MHz) from the FM detector and noise generated after the limiter.

The post-detection filter also helps for attenuating the first adjacent channel signal. The equalizer improves the eye-opening for 101010 patterns. The post-detection filter is a third order Butterworth filter.

10.4 AUTOTUNING CIRCUITRY

The autotuning circuitry is used for tuning the bandpass filter, the detector, the post-detection filter, the equalizer, and the transmit filters for process and temperature variations. The circuit also includes an offset compensation for the FM detector.

10.5 SYNTHESIZER

The synthesizer consists of a phase-frequency detector, a charge pump, a low-pass loop filter, a programmable frequency divider, a voltage-controlled oscillator (VCO), a delta-sigma modulator, and a lookup table.

The frequency divider consists of a divide-by-2 circuit (divides the 5 GHz signal from the VCO down to 2.5 GHz), a divide-by-8-or-9 divider, and a digital modulus control. The delta-sigma modulator controls the division ratio and also generates an input channel value to the lookup table.

10.5.1 Phase-Frequency Detector

The phase-frequency detector is a 5-state phase-detector. It responds only to transitions, hence phase-error is independent of input waveform duty cycle or amplitude variations. Loop lockup occurs when all the negative transitions on the inputs, F_REF and F_MOD, coincide. Both outputs (i.e., Up and Down) then remain high. This is equal to the zero error mode. The phase-frequency detector input frequency range operates at 12MHz.

10.6 TRANSMITTER CIRCUITRY

The transmitter consists of ROM tables, two Digital to Analog (DA) converters, two low-pass filters, IQ mixers, and a power amplifier (PA).

The ROM tables generate a digital IQ signal based on the transmit data. The output of the ROM tables is inserted into IQ-DA converters and filtered through two low-pass filters. The two signal components are mixed up to 2.5 GHz by the TX mixers and added together before being inserted into the transmit PA.

10.6.1 IQ-DA Converters and TX Mixers

The ROM output signals drive an I- and a Q-DA converter. Two Butterworth low-pass filters filter the DA output signals. The 6 MHz clock for the DA converters and the logic circuitry around the ROM tables are derived from the autotuner.

The TX mixers mix the balanced I- and Q-signals up to 2.4-2.5 GHz. The output signals of the I- and Q-mixers are summed.

10.7 CRYSTAL REQUIREMENTS

The LMX9830 contains a crystal driver circuit. This circuit operates with an external crystal and capacitors to form an oscillator. shows the recommended crystal circuit. *Table 21* specifies system clock requirements.

The RF local oscillator and internal digital clocks for the LMX9830 is derived from the reference clock at the CLK+ input. This reference may either come from an external clock or a dedicated crystal oscillator. The crystal oscillator connections require an Xtal and two grounded capacitors.

It is also important to consider board and design dependant capacitance in tuning crystal circuit. Equations that follow allow a close approximation of crystal tuning capacitance required, but actual values on board will vary with capacitive properties of the board. As a result, there is some fine tuning of crystal circuit that has to be done that can not be calculated, must be tuned by testing different values of load capacitance.

Many different crystals can be used with the LMX9830. Key requirements from Bluetooth specification is + 20ppm. Additionally, ESR (Equivalent Series Resistance) must be carefully considered. LMX9830 can support maximum of 230 Ω ESR, but it is recommended to stay <100 Ω ESR for best performance over voltage and temperature. Reference *Figure 9* for ESR as part of crystal circuit for more information.

10.7.1 Crystal

The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors. The resonant frequency may be trimmed with the crystal load capacitance.

1. Load Capacitance
   For resonance at the correct frequency, the crystal should be loaded with its specified load capacitance, which is the value of capacitance used in conjunction with the crystal unit. Load capacitance is a parameter specified by the crystal, typically expressed in pF. The crystal circuit shown in *Figure 5* is composed of:
   — C1 (motional capacitance)
   — R1 (motional resistance)
   — L1 (motional inductance)
   — C0 (static or shunt capacitance)
   The LMX9830 provides some of the load with internal capacitors Cint. The remainder must come from the external capacitors and tuning capacitors labeled Ct1 and Ct2 as shown in *Figure 4*. Ct1 and Ct2 should have the same the value for best noise performance.
   The LMX9830 has an additional internal capacitance CTUNE of 2.6pF. Crystal load capacitance (C_L) is calculated as the following:

   $$C_L = C_{int} + C_{TUNE} + Ct1//Ct2$$

   The C_L above does not include the crystal internal self-capacitance C_0 as shown in *Figure 5*, so the total capacitance is:

   $$C_{total} = C_L + C_0$$

   Based on crystal spec and equation:

   $$C_L = C_{int} + C_{TUNE} + Ct1//Ct2$$
   $$C_L = 8pF + 2.6pF + 6pF = 16.6pF$$

   16.6pF is very close to the TEW crystal requirement of 16pF load capacitance. With the internal shunt capacitance Ctotal:

   $$Ctotal = 16.6pF + 5pF = 21.6pF$$

2. Crystal Pullability
   Pullability is another important parameter for a crystal, which is the change in frequency of a crystal with units of ppm/pF, either from the natural resonant frequency to a load resonant frequency, or from one load resonant frequency to another. The frequency can be pulled in a parallel resonant circuit by changing the value of load capacitance. A decrease in load capacitance causes an increase in frequency, and an increase in load capacitance causes a decrease in frequency.

3. Frequency Tuning
   Frequency Tuning is achieved by adjusting the crystal load capacitance with external capacitors. It is a Bluetooth requirement that the frequency is always within ±20 ppm. Crystal/oscillator must have cumulative accuracy specifications of **±15 ppm** to provide margin for frequency drift with aging and temperature.
   TEW Crystal
   The LMX9830 has been tested with the TEW TAS-4025A crystal, reference *Table 18* for specification. Since the internal capacitance of the crystal circuit is 8 pF and the load capacitance is 16 pF, 12 pF is a good starting point for both Ct1 and Ct2. The 2480 MHz RF frequency offset is then tested. *Figure 6*shows the RF frequency offset test results.
   Figure 6 shows the results are -20 kHz off the center frequency, which is –1 ppm. The pullability of the crystal is 2 ppm/pF, so the load capacitance must be decreased by about 1.0 pF. By changing Ct1 or Ct2 to 10 pF, the total load capacitance is decreased by 1.0 pF. *Figure 7* shows the frequency offset test results. The frequency offset is now zero with Ct1 = 10 pF, Ct2 = 10 pF. Reference *Table 19* for crystal tuning values used on Mesa Development Board with TEW crystal.

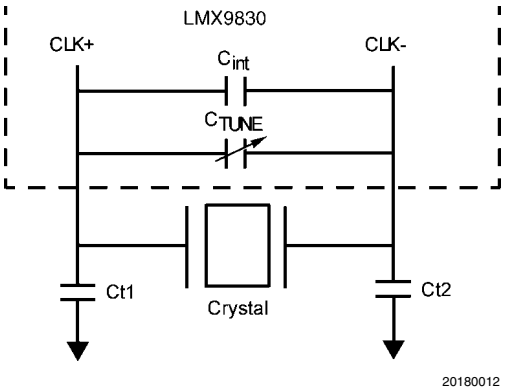


FIGURE 4. LMX9830 Crystal Recommended Circuit

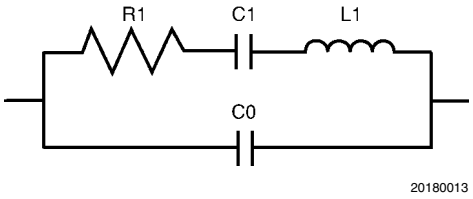


FIGURE 5. Crystal Equivalent Circuit

TABLE 18. TEW TAS-4025A

Specification	Value
Package	4.0x2.5x0.65 mm - 4 pads
Frequency	13.000 MHz
Mode	Fundamental
Stability	> ±15 ppm @ -40 to +85°C
C_L Load Capacitance	16pF
ESR	80 Ω max.
C_0 Shunt Capacitance	5pF
Drive Level	50 ±10 µV
Pullability	2 ppm/pF min
Storage Temperature	-40 to +85°C

TABLE 19. TEW on LMX9830 DONGLE

Reference	LMX9830
Ct1	12 pF
Ct2	12 pF

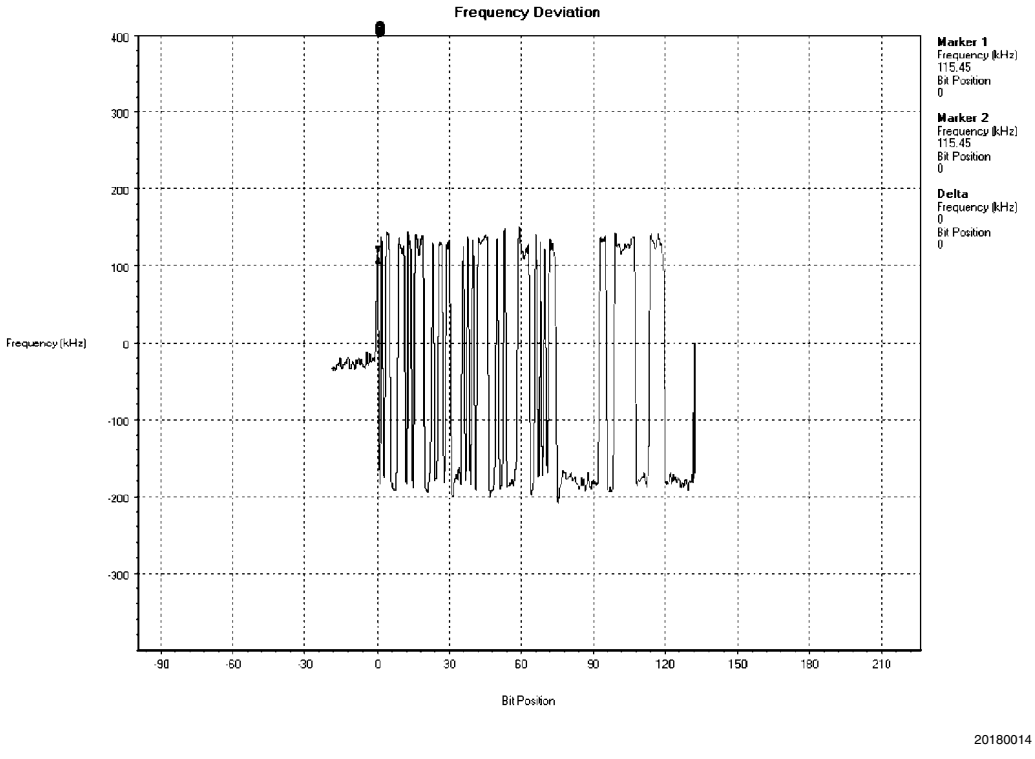


FIGURE 6. Frequency Offset with 12 pF//12 pF Capacitors

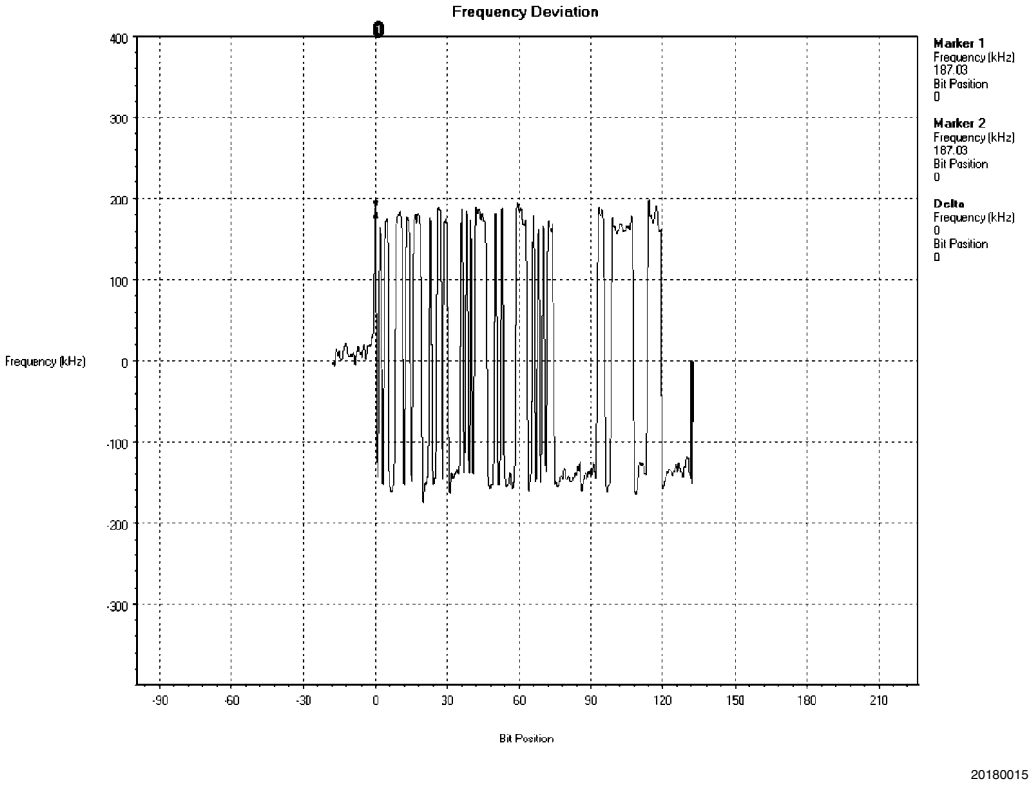


FIGURE 7. Frequency Offset with 10 pF//10 pF Capacitors

10.7.2 TCXO (Temperature Compensated Crystal Oscillator)

The LMX9830 also can operate with an external TCXO (Temperature Compensated Crystal Oscillator). The TCXO signal is directly connected to the CLK+.

1. Input Impedance
   The LMX9830 CLK+ pin has in input impedance of 2pF capacitance in parallel with >400kW resistance

10.7.3 Optional 32 kHz Oscillator

A second oscillator is provided (see *Figure 8*) that is tuned to provide optimum performance and low-power consumption while operating with a 32.768 kHz crystal. An external crystal clock network is required between the X2_CKI clock input and the X2_CKO clock output signals.The oscillator is built in a Pierce configuration and uses two external capacitors. *Table 20* provides the oscillator's specifications.

In case the 32kHz is not used, it is recommended to leave X2_CKO open and connect X2_CKI to GND.

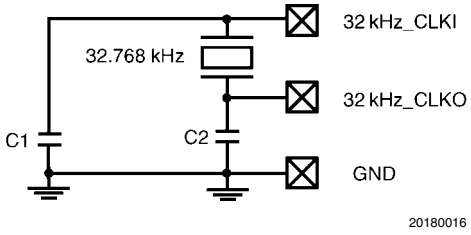


FIGURE 8. 32.768 kHz Oscillator

TABLE 20. 32.768 kHz Oscillator Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Supply Voltage		1.62	1.8	1.98	V
I_{DDACT}	Supply Current (Active)			2		µA
f	Nominal Output Frequency			32.768		kHz
V_{PPOSC}	Oscillating Amplitude			1.8		V
	Duty Cycle		40		60	%

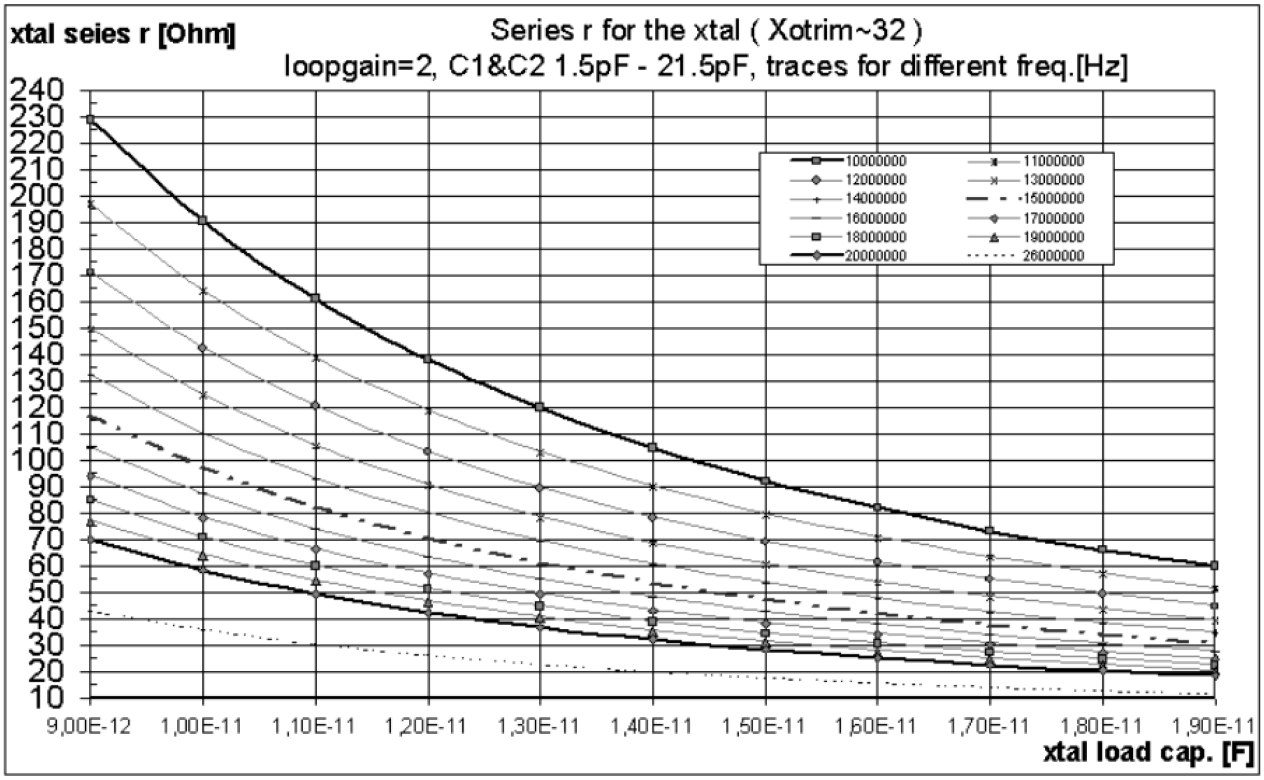
10.7.4 ESR (Equivalent Series Resistance)

LMX9830 can operate with a wide range of crystals with different ESR ratings. Reference *Table 21* and *Figure 9* for more details.

TABLE 21. System Clock Requirements

Parameter	Min	Typ	Max	Unit
External Reference Clock Frequency (Note 39)	10	13	20	MHz
Frequency Tolerance (over full operating temperature and aging)	-20	±15	+20	ppm
Crystal Serial Resistance			230	Ω
External Reference Clock Power Swing, pk to pk	100	200	400	mV
Aging			±1	ppm per year

Note 39: Supported frequencies from external oscillator (in MHz): 10.00, 10.368, 12.00, 12.60, 12.80, 13.00, 13.824, 14.40, 15.36, 16.00, 16.20, 16.80, 19.20, 19.68, 19.80

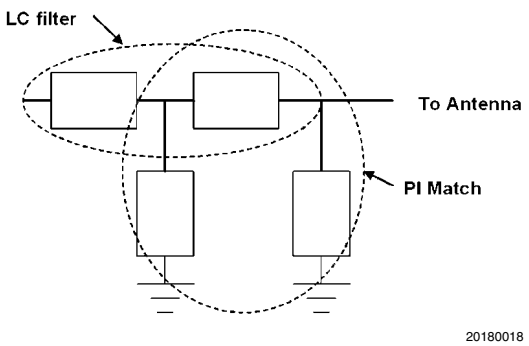


20180017

FIGURE 9. ESR vs. Load Capacitance for the Crystal Circuit

10.8 ANTENNA MATCHING AND FRONT-END FILTERING

Figure 10 shows the recommended component layout to be used between RF output and antenna input. Allows for versatility in the design such that the match to the antenna maybe improved and/or the blocking margin increased by addition of a LC filter. Refer to antenna application note for further details.



20180018

FIGURE 10. Front End Layout

10.9 LOOP FILTER DESIGN

The LMX9830 has an external loop filter which must be designed for best performance by the end customer. This section therefore gives some foresight into its design. Refer also to Loop Filter application note and National's Webench online design tool for more information.

10.9.1 Component Calculations

The following parameters are required for component value calculation of a third order passive loop filter.

Φ	Phase Margin: Phase of the open loop transfer function
F_c	Loop Bandwidth
F_{comp}	Comparison Frequency: Phase detector frequency
KVOC	VCO gain: Sensitivity of the VCO to control volts
KΦ	Charge Pump gain: Magnitude of the alternating current during lock
F_{OUT}	Maximum RF output frequency
T31	Ratio of the poles T3 to T1 in a 3rd order filter
γ	Gamma optimization parameter

The third order loop filter being defined has the following topology. shown in *Figure 11*.

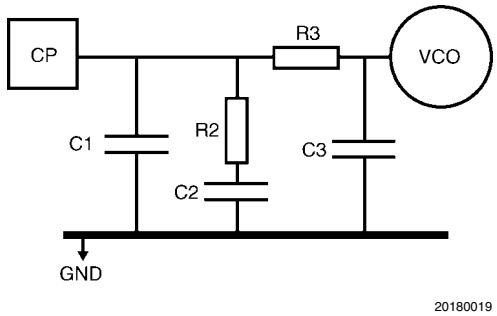


FIGURE 11. Third Order Loop Filter

$$N = \frac{F_{out}}{F_{comp}} \quad \text{and} \quad \omega_C = 2\pi F_C$$

20180041

Calculate the poles and zeros. Use exact method to solve for T1 using numerical methods,

$$\phi = \tan^{-1}\left(\frac{\gamma}{\omega_C \bullet T1 \bullet T1 + T31}\right) - \tan^{-1}(\omega_C \bullet T1) - \tan^{-1}(\omega_C \bullet T1 \bullet T31)$$

20180042

$$T3 = T31 \times T1 \qquad T2 = \frac{\gamma}{\omega_C^2 \bullet (T1 + T3)}$$

20180043

Calculate the loop filter coefficients,

$$A0 = \frac{K\phi \bullet K_{VCO}}{\omega_C^2 \bullet N} \bullet \sqrt{\frac{1 + \omega_C^2 \bullet T2^2}{(1 + \omega_C^2 \bullet T1^2)(1 + \omega_C^2 \bullet T3^2)}}$$

$$A1 = A0 \bullet (T1 + T3) \qquad A2 = A0 \bullet T1 \bullet T3$$

20180044

Summary:

Symbol	Description	Units
n	N counter value	None
	Loop Bandwidth	rad/s
T1	Loop filter pole	S
T2	Loop filter zero	S
T3	Loop filter zero	S
A0	Total capacitance	nF
A1	First order loop filter coefficient	nFs
A2	Second order loop filter coefficient	nFs2

Components can then be calculated from loop filter coefficients

$$C1 = \frac{A2}{T2^2} \bullet \left(1 + \sqrt{1 + \left(\frac{T2 \bullet A0 - T2 \bullet A1}{A2}\right)}\right)$$

20180045

$$C3 = \frac{1 \bullet T2^2 \bullet C1^2 + T2 \bullet A1 \bullet C1 - A2 \bullet A0}{T2^2 \bullet C1 - A2} \qquad C2 = A0 - C1 - C3$$

20180046

$$R2 = \frac{T2}{C2} \qquad R3 = \frac{A2}{C1 \bullet C3 \bullet T2}$$

20180047

Some typical values for the LMX9830 are:

Comparison Frequency	13	MHz
Phase Margin	48	Pl rad
Loop bandwidth	100	kHz
T3 over T1 ratio	40	%
Gamma	1.0	
VCO gain	120	MHz per V
Charge pump gain	0.6	mA
Fout	2441	MHz

Which give the following component values:

C1	0.17	nF
C2	2.38	nF
C3	0.04	nF
R2	1737	Ω
R3	7025	Ω

10.9.2 Phase Noise and Lock-Time Calculations

Phase noise has three sources, the VCO, crystal oscillator and the rest of the PLL consisting of the phase detector, dividers, charge pump and loop filter. Assuming the VCO and crystal are very low noise, it is possible to put down approximate equations that govern the phase noise of the PLL.

Phase noise (in-band) = PN1Hz + 20Log[N] + 10Log[F_{comp}]

Where PH1Hz is the PLL normalized noise floor in 1 Hz resolution bandwidth.

Further out from the carrier, the phase noise will be affected by the loop filter roll-off and hence its bandwidth.

As a rule-of-thumb; ΔPhase noise = 40Log[ΔFc]

Where Fc is the relative change in loop BW expressed as a fraction.

For example if the loop bandwidth is reduced from 100 kHz to 50 kHz or by one half, then the change in phase noise will be -12dB. Loop BW in reality should be selected to meet the

lower limit of the modulation deviation, this will yield the best possible phase noise.

Even further out from the carrier, the phase noise will be mainly dominated by the VCO noise assuming the crystal is relatively clean.

Lock-time is dependent on three factors, the loop bandwidth, the maximum frequency jump that the PLL must make and the final tolerance to which the frequency must settle. As a rule-of-thumb it is given by:

$$LT = \frac{400}{F_C}(1 - \log_{10}\Delta F) \qquad \text{Where } \Delta F = \frac{\text{Frequency} - \text{tolerance}}{\text{Frequency} - \text{jump}}$$

These equations are approximations of the ones used by Webench to calculate phase noise and lock-time.

10.9.3 Practical Optimization

In an example where frequency drift and drift rate can be improved though loop filter tweaks, consider the results taken below. The drift rate is 26.1 kHz per 50µs and the maximum drift is 25 kHz for DH1 packets, both of which are exceeding or touching the Bluetooth pass limits. These measurements are taken with component values shown above.

20180048

TRM/CA/09/C (Carrier Drift				
Hoppong On- Low Channel				
	DH1	**DH3**	**DH5**	**Limits**
Drift Rate/50 µs	26.1 kHz	N/A	–30.5 kHz	±20 kHz
Max Drift	25 kHz	N/A	36 kHz	DHI: ±25 kHz
Average Drift	–1 kHz	N/A	12 kHz	DH3: ±40 kHz
Packets Tested	10	N/A	10	D5I: ±40 kHz
Packets Failed	2	N/A	10	
Overall Result	Failed	N/A	Failed	

Results below were taken on the same board with three loop filter values changed. C2 and R2 have been increased in value and C1 has been reduced. The drift rate has improved by 13 kHz per 50 µs and the maximum drift has improved by 10 kHz.

TRM/CA/09/C (Carrier Drift				
Hoppong On- Low Channel				
	DH1	**DH3**	**DH5**	**Limits**
Drift Rate/50 µs	–13.6 kHz	N/A	–15.6 kHz	±20 kHz
Max Drift	15 kHz	N/A	21 kHz	DHI: ±25 kHz
Average Drift	3 kHz	N/A	1 kHz	DH3: ±40 kHz
Packets Tested	10	N/A	10	D5I: ±40 kHz
Packets Failed	0	N/A	0	
Overall Result	Passed	N/A	Passed	

The effect of changing these three components is to reduce the loop bandwidth which reduces the phase noise. The reduction in this noise level corresponds directly to the reduction of noise in the payload area where drift is measured. This noise reduction comes at the expense of lock-time which can be increased to 120 µs without suffering any ill effects, however if we continue to reduce the loop BW further the lock-time will increase such that the PLL does not have time to lock before data transmission and the drift will again increase. Before the lock-time goes out of spec, the modulation index will start to fall since it is being cut by the reducing loop BW. Therefore a compromise has to be found between lock-time, phase noise and modulation, which yields best performance.

Note: The values shown in the LMX9830 datasheet, are the best case optimized values that have been shown to produce the best overall results and are recommended as a starting point for this design.

Another example of how the loop filter values can affect frequency drift rate, these results below show the DUT with maximum drift on mid and high channels failing. Adjusting the loop bandwidth as shown provides the improvement required to pass qualification.

Original results:

Hoppong On- Low Channel				
	DH1	**DH3**	**DH5**	**Limits**
Drift Rate/50 µs15.00	15.00 kHz	–28.10 kHz	–19.10 kHz	±20 kHz
Maximum Drift	19 kHz	–37 kHz	–20kHz	DHI: ±25 kHz
Average Drift	11 kHz	–32 kHz	–10 kHz	DH3: ±40 kHz
Packets Tested	10	10	10	D5I: ±40 kHz
Packets Failed	0	1	0	
Result	Pass	Fail	Pass	
Hoppong On- Med Channel				
	DH1	**DH3**	**DH5**	**Limits**
Drift Rate/50 µs	15.00 kHz	–28.10 kHz	–19.10 kHz	±20 kHz
Max Drift	19 kHz	–37 kHz	–20kHz	DHI: ±25 kHz
Average Drift	11 kHz	–32 kHz	–10 kHz	DH3: ±40 kHz
Packets Tested	10	10	10	D5I: ±40 kHz
Packets Failed	0	1	0	
Overall Result	Pass	Fail	Pass	
Hoppong On- High Channel				
	DH1	**DH3**	**DH5**	**Limits**
Drift Rate/50 µs	15.00 kHz	–28.10 kHz	–19.10 kHz	±20 kHz
Max Drift	19 kHz	–37 kHz	–20kHz	DHI: ±25 kHz
Average Drift	11 kHz	–32 kHz	–10 kHz	DH3: ±40 kHz
Packets Tested	10	10	10	D5I: ±40 kHz
Packets Failed	0	1	0	
Overall Result	Pass	Fail	Pass	

New results:

Hoppong On- Low Channel				
	DH1	**DH3**	**DH5**	**Limits**
Drift Rate/50 µs	−12.00 kHz	−15.10 kHz	18.8 kHz	±20 kHz
Max Drift	−15 kHz	−35 kHz	−19 kHz	DHI: ±25 kHz
Average Drift	−6 kHz	−25 kHz	−9 kHz	DH3: ±40 kHz
Packets Tested	10	10	10	D5I: ±40 kHz
Packets Failed	0	0	0	
Overall Result	Pass	Pass	Pass	
Hoppong On- Med Channel				
	DH1	**DH3**	**DH5**	**Limits**
Drift Rate/50 µs	−14.20 kHz	−16.10kHz	17.20 kHz	±20 kHz
Max Drift	−16 kHz	−354 kHz	−22 kHz	DHI: ±25 kHz
Average Drift	−11kHz	−27 kHz	−9 kHz	DH3: ±40 kHz
Packets Tested	10	10	10	D5I: ±40 kHz
Packets Failed	0	0	0	
Overall Result	Pass	Pass	Pass	
Hoppong On- High Channel				
	DH1	**DH3**	**DH5**	**Limits**
Drift Rate/50 µs	−12.70 kHz	−17.40 kHz	16.50 kHz	±20 kHz
Max Drift	−23 kHz	−29 kHz	−25 kHz	DHI: ±25 kHz
Average Drift	−12 kHz	−25 kHz	−16 kHz	DH3: ±40 kHz
Packets Tested	10	10	10	D5I: ±40 kHz
Packets Failed	0	0	0	
Overall Result	Pass	Pass	Pass	

10.9.4 Component Values for NSC Reference Designs

The following is a list of components for the loop filter values used on National reference design, (Serial Dongle) they have been tweaked and optimized in each case to yield optimum performance for each case. The values differ slightly from one platform to another due to board paracitics caused by layout differences.

Platform	C8	C7	C9	R23	R14
LMX9830 Dongle	220pF	2200pF	39pF	3.3k	10k

11.0 Integrated Firmware

The LMX9830 includes the full Bluetooth stack up to RFComm to support the following profiles:

- GAP (Generic Access Profile)
- SDAP (Service Discovery Application Profile)
- SPP (Serial Port Profile)

Figure 12 shows the Bluetooth protocol stack with command interpreter interface. The command interpreter offers a number of different commands to support the functionality given by the different profiles. Execution and interface timing is handled by the control application.

The chip has an internal data area in RAM that includes the parameters shown in *Table 22*.

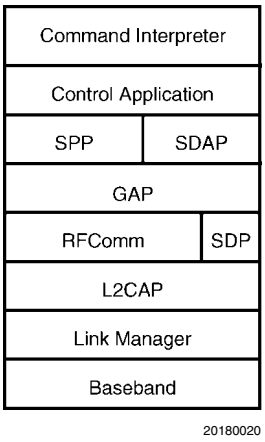


FIGURE 12. LMX9830 Software Implementation

11.1 FEATURES

11.1.1 Operation Modes

On boot-up, the application configures the module following the parameters in the data area.

Automatic Operation

No Default Connections Stored:

In Automatic Operation the module is connectable and discoverable and automatically answers to service requests. The command interpreter listens to commands and links can be set up. The full command list is supported.

If connected by another device, the module sends an event back to the host, where the RFComm port has been connected, and switches to transparent mode.

Default Connections Stored:

If default connections were stored on a previous session, once the LMX9830 is reset, it will attempt to connect each device stored within the data RAM three times. The host will be notified about the success of the link setup via a link status event.

Non-Automatic Operation

In Non-Automatic Operation, the LMX9830 does not check the default connections section within the Data RAM. If connected by another device, it will NOT switch to transparent mode and continue to interpret data sent on the UART.

Transparent Mode

The LMX9830 supports transparent data communication from the UART interface to a bluetooth link.

If activated, the module does not interpret the commands on the UART which normally are used to configure and control the module. The packages don't need to be formatted as described in *Table 24*. Instead all data are directly passed through the firmware to the active bluetooth link and the remote device.

Transparent mode can only be supported on a point-to-point connection. To leave Transparent mode, the host must send a UART_BREAK signal to the module.

Force Master Mode

In Force Master mode tries to act like an Accesspoint for multiple connections. For this it will only accept the link if a Master/slave role switch is accepted by the connecting device. After successful link establishment the LMX9830 will be Master and available for additional incoming links. On the first incoming link the LMX9830 will switch to transparent depending on the setting for automatic or command mode. Additional links will only be possible if the device is not in transparent mode.

11.1.2 Default Connections

The LMX9830 supports the storage of up to 3 devices within its NVS. Those connections can either be connected after reset or on demand using a specific command.

11.1.3 Event Filter

The LMX9830 uses events or indicators to notify the host about successful commands or changes at the bluetooth interface. Depending on the application the LMX9830 can be configured. The following levels are defined:

- No Events:
  – The LMX9830 is not reporting any events. Optimized for passive cable replacement solutions.
- Standard LMX9830 events:
  – Only necessary events will be reported
- All events:
  – Additional to the standard all changes at the physical layer will be reported.

11.1.4 Default Link Policy

Each Bluetooth Link can be configured to support M/S role switch, Hold Mode, Sniff Mode and Park Mode. The default link policy defines the standard setting for incoming and outgoing connections.

11.1.5 Audio Support

The LMX9830 offers commands to establish and release synchronous connections (SCO) to support Headset or Handsfree applications. The firmware supports one active link with all available package types (HV1, HV2, HV3), routing the audio data between the bluetooth link and the advanced audio interface. In order to provide the analog data interface, an external audio codec is required. The LMX9830 includes a list of codecs which can be used.

TABLE 22. Operation Parameters Stored in LMX9830

Parameter	Default Value	Description
BDADDR	(To be requested from IEEE)	Bluetooth device address
Local Name	Serial port device	Friendly Name
PinCode	0000	Bluetooth PinCode
Operation Mode	Automatic ON	Automatic mode ON or OFF
Default Connections	0	Up to seven default devices to connect to
SDP Database	1 SPP entry: Name: COM1 Authentication and encryption enabled	Service discovery database, control for supported profiles
UART Speed	9600	Sets the speed of the physical UART interface to the host
UART Settings	1 Stop bit, parity disabled	Parity and stop bits on the hardware UART interface
Ports to Open	0000 0001	Defines the RFComm ports to open
Link Keys	No link keys	Link keys for paired devices
Security Mode	2	Security mode
Page Scan Mode	Connectable	Connectable/Not connectable for other devices
Inquiry Scan Mode	Discoverable	Discoverable/Not Discoverable/Limited Discoverable for other devices
Default Link Policy	All modes allowed	Configures modes allowed for incoming or outgoing connections (Role switch, Hold mode, Sniff mode...)
Default Link Timeout	20 seconds	The Default Link Timeout configures the timeout, after which the link is assumed lost, if no packages have been received from the remote device.
Event Filter	Standard LMX9830 events reported	Defines the level of reporting on the UART –no events –standard events –standard including ACL link events
Default Audio Settings	non	Configures the settings for the external codec and the air format. • Codecs: Motorola MC145483 / Winbond W681360 OKI MSM7717 / Winbond W681310 PCM Slave • Airformat: CVSD µ-Law A-Law

12.0 Low Power Modes

The LMX9830 supports different Low Power Modes to reduce power in different operating situations. The modular structure of the LMX9830 allows the firmware to power down unused modules.

The Low power modes have influence on:

- UART transport layer
  – enabling or disabling the interface
- Bluetooth Baseband activity
  – firmware disables LLC and Radio if possible

12.1 POWER MODES

The following LMX9830 power modes, which depend on the activity level of the UART transport layer and the radio activity are defined:

The radio activity level mainly depends on application requirements and is defined by standard bluetooth operations like inquiry/page scanning or an active link.

A remote device establishing or disconnecting a link may also indirectly change the radio activity level.

The UART transport layer by default is enabled on device power up. In order to disable the transport layer the command “Disable Transport Layer” is used. Thus only the Host side command interface can disable the transport layer. Enabling the transport layer is controlled by the HW Wakeup signalling. This can be done from either the Host or the LMX9830. See also “LMX9830 Software User’s Guide” for detailed information on timing and implementation requirements.

TABLE 23. Power Mode Activity

Power Mode	UART Activity	Radio Activity	Reference Clock
PM0	OFF	OFF	none
PM1	ON	OFF	Main Clock
PM2	OFF	Scanning	Main Clock / 32.768 kHz
PM3	ON	Scanning	Main Clock
PM4	OFF	SPP Link	Main Clock
PM5	ON	SPP Link	Main Clock

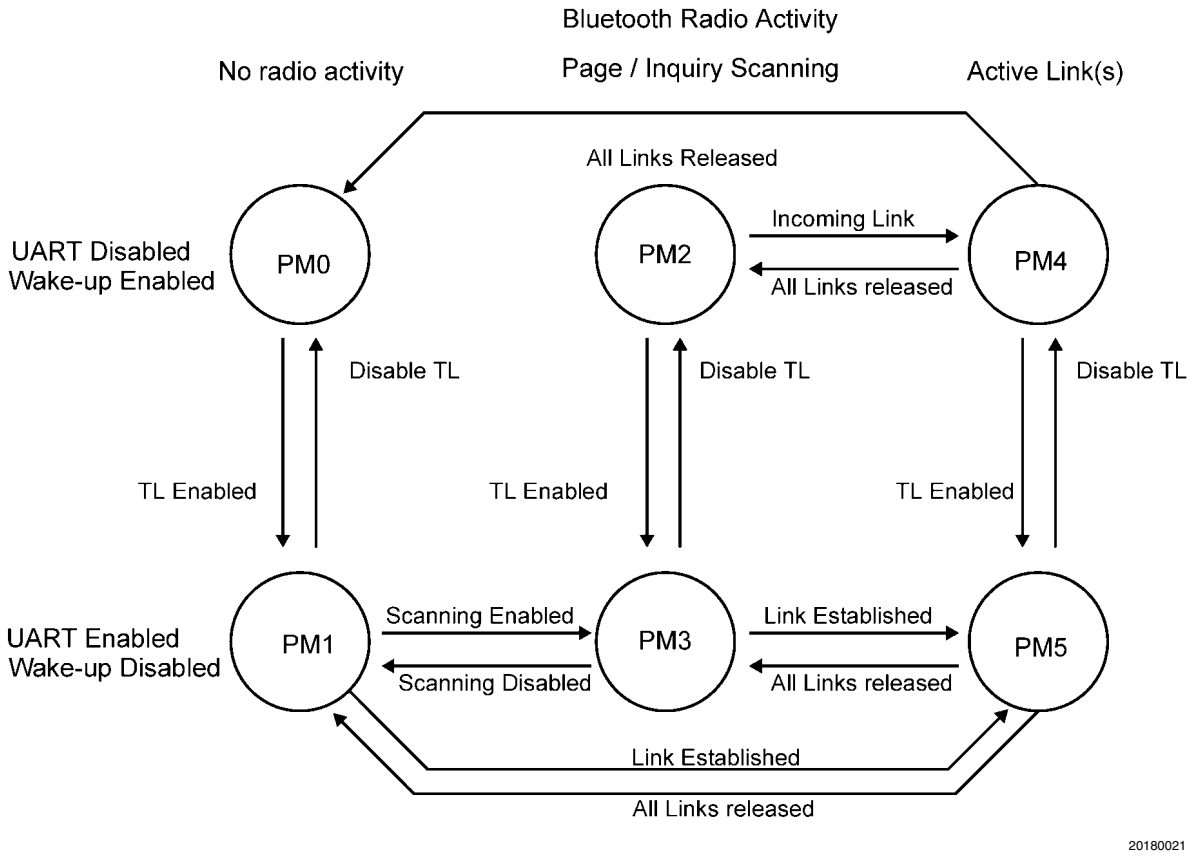


FIGURE 13. Transition between different Hardware Power Modes

12.2 ENABLING AND DISABLING UART TRANSPORT

12.2.1 Hardware Wake up functionality

In certain usage scenarios the host is able to switch off the transport layer of the LMX9830 in order to reduce power consumption. Afterwards both devices, host and LMX9830 are able to shut down their UART interfaces.

In order to save system connections the UART interface is reconfigured to hardware wakeup functionality. For a detailed timing and command functionality please see also the "LMX9830 Software User's Guide".

The interface between host and LMX9830 is defined as described in *Figure 14*.

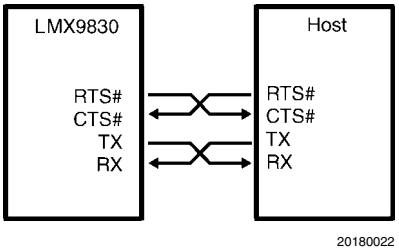


FIGURE 14. UART NULL Modem Connection

12.2.2 Disabling the UART Transport Layer

The Host can disable the UART transport layer by sending the "Disable Transport Layer" Command. The LMX9830 will empty its buffers, send the confirmation event and disable its UART interface. Afterwards the UART interface will be reconfigured to wake up on a falling edge of the CTS pin.

12.2.3 LMX9830 Enabling the UART Interface

As the Transport Layer can be disabled in any situation the LMX9830 must first make sure the transport layer is enabled before sending data to the host. Possible scenarios can be incoming data or incoming link indicators. If the UART is not enabled the LMX9830 assumes that the Host is sleeping and waking it up by activating RTS. To be able to react on that Wake up, the host has to monitor the CTS pin.

As soon as the host activates its RTS pin, the LMX9830 will first send a confirmation event and then start to transmit the events.

12.2.4 Enabling the UART Transport Layer from the Host

If the host needs to send data or commands to the LMX9830 while the UART Transport Layer is disabled it must first assume that the LMX9830 is sleeping and wake it up using its RTS signal.

When the LMX9830 detects the Wake-Up signal it activates the UART HW and acknowledges the Wake-Up signal by settings its RTS. Additionally the Wake up will be confirmed by a confirmation event. When the Host has received this "Transport Layer Enabled" event, the LMX9830 is ready to receive commands.

13.0 Command Interface

The LMX9830 offers Bluetooth functionality in either a self contained slave functionality or over a simple command interface. The interface is listening on the UART interface.

The following sections describe the protocol transported on the UART interface between the LMX9830 and the host in command mode (see *Figure 15*). In Transparent mode, no data framing is necessary and the device does not listen for commands.

13.1 FRAMING

The connection is considered "Error free". But for packet recognition and synchronization, some framing is used.

All packets sent in both directions are constructed per the model shown in *Table 24*.

13.1.1 Start and End Delimiter

The "STX" char is used as start delimiter: STX = 0x02. ETX = 0x03 is used as end delimiter.

13.1.2 Packet Type ID

This byte identifies the type of packet. See *Table 25* for details.

13.1.3 Opcode

The opcode identifies the command to execute. The opcode values can be found within the "LMX9830 Software User's Guide" included within the LMX9830 Evaluation Board.

13.1.4 Data Length

Number of bytes in the Packet Data field. The maximum size is defined with 333 data bytes per packet.

13.1.5 Checksum:

This is a simple Block Check Character (BCC) checksum of the bytes "Packet type", "Opcode" and "Data Length". The BCC checksum is calculated as low byte of the sum of all bytes (e.g., if the sum of all bytes is 0x3724, the checksum is 0x24).

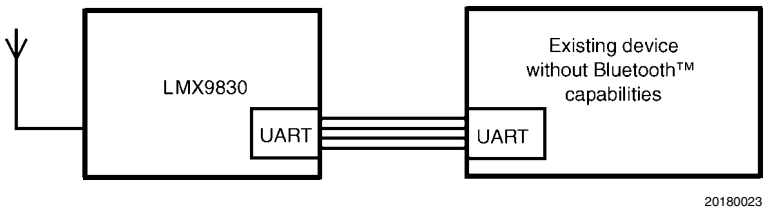


FIGURE 15. Bluetooth Functionality

TABLE 24. Package Framing

StartD elimiter	Packet Type ID	Opcode	Data Length	Check sum	Packet Data	End Delimiter
1 Byte	1 Byte	1 Byte	2 Bytes	1 Byte	<Data Length> Bytes	1 Byte
	- - - - - - - - - - - - Checksum - - - - - - - - - - - -					

TABLE 25. Packet Type Identification

ID	Direction	Description
0x52 'R'	REQUEST (REQ)	A request sent to the Bluetooth module. All requests are answered by exactly one confirm.
0x43 'C'	Confirm (CFM)	The Bluetooth modules confirm to a request. All requests are answered by exactly one confirm.
0x69 'i'	Indication (IND)	Information sent from the Bluetooth module that is not a direct confirm to a request. Indicating status changes, incoming links, or unrequested events.
0x72 'r'	Response (RES)	An optional response to an indication. This is used to respond to some type of indication message.

13.2 COMMAND SET OVERVIEW

The LMX9830 has a well defined command set to:

- Configure the device:
  - Hardware settings
  - Local Bluetooth parameters
  - Service database
- Set up and handle links

Table 26 through *Table 36* show the actual command set and the events coming back from the device. A full documented description of the commands can be found in the "LMX9830 Software User's Guide".

Note: For standard Bluetooth operation only commands from *Table 26* through *Table 28* will be used. Most of the remaining commands are for configuration purposes only.

TABLE 26. Device Discovery

Command	Event	Description
Inquiry	Inquiry Complete	Search for devices
	Device Found	Lists BDADDR and class of device
Remote Device Name	Remote Device Name Confirm	Get name of remote device

TABLE 27. SDAP Client Commands

Command	Event	Description
SDAP Connect	SDAP Connect Confirm	Create an SDP connection to remote device
SDAP Disconnect	SDAP Disconnect Confirm	Disconnect an active SDAP link
	Connection Lost	Notification for lost SDAP link
SDAP Service Browse	Service Browse Confirm	Get the services of the remote device
SDAP Service Search	SDAP Service Search Confirm	Search a specific service on a remote device
SDAP Attribute Request	SDAP Attribute Request Confirm	Searches for services with specific attributes

TABLE 28. SPP Link Establishment

Command	Event	Description
Establish SPP Link	Establishing SPP Link Confirm	Initiates link establishment to a remote device
	Link Established	Link successfully established
	Incoming Link	A remote device established a link to the local device
Set Link Timeout	Set Link Timeout Confirm	Confirms the Supervision Timeout for the existing Link
Get Link Timeout	Get Link Timeout Confirm	Get the Supervision Timeout for the existing Link
Release SPP Link	Release SPP Link Confirm	Initiate release of SPP link
SPP Send Data	SPP Send Data Confirm	Send data to specific SPP port
	Incoming Data	Incoming data from remote device
Transparent Mode	Transparent Mode Confirm	Switch to Transparent mode on the UART

TABLE 29. Storing Default Connections

Command	Event	Description
Connect Default Connection	Connect Default Connection Confirm	Connects to either one or all stored default connections
Store Default Connection	Store Default Connection Confirm	Store device as default connection
Get list of Default Connections	List of Default Devices	
Delete Default Connections	Delete Default Connections Confirm	

TABLE 30. Bluetooth Low Power Modes

Command	Event	Description
Set Default Link Policy	Set Default Link Policy Confirm	Defines the link policy used for any incoming or outgoing link
Get Default Link Policy	Get Default Link Policy Confirm	Returns the stored default link policy
Set Link Policy	Set Link Policy Confirm	Defines the modes allowed for a specific link
Get Link Policy	Get Link Policy Confirm	Returns the actual link policy for the link
Enter Sniff Mode	Enter Sniff Mode Confirm	
Exit Sniff Mode	Exit Sniff Mode Confirm	
Enter Hold Mode	Enter Hold Mode Confirm	
	Power Save Mode Changed	Remote device changed power save mode on the link

TABLE 31. Audio Control Commands

Command	Event	Description
Establish SCO Link	Establish SCO Link Confirm	Establish SCO Link on existing RFComm Link
	SCO Link Established Indicator	A remote device has established a SCO link to the local device
Release SCO Link	Release SCO Link Confirm	Release SCO Link Audio Control
	SCO Link Released Indicator	SCO Link has been released
Change SCO Packet Type	Change SCO Packet Type Confirm	Changes Packet Type for existing SCO link
	SCO Packet Type changed indicator	SCO Packet Type has been changed
Set Audio Settings	Set Audio Settings Confirm	Set Audio Settings for existing Link
Get Audio Settings	Get Audio Settings Confirm	Get Audio Settings for existing Link
Set Volume	Set Volume Confirm	Configure the volume
Get Volume	Get Volume Confirm	Get current volume setting
Mute	Mute Confirm	Mutes the microphone input

TABLE 32. Wake Up Functionality

Command	Event	Description
Disable Transport Layer	Transport Layer Enabled	Disabling the UART Transport Layer and activates the Hardware Wakeup function

TABLE 33. SPP Port Configuration and Status

Command	Event	Description
Set Port Config	Set Port Config Confirm	Set port setting for the virtual serial port link over the air
Get Port Config	Get Port Config Confirm	Read the actual port settings for a virtual serial port
	Port Config Changed	Notification if port settings were changed from remote device
SPP Get Port Status	SPP Get Port Status Confirm	Returns status of DTR, RTS (for the active RFComm link)
SPP Port Set DTR	SPP Port Set DTR Confirm	Sets the DTR bit on the specified link
SPP Port Set RTS	SPP Port Set RTS Confirm	Sets the RTS bit on the specified link
SPP Port BREAK	SPP Port BREAK	Indicates that the host has detected a break
SPP Port Overrun Error	SPP Port Overrun Error Confirm	Used to indicate that the host has detected an overrun error
SPP Port Parity Error	SPP Port Parity Error Confirm	Host has detected a parity error
SPP Port Framing Error	SPP Port Framing Error Confirm	Host has detected a framing error
	SPP Port Status Changed	Indicates that remote device has changed one of the port status bits

TABLE 34. Local Bluetooth Settings

Command	Event	Description
Read Local Name	Read Local Name Confirm	Read actual friendly name of the device
Write Local Name	Write Local Name Confirm	Set the friendly name of the device
Read Local BDADDR	Read Local BDADDR Confirm	
Change Local BDADDR	Change Local BDADDR Confirm	**Note:** The BDADDR has to be obtained from the IEEE organization. See http://standarts.ieee.org/regauth/oui/
Store Class of Device	Store Class of Device Confirm	
Set Scan Mode	Set Scan Mode Confirm	Change mode for discoverability and connectability
	Set Scan Mode Indication	Reports end of Automatic limited discoverable mode
Get Fixed Pin	Get Fixed Pin Confirm	Reads current PinCode stored within the device
Set Fixed Pin	Set Fixed Pin Confirm	Set the local PinCode
	PIN request	A PIN code is requested during authentication of an ACL link
Get Security Mode	Get Security Mode Confirm	Get actual Security mode
Set Security Mode	Set Security Mode Confirm	Configure Security mode for local device (default 2)
Remove Pairing	Remove Pairing Confirm	Remove pairing with a remote device
List Paired Devices	List of Paired Devices	Get list of paired devices stored in the LMX9830 data memory
Set Default Link Timeout	Set Default Link Timeout Confirm	Store default link supervision timeout
Get Default Link Timeout	Get Default Link Timeout Confirm	Get stored default link supervision timeout
Force Master Role	Force Master Role Confirm	Enables/Disables the request for master role at incoming connections

TABLE 35. Local Service Database Configuration

Command	Event	Description
Store generic SDP Record	Store SDP Record Confirm	Create a new service record within the service database
Enable SDP Record	Enable SDP Record Confirm	Enable or disable SDP records
Delete All SDP Records	Delete All SDP Records Confirm	
Ports to Open	Ports to Open Confirmed	Specify the RFComm Ports to open on startup

TABLE 36. Local Hardware Commends

Command	Event	Description
Get Default Audio Settings	Get Default Audio Settings Confirm	Get stored Default Audio Settings
Set Default Audio Settings	Set Default Audio Settings Confirm	Configure Default Settings for Audio Codec and Air Format, stored in NVS
Set Event Filter	Set Event Filter Confirm	Configures the reporting level of the command interface
Get Event Filter	Get Event Filter Confirm	Get the status of the reporting level
Read RSSI	Read RSSI Confirm	Returns an indicator for the incoming signal strength
Change UART Speed	Change UART Speed Confirm	Set specific UART speed; needs proper ISEL pin setting
Change UART Settings	Change UART Settings Confirm	Change configuration for parity and stop bits
Test Mode	Test Mode Confirm	Enable Bluetooth, EMI test, or local loopback
Restore Factory Settings	Restore Factory Settings Confirm	
Reset	Dongle Ready	Soft reset
Firmware Upgrade		Stops the bluetooth firmware and executes the In-system-programming code
Set Clock Frequency	Set Clock Frequency Confirm	Write Clock Frequency setting in the NVS
Get Clock Frequency	Get Clock Frequency Confirm	Read Clock Frequency setting from the NVS
Set PCM Slave Configuration	Set PCM Slave Configuration Confirm	Write the PCM Slave Configuration in the NVS
Write ROM Patch	Write ROM Patch Confirm	Store ROM Patch in the SimplyBlue module
Read Memory	Read Memory Confirm	Read from the internal RAM
Write Memory	Write Memory Confirm	Write to the internal RAM
Read NVS	Read NVS Confirm	Read from the NVS (EEPROM)
Write NVS	Write NVS Confirm	Write to the NVS (EEPROM)

TABLE 37. Initialization Commands

Command	Event	Description
Set Clock and Baudrate	Set Clock and Baudrate Confirm	Write Baseband frequency and Baudrate used
Enter Bluetooth Mode	Enter Bluetooth Mode Confirm	Request SimplyBlue module to enter BT mode
Set Clock and Baudrate	Set Clock and Baudrate Confirm	Write Baseband frequency and Baudrate used

TABLE 38. GPIO Control commands

Command	Event	Description
Set GPIO WPU	Set GPIO WPU Confirm	Enable/Disable weak pull up resistor on GPIOs
Get GPIO Input State	Get GPIO Input States Confirm	Read the status of the GPIOs
Set GPIO Direction	Set GPIO Direction Confirm	Set the GPIOs direction (Input, Ouput)
Set GPIO Output High	Set GPIO Output High Confirm	Set GPIOs Output to logical High
Set GPIO Output Low	Set GPIO Output Low Confirm	Set GPIOs Output to logical Low

14.0 Usage Scenarios

14.1 SCENARIO 1: POINT-TO-POINT CONNECTION

LMX9830 acts only as slave, no further configuration is required.

Example: Sensor with LMX9830; hand-held device with standard Bluetooth option.

The SPP conformance of the LMX9830 allows any device using the SPP to connect to the LMX9830.

Because of switching to Transparent automatically, the controller has no need for an additional protocol layer; data is sent raw to the other Bluetooth device.

On default, a PinCode is requested to block unallowed targeting.

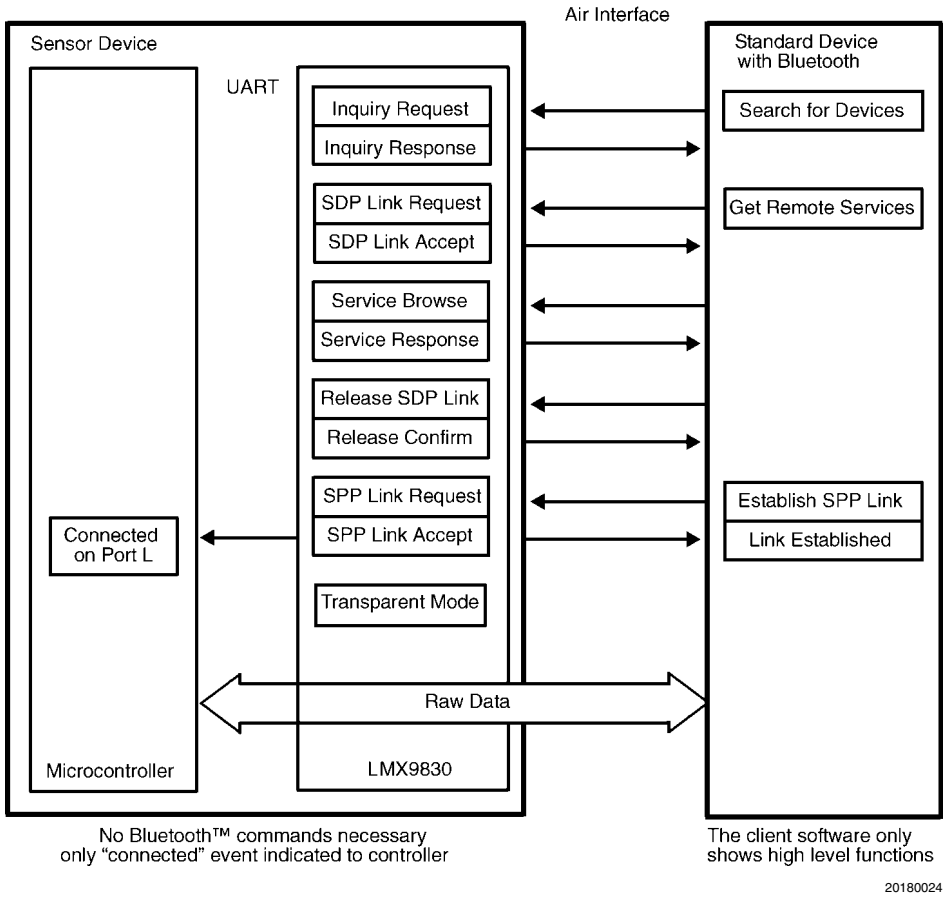


FIGURE 16. Point-to-Point Connection

14.2 SCENARIO 2: AUTOMATIC POINT-TO-POINT CONNECTION

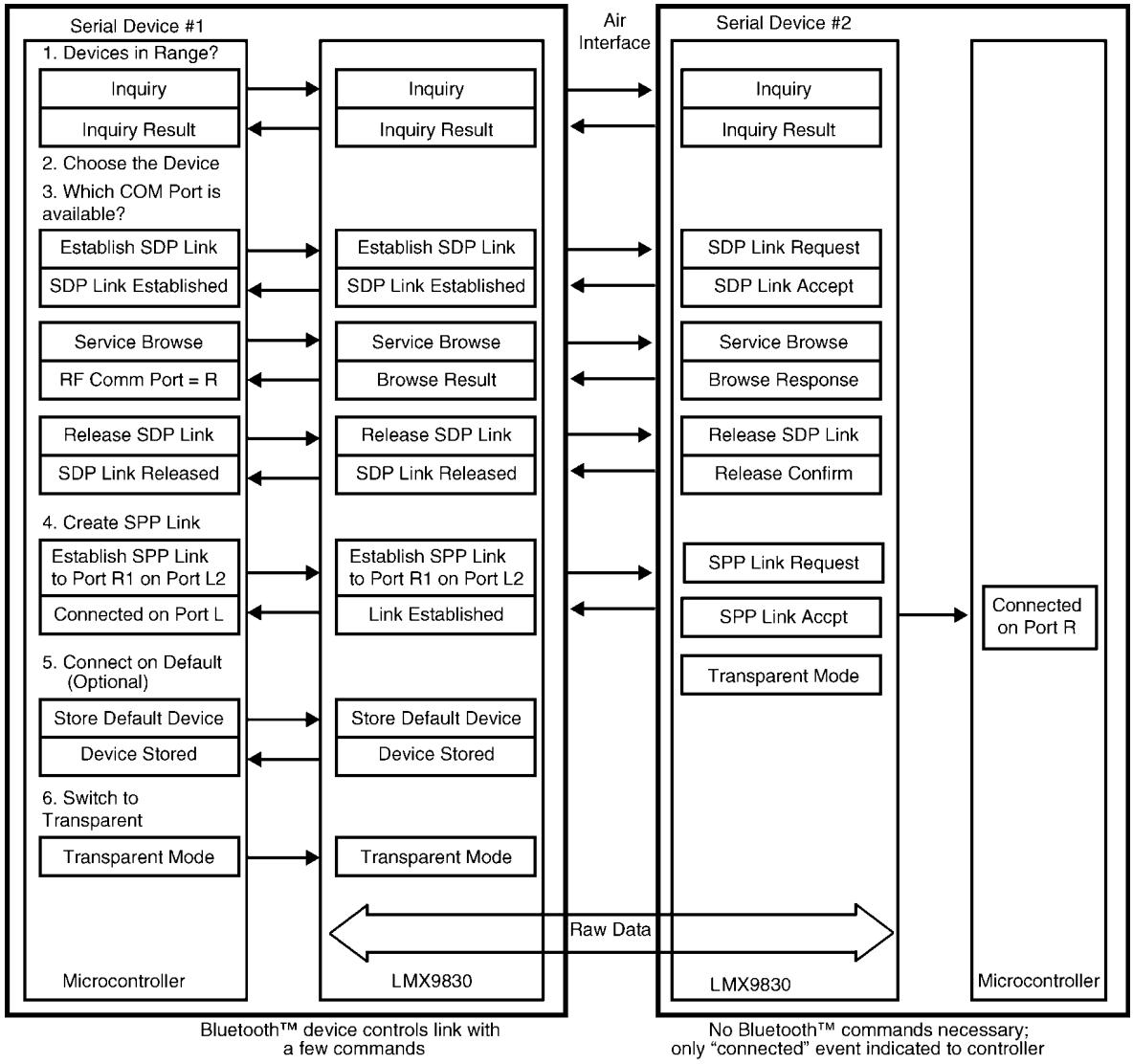
LMX9830 at both sides.

Example: Serial Cable Replacement.

Device #1 controls the link setup with a few commands as described.

If step 5 is executed, the stored default device is connected (step 4) after reset (in Automatic mode only) or by sending the command “Connect to Default Device”. The command can be sent to the device at any time.

If step 6 is left out, the microcontroller has to use the command “Send Data” instead of sending data directly to the module.



1. Port R indicates the remote RFComm channel to connect to. Usually the result of the SDP request.
2. Port L indicates the Local RFComm channel used for that connection.

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FIGURE 17. Automatic Point-to-Point Connection

14.3 SCENARIO 3: POINT-TO-MULTIPOINT CONNECTION

LMX9830 acts as master for several slaves.

Example: Two sensors with LMX9830; one hand-held device with implemented LMX9830.

Serial Devices #2 and #3 establish the link automatically as soon as they are contacted by another device. No controller interaction is necessary for setting up the Bluetooth link. Both switch automatically into Transparent mode. The host sends raw data over the UART.

Serial Device #1 is acting as master for both devices. As the host has to decide to or from which device data is coming from, data must be sent using the “Send data command”. If the device receives data from the other devices, it is packaged into an event called “Incoming data event”. The event includes the device related port number.

If necessary, a link configuration can be stored as default in the master Serial Device #1 to enable the automatic reconnect after reset, power-up, or by sending the “connect default connection” command.

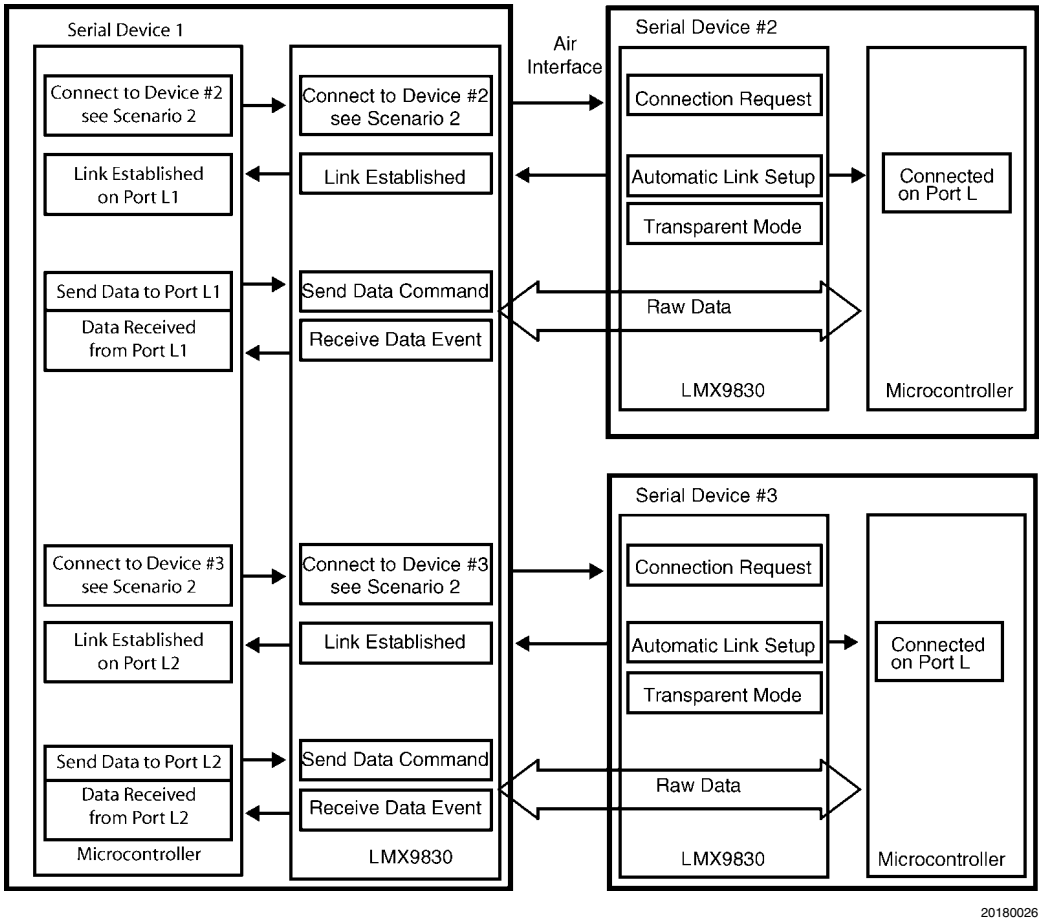


FIGURE 18. Automatic Point-to-Point Connection

15.0 Application Information

Figure 19 represents a typical system functional schematic for the LMX9830 in its normal 3.0V or 3.3V system interface operation.

In *Figure 20* represents a typical system functional schematic for the LMX9830 in its 1.8V system interface operation.

15.1 ANTENNA MATCHING NETWORK

The antenna matching network may or may not be required, depending upon the impedance of the antenna chosen and the trace impedance on the PCB. A 6.8 pF blocking capacitor is recommended.

Note: Additional L network placement is recommended for tuning the trace impedance if needed.

15.2 FILTERED POWER SUPPLY

It is important to provide the LMX9830 with adequate ground planes and a filtered power supply. It is highly recommended that a 0.1 µF and a 10 pF bypass capacitor be placed as close as possible to V_{CC} (pin E1) on the LMX9830 for 2.5V and 3.3V operations.

Note: For 1.8V operations V_{CC} filtering is not required and V_{CC} should be tied directly to ground.

15.3 HOST INTERFACE

To set the logic thresholds of the LMX9830 to match the host system, IOVCC (pin C4) must be connected to the logic power supply of the host system. It is highly recommended that a 10 pF bypass capacitor be placed as close as possible to the IOVCC pad on the LMX9830.

15.4 FREQUENCY AND BAUD RATE SELECTIONS

OP3, OP4, OP5 can be strapped to the host logic 0 and 1 levels to set the host interface boot-up configuration. Alternatively all OP3, OP4, OP5 can be hardwired over 1kW pullup/pulldown resistors. See *Table 18*.

15.5 START UP SEQUENCE OPTIONS

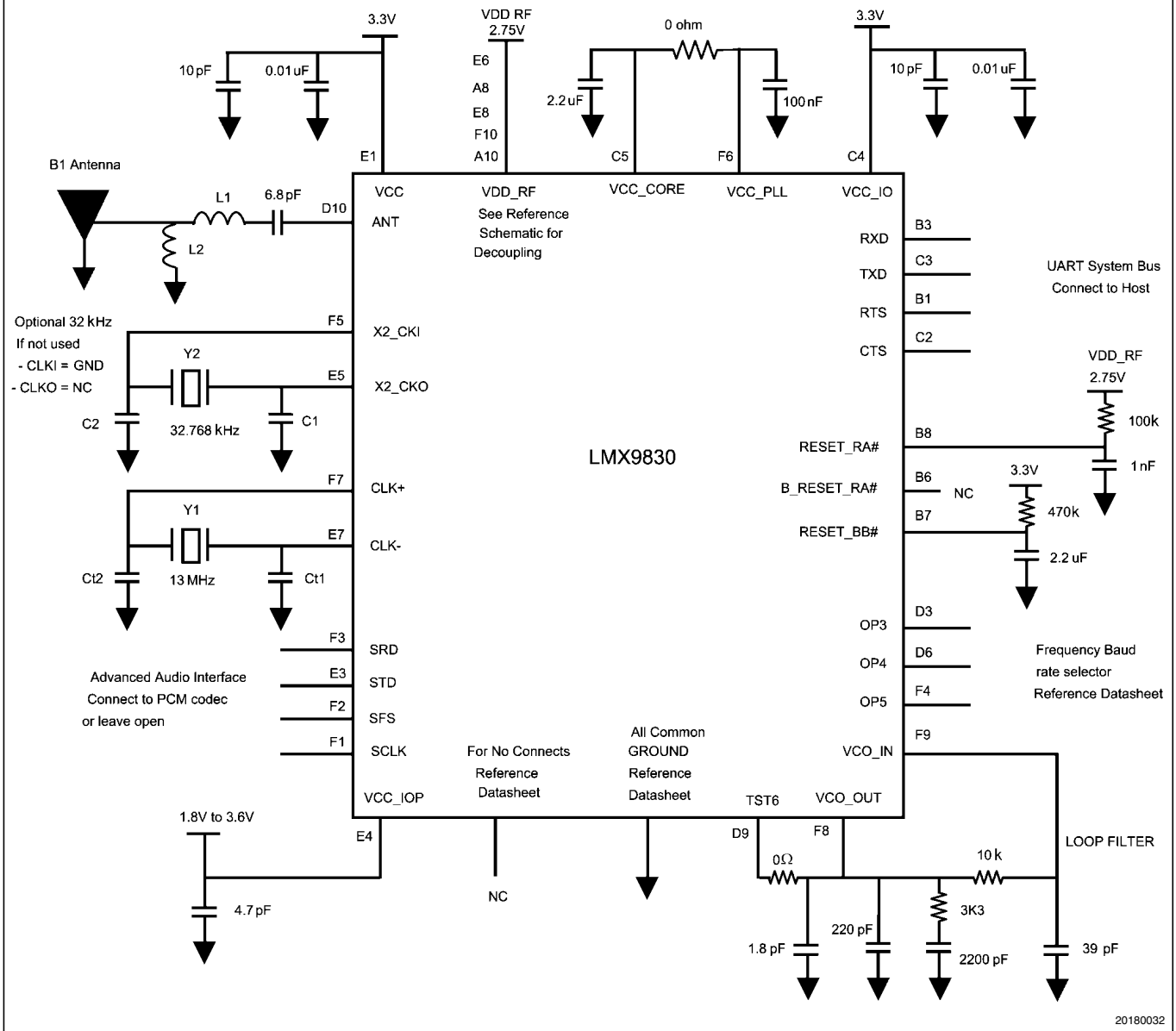
OP6, OP7, and Env1 can be left unconnected (both OP6 and OP7 are pulled low and ENV1 is pulled high internally), These can be hardwired over 1kW pullup/pulldown resistors. See *Table 17*.

15.6 CLOCK INPUT

The clock source must be placed as close as possible to the LMX9830. The quality of the radio performance is directly related to the quality of the clock source connected to the oscillator port on the LMX9830. Careful attention must be paid to the crystal/oscillator parameters or radio performance could be drastically reduced.

15.7 SCHEMATIC AND LAYOUT EXAMPLES

See *Figure 19*, *Figure 20*, and full schematic in *Section 16.0 Reference Design*.



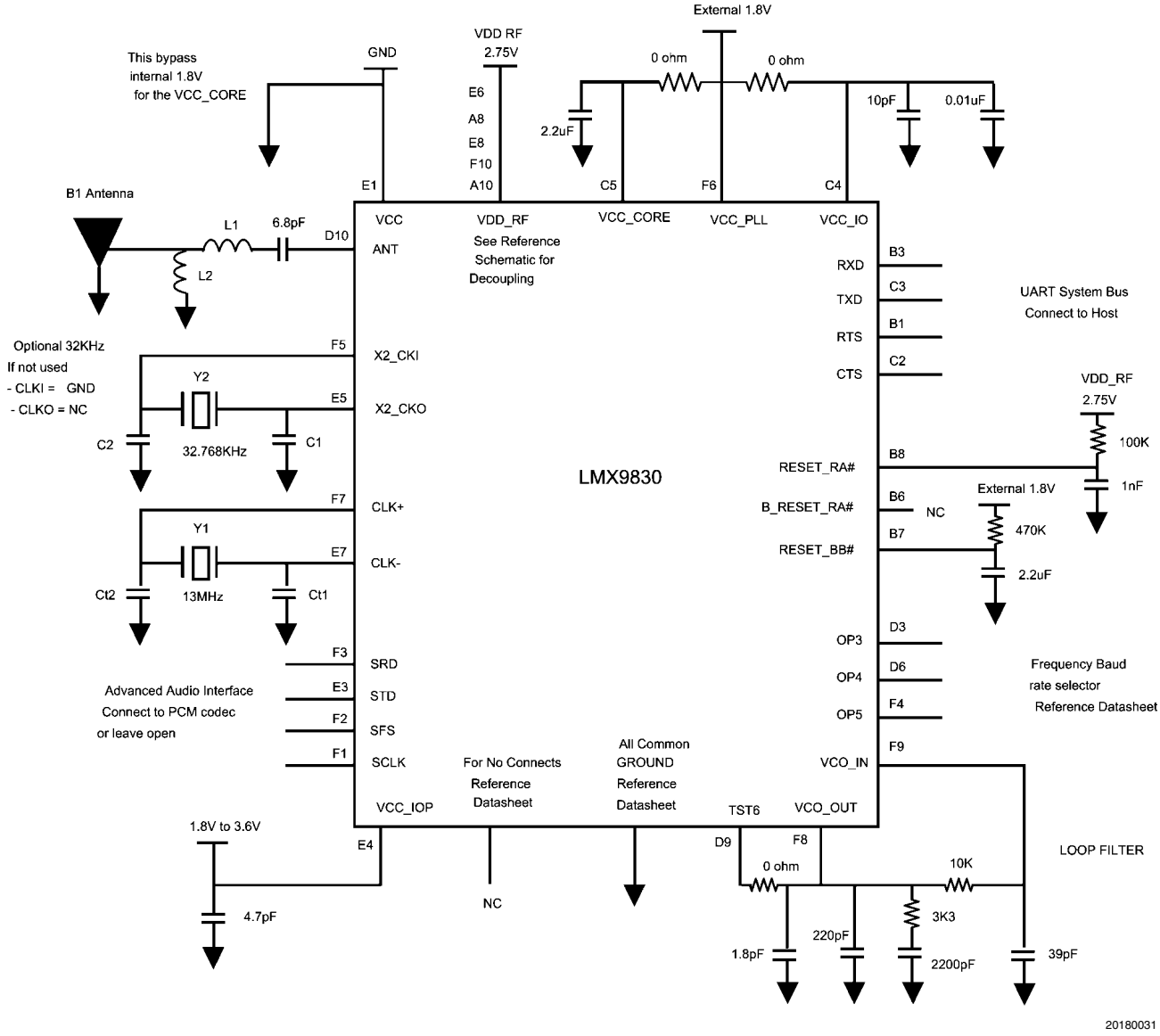
Note 40: Capacitor values, Ct1 and Ct2 may vary depending on board design crystal manufacturer specification.

Note: (C_L = crystal capacitance load rating) of 12pF or greater rating is required from the crystal vendor of choice to best match module impedance and give a viable tuning range for the system.

For grounding a single ground plane is used for both RF and Digital Grounding.

For Antenna it is recommend that a 3 component L type pad with series 6.8pF blocker cap be used between RF output and antenna matching L network. This allows for versatility in the design such that the match to the antenna maybe improved and/or the blocking margin increased by use a LC filter.

FIGURE 19. 2.5V to 3.3V Example Functional System Schematic



Note 41: Capacitor values, Ct1 and Ct2 may vary depending on board design crystal manufacturer specification.

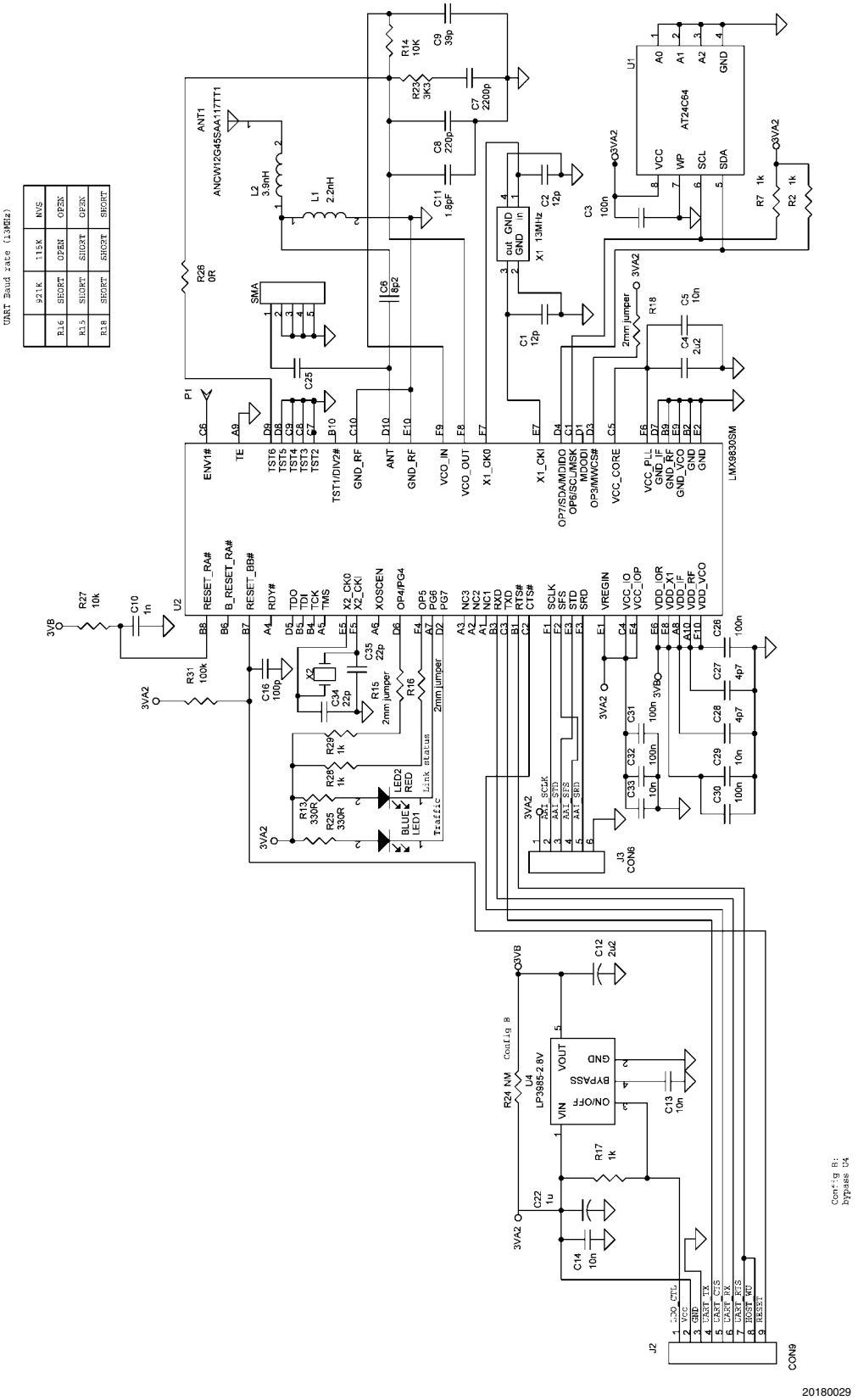
Note: (C_L = crystal capacitance load rating) of 12pF or greater rating is required from the crystal vendor of choice to best match module impedance and give a viable tuning range for the system.

For grounding a single ground plane is used for both RF and Digital Grounding.

For Antanna it is recommend that a 3 component L type pad with series 6.8pF blocker cap be used between RF output and antenna matching L network as shown above. This allows for versatility in the design such that the match to the antenna maybe improved and/or the blocking margin increased by use a LC filter.

FIGURE 20. 1.8V Example Functional System Schematic

16.0 Reference Design



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Note: For a schematic including an RS232 communication with the host, please refer to the “LMX9830DONGLE designer guide”.

Recommended that a 4 component T-PI pad be used between RF out and antenna input. Allows for versatility in the design such that the match to the antenna maybe improved and/or blocking margin increased by adding a LC filter.

17.0 Soldering

The LMX9830 bumps are designed to melt as part of the Surface Mount Assembly (SMA) process. In order to ensure reflow of all solder bumps and maximum solder joint reliability while minimizing damage to the package, recommended reflow profiles should be used.

Table 39, *Table 40* and *Figure 21*provide the soldering details required to properly solder the LMX9830 to standard PCBs. The illustration serves only as a guide and National is not liable if a selected profile does not work.

See IPC/JEDEC J-STD-020C, July 2004 for more information.

TABLE 39. Soldering Details

Parameter	Value
PCB Land Pad Diameter	13 mil
PCB Solder Mask Opening	19 mil
PCB Finish (HASL details)	Defined by customer or manufacturing facility
Stencil Aperture	17 mil
Stencil Thickness	5 mil
Solder Paste Used	Defined by customer or manufacturing facility
Flux Cleaning Process	Defined by customer or manufacturing facility
Reflow Profiles	See *Figure 21*

TABLE 40. Classification Reflow Profiles (Note 42), (Note 43)

Profile Feature	NOPB Assembly
Average Ramp-Up Rate (TsMAX to Tp)	3°C/second maximum
Preheat:	
Temperature Min (TsMIN)	150°C
Temperature Max (TsMAX)	200°C
Time (tsMIN to tsMAX)	60180 seconds
Time maintained above:	
Temperature (TL)	217°C
Time (tL)	60150 seconds
Peak/Classification Temperature (Tp)	260 + 0°C
Time within 5°C of actual Peak Temperature (tp)	20 – 40 seconds
Ramp-Down Rate	6°C/second maximum
Time 25 °C to Peak Temperature	8 minutes maximum
Reflow Profiles	See *Figure 21*

Note 42: See IPC/JEDEC J-STD-020C, July 2004.

Note 43: All temperatures refer to the top side of the package, measured on the package body surface.

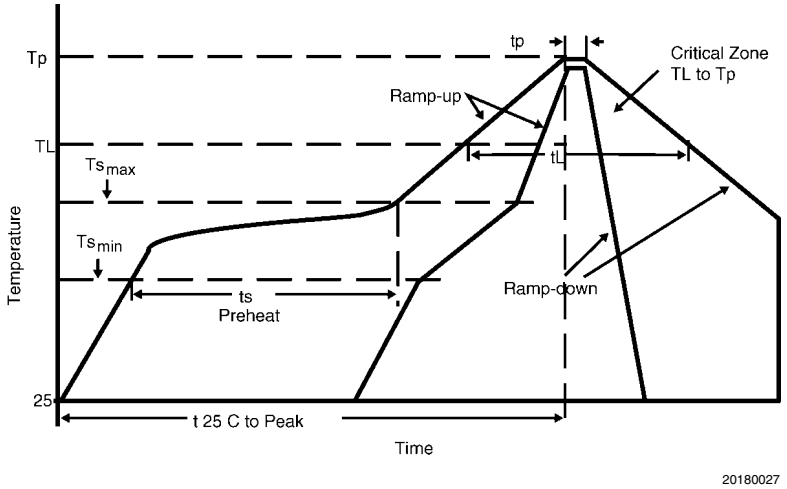
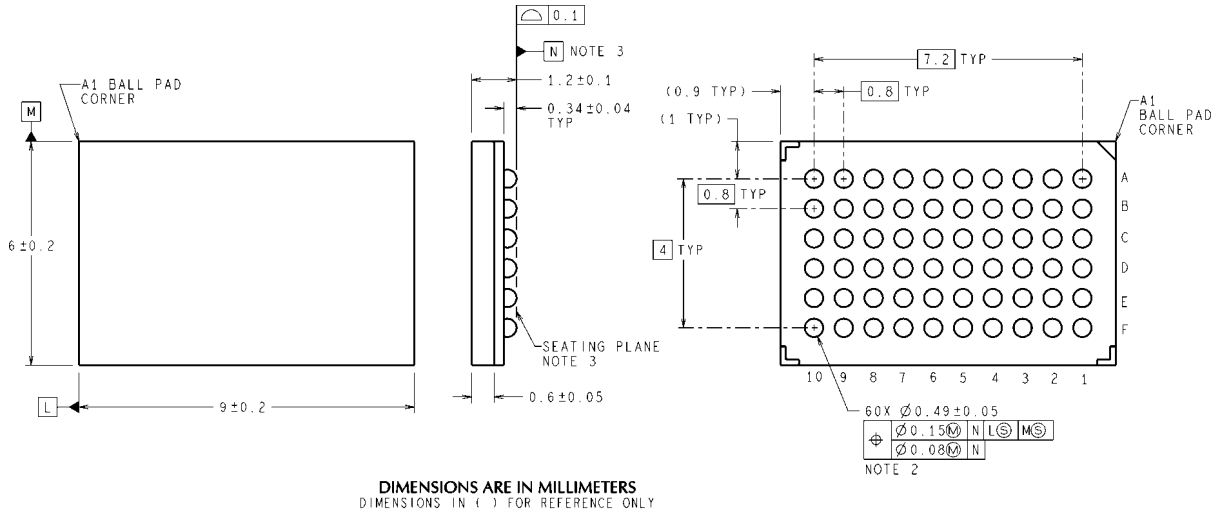


FIGURE 21. Typical Reflow Profiles

18.0 Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

SLF60A (Rev A)

FBGA, Plastic, Laminate, 9x6x1.2mm, 60 Ball, 0.8mm Pitch Package
NS Package Number SLF60A

Notes

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Power Management	www.national.com/power	Feedback	www.national.com/feedback
Switching Regulators	www.national.com/switchers		
LDOs	www.national.com/ldo		
LED Lighting	www.national.com/led		
PowerWise	www.national.com/powerwise		
Serial Digital Interface (SDI)	www.national.com/sdi		
Temperature Sensors	www.national.com/tempsensors		
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