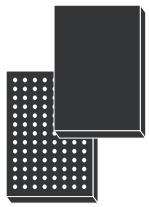
STA8058

TESEO™
high performance GPS multichip module (MCM)

Data Brief

Features

- GPS multichip module:
  - STA2058 TESEO Baseband
  - STA5620 RF Front-end
- Complete embedded memory system:
  - Flash 256 KB + 16 Kbytes
  - RAM 64 Kbytes.
- 66-MHz ARM7TDMI 32 bit processor
- High performance GPS engine (HPGPS)
- SBAS (WAAS and EGNOS) supported
- Sensitivity (-146 dBm acquisition, -159 dBm tracking)
- Time to first fix (1 s reacquisition, 2.5 s hot start, 34 s warm start, 39 s cold start)
- Accuracy (2 m autonomous)
- Extensive GPS receiver interfaces: 32 GPIOs, 4 UARTs, 2 SPIs, 2 I2Cs, 1CANs 2.0, 1 USB 1.1, 1 HDLC and 4 channels ADC
- Compatible with L1 signal (C/A code)
- ST proprietary technology
  - CMOS Flash embebbed technology for STA2058
  - BiCMOS Sige technology for STA5620
- LFBGA104 lead-free package
- -40 °C to 85 °C operating temperature range



LFBGA104 (7x11x1.4 mm)

Evaluation kits

- STA8058 module reference designs (17x19 mm and 25x25 mm)
- Evaluation board hosting STA8058 module

Description

STA8058 TESEO MCM is a fully embedded GPS engine integrating STA2058 TESEO baseband. and STA5620 RF front-end. The embedded Flash memory enables the equipment manufacturer to load the entire GPS software (including tracking, acquisition, navigation and data output) after customising its interfaces to his needs.

A standard GPS library is available from ST. By combining the ARM7TDMI microcontroller core with on-chip Flash/RAM, 16-channel GPS correlator DSP, RF Front-end and an extensive range of interfaces on single package solution, the STA8058 provides a highly-flexible and cost-effective solution for GPS applications.

Table 1. Device summary

Order Code	Package	Packing	Automotive Grade
STA8058	LFBGA104 (7x11x1.4mm)	Tray	No
STA8058TR	LFBGA104 (7x11x1.4mm)	Tape and reel	No
STA8058A	LFBGA104 (7x11x1.4mm)	Tray	Yes
STA8058ATR	LFBGA104 (7x11x1.4mm)	Tape and reel	Yes

Contents

1 Features summary

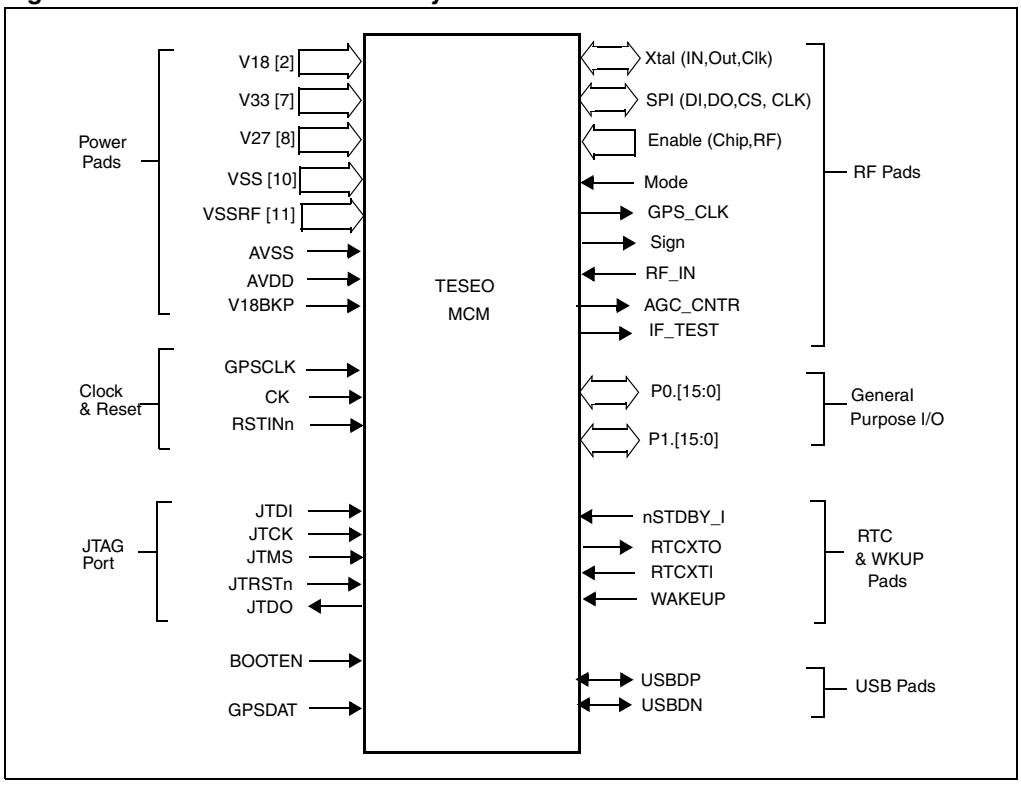
- ARM7TDMI 16/32 bit RISC CPU based host microcontroller running at a frequency up to 66 MHz.
- Complete Embedded Memory System:
  - Flash 256 Kbytes + 16 Kbytes (100 KB erasing/programming cycles)
  - RAM 64 Kbytes.
- 16 channel High performance GPS correlation DSP.
- ST propietary technology:
  - CMOS Flash embedded technology for baseband
  - BiCMOS Sige for radio front-end
- SBAS (WAAS and EGNOS) supported.
- -40 °C to 85 °C operating temperature range.
- 104-pin LFBGA104 package.
- Power supply:
  - 3.0 V to 3.6 V operating supply range for input/output periphery
  - 3.0 V to 3.6 V operating supply range for A/D converter reference
  - 1.8 V operating supply range for core supply provided by internal voltage regulator with external stabilization capacitor or by external supply voltage
  - 2.4 V to 3 V operating supply range for RF front-end section
- Reset and clock control unit able to provide low power modes (WAIT, SLOW, STOP, Standby) and to generate the internal clock from the external reference through integrated PLL.
- 32 programmable general purpose I/O, each pin programmable independently as digital input or digital output; 30 are multiplexed with peripheral functions; 16 can generate an interrupt on input level/transition.
- Real time clock module with 32 kHz low power oscillator and separate power supply to continue running during stand-by mode.
- 16-bit Watchdog timer with 8 bits prescaler for system reliability and integrity.
- One CAN module compliant with the CAN specification V2.0 part B (active) and bit rate can be programmed up to 1 MBaud.
- Four 16-bit programmable timers with 7 bit prescaler, up to two input capture/output compare, one pulse counter function, one PWM channel with selectable frequency each.
- 4 channels 12-bit sigma-delta analog to digital converter, single channel or multi channel conversion modes, single-shot or continuous conversion modes, sample rate 1 kHz, conversion range 0-2.5V .
- Three serial communication interfaces (UART) allow full duplex, asynchronous, communications with external devices, independently programmable TX and RX baud rates up to 625K baud.
- One UART adapted to suit smart card interface needs, for asynchronous SC as defined by ISO 7816-3. It includes SC clock generation.
- Two serial peripheral interfaces (SPI) allow full duplex, synchronous communications with external devices, master or slave operation, max baud rate of 5.5Mb/s. One SPI may be used as multimedia card interface.

- Two I^2C interfaces provide multi-master and slave functions, support normal and fast I^2C mode (400 KHz), 7/10 bit addressing modes. One I^2C Interface is multiplexed with one SPI, so either 2 x SPI + 1 x I^2C or 1 x SPI + 2 x I^2C may be used at a time.
- Enhanced interrupt controller supports 32 interrupt vectors, independently maskable, with interrupt vector table for faster response and 16 priority levels, software programmable for each source. Up to 2 maskable interrupts may be mapped on FIQ.
- Wake-up unit allows exiting from powerdown modes by detection of an event on two external pins (one is active high and other is active low) or on internal Real Time Clock alarm.
- USB unit V1.1 compliant, software configurable endpoint setting, USB suspend/resume support
- High level data link controller (HDLC) unit supports full duplex operating mode, NRZ, NRZI, FM0 and MANCHESTER modes, and internal 8-bit Baud Rate Generator.
- RF front-end features:
  - LOW IF (4 MHz) architecture
  - Compatible with GPS L1 signal
  - VGA gain internally regulated
  - On chip programmable PLL
  - SPI interface

2 Pin description

2.1 Logic symbol

Figure 1. STA8058 TESEO MCM symbol



2.2 System block diagram

Figure 2. STA8058 TESEO baseband block diagram

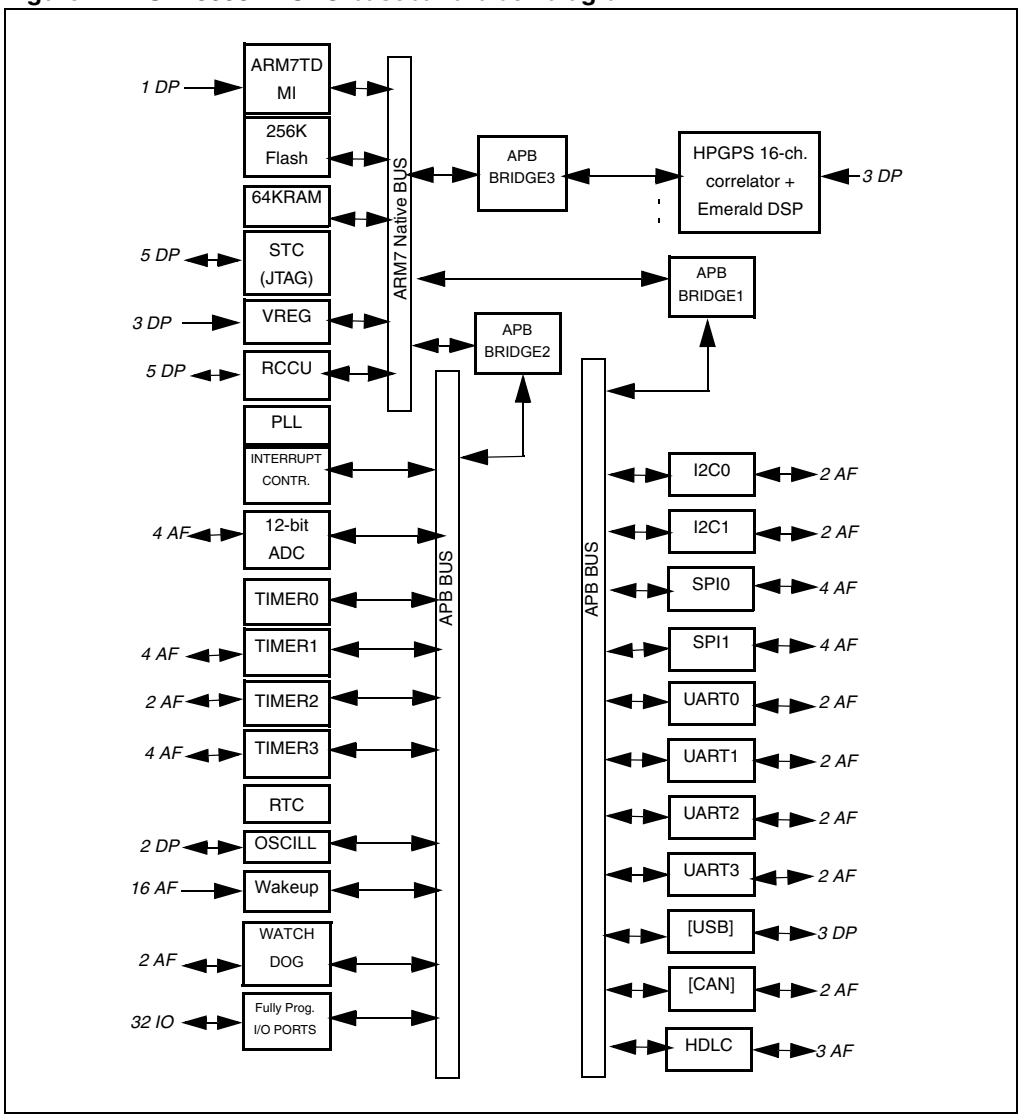


Figure 3. STA5620 RF front-end

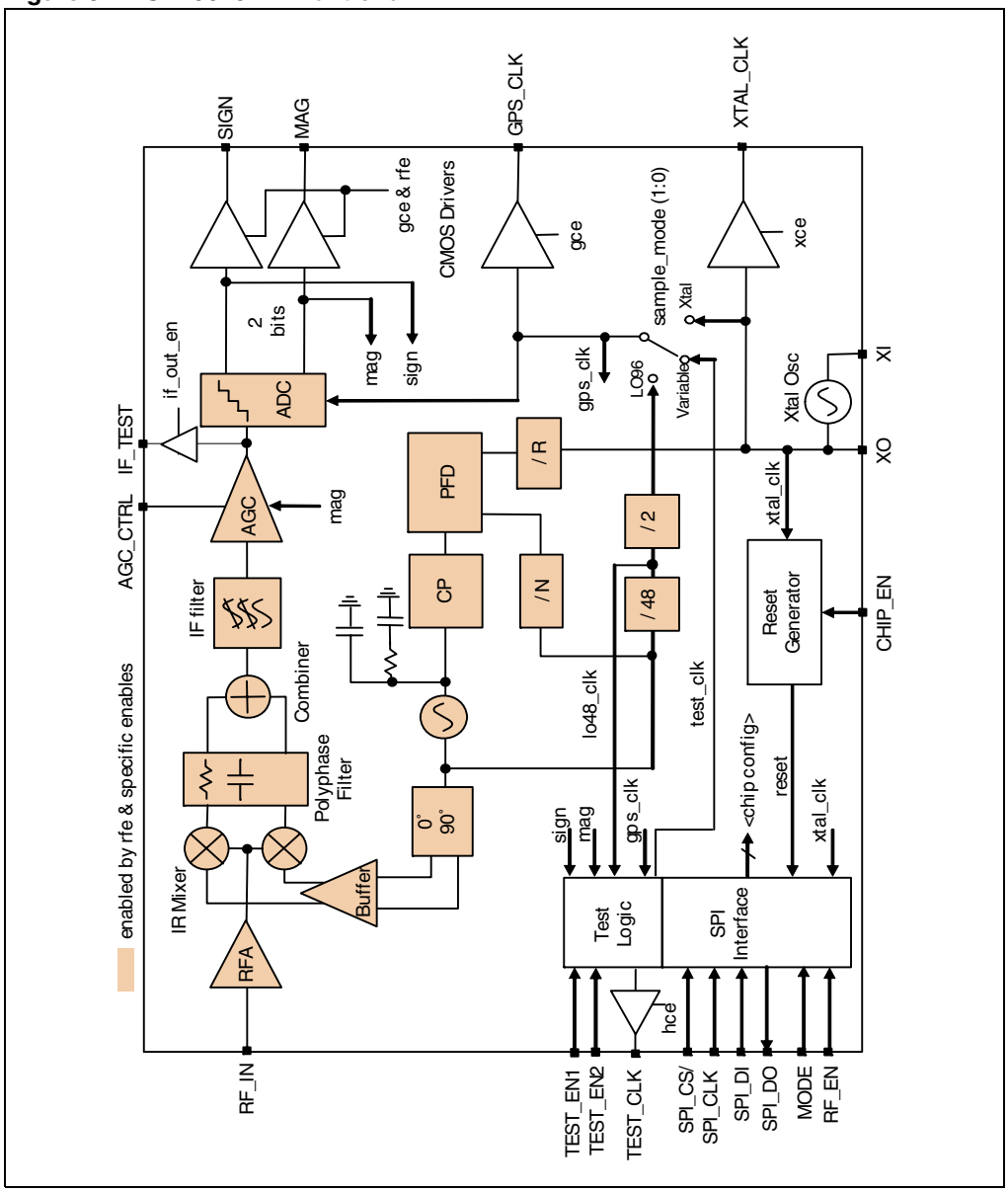
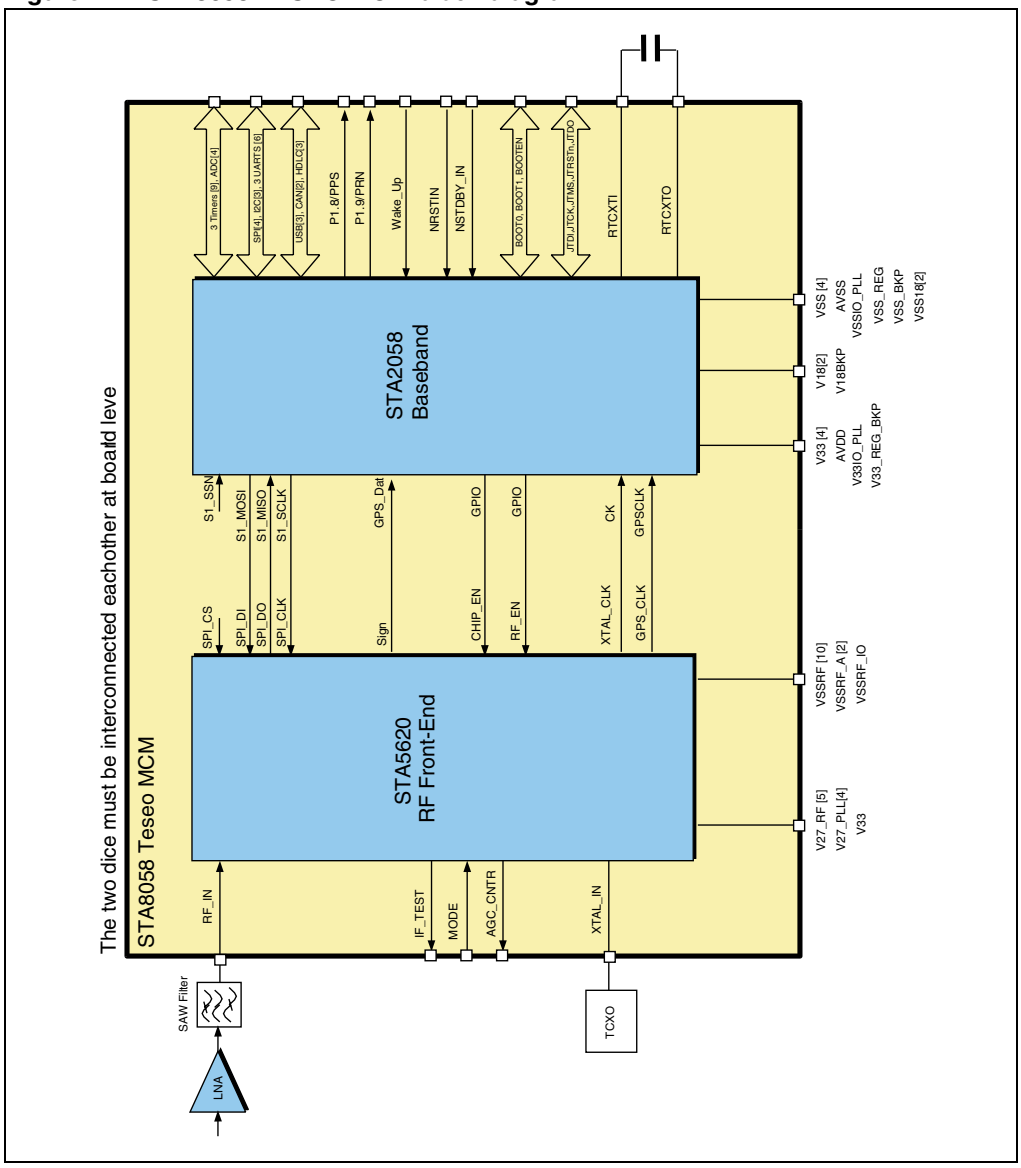


Figure 4. STA8058 TESEO MCM block diagram



2.3 LFBGA104 ball out

Table 2. Ball out for LFBGA104 package

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	VSS	AVSS	AVDD	V18BKP	RTCXTO	RTCXTI	V33REG_BKP	GPSDAT	nJTRST	RF_EN	XTAL_OUT	XTAL_IN	VSSRF
B	P1.2/T3_OCMPA/AIN.2	VSS18	V18	VSSBKP	NSTDBY_IN	V33	VSSREG	GPSCLK	GPS_CLK	CHIP_EN	V27PLL	V27PLL	V27PLL
C	P1.1/T3_ICAPA/AIN.1	P1.0/T3_OCMPB/AIN.0	P1.4/T1_ICAPA	P1.5/T1_ICAPB	NRSTIN	PO.15/WAKEUP	CK	P0.5/S1_MOSI	SPI_DI	XTAL_CLK	VSSRF	V27PLL	V27RF
D	V33IO_PLL	P1.3/T3_ICAPB/AIN.3	P1.7/T1_OCMPA	VSS	VSS	JTCK	JTDO	P0.6/S1_SCLK	SPI_CLK	MODE	VSSRF	VSSRF	VSSRF_A
E	VSSIO_PLL	P1.8/PPS	P1.9/PRN.11	P1.6/T1_OCMPB	VSS18	P0.13/U2_RX/T2.OCMPA	JTMS	JTDI	SPI_CS	IF_TEST	VSSRF	VSSRF	RF_IN
F	P1.11/CANRX	USBDP	P1.10/USBCLK	P0.3/SO_SSN/I1.SDA	V18	P0.14/U2_TX/T2.ICAPA	V33	P0.4/S1_MISO	SPI_DO	AGC_CNTR	VSSRF	VSSRF	VSSRF_A
G	P1.12/CANTX	USBDN	P0.1/SO_MOSI/U3.RX	P0.0/SO_MISO/U3.TX	P0.7/S1_SSN	P0.9/UO_TX/BOOT.0	P0.11/U1_TX/BOOT.1	BOOTEN	SIGN	V27RF	V27RF	V27RF	VSSRF
H	VSS	P1.13/HCLK/IO.SCL	P1.14/HRXD/IO.SDA	P1.15/HTXD	P0.2/SO_SCLK/I1.SCL	PO.12/SCCLK	PO.8/UO_RX/U0.TX	P0.10/U1_RX/U1.TX	V33	VSSRF:IO	V33	V27RF	VSSRF

2.4 Power supply pins

Table 3. Power supply pins

Symbol	I/O	Function	LFBGA104
V_{33}	-	Digital supply voltage for I/O circuitry (3.3 Volt)	B6,F7,G10,H9,H11
V_{SS}	-	Digital ground for I/O circuitry	A1,D4,D5,H1
$V_{33IO-PLL}$	-	Digital supply voltage for I/O circuitry and for PLL reference (3.3V)	D1
$V_{SSIO-PLL}$	-	Digital ground for I/O circuitry and for PLL reference	E1
V_{33REG_BKP}	-	Digital supply voltage for backup block I/O circuitry and for Ballast I/O (3.3V)	A7
V_{SSREG}	-	Digital ground for Ballast I/O	B7
V_{18}	-	Digital supply voltage for core circuitry (1.8 Volt): When using the internal voltage regulator, this pin shall not be driven by an external voltage supply, but a capacitance of at least 10µF (Tantalum, low series resistance) + 33nF (ceramic) shall be connected between these pins and V_{SS18} to guarantee on-chip voltage stability.	B3,F5
V_{SS18}	-	Digital ground for core circuitry	B2,E5
V_{18BKP}	-	Digital supply voltage for backup block (RTC, oscillator, Wake-up controller - 1.8 Volt): when using the internal voltage regulator, this pin shall not be driven by an external voltage supply, but a capacitance of at least 1µF shall be connected between this pin and V_{SSBKP} to guarantee on-chip voltage stability.	A4

Table 3. Power supply pins (continued)

Symbol	I/O	Function	LFBGA104
V_{SSBKP}	-	Digital ground for backup logic	B4
AV_{DD}	-	Analog supply voltage for the A/D converter	A3
AV_{SS}	-	Analog supply ground for the A/D converter	A2
V_{27RF}	-	Analog supply voltage for RF chain (2.7V)	C13,G10,G11,G12,H12
V_{27PLL}	-	Analog supply voltage for PLL embedded into RF part (2.7V)	B11,B12,B13,C12
V_{SSRF}	-	Analog supply ground for RF core	A13,C11,D11,D13, E11,E12,F11,F12, G13,H13
V_{SSRF_A}	-	Analog supply ground for RF amplifier	D13, F13
V_{SSRF_IO}	-	Analog supply ground for RF IO circuirty	H10

Note: V_{33} and $V_{33IO\text{-}PLL}$ are all internally connected. Same for V_{SS} and $V_{SSIO\text{-}PLL}$.

All V_{SS}, V_{SS18}, V_{SSBKP}, AV_{SS}, V_{SSRF}, V_{SSRF_A} and V_{SSRF_IO} pins must be tied together to the common ground plane, taking care of noise filtering, especially on AV_{SS}, V_{SSRF}, V_{SSRF_A} and V_{SSRF_IO}

3 Electrical characteristics

See STA2058 (Teseo Baseband) and STA5620 (RF Front-end) datasheet for related data.

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

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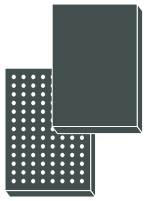
Figure 5. LFBGA104 (11x7x1.4mm) mechanical data and package dimensions

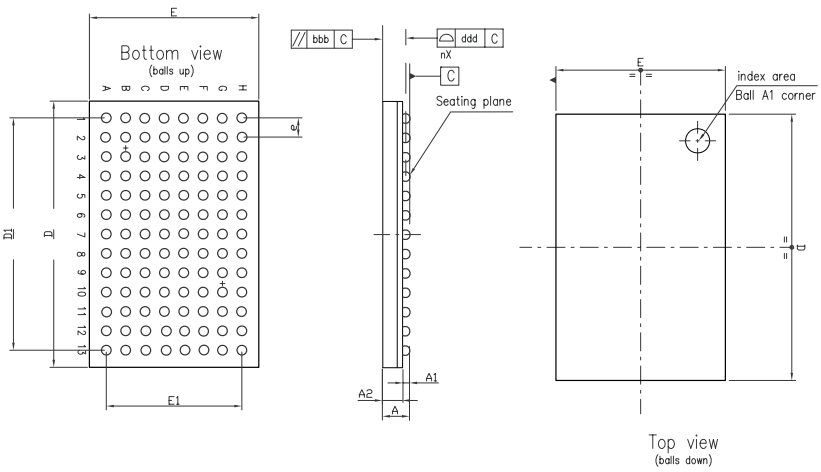
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.400			0.0551
A1	0.210			0.0083		
A2		0.990			0.0390	
A3		0.200			0.0079	
A4			0.800			0.0315
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	10.900	11.000	11.100	0.4291	0.4331	0.4370
D1		9.600			0.3780	
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
E1		5.600			0.2205	
e		0.800			0.0315	
F		0.700			0.0276	
ddd			0.100			0.0039
eee			0.150			0.0059
fff			0.080			0.0031

OUTLINE AND MECHANICAL DATA



Body: 11 x 7 x 1.4mm

LFBGA104
Low profile **F**ine Pitch **B**all **G**rid **A**rray



5 Revision history

Table 4. Document revision history

Date	Revision	Changes
25-Oct-2007	1	Initial release.
19-Mar-2009	2	Updated *Table 1: Device summary on page 1*. Updated ECOPACK description in *Section 4: Package information on page 12*.

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