50 MHz to 2200 MHz Quadrature Modulator

ADL5385

FEATURES

Output frequency range: 50 MHz to 2200 MHz
1 dB output compression: 11 dBm @ 350 MHz
Noise floor: −159 dBm/Hz @ 350 MHz
Sideband suppression: −50 dBc @ 350 MHz
Carrier feedthrough: −46 dBm @ 350 MHz
Single supply: 4.75 V to 5.5 V
24-lead, Pb-free LFCSP_VQ with exposed paddle

APPLICATIONS

Radio-link infrastructure
Cable modem termination systems
Wireless infrastructure systems
Wireless local loop
WiMAX/broadband wireless access systems

FUNCTIONAL BLOCK DIAGRAM

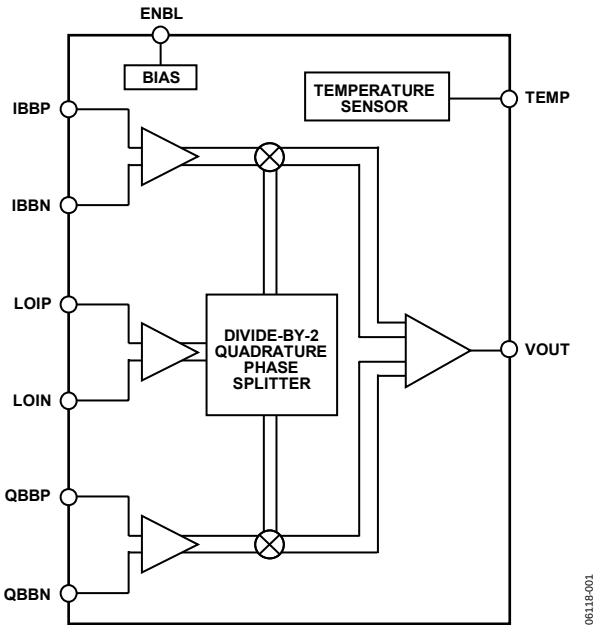

Figure 1.

PRODUCT DESCRIPTION

The ADL5385 is a silicon, monolithic, quadrature modulator designed for use from 50 MHz to 2200 MHz. Its excellent phase accuracy and amplitude balance enable both high performance intermediate frequency (IF) and direct radio frequency (RF) modulation for communication systems.

The AD5385 takes the signals from two differential baseband inputs and modulates them onto two carriers in quadrature with each other. The two internal carriers are derived from a single-ended, external local oscillator input signal at twice the frequency as the desired carrier output. The two modulated signals are summed together in a differential-to-single-ended amplifier designed to drive 50 Ω loads.

The ADL5385 can be used as either an IF or a direct-to-RF modulator in digital communication systems. The wide baseband input bandwidth allows for either baseband drive or drive from a complex IF. Typical applications are in radio-link transmitters, cable modem termination systems, and broadband wireless access systems.

The ADL5385 is fabricated using the Analog Devices, Inc., advanced silicon germanium bipolar process and is packaged in a 24-lead, Pb-free LFCSP_VQ with exposed paddle. Performance is specified over −40°C to +85°C. A Pb-free evaluation board is also available.

Rev. 0

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REVISION HISTORY

10/06—Revision 0: Initial Version

SPECIFICATIONS

Unless otherwise noted, V_S = 5 V; T_A = 25°C; LO = −7 dBm; I/Q inputs = 1.4 V p-p differential sine waves in quadrature on a 500 mV dc bias; baseband frequency = 1 MHz; LO source and RF output load impedances are 50 Ω.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OUTPUT FREQUENCY RANGE		50		2200	MHz
EXTERNAL LO FREQUENCY RANGE	External LO frequency is twice output frequency	100		4400	MHz
OUTPUT FREQUENCY = 50 MHz					
Output Power	Single (lower) sideband output	4	5.6	8	dBm
Output P1 dB			11		dBm
Carrier Feedthrough	Unadjusted (nominal drive level)		−57		dBm
	@ +85°C after optimization at +25°C		−67		dBm
	@ −40°C after optimization at +25°C		−67		dBm
Sideband Suppression	Unadjusted (nominal drive level)		−57		dBc
	@ +85°C after optimization at +25°C		−64		dBc
	@ −40°C after optimization at +25°C		−68		dBc
Second Baseband Harmonic	(F_{LO} − (2 × F_{BB})), P_{OUT} = 5 dBm		−83		dBc
Third Baseband Harmonic	(F_{LO} + (3 × F_{BB})), P_{OUT} = 5 dBm		−58		dBc
Output IP2	F1 = +3.5 MHz, F2 = +4.5 MHz, P_{OUT} = −3 dBm per tone		69		dBm
Output IP3	F1 = +3.5 MHz, F2 = +4.5 MHz, P_{OUT} = −3 dBm per tone		26		dBm
Quadrature Phase Error			−0.17		degrees
I/Q Amplitude Balance			−0.03		dB
Noise Floor	20 MHz offset from LO, all BB inputs at a bias of 500 mV		−155		dBm/Hz
	20 MHz offset from LO, output power = −5 dBm		−150		dBm/Hz
Output Return Loss			−19		dB
OUTPUT FREQUENCY = 140 MHz					
Output Power	Single (lower) sideband output		5.7		dBm
Output P1 dB			11		dBm
Carrier Feedthrough	Unadjusted (nominal drive level)		−52		dBm
	@ +85°C after optimization at +25°C		−66		dBm
	@ −40°C after optimization at +25°C		−67		dBm
Sideband Suppression	Unadjusted (nominal drive level)		−53		dBc
	@ +85°C after optimization at +25°C		−63		dBc
	@ −40°C after optimization at +25°C		−68		dBc
Second Baseband Harmonic	(F_{LO} − (2 × F_{BB})), P_{OUT} = 5 dBm		−83		dBc
Third Baseband Harmonic	(F_{LO} + (3 × F_{BB})), P_{OUT} = 5 dBm		−57		dBc
Output IP2	F1 = +3.5 MHz, F2 = +4.5 MHz, P_{OUT} = −3 dBm per tone		70		dBm
Output IP3	F1 = +3.5 MHz, F2 = +4.5 MHz, P_{OUT} =−3 dBm per tone		26		dBm
Quadrature Phase Error			−0.33		degrees
I/Q Amplitude Balance			−0.03		dB
Noise Floor	20 MHz offset from LO, all BB inputs at a bias of 500 mV		−160		dBm/Hz
Output Return Loss			−20		dB
OUTPUT FREQUENCY = 350 MHz					
Output Power	Single (lower) sideband output	3	5.6	7	dBm
Output P1 dB			11		dBm
Carrier Feedthrough	Unadjusted (nominal drive level)		−46		dBm
	@ +85°C after optimization at +25°C		−65		dBm
	@ −40°C after optimization at +25°C		−66		dBm
Sideband Suppression	Unadjusted (nominal drive level)		−50		dBc
	@ +85°C after optimization at +25°C		−63		dBc
	@ −40°C after optimization at+25°C		−61		dBc

Parameter	Conditions	Min	Typ	Max	Unit
Second Baseband Harmonic	(F_{LO} − (2 × F_{BB})), P_{OUT} = 5 dBm		−80		dBc
Third Baseband Harmonic	(F_{LO} + (3 × F_{BB})), P_{OUT} = 5 dBm		−53		dBc
Output IP2	F1 = 3.5 MHz, F2 = 4.5 MHz, P_{OUT} = −3 dBm per tone		71		dBm
Output IP3	F1 = 3.5 MHz, F2 = 4.5 MHz, P_{OUT} = −3 dBm per tone		26		dBm
Quadrature Phase Error			0.39		degrees
I/Q Amplitude Balance			−0.03		dB
Noise Floor	20 MHz offset from LO, all BB inputs at a bias of 500 mV		−159		dBm/Hz
	20 MHz offset from LO, output power = −5 dBm		−157		dBm/Hz
Output Return Loss			−21		dB
OUTPUT FREQUENCY = 860 MHz					
Output Power	Single (lower) sideband output	2.5	5.3	6.5	dBm
Output P1 dB			11		dBm
Carrier Feedthrough	Unadjusted (nominal drive level)		−41	−35	dBm
	@ +85°C after optimization at +25°C		−63		dBm
	@ −40°C after optimization at +25°C		−65		dBm
Sideband Suppression	Unadjusted (nominal drive level)		−41	−35	dBc
	@ +85°C after optimization at +25°C		−58		dBc
	@ −40°C after optimization at +25°C		−59		dBc
Second Baseband Harmonic	(F_{LO} − (2 × F_{BB})), P_{OUT} = 5 dBm		−73	−57	dBc
Third Baseband Harmonic	(F_{LO} + (3 × F_{BB})), P_{OUT} = 5 dBm		−50	−45	dBc
Output IP2	F1 = +3.5 MHz, F2 = +4.5 MHz, P_{OUT} = −3 dBm per tone		70		dBm
Output IP3	F1 = +3.5 MHz, F2 = +4.5 MHz, P_{OUT} = −3 dBm per tone		25		dBm
Quadrature Phase Error			0.67		degrees
I/Q Amplitude Balance			−0.03		dB
Noise Floor	20 MHz offset from LO, all BB inputs at a bias of 500 mV		−159		dBm/Hz
	20 MHz offset from LO, output power = −5 dBm		−157		dBm/Hz
Output Return Loss			−19		dB
OUTPUT FREQUENCY = 1450 MHz					
Output Power	Single (lower) sideband output		4.4		dBm
Output P1 dB			10		dBm
Carrier Feedthrough	Unadjusted (nominal drive level)		−36		dBm
	@ +85°C after optimization at +25°C		−50		dBm
	@ −40°C after optimization at +25°C		−50		dBm
Sideband Suppression	Unadjusted (nominal drive level)		−44		dBc
	@ +85°C after optimization at +25°C		−61		dBc
	@ −40°C after optimization at +25°C		−51		dBc
Second Baseband Harmonic	(F_{LO} − (2 × F_{BB})), P_{OUT} = 4 dBm		−64		dBc
Third Baseband Harmonic	(F_{LO} + (3 × F_{BB})), P_{OUT} = 4 dBm		−52		dBc
Output IP2	F1 = 3.5 MHz, F2 = 4.5 MHz, P_{OUT} = −3 dBm per tone		63		dBm
Output IP3	F1 = 3.5 MHz, F2 = 4.5 MHz, P_{OUT} = −3 dBm per tone		24		dBm
Quadrature Phase Error			0.42		degrees
I/Q Amplitude Balance			−0.02		dB
Noise Floor	20 MHz offset from LO, all BB inputs at a bias of 500 mV		−160		dBm/Hz
Output Return Loss			−33		dB
OUTPUT FREQUENCY = 1900 MHz					
Output Power	Single (lower) sideband output		3.4		dBm
Output P1 dB			9		dBm
Carrier Feedthrough	Unadjusted (nominal drive level)		−35		dBm
	@ +85°C after optimization at +25°C		−51		dBm
	@ −40°C after optimization at +25°C		−51		dBm
Sideband Suppression	Unadjusted (nominal drive level)		−33		dBc

Parameter	Conditions	Min	Typ	Max	Unit
	@ +85°C after optimization at +25°C		−43		dBc
	@ −40°C after optimization at +25°C		−47		dBc
Second Baseband Harmonic	(F_{LO} − (2 × F_{BB})), P_{OUT} = 3 dBm		−58		dBc
Third Baseband Harmonic	(F_{LO} + (3 × F_{BB})), P_{OUT} = 3 dBm		−47		dBc
Output IP2	F1 = +3.5 MHz, F2 = +4.5 MHz, P_{OUT} = −3 dBm per tone		57		dBm
Output IP3	F1 = +3.5 MHz, F2 = +4.5 MHz, P_{OUT} = −3 dBm per tone		22		dBm
Quadrature Phase Error			2.6		degrees
I/Q Amplitude Balance			0.003		dB
Noise Floor	20 MHz offset from LO, all BB inputs at a bias of 500 mV		−160		dBm/Hz
	20 MHz offset from LO, output power = −5 dBm		−156		dBm/Hz
Output Return Loss			−20		dB
OUTPUT FREQUENCY = 2150 MHz					
Output Power	Single (lower) sideband output		2.6		dBm
Output P1 dB			8		dBm
Carrier Feedthrough	Unadjusted (nominal drive level)		−36		dBm
	@ +85°C after optimization at +25°C		−47		dBm
	@ −40°C after optimization at +25°C		−48		dBm
Sideband Suppression	Unadjusted (nominal drive level)		−37		dBc
Second Baseband Harmonic	(F_{LO} − (2 × F_{BB})), P_{OUT} = 2.6 dBm		−56		dBc
Third Baseband Harmonic	(F_{LO} + (3 × F_{BB})), P_{OUT} = 2.6 dBm		−45		dBc
Output IP2	F1 = +3.5 MHz, F2 = +4.5 MHz, P_{OUT} = −3 dBm per tone		54		dBm
Output IP3	F1 = +3.5 MHz, F2 = +4.5 MHz, P_{OUT} = −3 dBm per tone		21		dBm
Quadrature Phase Error			1.5		degrees
I/Q Amplitude Balance			< 0.05		dB
Noise Floor	20 MHz offset from LO, all BB inputs at a bias of 500 mV		−160		dBm/Hz
	20 MHz offset from LO, output power = −5 dBm		−156		dBm/Hz
Output Return Loss			−15		dB
LO INPUTS	Pin LOIP and Pin LOIN				
LO Drive Level	Characterization performed at typical level	−10	−7	+5	dBm
Input Impedance			50		Ω
Input Return Loss	350 MHz, LOIN ac-coupled to ground		−20		dB
BASEBAND INPUTS	Pin IBBP, Pin IBBN, Pin QBBP, Pin QBBN				
I and Q Input Bias Level			500		mV
Input Bias Current			−70		µA
Bandwidth (0.1 dB)	RF = 500 MHz, output power = 0 dBm		80		MHz
Bandwidth (3 dB)	RF = 500 MHz, output power = 0 dBm		>500		MHz
ENABLE INPUT	ENBL				
Turn-On Settling Time	ENBL = high (for output to within 0.5 dB of final value)		1.0		µs
Turn-Off Settling Time	ENBL = low (at supply current falling below 20 mA)		1.4		µs
ENBL High Level (Logic 1)		1.5			V
ENBL Low Level (Logic 0)				0.4	V
TEMPERATURE OUTPUT	TEMP				
Output Voltage	T_A = 27.15°C, 300K, R_L = 1 MΩ (after full warmup)		1.56		V
Temperature Slope	−40°C ≤ T_A ≤ +85°C, R_L = 1 MΩ		4.6		mV/°C
Output Impedance			1.0		kΩ
POWER SUPPLIES	Pin VPS1 and Pin VPS2				
Voltage		4.75		5.5	V
Supply Current	ENBL = high		215	240	mA
	ENBL = low		80		µA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage VPOS	5.5 V
IBBP, IBBN, QBBP, QBBN Range	0 V to 2.0 V
LOIP and LOIN	13 dBm
Internal Power Dissipation	1.375 W
θ_{JA} (Exposed Paddle Soldered Down)	58°C/W
Maximum Junction Temperature	164°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

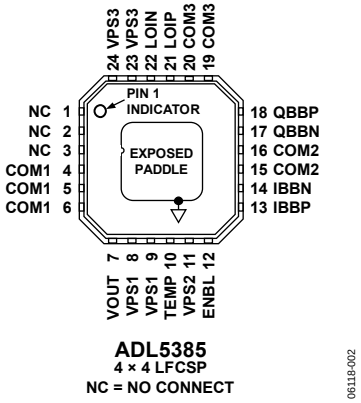


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 3	NC	No Connection. These pins can be left open or tied to ground.
4, 5, 6, 15, 16, 19, 20	COM1, COM2, COM3	Power Supply Common Pins. COM1, COM2, and COM3 must all be connected to a ground plane via a low impedance path.
7	VOUT	Device Output. Single-ended, 50 Ω internally biased RF/IF output; pin must be ac-coupled to the load.
8, 9, 11, 23, 24	VPS1, VPS2, VPS3	Power Supply Pins. Decouple each pin with a 0.1 µF capacitor; Pin 8 and Pin 9 can share a single capacitor, as can Pin 23 and Pin 24. All pins must be connected to the same supply (V_S).
10	TEMP	Temperature Sensor Output. Provides dc voltage proportional to die temperature. Slope is 4.6 mV/°C
12	ENBL	Device Enable. Shuts device down when grounded and enables device when pulled to supply voltage.
13, 14, 17, 18	IBBP, IBBN, QBBN, QBBP	Differential In-Phase and Quadrature Baseband Inputs. These high impedance inputs must be externally dc-biased to 500 mV dc and driven from a low impedance source. Nominal characterized ac signal swing is 700 mV p-p on each pin (150 mV to 850 mV). This results in a differential drive of 1.4 V p-p with a 500 mV dc bias.
21	LOIP	Single-Ended Two-Times Local Oscillator Input. This input is internally biased and must be ac-coupled to the LO source.
22	LOIN	Common for LO Input. Must be ac-coupled to ground through a low impedance path.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, V_S = 5 V; T_A = 25°C; LO = −7 dBm; I/Q inputs = 1.4 V p-p differential sine waves in quadrature on a 500 mV dc bias; baseband frequency = 1 MHz; LO source and RF output load impedances are 50 Ω.

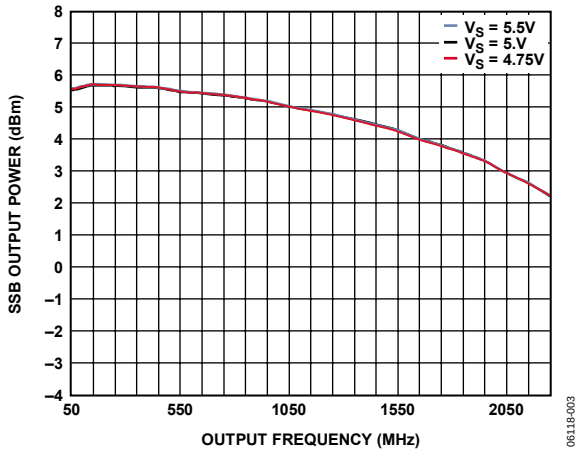


Figure 3. Single Sideband (SSB) Output Power (P_{OUT}) vs. Output Frequency and Power Supply

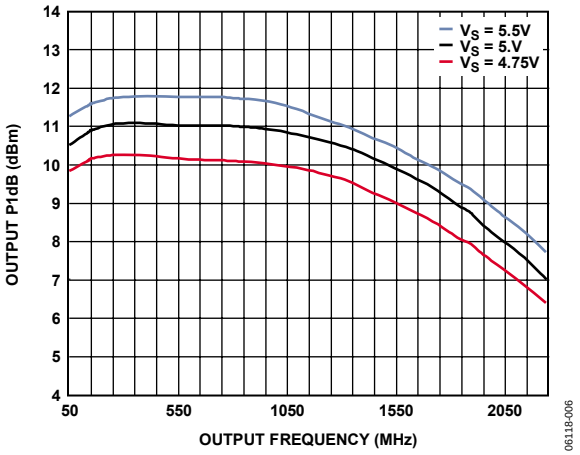


Figure 6. Output 1 dB Compression Point (OP1dB) vs. Output Frequency and Power Supply

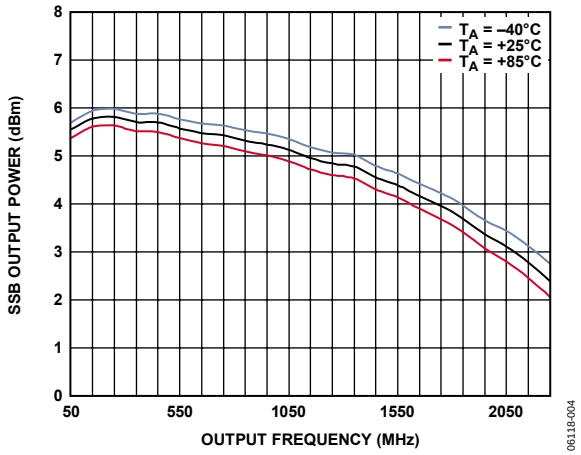


Figure 4. Single Sideband (SSB) Output Power (P_{OUT}) vs. Output Frequency and Temperature

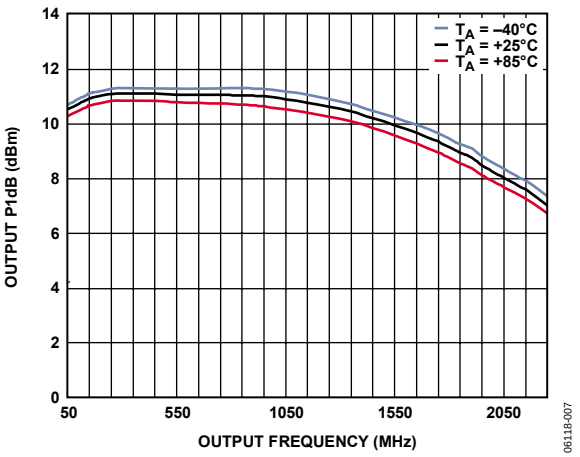


Figure 7. Output 1 dB Compression Point (OP1dB) vs. Output Frequency and Temperature

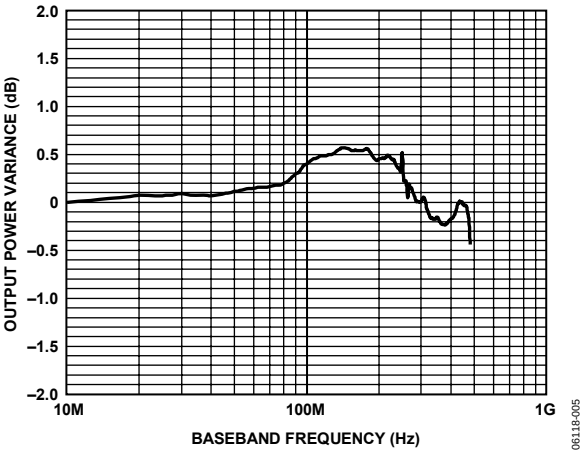


Figure 5. Baseband Frequency Response Normalized to Response for 1 MHz BB Signal; Carrier Frequency = 500 MHz

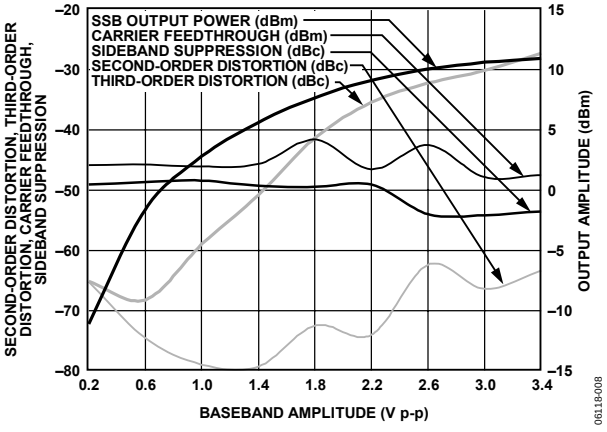


Figure 8. SSB Output Power, Second- and Third-Order Distortion, Carrier Feedthrough and Sideband Suppression vs. Differential Baseband Input Level; Output Frequency = 350 MHz

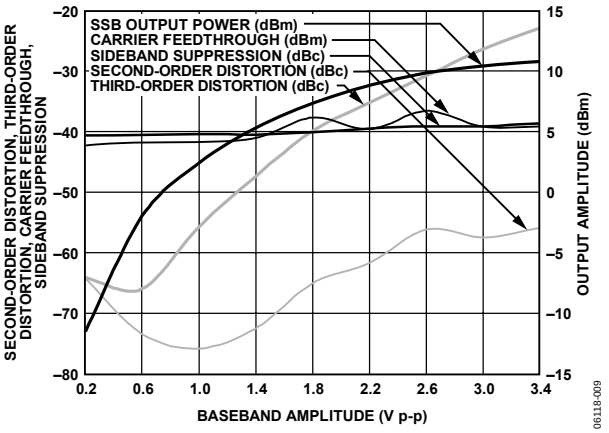


Figure 9. SSB Output Power, Second- and Third-Order Distortion, Carrier Feedthrough and Sideband Suppression vs. Baseband Single-Ended Input Level; Output Frequency = 860 MHz

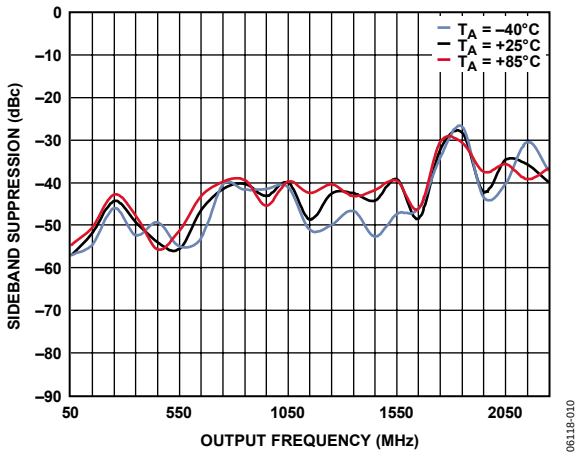


Figure 10. Sideband Suppression vs. Output Frequency and Temperature

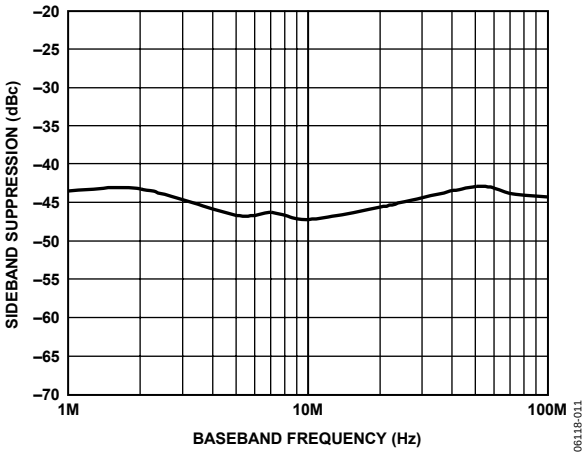


Figure 11. Sideband Suppression vs. Baseband Frequency; Output Frequency = 350 MHz

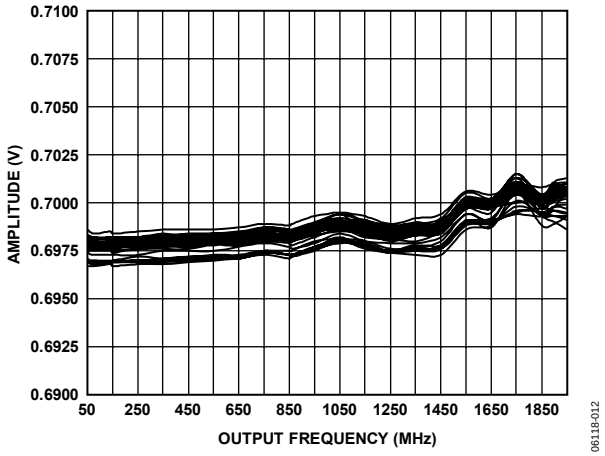


Figure 12. Distribution of Peak Q Amplitude to Null Undesired Sideband (Peak I Amplitude Held Constant at 0.7 V)

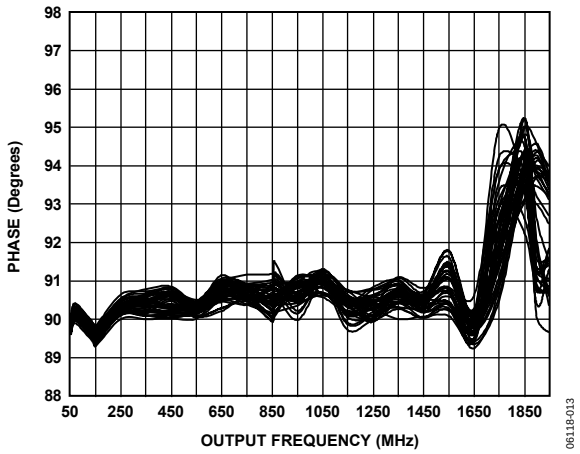


Figure 13. Distribution of IQ Phase to Null Undesired Sideband

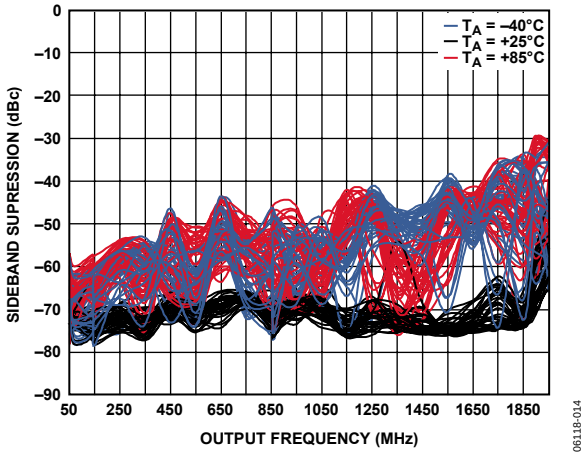


Figure 14. Sideband Suppression Distribution at Temperature Extremes, After Sideband Suppression Nulled to < –50 dBc at T_A = +25°C

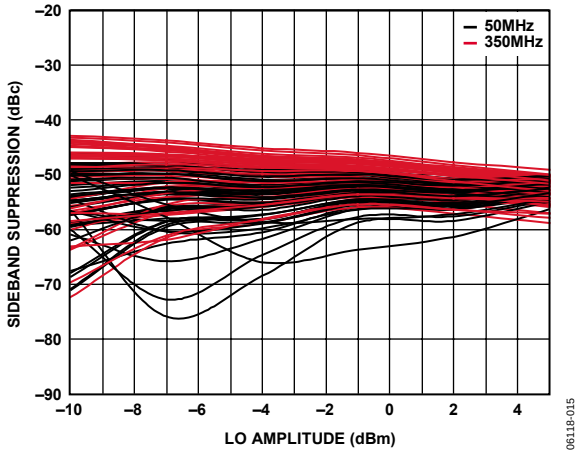


Figure 15. Distribution of Sideband Suppression vs. LO Input Power at 50 MHz and 350 MHz

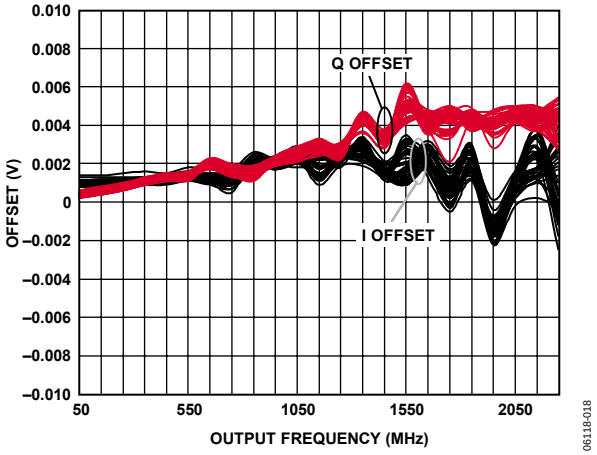


Figure 18. Distribution of I and Q Offset Required to Null Carrier Feedthrough

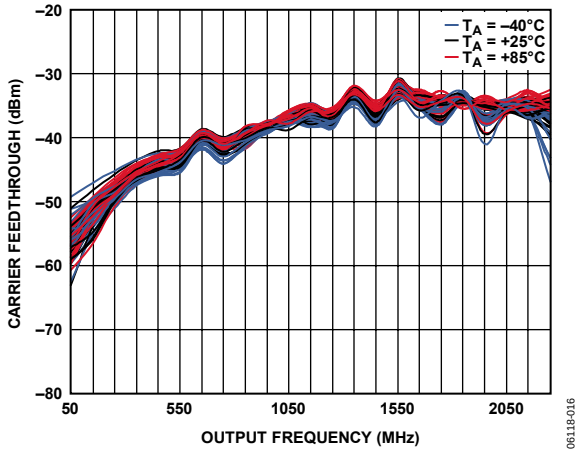


Figure 16. Distribution Carrier Feedthrough vs. Output Frequency and Temperature

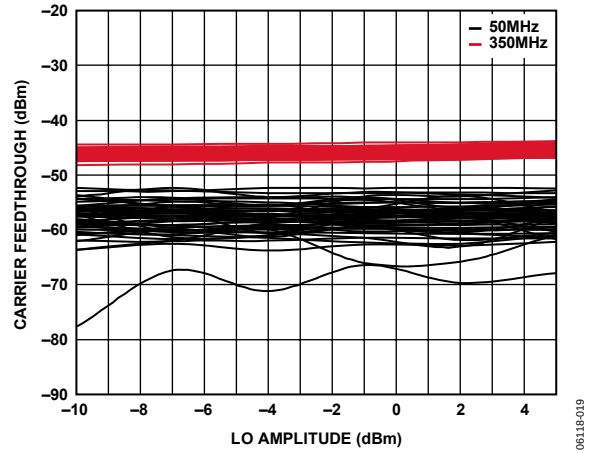


Figure 19. Distribution Carrier Feedthrough vs. LO Input Power at 50 MHz and 350 MHz

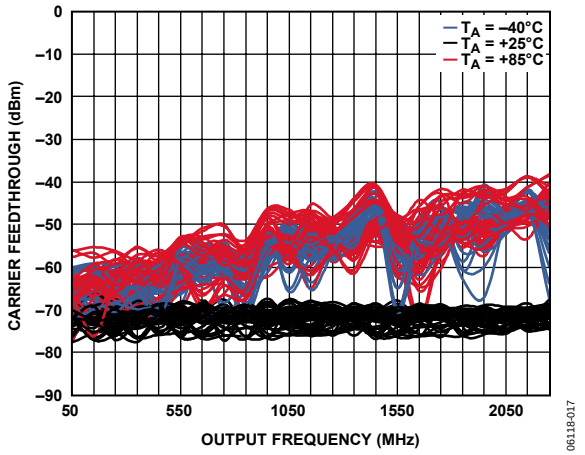


Figure 17. Carrier Feedthrough Distribution at Temperature Extremes, After Nulling to < −65 dBm at T_A = +25°C

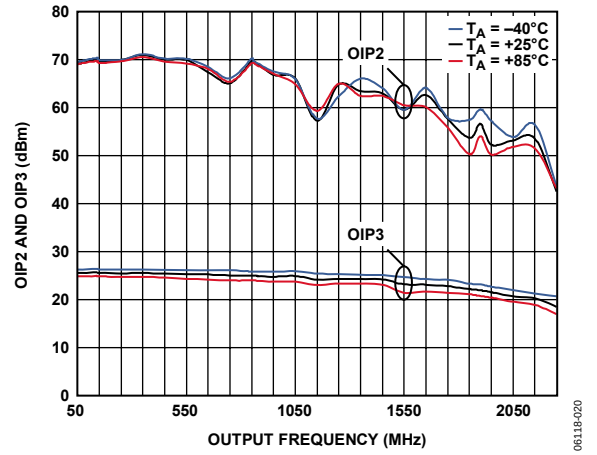


Figure 20. OIP3 and OIP2 vs. Output Frequency and Temperature

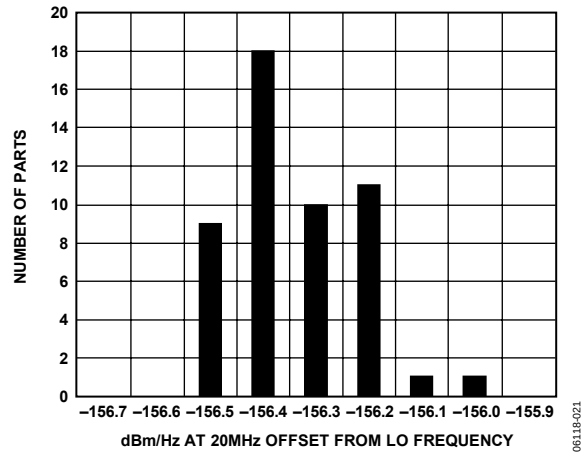


Figure 21. 20 MHz Offset Noise Floor Distribution, Output Frequency = 350 MHz, P_{OUT} = −5 dBm, QPSK Carrier, Symbol Rate = 3.84 MSPS

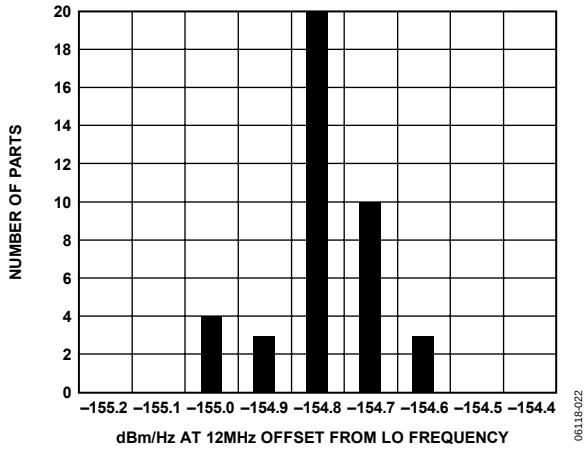


Figure 22. 12 MHz Offset Noise Floor Distribution, Output Frequency = 860 MHz, P_{OUT} = −5 dBm, 64 QAM Carrier, Symbol Rate = 5 MSPS

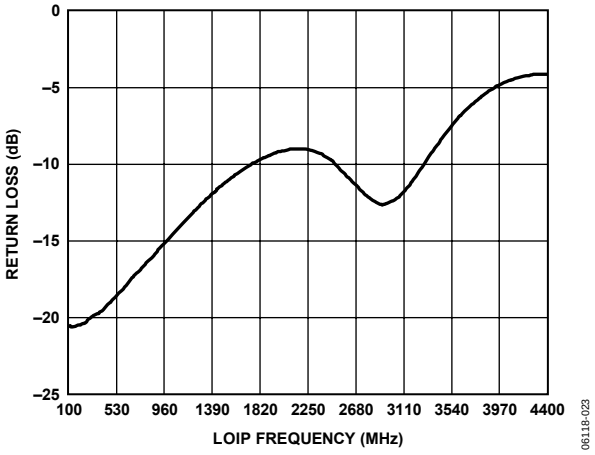


Figure 23. LO Port Input Return Loss vs. Frequency

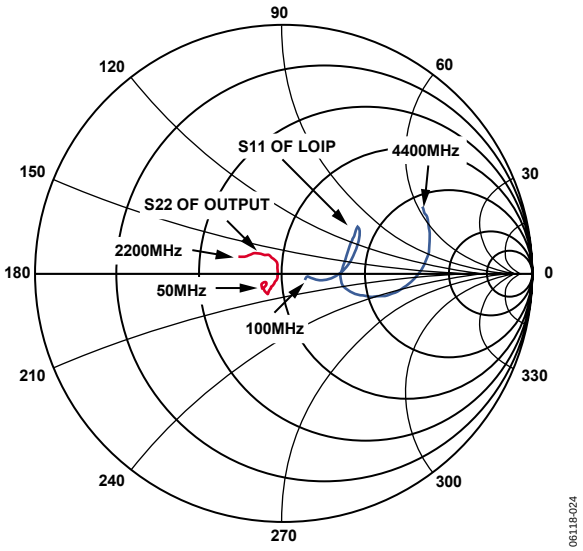


Figure 24. Output Impedance and LO Input Impedance vs. Frequency

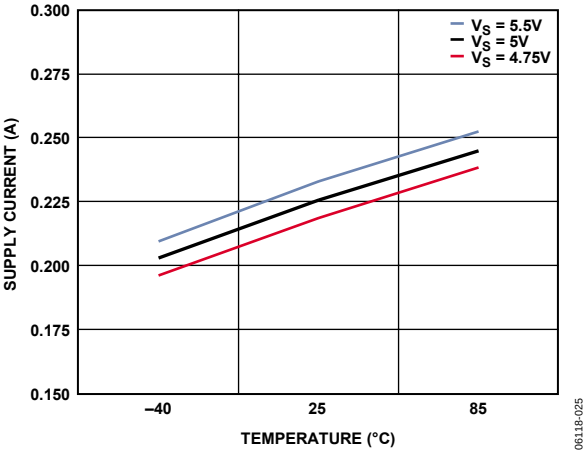


Figure 25. Power Supply Current vs. Temperature and Supply Voltage

CIRCUIT DESCRIPTION

OVERVIEW

The ADL5385 can be divided into five sections: the local oscillator (LO) interface, the baseband voltage-to-current (V-to-I) converter, the mixers, the differential-to-single-ended (D-to-S) amplifier, and the bias circuit. A detailed block diagram of the device is shown in Figure 26.

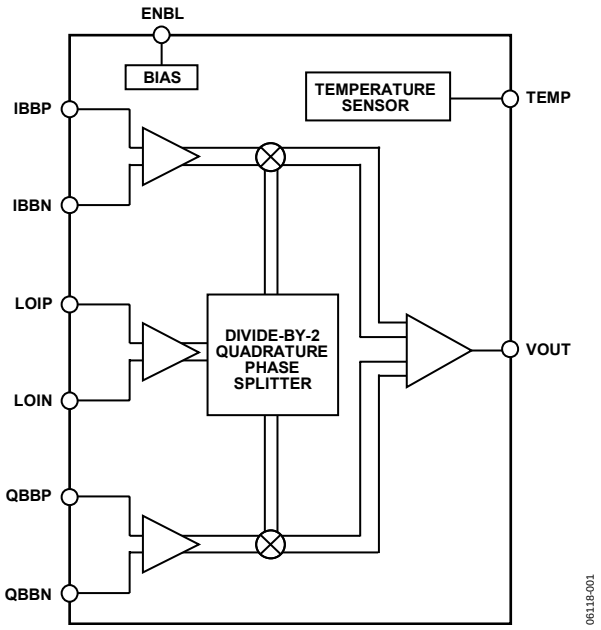


Figure 26. ADL5385 Block Diagram

The LO interface generates two LO signals at 90° of phase difference to drive two mixers in quadrature. Baseband signals are converted into currents by the V-to-I converters that feed into the two mixers. The outputs of the mixers are combined in the differential-to-single-ended amplifier, which provides a 50 Ω output interface. Reference currents to each section are generated by the bias circuit. A detailed description of each section follows.

LO INTERFACE

The LO interface consists of a buffer amplifier followed by a pair of frequency dividers that generate two carriers at half the input frequency and in quadrature with each other. Each carrier is then amplified and amplitude-limited to drive the double-balanced mixers.

V-TO-I CONVERTER

The differential baseband input voltages that are applied to the baseband input pins are fed to a pair of common-emitter, voltage-to-current converters. The output currents then modulate the two half-frequency LO carriers in the mixer stage.

MIXERS

The ADL5385 has two double-balanced mixers: one for the in-phase channel (I channel) and one for the quadrature channel (Q channel). These mixers are based on the Gilbert cell design of four cross-connected transistors. The output currents from the two mixers are summed together in the resistor-inductor (RL) loads in the D-to-S amplifier.

D-TO-S AMPLIFIER

The output D-to-S amplifier consists of two emitter followers driving a totem-pole output stage. Output impedance is established by the emitter resistors in the output transistors. The output of this stage connects to the output (VOUT) pin.

BIAS CIRCUIT

A band gap reference circuit generates the proportional-to-absolute-temperature (PTAT) as well as temperature-independent reference currents used by different sections. The band-gap circuit is turned on by a logic HIGH at the ENBL pin, which in turn powers up the whole device. A PTAT voltage output is available at the TEMP pin, which can be used for temperature monitoring as well as for temperature compensation purposes.

BASIC CONNECTIONS

Figure 27 shows the basic connections for the ADL5385.

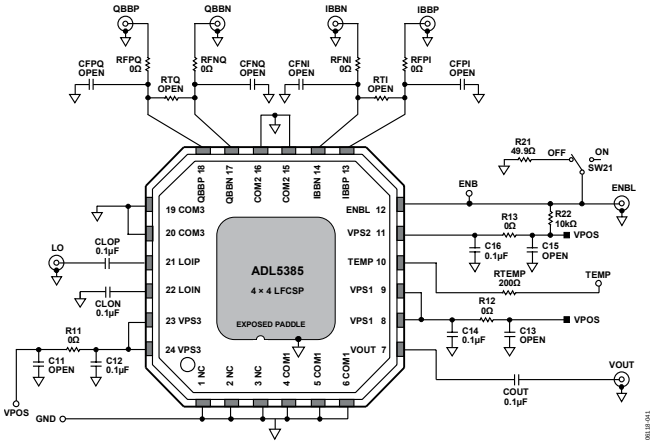


Figure 27. Basic Connections for the ADL5385

Power Supply and Grounding

All the VPS pins must be connected to the same 5 V source. Adjacent pins of the same name can be tied together and decoupled with a 0.1 µF capacitor. These capacitors are located as close as possible to the device. The power supply can range from 4.75 V to 5.5 V.

The COM1 pin, COM2 pin, and COM3 pin are tied to the same ground plane through low impedance paths. The exposed paddle on the underside of the package is also soldered to a low thermal and electrical impedance ground plane. If the ground plane spans multiple layers on the circuit board, they should be stitched together with nine vias under the exposed paddle. The Analog Devices AN-772 application note discusses the thermal and electrical grounding of the LFCSP in greater detail.

Baseband Inputs

The baseband inputs QBBP, QBBN, IBBP, and IBBN must be driven from a differential source. The nominal drive level of 1.4 V p-p differential (700 mV p-p on each pin) is biased to a common-mode level of 500 mV dc.

The dc common-mode bias level for the baseband inputs can range from 400 mV to 600 mV. This results in a reduction in the usable input ac swing range. The nominal dc bias of 500 mV allows for the largest ac swing, limited on the bottom end by the ADL5385 input range and on the top end by the output compliance range on most Analog Devices DACs.

LO Input

A single-ended LO signal is applied to the LOIP pin through an ac coupling capacitor. The recommended LO drive power is −7 dBm. The LO return pin, LOIN, must be ac-coupled to ground though a low impedance path.

The nominal LO drive of −7 dBm can be increased to up to +5 dBm. The effect of LO power on sideband suppression and carrier feedthrough is shown in Figure 15 and Figure 19.

RF Output

The RF output is available at the VOUT pin (Pin 7). This pin must also be ac-coupled. The VOUT pin has a nominal broadband impedance of 50 Ω and does not need further external matching.

OPTIMIZATION

The carrier feedthrough and sideband suppression performance of the ADL5385 can be improved through the use of optimization techniques.

Carrier Feedthrough Nulling

Carrier feedthrough results from minute dc offsets that occur between each of the differential baseband inputs. In an ideal modulator, the quantities ($V_{IOPP} - V_{IOPN}$) and ($V_{QOPP} - V_{QOPN}$) are equal to zero, and this results in no carrier feedthrough. In a real modulator, those two quantities are nonzero and, when mixed with the LO, result in a finite amount of carrier feedthrough. The ADL5385 is designed to provide a minimal amount of carrier feedthrough. If even lower carrier feedthrough levels are required, minor adjustments can be made to the ($V_{IOPP} - V_{IOPN}$) and ($V_{QOPP} - V_{QOPN}$) offsets. The I-channel offset is held constant while the Q-channel offset is varied until a minimum carrier feedthrough level is obtained. The Q-channel offset required to achieve this minimum is held constant while the offset on the I-channel is adjusted, until a better minimum is reached. Through two iterations of this process, the carrier feedthrough can be reduced to as low as the output noise. The ability to null is sometimes limited by the resolution of the offset adjustment. Figure 28 shows the relationship of carrier feedthrough vs. dc offset.

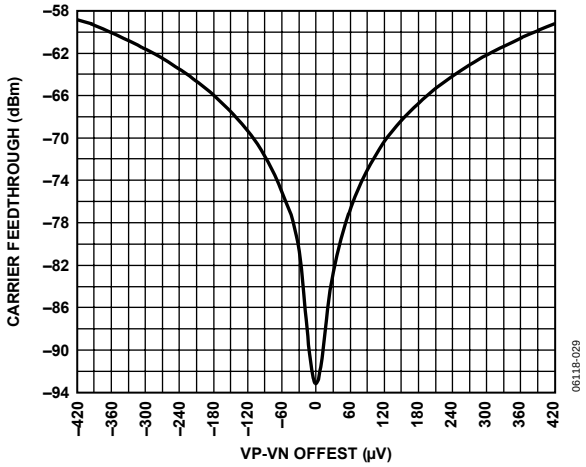


Figure 28. Carrier Feedthrough vs. DC Offset Voltage at 450 MHz

Note that throughout the nulling process, the dc bias for the baseband inputs remains at 500 mV. When no offset is applied,

$V_{IOPP} = V_{IOPN} = 500$ mV, or
$V_{IOPP} - V_{IOPN} = V_{IOS} = 0$ V

When an offset of $+V_{IOS}$ is applied to the I-channel inputs,

V_{IOPP} = 500 mV + V_{IOS}/2, while
V_{IOPN} = 500 mV − V_{IOS}/2, such that
$V_{IOPP} - V_{IOPN} = V_{IOS}$

The same applies to the Q channel.

It is often desirable to perform a one-time carrier null calibration. This is usually performed at a single frequency. Figure 29 shows how carrier feedthrough varies with LO frequency over a range of ±50 MHz on either side of a null at 350 MHz.

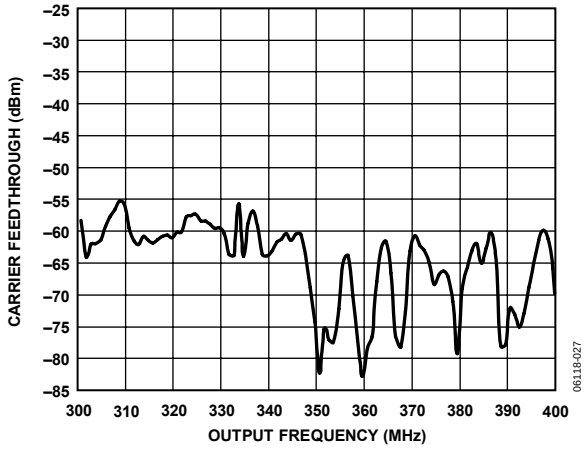


Figure 29. Carrier Feedthrough vs. Frequency After Nulling at 350 MHz

Sideband Suppression Optimization

Sideband suppression results from relative gain and relative phase offsets between the I and Q channels and can be suppressed through adjustments to those two parameters. Figure 30 illustrates how sideband suppression is affected by the gain and phase imbalances.

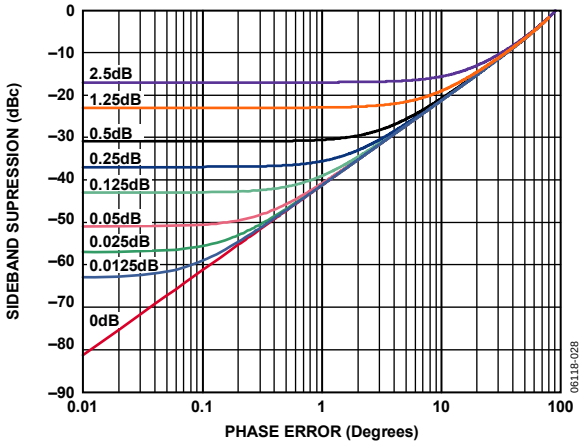


Figure 30. Sideband Suppression vs. Quadrature Phase Error for Various Quadrature Amplitude Offsets

Figure 30 underscores the fact that adjusting one parameter improves the sideband suppression only to a point; the other parameter must also be adjusted. For example, if the amplitude offset is 0.25 dB, improving the phase imbalance better than 1° does not yield any improvement in the sideband suppression. For optimum sideband suppression, an iterative adjustment between phase and amplitude is required.

The sideband suppression nulling can be performed either through adjusting the gain for each channel or through the modification of the phase and gain of the digital data coming from the digital signal processor.

APPLICATIONS

DAC MODULATOR INTERFACING

The ADL5385 is designed to interface with minimal components to members of the Analog Devices family of digital-to-analog converters (DAC). These DACs feature an output current swing from 0 to 20 mA, and the interface described in this section can be used with any DAC that has a similar output.

Driving the ADL5385 with an Analog Devices TxDAC®

An example of the interface using the AD9777 TxDAC is shown in Figure 31. The baseband inputs of the ADL5385 require a dc bias of 500 mV. The average output current on each of the outputs of the AD9777 is 10 mA. Therefore, a single 50 Ω resistor to ground from each of the DAC outputs results in an average current of 10 mA flowing through each of the resistors, thus producing the desired 500 mV dc bias for the inputs to the ADL5385.

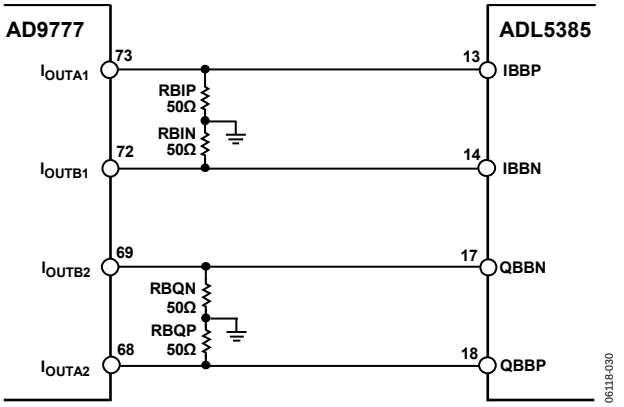


Figure 31. Interface Between AD9777 and ADL5385 with 50 Ω Resistors to Ground to Establish the 500 mV DC Bias for the ADL5385 Baseband Inputs

The AD9777 output currents have a swing that ranges from 0 to 20 mA. With the 50 Ω resistors in place, the ac voltage swing going into the ADL5385 baseband inputs ranges from 0 V to 1 V. A full-scale sine wave out of the AD9777 can be described as a 1 V p-p single-ended (or 2 V p-p differential) sine wave with a 500 mV dc bias.

Limiting the AC Swing

There are situations in which it is desirable to reduce the ac voltage swing for a given DAC output current. This can be achieved through the addition of another resistor to the interface. This resistor is placed in shunt between each side of the differential pair, as illustrated in Figure 32. It has the effect of reducing the ac swing without changing the dc bias already established by the 50 Ω resistors.

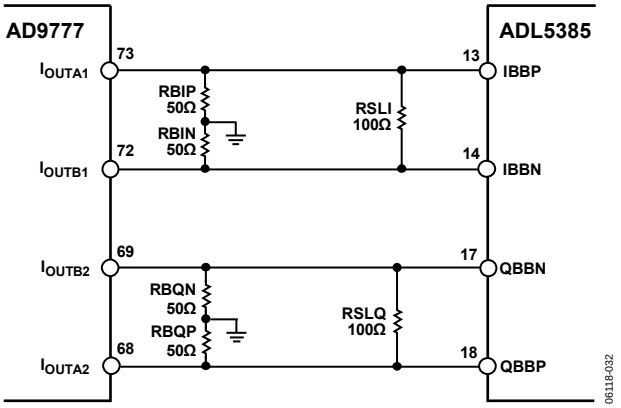


Figure 32. AC Voltage Swing Reduction Through Introduction of Shunt Resistor Between Differential Pair

The value of this ac voltage swing-limiting resistor is chosen based on the desired ac voltage swing. Figure 33 shows the relationship between the swing-limiting resistor and the peak-to-peak ac swing that it produces when 50 Ω bias-setting resistors are used.

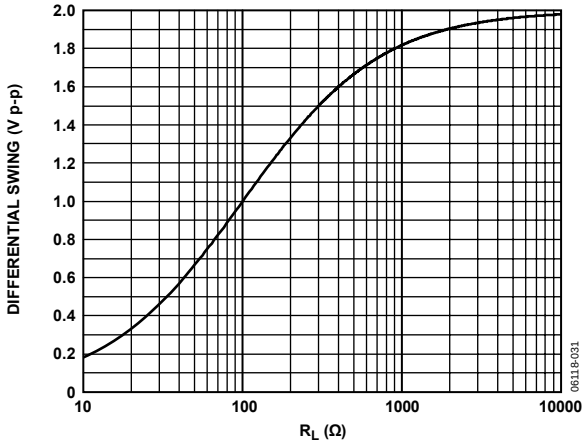


Figure 33. Relationship Between AC Swing-Limiting Resistor and Peak-to-Peak Voltage Swing with 50 Ω Bias-Setting Resistors

Filtering

When driving a modulator from a DAC, it is necessary to introduce a low-pass filter between the DAC and the modulator to reduce the DAC images. The interface for setting up the biasing and ac swing lends itself well to the introduction of such a filter. The filter can be inserted in between the dc bias setting resistors and the ac swing-limiting resistor, thus establishing the input and output impedances for the filter.

Examples of filters are discussed in the 155 MBPS (STM-1) 128 QAM Transmitter and the CMTS Transmitter Application sections.

Using AD9777 Auxiliary DAC for Carrier Feedthrough Nulling

The AD9777 features an auxiliary DAC that can be used to inject small currents into the differential outputs for each channel. The auxiliary DAC can produce the small offset currents necessary to implement the nulling described in the Carrier Feedthrough Nulling section.

155 Mbps (STM-1) 128 QAM TRANSMITTER

Figure 34 shows how the ADL5385 can be interfaced to the AD9777 DAC (or any Analog Devices dual DAC with an output bias level of 0.5 V) to generate a 155 Mbps 128 QAM carrier at 355 MHz. Because the TxDAC output and the IQ modulator inputs operate at the same bias levels of 0.5 V, a simple dc-coupled connection can be implemented without any active or passive level shifting. The bias level and modulator drive level is set by the 50 Ω ground-referenced resistors and the 100 Ω shunt resistors, respectively (see the DAC Modulator Interfacing section). A baseband filter is placed between the bias and signal swing resistors. This 5-pole Chebychev filter with in-band ripple of 0.1 dB has a corner frequency of 39 MHz.

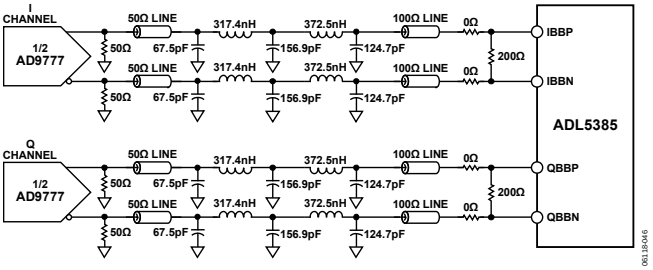


Figure 34. Recommended DAC-Modulator Interconnect for128 QAM Transmitter

Figure 35 shows a spectral plot of the 128 QAM spectrum at a carrier power of −6.3 dBm. Figure 36 shows how EVM (measured with the analyzer's internal equalizer both on and off) and SNR, measured at 55 MHz carrier offset (2.5 times the carrier bandwidth) varies with output power.

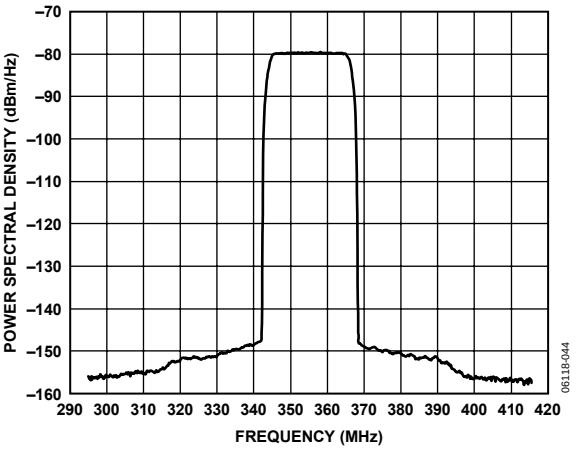


Figure 35. Spectral Plot of 128 QAM Transmitter at −6.3 dBm Output Power

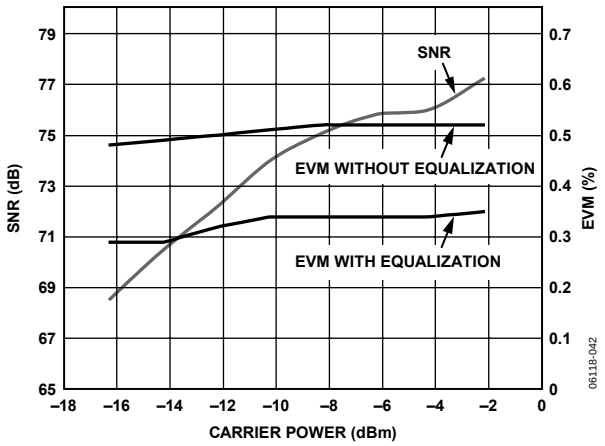


Figure 36. EVM and SNR vs. Output Power for 128 QAM Transmitter Application

CMTS TRANSMITTER APPLICATION

Because of its broadband operating range from 50 MHz to 2200 MHz, the ADL5385 can be used in direct-launch cable modem termination systems (CMTS) applications in the 50 MHz to 860 MHz cable band.

The same DAC and DAC-to-modulator interface and filtering circuit shown in Figure 34 was used in this application. Figure 37 shows a plot of a 4-carrier 256 QAM spectrum at an output frequency of 485 MHz. Figure 38 shows how adjacent channel power (measured at 750 KHz, 5.25 MHz, and 12 MHz offset from the last carrier) and modulation error ratio (MER) vary with carrier power.

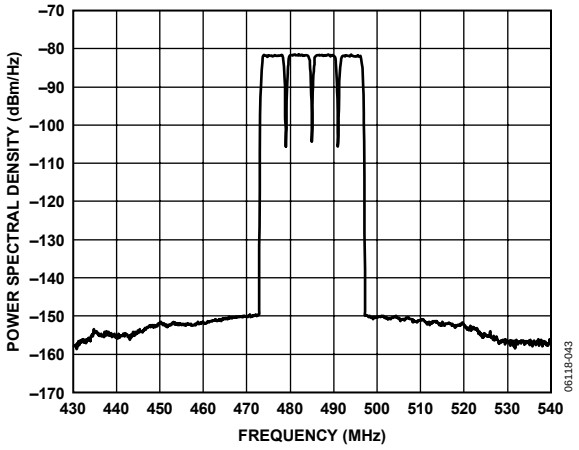


Figure 37. Spectrum of 4-Carrier 256 QAM CMTS Signal at 485 MHz

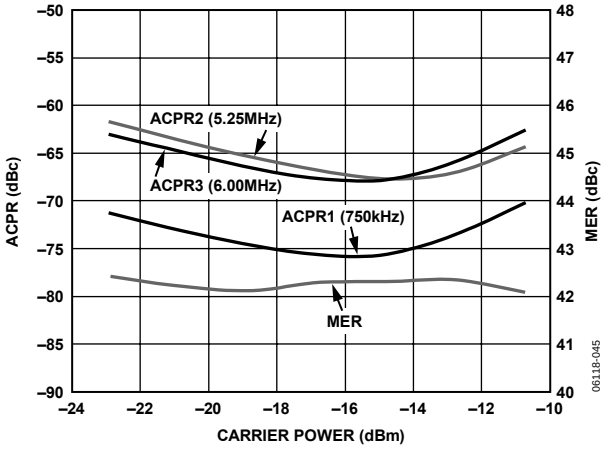


Figure 38. ACP1, ACP2, ACP3, and Modulation Error Ratio (MER) vs. Output Power for 256 QAM Transmitter

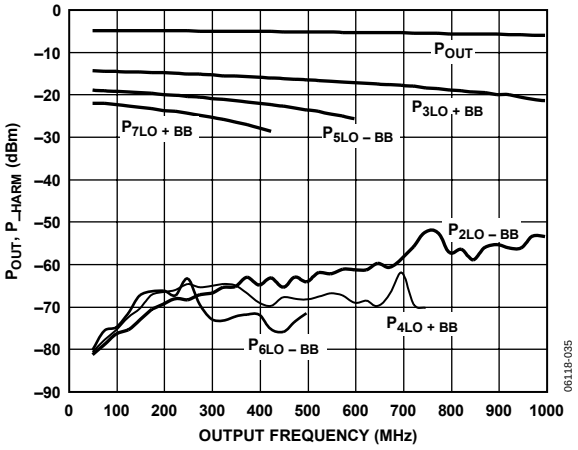


Figure 39. Spectral Components for Output Frequencies from 50 MHz to 1000 MHz

SPECTRAL PRODUCTS FROM HARMONIC MIXING

For broadband applications such as cable TV head-end modulators, special attention must be paid to harmonics of the LO. Figure 39 shows the level of these harmonics (out to 3 GHz) as a function of the output frequency from 50 MHz to 1000 MHz, in a single-sideband (SSB) test configuration, with a baseband signal of 1 MHz and a SSB level of approximately −5 dBm. To read this plot correctly, first pick the output frequency of interest on the trace called P_{OUT}. The associated harmonics can be read off the harmonic traces at multiples of this frequency. For example, at an output frequency of 500 MHz, the fundamental power is −5 dBm. The power of the second (P_{2fc-BB}) and third (P_{3fc+BB}) harmonics is −63 dBm (at 1000 MHz) and −16 dBm (at 1500 MHz), respectively. Of particular importance are the products from odd-harmonics of the LO, generated from the switching operation in the mixers.

For cable TV operation at frequencies above approximately 500 MHz, these harmonics fall out of the band and can be filtered by a fixed filter. However, as the frequency drops below 500 MHz, these harmonics start to fall close to or inside the cable band. This calls for either limitation of the frequency range to above 500 MHz or the use of a switchable filter bank to block in-band harmonics at low frequencies.

RF SECOND-ORDER PRODUCTS

A two-tone RF output signal produces second-order spectral components at sum and difference frequencies. In broadband systems, these intermodulation products fall inside the carrier or in the adjacent channels. Output second-order RF intermodulation intercept is defined as

$$OIP2\_RF = P_{OUT} + (P_{OUT} - P_{IM(RF)})$$

where $P_{IM(RF)}$ is the level of the intermodulation product at $F_{OUT1} + F_{OUT2}$. OIP2_RF levels from a two-tone test are plotted as a function of carrier frequency in Figure 40, where the baseband tones are 3.5 MHz and 4.5 MHz at −5 dBm each.

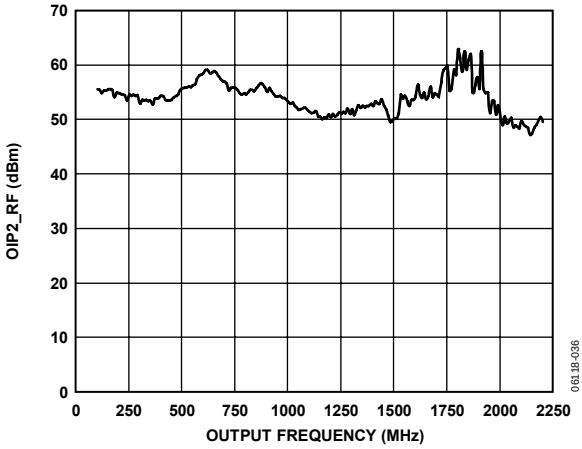


Figure 40. Output Second-Order Intermodulation vs. Carrier Frequency

LO GENERATION USING PLLs

Analog Devices has a line of PLLs that can be used for generating the LO signal. Table 4 lists the PLLs together with their maximum frequency and phase noise performance.

Table 4. PLL Selection Table

Model	Frequency F_{IN} (MHz)	@ 1 kHz Phase Noise dBc/Hz, 200 kHz PFD
ADF4110	550	–91 @ 540 MHz
ADF4111	1200	–87@ 900 MHz
ADF4112	3000	–90 @ 900 MHz
ADF4113	4000	–91 @ 900 MHz
ADF4116	550	–89 @ 540 MHz
ADF4117	1200	–87 @ 900 MHz
ADF4118	3000	–90 @ 900 MHz

The ADF4360 comes as a family of chips, with nine operating frequency ranges. One can be chosen depending on the local oscillator frequency required. While the use of the integrated synthesizer might come at the expense of slightly degraded noise performance from the ADL5385, it can be a cheaper alternative to a separate PLL and VCO solution. Table 5 shows the options available.

Table 5. ADF4360 Family Operating Frequencies

Model	Output Frequency Range (MHz)
ADF4360-0	2400/2725
ADF4360-1	2050/2450
ADF4360-2	1850/2150
ADF4360-3	1600/1950
ADF4360-4	1450/1750
ADF4360-5	1200/1400
ADF4360-6	1050/1250
ADF4360-7	350/1800
ADF4360-8	65/400

TRANSMIT DAC OPTIONS

The AD9777 recommended in the previous sections is by no means the only DAC that can be used to drive the ADL5385. There are other appropriate DACs depending on the level of performance required. Table 6 lists the dual Tx-DACs that Analog Devices offers.

Table 6. Dual Tx—DAC Selection Table

Part	Resolution (Bits)	Update Rate (MSPS Minimum)
AD9709	8	125
AD9761	10	40
AD9763	10	125
AD9765	12	125
AD9767	14	125
AD9773	12	160
AD9775	14	160
AD9777	16	160
AD9776	12	1000
AD9778	14	1000
AD9779	16	1000

All DACs listed have nominal bias levels of 0.5 V and use the same DAC-modulator interface shown in Figure 31.

MODULATOR/DEMODULATOR OPTIONS

Table 7 lists other Analog Devices modulators and demodulators.

Table 7. Modulator/Demodulator Options

Part	Mod/Demod	Frequency Range (MHz)	Comments
AD8345	Mod	140 to 1000	
AD8346	Mod	800 to 2500	
AD8349	Mod	700 to 2700	
ADL5390	Mod	20 to 2400	External Quadrature
ADL5370	Mod	300 to 1000	
ADL5371	Mod	700 to 1300	
ADL5372	Mod	1600 to 2400	
ADL5373	Mod	2300 to 3000	
ADL5374	Mod	3000 to 4000	
AD8347	Demod	800 to 2700	
AD8348	Demod	50 to 1000	
AD8340	Vector Mod	700 to 1000	
AD8341	Vector Mod	1500 to 2400	

EVALUATION BOARD

A populated, RoHS-compliant ADL5385 evaluation board is available. The ADL5385 has an exposed paddle underneath the package, which is soldered to the board. The evaluation board is designed without any components on the underside so that heat can be applied to the underside for easy removal and replacement of the ADL5385.

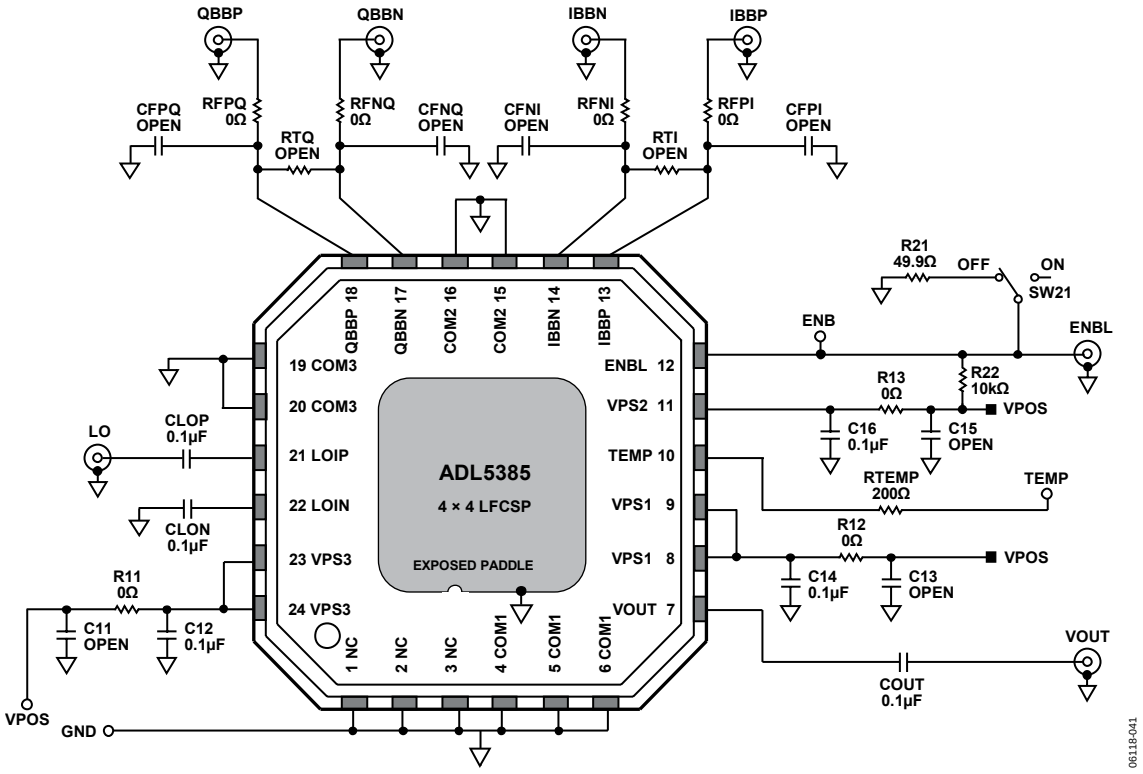


Figure 41. Evaluation Board Schematic

Table 8. Evaluation Board Configuration Options

Component	Function	Default Condition
VPOS, GND	Power Supply and Ground Clip Leads.	Not applicable
SW21, R21, R22, ENB Test Point, ENBL SMA	Device Enable. Set SW21 to the OFF position to power down the device; set SW21 to the ON position to enable the device. Part can be driven from an external enable control source via the test point or the SMA connector. R21 provides a 50 Ω termination for any 50 Ω driving source.	R21 = 50 Ω, R22 = 10k Ω, SW21 = ON
RFNQ, CFNQ, RTQ, CFPQ, RFPQ, RFNI, CFNI, RTI, CFPI, RFPI	Baseband Input Filters. These components can be used to implement a low-pass filter for the baseband signals.	RFNQ, RFPQ, RFNI RFPI = 0 Ω (0402) RTQ, RTI = open (0402) CFNQ, CFPQ, CFNI, CFPI = open (0402)

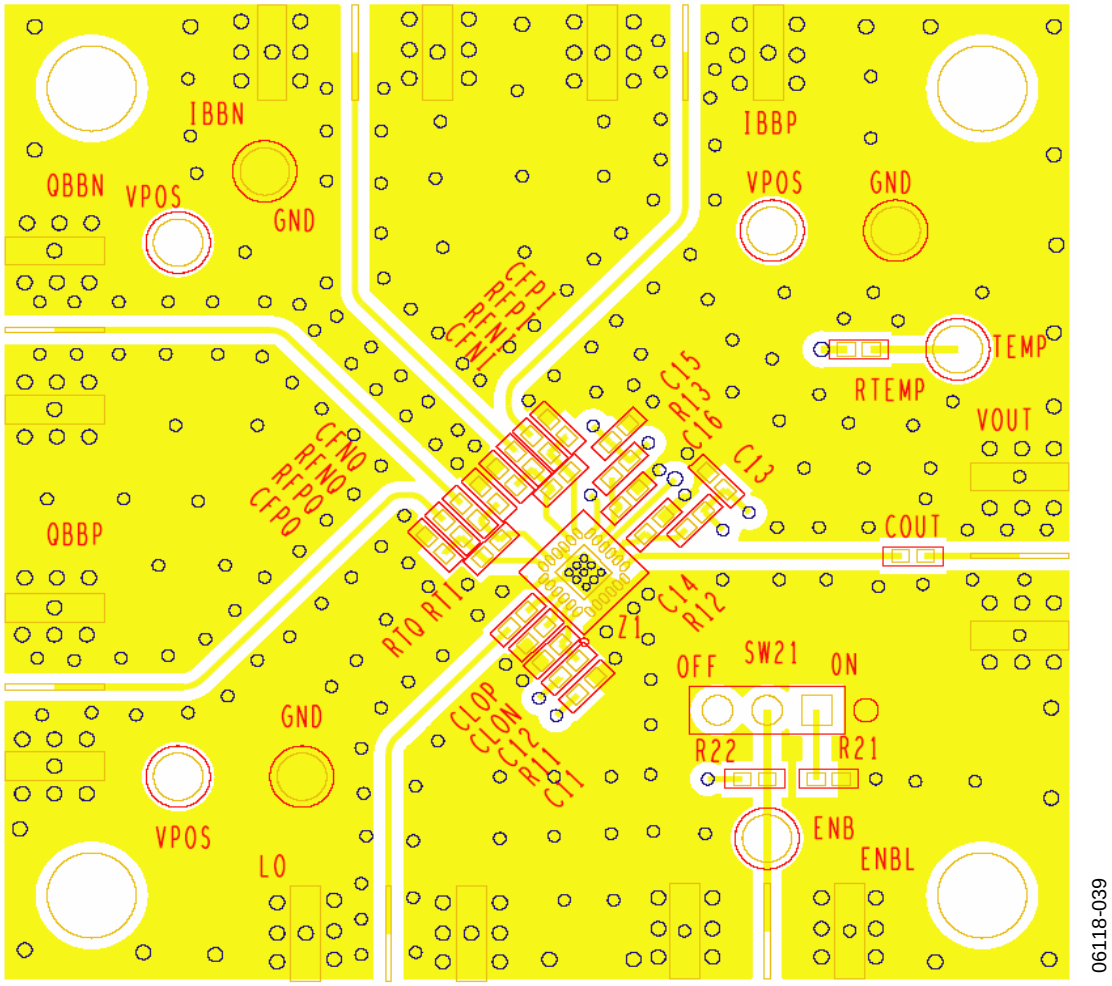


Figure 42. Layout of Evaluation Board

CHARACTERIZATION SETUP

SSB SETUP

Figure 43 is a diagram of the characterization test stand setup for the ADL5385, which is intended to test the product as a single-sideband modulator. The Aeroflex IFR3416 signal generator provides the I and Q inputs as well as the LO input. Output signals are measured directly using the spectrum analyzer, and currents and voltages are measured using the Agilent 34401A multimeter.

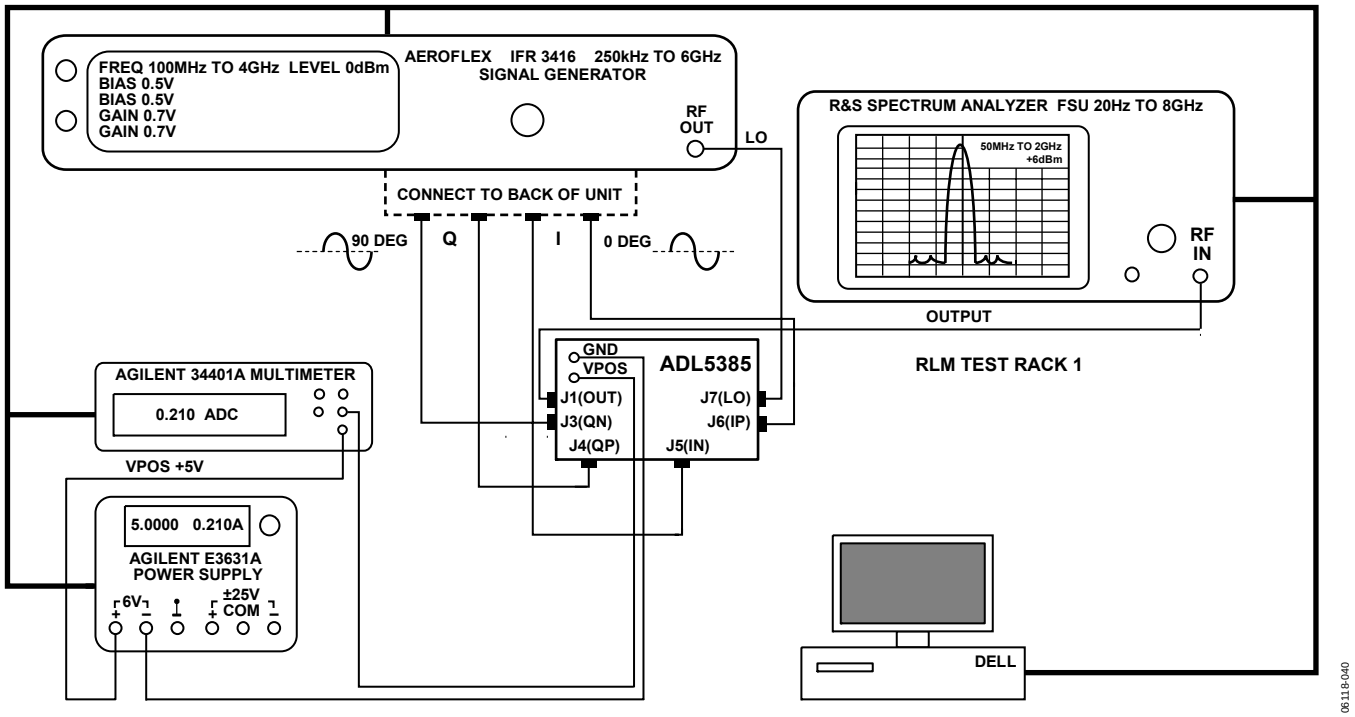
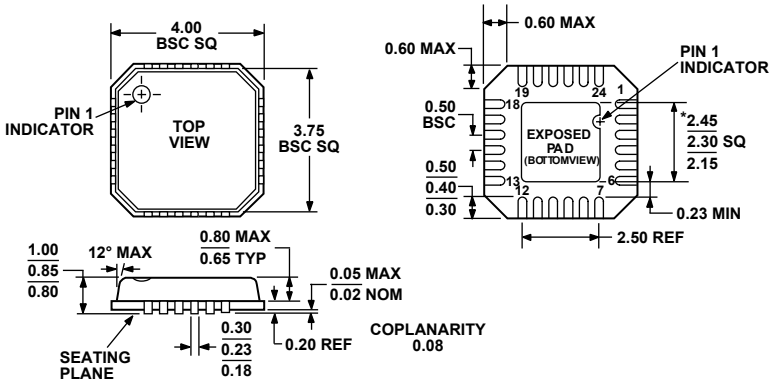


Figure 43. ADL5385 Characterization Board SSB Test Setup

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-2
EXCEPT FOR EXPOSED PAD DIMENSION

Figure 44. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-24-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
ADL5385ACPZ-WP[1]	–40°C to +85°C	24-Lead LFCSP_VQ, Waffle Pack	CP-24-2	64
ADL5385ACPZ-R2[1]	–40°C to +85°C	24-Lead LFCSP_VQ, 7″Tape and Reel	CP-24-2	250
ADL5385ACPZ-R7[1]	–40°C to +85°C	24-Lead LFCSP_VQ, 7″Tape and Reel	CP-24-2	1500
ADL5385-EVALZ[1]		Evaluation Board		1

[1] Z = Pb-free part.

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