

FEATURES

Broadband radio frequency (RF), intermediate frequency (IF), and local oscillator (LO) ports

Conversion loss: 6.8 dB

Noise figure: 6.5 dB

High input IP₃: 25 dBm

High input P_{1dB}: 19 dBm

Low LO drive level

Single-ended design: no need for baluns

Single-supply operation: 3 V @ 19 mA

Miniature, 2 mm × 3 mm, 8-lead LFCSP

RoHS compliant

APPLICATIONS

Cellular base stations

Point-to-point radio links

RF instrumentation

GENERAL DESCRIPTION

The ADL5350 is a high linearity, up-and-down converting mixer capable of operating over a broad input frequency range. It is well suited for demanding cellular base station mixer designs that require high sensitivity and effective blocker immunity. Based on a GaAs pHEMT, single-ended mixer architecture, the ADL5350 provides excellent input linearity and low noise figure without the need for a high power level LO drive.

In 850 MHz/900 MHz receive applications, the ADL5350 provides a typical conversion loss of only 6.7 dB. The input IP₃ is typically greater than 25 dBm, with an input compression point of 19 dBm. The integrated LO amplifier allows a low LO drive level, typically only 4 dBm for most applications.

FUNCTIONAL BLOCK DIAGRAM

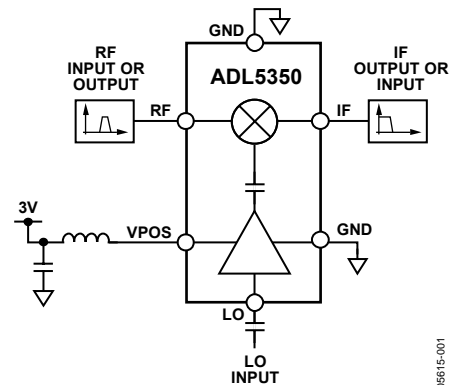


Figure 1.

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The high input linearity of the ADL5350 makes the device an excellent mixer for communications systems that require high blocker immunity, such as GSM 850 MHz/900 MHz and 800 MHz CDMA2000. At 2 GHz, a slightly greater supply current is required to obtain similar performance.

The single-ended broadband RF/IF port allows the device to be customized for a desired band of operation using simple external filter networks. The LO-to-RF isolation is based on the LO rejection of the RF port filter network. Greater isolation can be achieved by using higher order filter networks, as described in the Applications Information section.

The ADL5350 is fabricated on a GaAs pHEMT, high performance IC process. The ADL5350 is available in a 2 mm × 3 mm, 8-lead LFCSP. It operates over a -40°C to +85°C temperature range. An evaluation board is also available.

Rev. 0

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REVISION HISTORY

2/08—Revision 0: Initial Version

SPECIFICATIONS

850 MHz RECEIVE PERFORMANCE

$V_S = 3\text{ V}$, $T_A = 25^\circ\text{C}$, LO power = 4 dBm, re: 50 Ω , unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Conditions
RF Frequency Range	750	850	975	MHz	
LO Frequency Range	500	780	945	MHz	Low-side LO
IF Frequency Range	30	70	250	MHz	
Conversion Loss		6.7		dB	$f_{RF} = 850\text{ MHz}$, $f_{LO} = 780\text{ MHz}$, $f_{IF} = 70\text{ MHz}$
SSB Noise Figure		6.4		dB	$f_{RF} = 850\text{ MHz}$, $f_{LO} = 780\text{ MHz}$, $f_{IF} = 70\text{ MHz}$
Input Third-Order Intercept (IP3)		25		dBm	$f_{RF1} = 849\text{ MHz}$, $f_{RF2} = 850\text{ MHz}$, $f_{LO} = 780\text{ MHz}$, $f_{IF} = 70\text{ MHz}$; each RF tone 0 dBm
Input 1dB Compression Point (P1dB)		19.8		dBm	$f_{RF} = 820\text{ MHz}$, $f_{LO} = 750\text{ MHz}$, $f_{IF} = 70\text{ MHz}$
LO-to-IF Leakage		29		dBc	LO power = 4 dBm, $f_{LO} = 780\text{ MHz}$
LO-to-RF Leakage		13		dBc	LO power = 4 dBm, $f_{LO} = 780\text{ MHz}$
RF-to-IF Leakage		19.5		dBc	RF power = 0 dBm, $f_{RF} = 850\text{ MHz}$, $f_{LO} = 780\text{ MHz}$
IF/2 Spurious		-50		dBc	RF power = 0 dBm, $f_{RF} = 850\text{ MHz}$, $f_{LO} = 780\text{ MHz}$
Supply Voltage	2.7	3	3.5	V	
Supply Current		16.5		mA	LO power = 4 dBm

1950 MHz RECEIVE PERFORMANCE

$V_S = 3\text{ V}$, $T_A = 25^\circ\text{C}$, LO power = 6 dBm, re: 50 Ω , unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Conditions
RF Frequency Range	1800	1950	2050	MHz	
LO Frequency Range	1420	1760	2000	MHz	Low-side LO
IF Frequency Range	50	190	380	MHz	
Conversion Loss		6.8		dB	$f_{RF} = 1950\text{ MHz}$, $f_{LO} = 1760\text{ MHz}$, $f_{IF} = 190\text{ MHz}$
SSB Noise Figure		6.5		dB	$f_{RF} = 1950\text{ MHz}$, $f_{LO} = 1760\text{ MHz}$, $f_{IF} = 190\text{ MHz}$
Input Third-Order Intercept (IP3)		25		dBm	$f_{RF1} = 1949\text{ MHz}$, $f_{RF2} = 1951\text{ MHz}$, $f_{LO} = 1760\text{ MHz}$, $f_{IF} = 190\text{ MHz}$; each RF tone 0 dBm
Input 1dB Compression Point (P1dB)		19		dBm	$f_{RF} = 1950\text{ MHz}$, $f_{LO} = 1760\text{ MHz}$, $f_{IF} = 190\text{ MHz}$
LO-to-IF Leakage		13.5		dBc	LO power = 6 dBm, $f_{LO} = 1760\text{ MHz}$
LO-to-RF Leakage		10.5		dBc	LO power = 6 dBm, $f_{LO} = 1760\text{ MHz}$
RF-to-IF Leakage		11.5		dBc	RF power = 0 dBm, $f_{RF} = 1950\text{ MHz}$, $f_{LO} = 1760\text{ MHz}$
IF/2 Spurious		-54		dBc	RF power = 0 dBm, $f_{RF} = 1950\text{ MHz}$, $f_{LO} = 1760\text{ MHz}$
Supply Voltage	2.7	3	3.5	V	
Supply Current		19		mA	LO power = 6 dBm

ADL5350

SPUR TABLES

All spur tables are $(N \times f_{RF}) - (M \times f_{LO})$ mixer spurious products for 0 dBm input power, unless otherwise noted. N.M. indicates that a spur was not measured due to it being at a frequency >6 GHz.

850 MHz SPUR TABLE

Table 3.

		M															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
N	0	≤-100	-20.6	-19.2	-15.3	-16.7	-38.4	-26.6	-22.1	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.
	1	-21.6	-5.6	-23.6	-19.6	-31.9	-28.7	-46.1	-48.5	-33.2	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.
	2	-50.0	-69.2	-50.5	-59.8	-49.1	-57.5	-51.0	-77.7	-65.8	-60.8	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.
	3	-74.8	-66.0	-71.8	-68.1	-70.2	-67.4	-66.9	-70.8	-85.2	-87.3	-72.2	N.M.	N.M.	N.M.	N.M.	N.M.
	4	≤-100	-92.6	-91.6	-96.1	-92.7	-98.7	-90.2	-91.7	-88.8	≤-100	≤-100	-91.7	-88.6	N.M.	N.M.	N.M.
	5	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	N.M.
	6	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	N.M.
	7	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100
	8	N.M.	N.M.	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100
	9	N.M.	N.M.	N.M.	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100
	10	N.M.	N.M.	N.M.	N.M.	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100
	11	N.M.	N.M.	N.M.	N.M.	N.M.	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100
	12	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100
	13	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100
	14	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100
	15	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100

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1950 MHz SPUR TABLE

Table 4.

		M															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
N	0	≤-100	-13.1	-32.8	-22.4	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.
	1	-10.8	-7.0	-25.3	-27.7	-33.9	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.
	2	-48.2	-61.2	-41.2	-44.6	-47.0	-74.6	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.
	3	-72.3	-71.4	-83.6	-64.5	-62.4	-64.3	-83.7	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.
	4	N.M.	N.M.	-91.4	-84.2	-78.3	-76.5	-80.0	-92.0	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.
	5	N.M.	N.M.	N.M.	-90.8	-82.3	-77.1	-79.5	-83.8	-95.2	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.
	6	N.M.	N.M.	N.M.	N.M.	≤-100	≤-100	-93.4	-94.5	≤-100	-99.2	≤-100	N.M.	N.M.	N.M.	N.M.	N.M.
	7	N.M.	N.M.	N.M.	N.M.	N.M.	≤-100	≤-100	-94.0	-96.4	≤-100	≤-100	≤-100	N.M.	N.M.	N.M.	N.M.
	8	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	N.M.	N.M.
	9	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	N.M.
	10	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	N.M.
	11	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100
	12	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100
	13	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	≤-100	≤-100	≤-100	≤-100	≤-100
	14	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	≤-100	≤-100	≤-100	≤-100
	15	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	≤-100	≤-100	≤-100

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ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage, V_s	4.0 V
RF Input Level	23 dBm
LO Input Level	20 dBm
Internal Power Dissipation	324 mW
θ_{JA}	154.3°C/W
Maximum Junction Temperature	135°C
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ADL5350

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

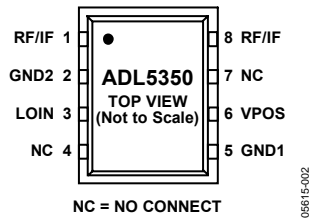


Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8	RF/IF	RF and IF Input/Output Ports. These nodes are internally tied together. RF and IF port separation is achieved using external tuning networks.
2, 5, Paddle	GND2, GND1, GND	Device Common (DC Ground).
3	LOIN	LO Input. Needs to be ac-coupled.
4, 7	NC	No Connect. Grounding NC pins is recommended.
6	VPOS	Positive Supply Voltage for the Drain of the LO Buffer. A series RF choke is needed on the supply line to provide proper ac loading of the LO buffer amplifier.

TYPICAL PERFORMANCE CHARACTERISTICS

850 MHz CHARACTERISTICS

Supply voltage = 3 V, RF frequency = 850 MHz, IF frequency = 70 MHz, RF level = 0 dBm, LO level = 4 dBm, $T_A = 25^\circ\text{C}$, unless otherwise noted.

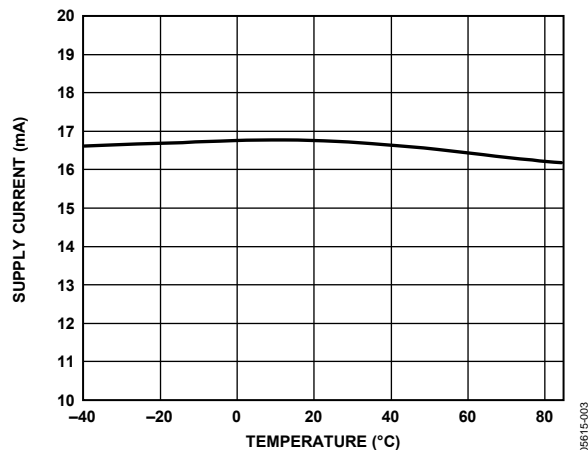


Figure 3. Supply Current vs. Temperature

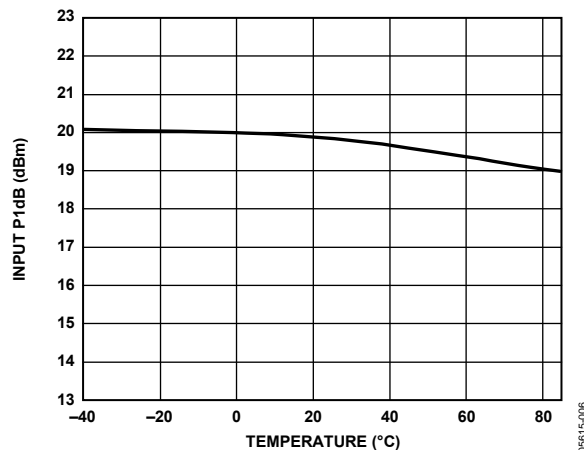


Figure 6. Input P1dB vs. Temperature

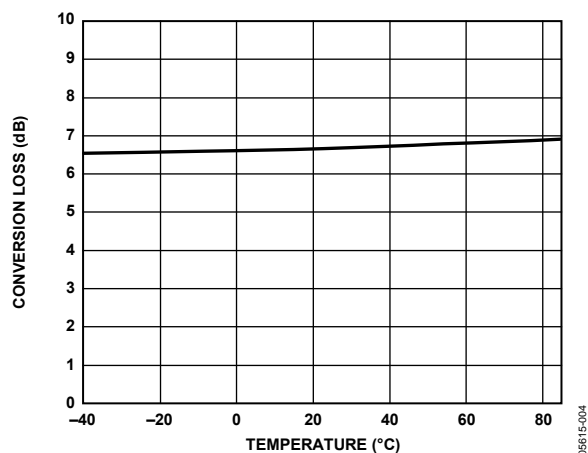


Figure 4. Conversion Loss vs. Temperature

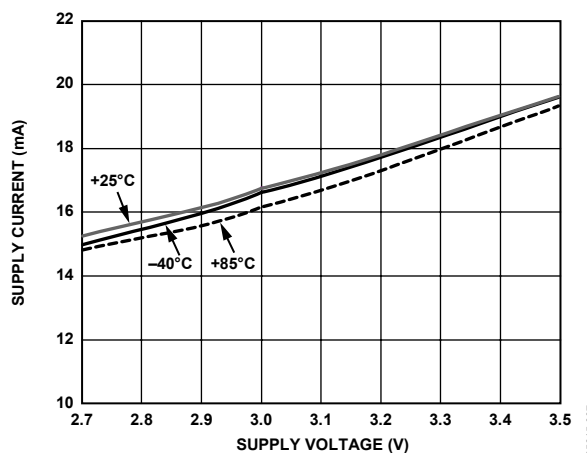


Figure 7. Supply Current vs. Supply Voltage

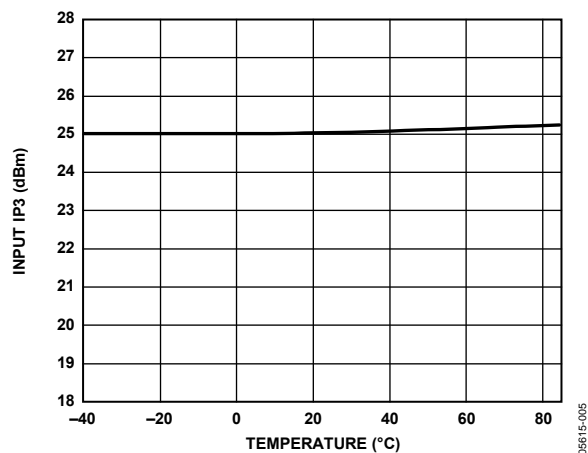


Figure 5. Input IP3 (IIP3) vs. Temperature

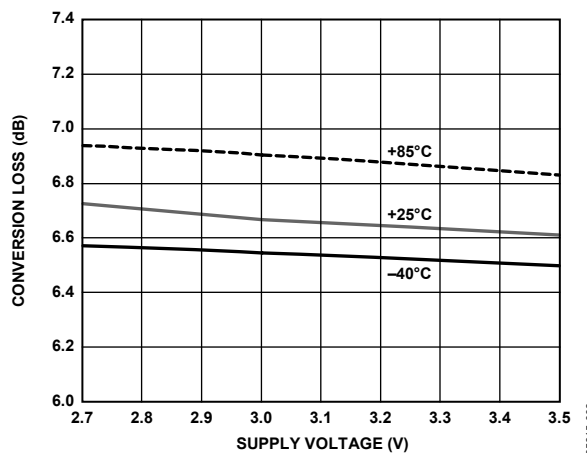


Figure 8. Conversion Loss vs. Supply Voltage

Supply voltage = 3 V, RF frequency = 850 MHz, IF frequency = 70 MHz, RF level = 0 dBm, LO level = 4 dBm, T_A = 25°C, unless otherwise noted.

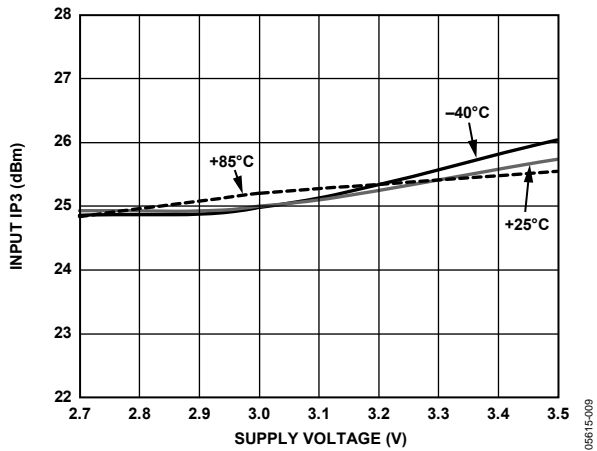


Figure 9. Input IP3 vs. Supply Voltage

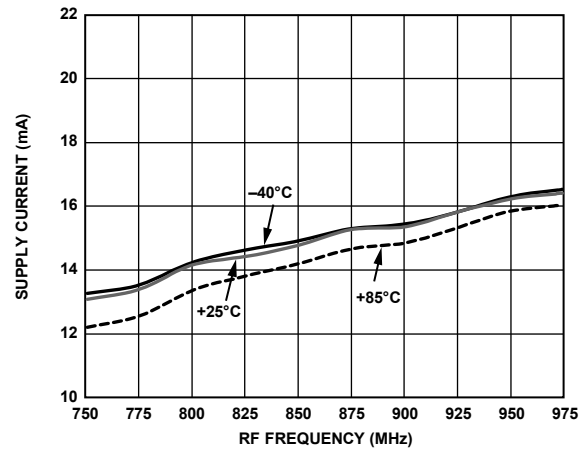


Figure 12. Supply Current vs. RF Frequency

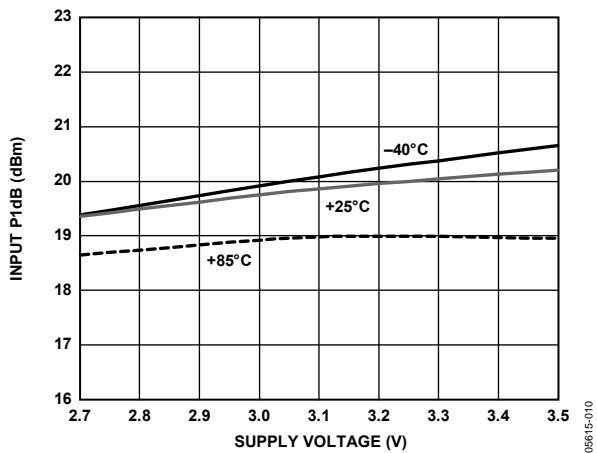


Figure 10. Input P1dB vs. Supply Voltage

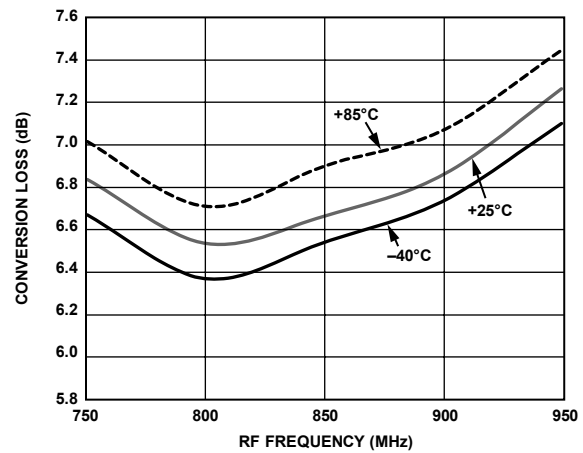


Figure 13. Conversion Loss vs. RF Frequency

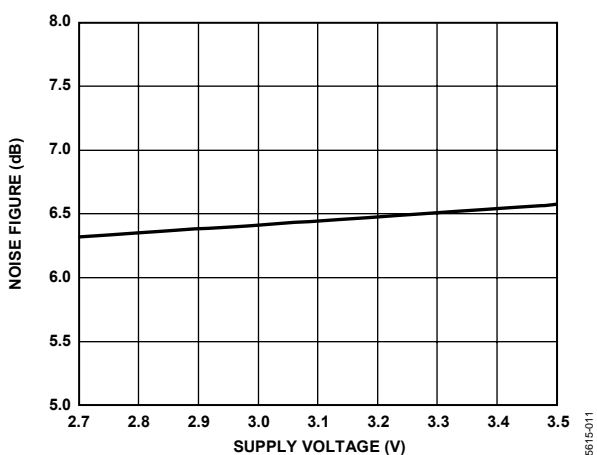


Figure 11. Noise Figure vs. Supply Voltage

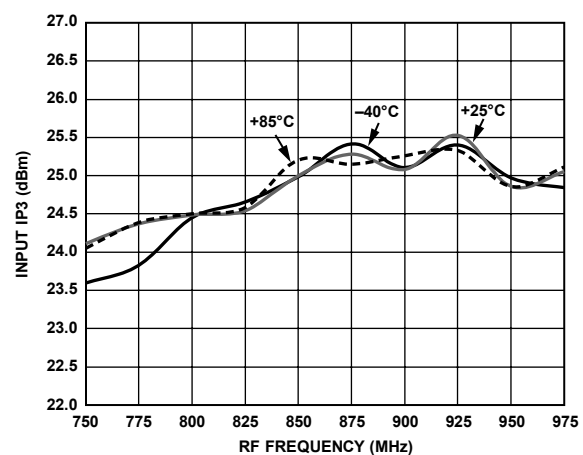


Figure 14. Input IP3 vs. RF Frequency

Supply voltage = 3 V, RF frequency = 850 MHz, IF frequency = 70 MHz, RF level = 0 dBm, LO level = 4 dBm, $T_A = 25^\circ\text{C}$, unless otherwise noted.

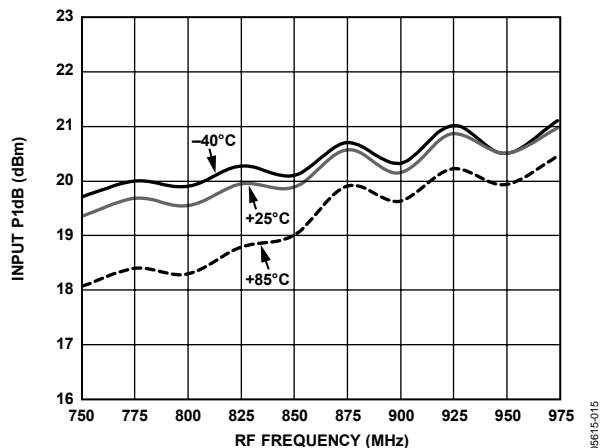


Figure 15. Input P1dB vs. RF Frequency

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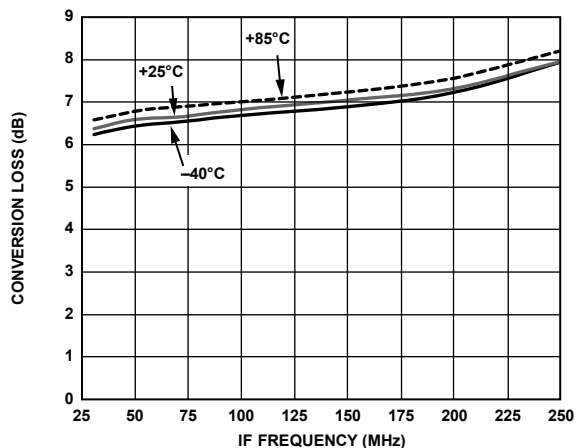


Figure 18. Conversion Loss vs. IF Frequency

05615-018

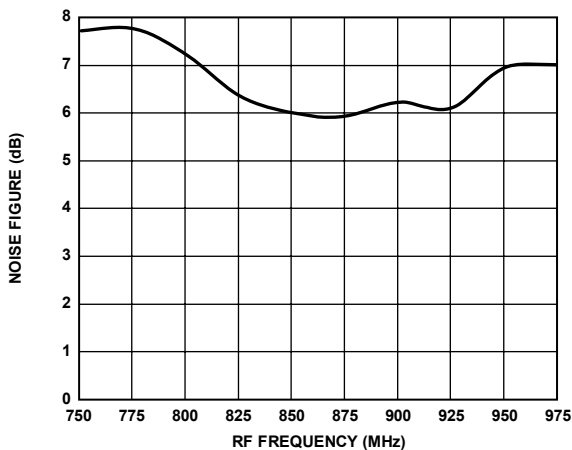


Figure 16. Noise Figure vs. RF Frequency

05615-016

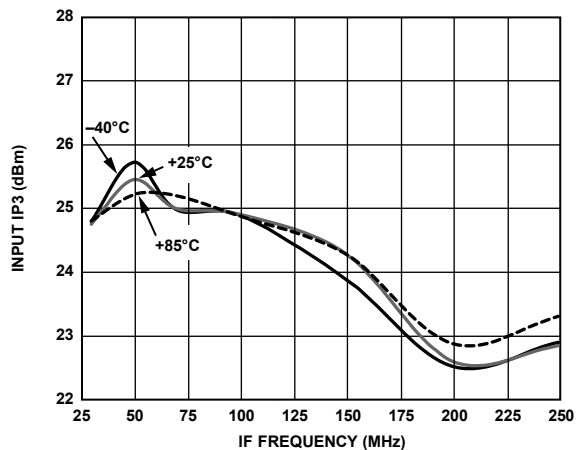


Figure 19. Input IP3 vs. IF Frequency

05615-019

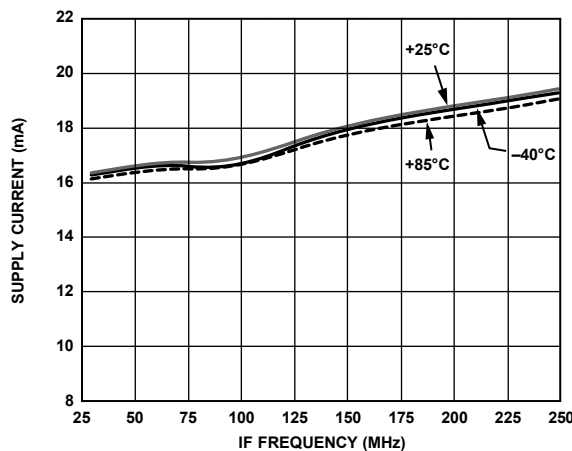


Figure 17. Supply Current vs. IF Frequency

05615-017

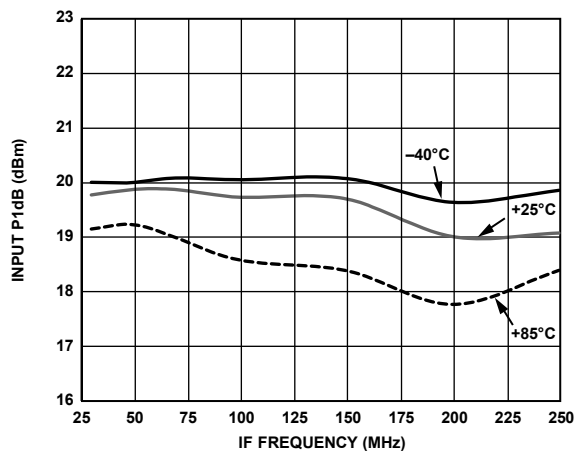


Figure 20. Input P1dB vs. IF Frequency

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Supply voltage = 3 V, RF frequency = 850 MHz, IF frequency = 70 MHz, RF level = 0 dBm, LO level = 4 dBm, $T_A = 25^\circ\text{C}$, unless otherwise noted.

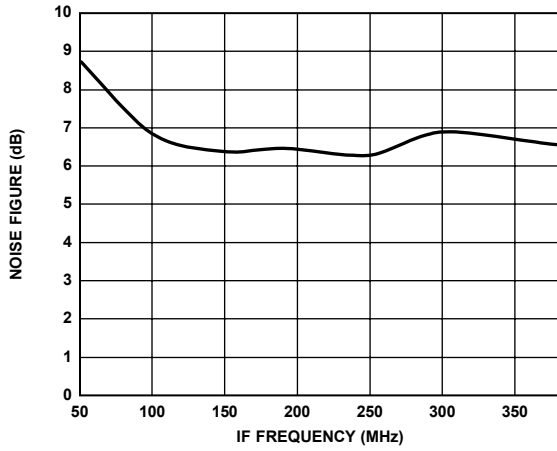


Figure 21. Noise Figure vs. IF Frequency

05615-021

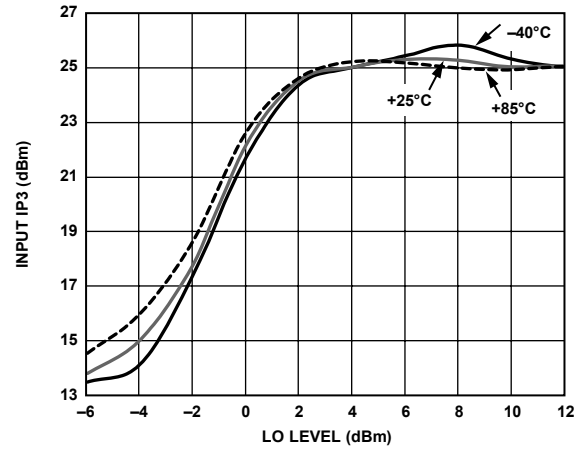


Figure 24. Input IP3 vs. LO Level

05615-024

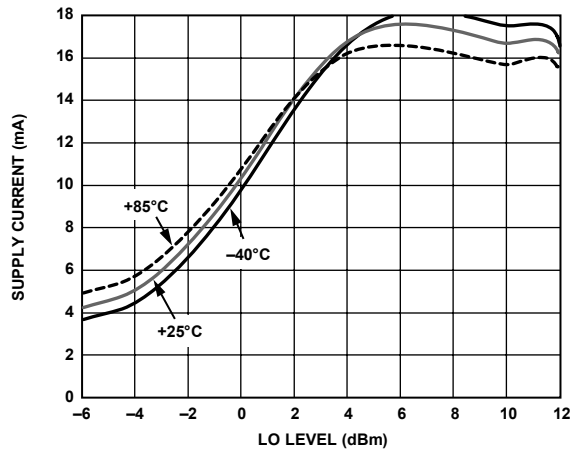


Figure 22. Supply Current vs. LO Level

05615-022

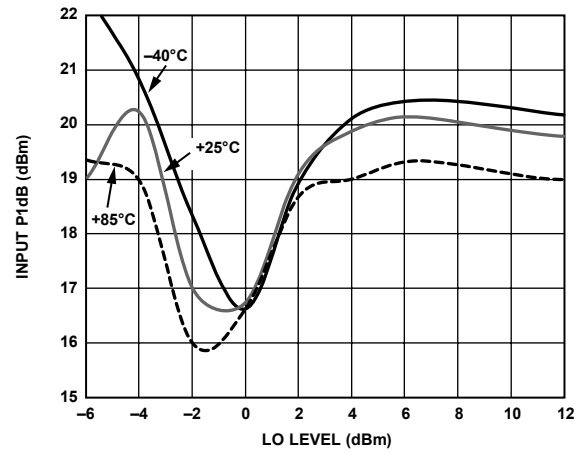


Figure 25. Input P1dB vs. LO Level

05615-025

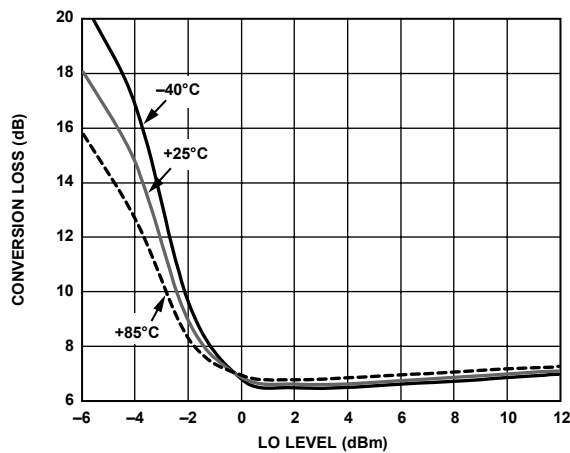


Figure 23. Conversion Loss vs. LO Level

05615-023

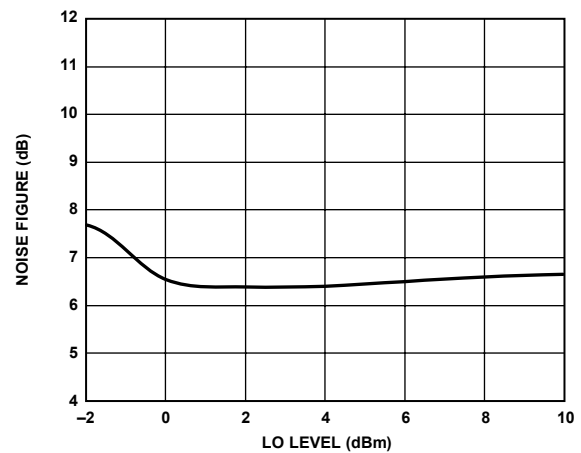


Figure 26. Noise Figure vs. LO Level

05615-026

Supply voltage = 3 V, RF frequency = 850 MHz, IF frequency = 70 MHz, RF level = 0 dBm, LO level = 4 dBm, $T_A = 25^\circ\text{C}$, unless otherwise noted.

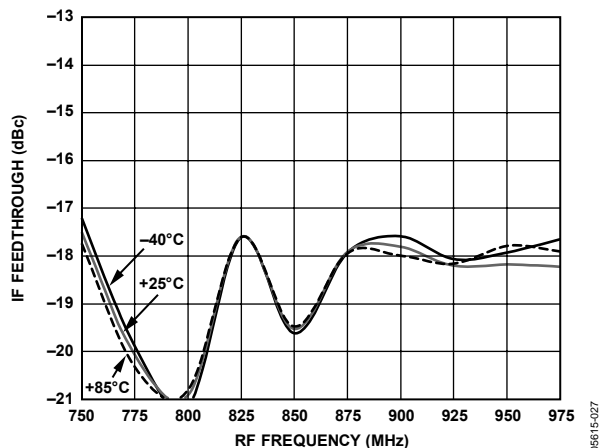


Figure 27. IF Feedthrough vs. RF Frequency

09615-027

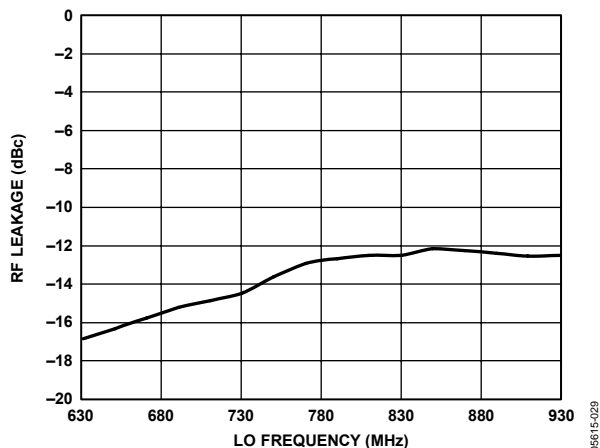


Figure 29. RF Leakage vs. LO Frequency

09615-029

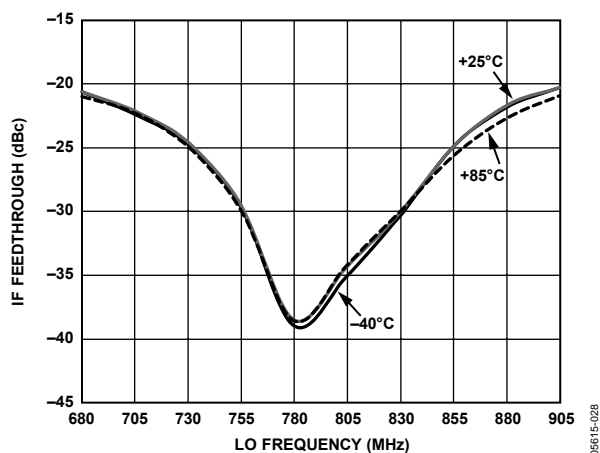


Figure 28. IF Feedthrough vs. LO Frequency

09615-028

ADL5350

1950 MHz CHARACTERISTICS

Supply voltage = 3 V, RF frequency = 1950 MHz, IF frequency = 190 MHz, RF level = -10 dBm, LO level = 6 dBm, $T_A = 25^\circ\text{C}$, unless otherwise noted.

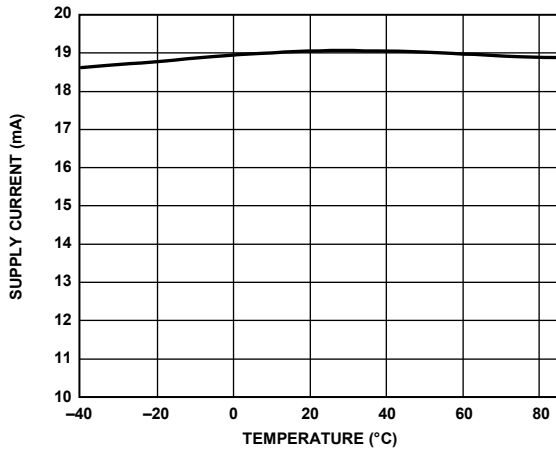


Figure 30. Supply Current vs. Temperature

05615-030

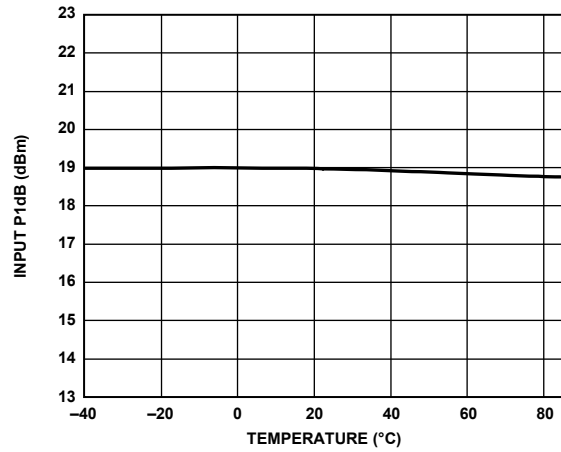


Figure 33. Input P1dB vs. Temperature

05615-033

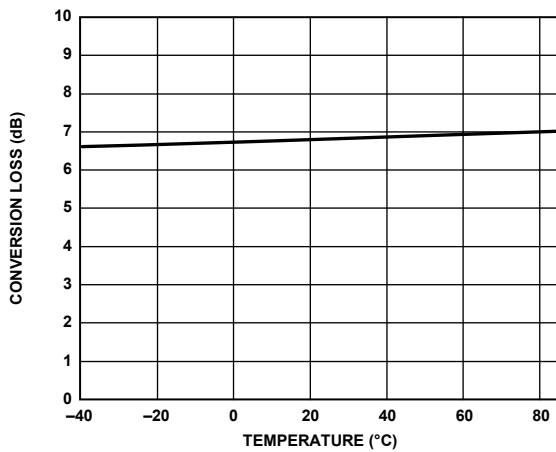


Figure 31. Conversion Loss vs. Temperature

05615-031

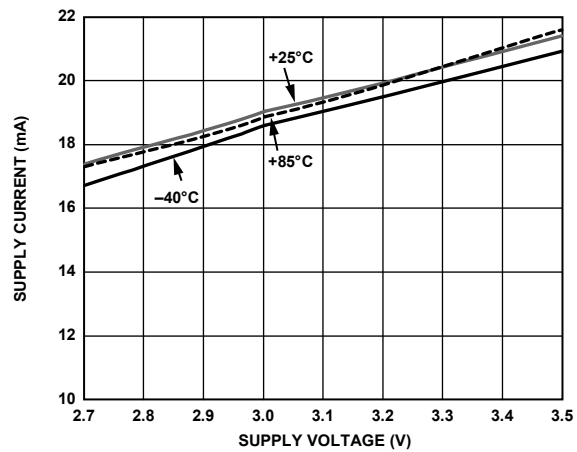


Figure 34. Supply Current vs. Supply Voltage

05615-034

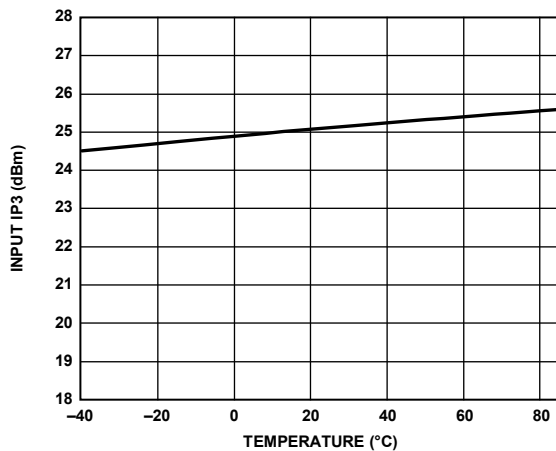


Figure 32. Input IP3 vs. Temperature

05615-032

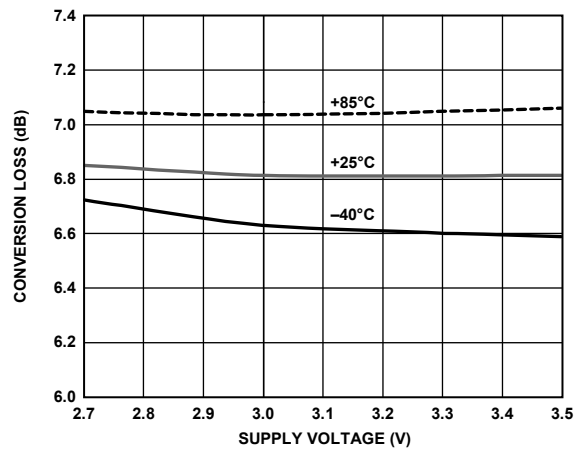


Figure 35. Conversion Loss vs. Supply Voltage

05615-035

Supply voltage = 3 V, RF frequency = 1950 MHz, IF frequency = 190 MHz, RF level = -10 dBm, LO level = 6 dBm, $T_A = 25^\circ\text{C}$, unless otherwise noted.

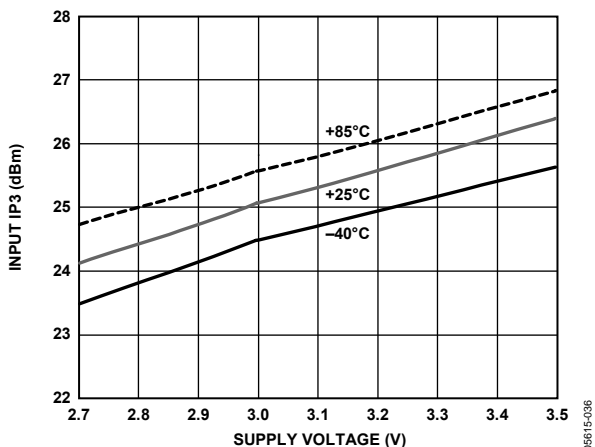


Figure 36. Input IP3 vs. Supply Voltage

05615-036

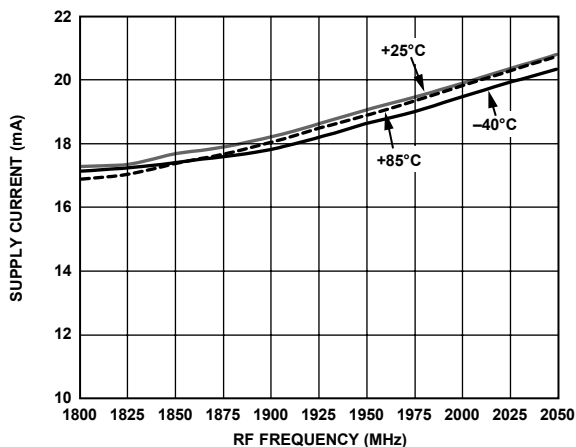


Figure 39. Supply Current vs. RF Frequency

05615-039

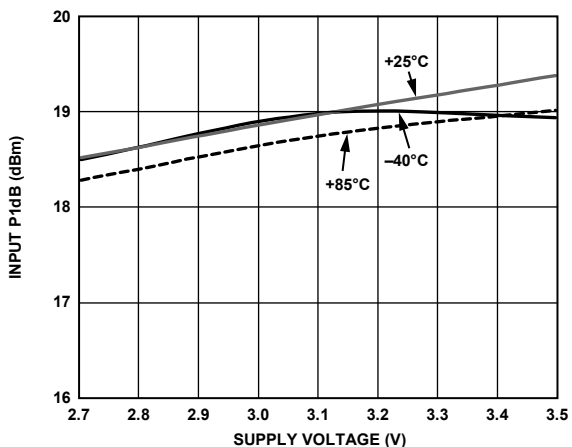


Figure 37. Input P1dB vs. Supply Voltage

05615-037

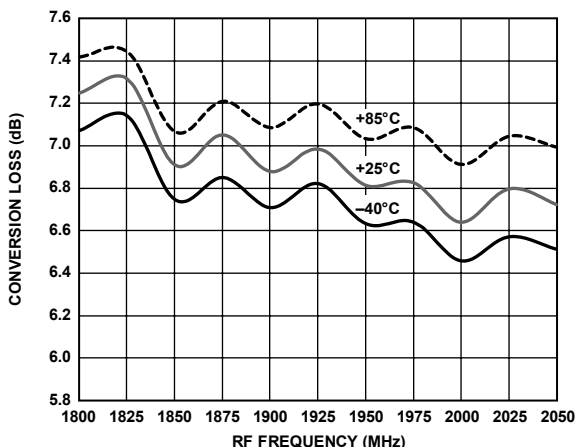


Figure 40. Conversion Loss vs. RF Frequency

05615-040

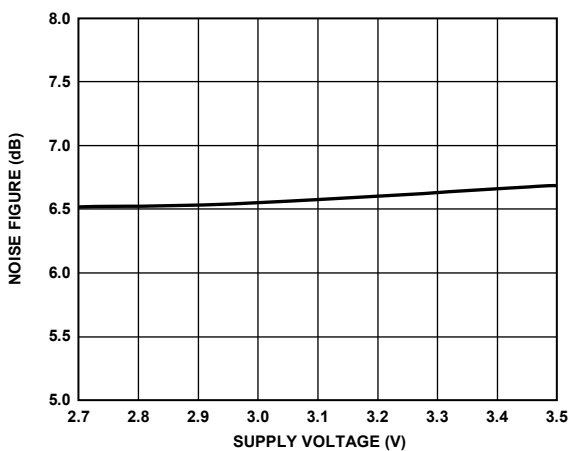


Figure 38. Noise Figure vs. Supply Voltage

05615-038

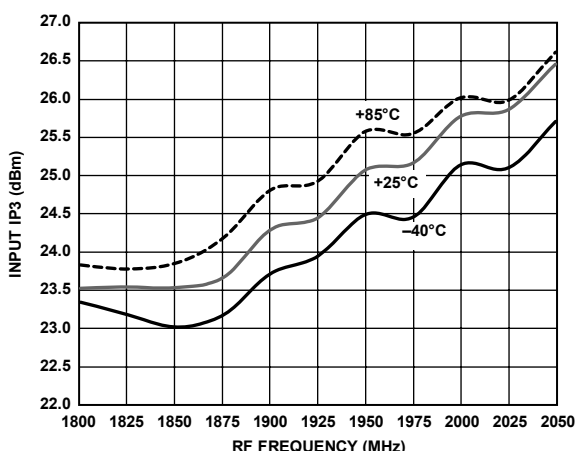


Figure 41. Input IP3 vs. RF Frequency

05615-041

ADL5350

Supply voltage = 3 V, RF frequency = 1950 MHz, IF frequency = 190 MHz, RF level = -10 dBm, LO level = 6 dBm, $T_A = 25^\circ\text{C}$, unless otherwise noted.

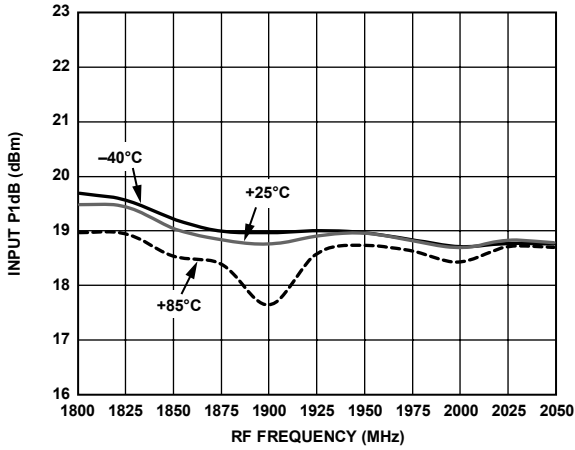


Figure 42. Input P1dB vs. RF Frequency

05615-042

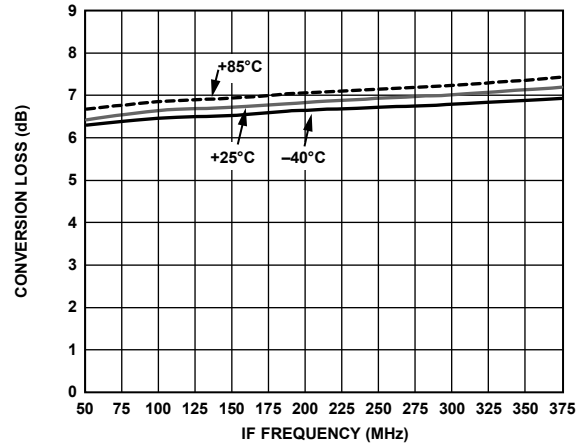


Figure 45. Conversion Loss vs. IF Frequency

05615-045

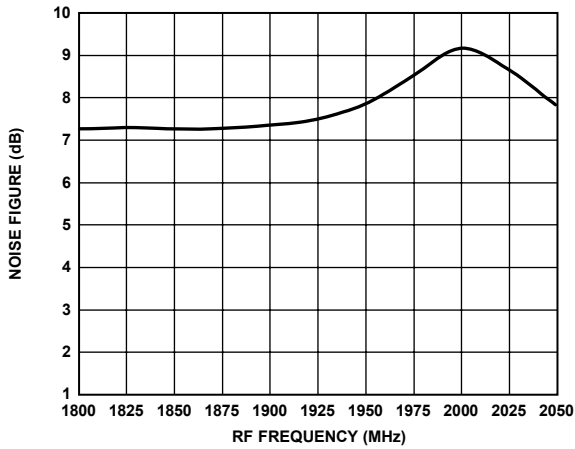


Figure 43. Noise Figure vs. RF Frequency

05615-043

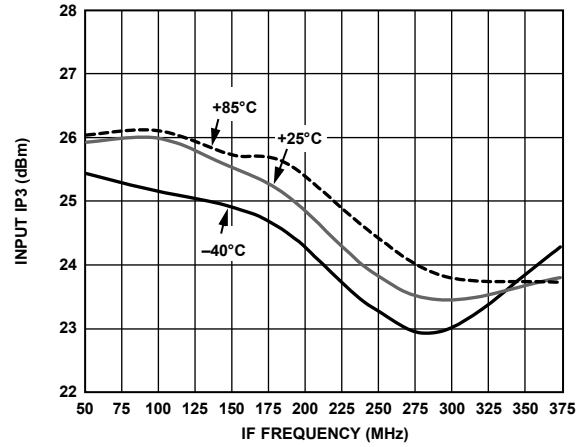


Figure 46. Input IP3 vs. IF Frequency

05615-046

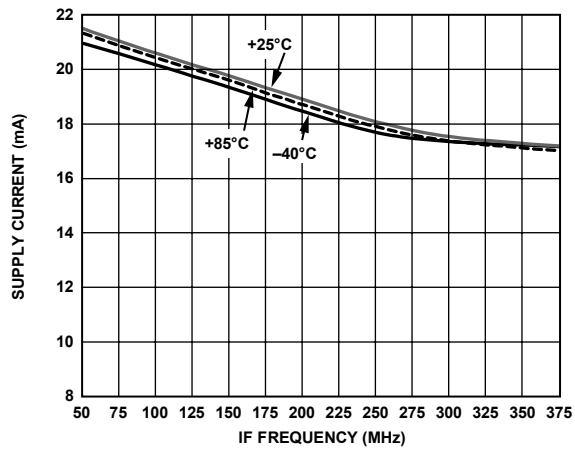


Figure 44. Supply Current vs. IF Frequency

05615-044

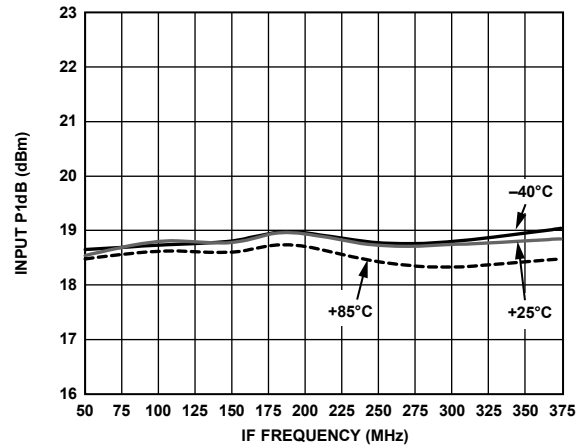


Figure 47. Input P1dB vs. IF Frequency

05615-047

Supply voltage = 3 V, RF frequency = 1950 MHz, IF frequency = 190 MHz, RF level = -10 dBm, LO level = 6 dBm, $T_A = 25^\circ\text{C}$, unless otherwise noted.

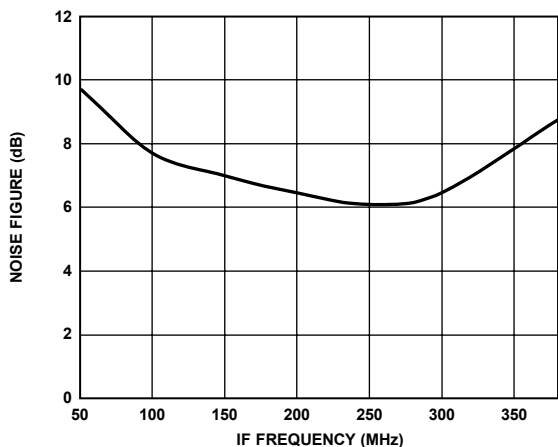


Figure 48. Noise Figure vs. IF Frequency

05615-048

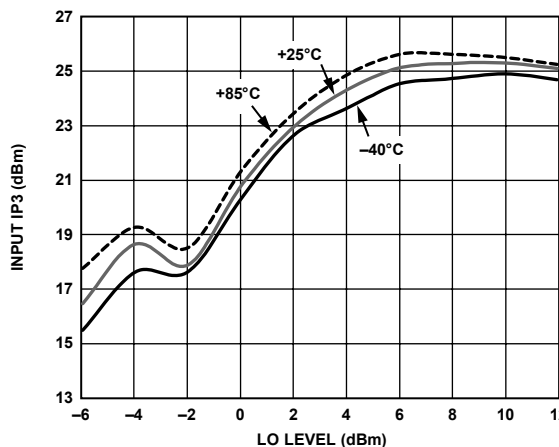


Figure 51. Input IP3 vs. LO Level

05615-051

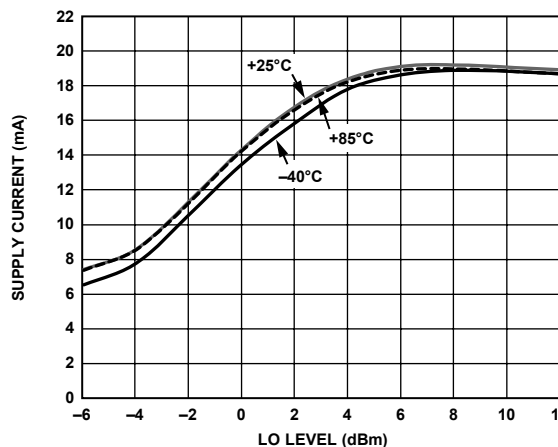


Figure 49. Supply Current vs. LO Level

05615-049

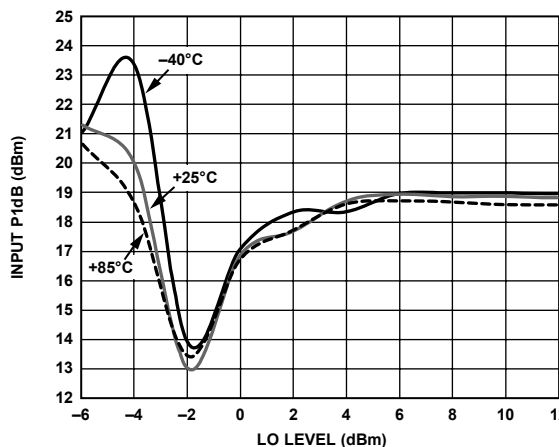


Figure 52. Input P1dB vs. LO Level

05615-052

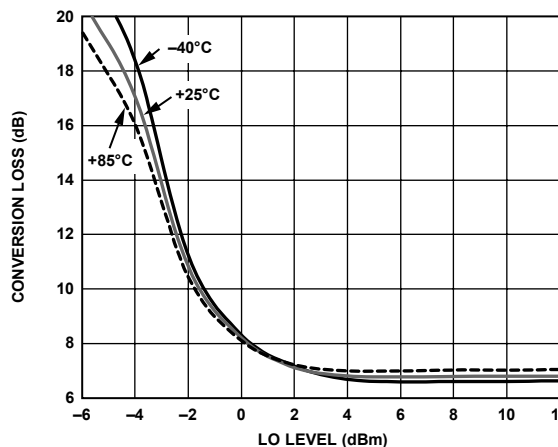


Figure 50. Conversion Loss vs. LO Level

05615-050

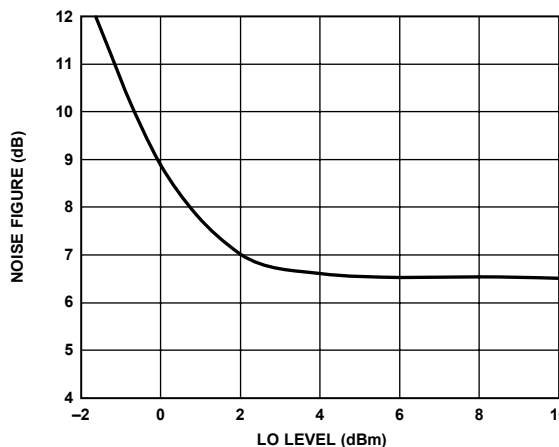


Figure 53. Noise Figure vs. LO Level

05615-053

ADL5350

Supply voltage = 3 V, RF frequency = 1950 MHz, IF frequency = 190 MHz, RF level = -10 dBm, LO level = 6 dBm, $T_A = 25^\circ\text{C}$, unless otherwise noted.

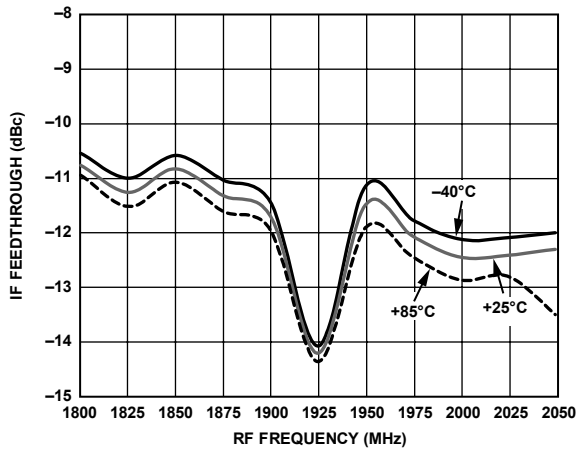


Figure 54. IF Feedthrough vs. RF Frequency

09615-054

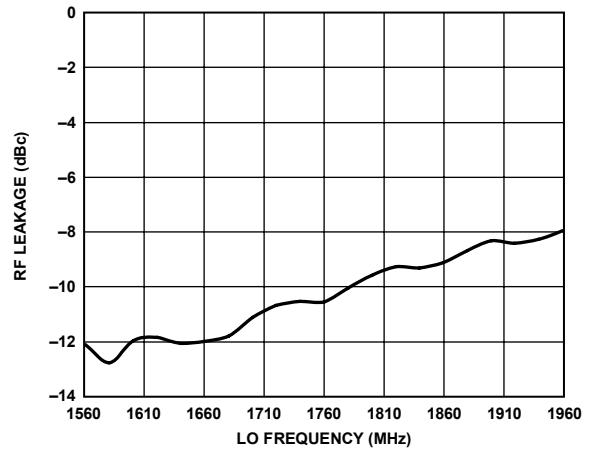


Figure 56. RF Leakage vs. LO Frequency

09615-056

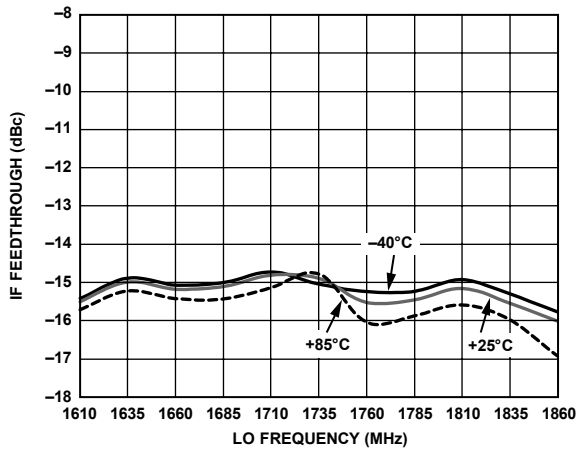


Figure 55. IF Feedthrough vs. LO Frequency

09615-055

FUNCTIONAL DESCRIPTION

CIRCUIT DESCRIPTION

The ADL5350 is a GaAs pHEMT, single-ended, passive mixer with an integrated LO buffer amplifier. The device relies on the varying drain to source channel conductance of a FET junction to modulate an RF signal. A simplified schematic is shown in Figure 57.

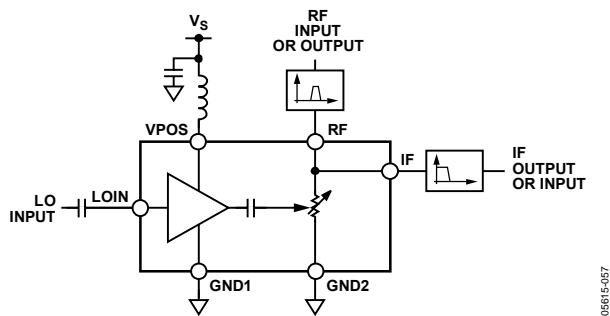


Figure 57. Simplified Schematic

The LO signal is applied to the gate contact of a FET-based buffer amplifier. The buffer amplifier provides sufficient gain of the LO signal to drive the resistive switch. Additionally, feedback circuitry provides the necessary bias to the FET buffer amplifier and RF/IF ports to achieve optimum modulation efficiency for common cellular frequencies.

The mixing of RF and LO signals is achieved by switching the channel conductance from the RF/IF port to ground at the rate of the LO. The RF signal is passed through an external band-pass network to help reject image bands and reduce the broadband noise presented to the mixer. The band-limited RF signal is presented to the time-varying load of the RF/IF port, which causes the envelope of the RF signal to be amplitude modulated at the rate of the LO. A filter network applied to the IF port is necessary to reject the RF signal and pass the wanted mixing product. In a down-conversion application, the IF filter network is designed to pass the difference frequency and present an open circuit to the incident RF frequency. Similarly, for an upconversion application, the filter is designed to pass the sum frequency and reject the incident RF. As a result, the frequency response of the mixer is determined by the response characteristics of the external RF/IF filter networks.

IMPLEMENTATION PROCEDURE

The ADL5350 is a simple single-ended mixer that relies on off-chip circuitry to achieve effective RF dynamic performance. The following steps should be followed to achieve optimum performance (see Figure 58 for component designations):

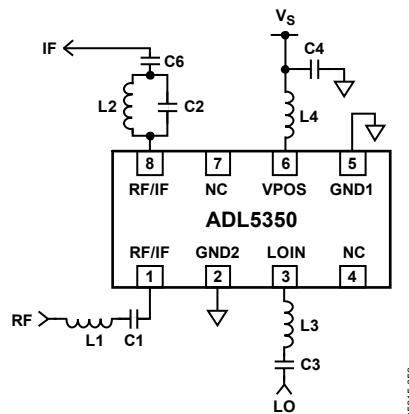


Figure 58. Reference Schematic

- Table 7 shows the recommended LO bias inductor values for a variety of LO frequencies. To ensure efficient commutation of the mixer, the bias inductor needs to be properly set. For other frequencies within the range shown, the values can be interpolated. For frequencies outside this range, see the Applications Information section.

Table 7. Recommended LO Bias Inductor

Desired LO Frequency (MHz)	Recommended LO Bias Inductor, L4 ¹ (nH)
380	68
750	24
1000	18
1750	3.8
2000	2.1

¹ The bias inductor should have a self-resonant frequency greater than the intended frequency of operation.

2. Tune the LO port input network for optimum return loss. Typically, a band-pass network is used to pass the LO signal to the LOIN pin. It is recommended to block high frequency harmonics of the LO from the mixer core. LO harmonics cause higher RF frequency images to be downconverted to the desired IF frequency and result in sensitivity degradation. If the intended LO source has poor harmonic distortion and spectral purity, it may be necessary to employ a higher order band-pass filter network. Figure 58 illustrates a simple LC band-pass filter used to pass the fundamental frequency of the LO source. Capacitor C3 is a simple dc block, while the Series Inductor L3, along with the gate-to-source capacitance of the buffer amplifier, form a low-pass network. The native gate input of the LO buffer (FET) alone presents a rather high input impedance. The gate bias is generated internally using feedback that can result in a positive return loss at the intended LO frequency.

If a better than –10 dB return loss is desired, it may be necessary to add a shunt resistor to ground before the coupling capacitor (C3) to present a lower loading impedance to the LO source. In doing so, a slightly greater LO drive level may be required.

3. Design the RF and IF filter networks. Figure 58 depicts simple LC tank filter networks for the IF and RF port interfaces. The RF port LC network is designed to pass the RF input signal. The series LC tank has a resonant frequency at $1/(2\pi\sqrt{LC})$. At resonance, the series reactances are canceled, which presents a series short to the RF signal. A parallel LC tank is used on the IF port to reject the RF and LO signals. At resonance, the parallel LC tank presents an open circuit.

It is necessary to account for the board parasitics, finite Q, and self-resonant frequencies of the LC components when designing the RF, IF, and LO filter networks. Table 8 provides suggested values for initial prototyping.

Table 8. Suggested RF, IF, and LO Filter Networks for Low-Side LO Injection

RF Frequency (MHz)	L1 (nH) ¹	C1 (pF)	L2 (nH)	C2 (pF)	L3 (nH)	C3 (pF)
450	8.3	10	10	10	10	100
850	6.8	4.7	4.7	5.6	8.2	100
1950	1.7	1.5	1.7	1.2	3.5	100
2400	0.67	1	1.5	0.7	3.0	100

¹ The inductor should have a self-resonant frequency greater than the intended frequency of operation. L1 should be a high Q inductor for optimum NF performance.

APPLICATIONS INFORMATION

LOW FREQUENCY APPLICATIONS

The ADL5350 can be used in low frequency applications. The circuit in Figure 59 is designed for an RF of 136 MHz to 176 MHz and an IF of 45 MHz using a high-side LO. The series and parallel resonant circuits are tuned for 154 MHz, which is the geometric mean of the desired RF frequencies. The performance of this circuit is depicted in Figure 60.

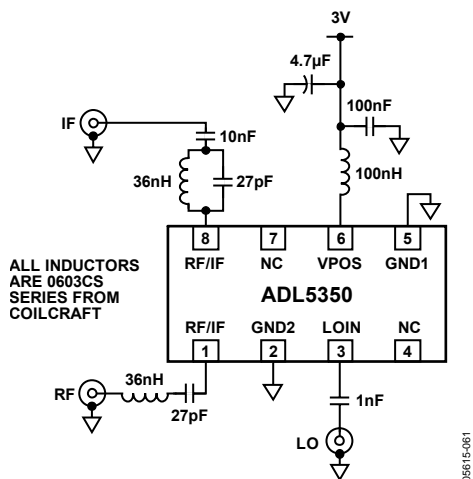


Figure 59. 136 MHz to 176 MHz RF Downconversion Schematic

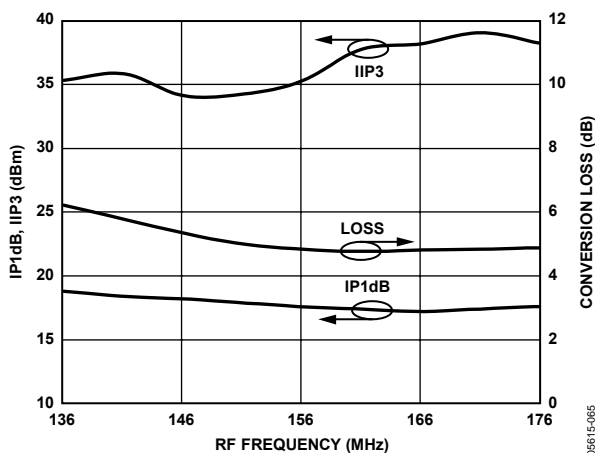


Figure 60. Measured Performance for Circuit in Figure 59 Using High-Side LO Injection and 45 MHz IF

HIGH FREQUENCY APPLICATIONS

The ADL5350 can be used at extended frequencies with some careful attention to board and component parasitics. Figure 61 is an example of a 2560 MHz to 2660 MHz down-conversion using a low-side LO. The performance of this circuit is depicted in Figure 62. Note that the inductor and capacitor values are very small, especially for the RF and IF ports. Above 2.5 GHz, it is necessary to consider alternate solutions to avoid unreasonably small inductor and capacitor values.

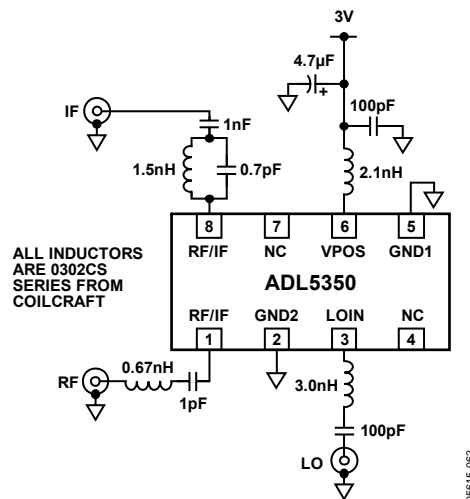


Figure 61. 2560 MHz to 2660 MHz RF Downconversion Schematic

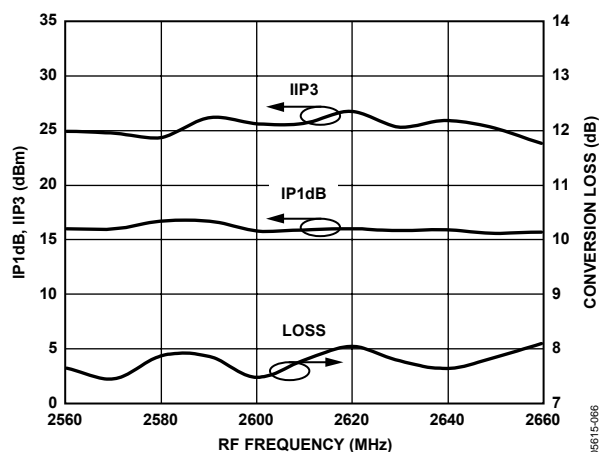


Figure 62. Measured Performance for Circuit in Figure 61 Using Low-Side LO Injection and 374 MHz IF

The typical networks used for cellular applications below 2.6 GHz use band-select and band-reject networks on the RF and IF ports. At higher RF frequencies, these networks are not easily realized by using lumped element components. As a result, it is necessary to consider alternate filter network topologies to allow more reasonable values for inductors and capacitors.

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Figure 63 depicts a crossover filter network approach to provide isolation between the RF and IF ports for a downconverting application. The crossover network essentially provides a high-pass filter to allow the RF signal to pass to the RF/IF node (Pin 1 and Pin 8), while presenting a low-pass filter (which is actually a band-pass filter when considering the dc blocking capacitor, C_{AC}). This allows the difference component ($f_{RF} - f_{LO}$) to be passed to the desired IF load.

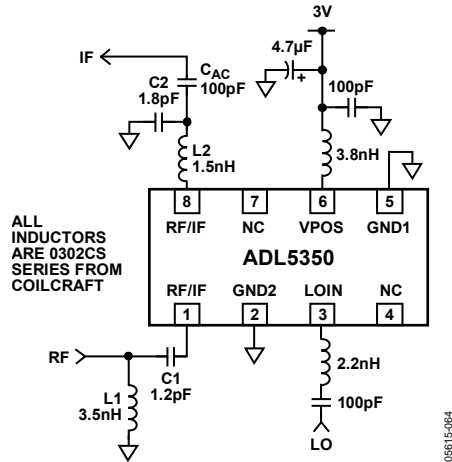


Figure 63. 3.3 GHz to 3.8 GHz RF Downconversion Schematic

When designing the RF port and IF port networks, it is important to remember that the networks share a common node (the RF/IF pins). In addition, the opposing network presents some loading impedance to the target network being designed.

Classic audio crossover filter design techniques can be applied to help derive component values. However, some caution must be applied when selecting component values. At high RF frequencies, the board parasitics can significantly influence the final optimum inductor and capacitor component selections. Some empirical testing may be necessary to optimize the RF and IF port filter networks. The performance of the circuit depicted in Figure 63 is provided in Figure 64.

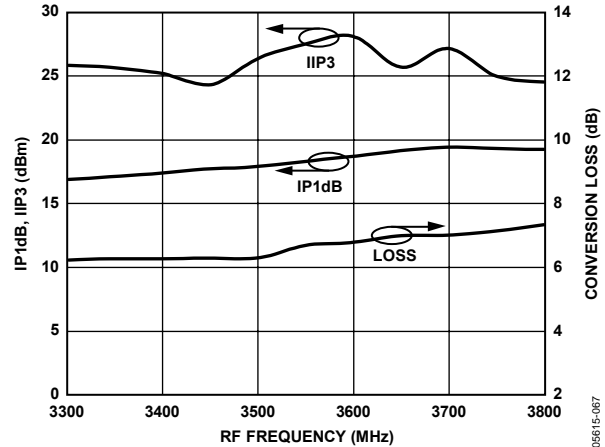


Figure 64. Measured Performance for Circuit in Figure 63 Using Low-Side LO Injection and 800 MHz IF

EVALUATION BOARD

An evaluation board is available for the ADL5350. The evaluation board has two halves: a low band board designated as Board A and a high band board designated as Board B. The schematic for the evaluation board is shown in Figure 65.

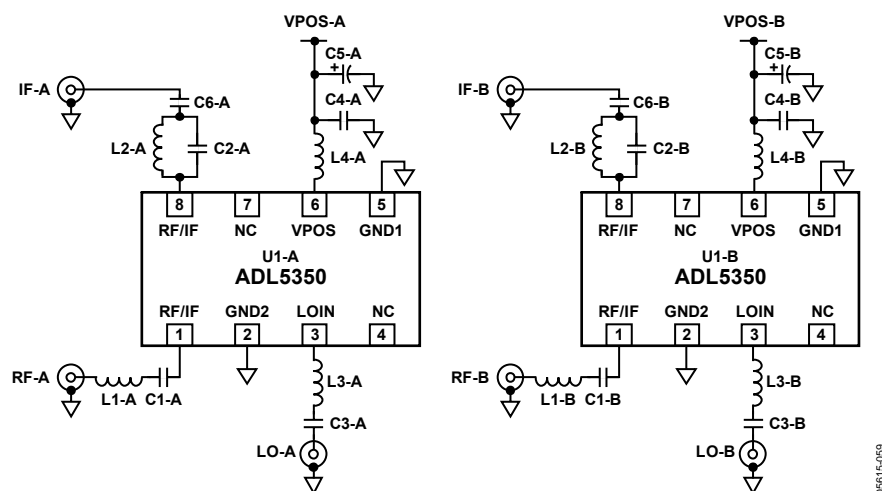


Figure 65. Evaluation Board

Table 9. Evaluation Board Configuration Options

Component	Function	Default Conditions
C4-A, C4-B, C5-A, C5-B	Supply Decoupling. C4-A and C4-B provide local bypassing of the supply. C5-A and C5-B are used to filter the ripple of a noisy supply line. These are not always necessary.	C4-A = C4-B = 100 pF, C5-A = C5-B = 4.7 μ F
L1-A, L1-B, C1-A, C1-B	RF Input Network. Designed to provide series resonance at the intended RF frequency.	L1-A = 6.8 nH (0603CS from Coilcraft), L1-B = 1.7 nH (0302CS from Coilcraft), C1-A = 4.7 pF, C1-B = 1.5 pF
L2-A, L2-B, C2-A, C2-B, C6-A, C6-B	IF Output Network. Designed to provide parallel resonance at the geometric mean of the RF and LO frequencies.	L2-A = 4.7 nH (0603CS from Coilcraft), L2-B = 1.7 nH (0302CS from Coilcraft), C2-A = 5.6 pF, C2-B = 1.2 pF, C6-A = C6-B = 1 nF
L3-A, L3-B, C3-A, C3-B	LO Input Network. Designed to block dc and optimize LO voltage swing at LOIN.	L3-A = 8.2 nH (0603CS from Coilcraft), L3-B = 3.5 nH (0302CS from Coilcraft), C3-A = C3-B = 100 pF
L4-A, L4-B	LO Buffer Amplifier Choke. Provides bias and ac loading impedance to LO buffer amplifier.	L4-A = 24 nH (0603CS from Coilcraft), L4-B = 3.8 nH (0302CS from Coilcraft)

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OUTLINE DIMENSIONS

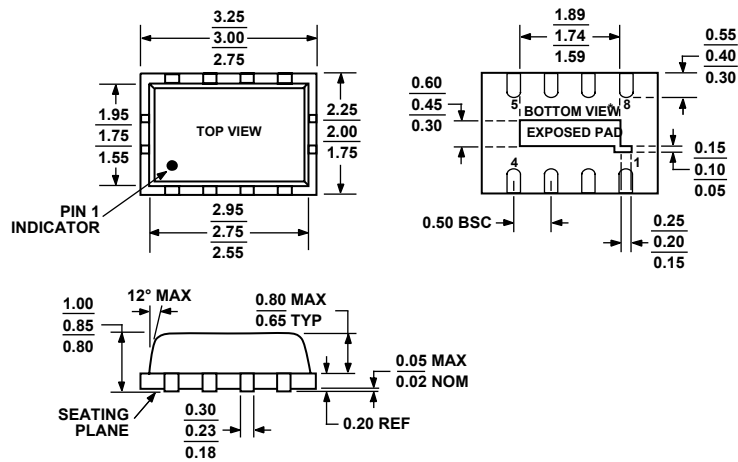


Figure 66. 8-Lead Lead Frame Chip Scale Package [LFCSP_VD]
 2 mm × 3 mm Body, Very Thin, Dual Lead
 (CP-8-1)
 Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding	Ordering Quantity
ADL5350ACPZ-R7 ¹	-40°C to +85°C	8-Lead Lead Frame Chip Scale Package [LFCSP_VD]	CP-8-1	08	3000, Reel
ADL5350ACPZ-WP ¹	-40°C to +85°C	8-Lead Lead Frame Chip Scale Package [LFCSP_VD]	CP-8-1	08	50, Waffle Pack
ADL5350-EVALZ ¹		Evaluation Board			

¹ Z = RoHS Compliant Part.

NOTES

ADL5350

NOTES