

FET BIAS CONTROLLER WITH POLARISATION SWITCH AND TONE DETECTION

ISSUE 2 - FEBRUARY 2000

ZNBG3210
ZNBG3211

DEVICE DESCRIPTION

The ZNBG series of devices are designed to meet the bias requirements of GaAs and HEMT FETs commonly used in satellite receiver LNBS, PMR cellular telephones etc. with a minimum of external components.

With the addition of two capacitors and a resistor the devices provide drain voltage and current control for three external grounded source FETs, generating the regulated negative rail required for FET gate biasing whilst operating from a single supply. This negative bias, at -3 volts, can also be used to supply other external circuits.

The ZNBG3210/11 includes bias circuits to drive up to three external FETs. A control input to the device selects either one of two FETs as operational using 0V gate switching methodology, the third FET is permanently active. This feature is particularly used as an LNB polarisation switch. Also specific to LNB applications is the enhanced 22kHz tone detection and logic output feature which is used to enable high and low band frequency switching. The detector has been specifically designed to reject interference such as low frequency signals and DiSEqC™ tone bursts - without the use of additional external components.

Drain current setting of the ZNBG3210/11 is user selectable over the range 0 to 15mA, this

is achieved with the addition of a single resistor. The series also offers the choice of FET drain voltage, the 3210 gives 2.2 volts drain whilst the 3211 gives 2 volts.

These devices are unconditionally stable over the full working temperature with the FETs in place, subject to the inclusion of the recommended gate and drain capacitors. These ensure RF stability and minimal injected noise.

It is possible to use less than the devices full complement of FET bias controls, unused drain and gate connections can be left open circuit without affecting operation of the remaining bias circuits.

In order to protect the external FETs the circuits have been designed to ensure that, under any conditions including power up/down transients, the gate drive from the bias circuits cannot exceed the range -3.5V to 1V. Furthermore if the negative rail experiences a fault condition, such as overload or short circuit, the drain supply to the FETs will shut down avoiding excessive current flow.

The ZNBG3210/11 are available in QSOP20 for the minimum in device size. Device operating temperature is -40 to 70°C to suit a wide range of environmental conditions.

FEATURES

- Provides bias for GaAs and HEMT FETs
- Drives up to three FETs
- Dynamic FET protection
- Drain current set by external resistor
- Regulated negative rail generator requires only 2 external capacitors
- Choice in drain voltage
- Wide supply voltage range
- Polarisation switch for LNBS - supporting zero volt gate switching topology.
- 22kHz tone detection for band switching
- Compliant with ASTRA control specifications
- QSOP surface mount package

APPLICATIONS

- Satellite receiver LNBS
- Private mobile radio (PMR)
- Cellular telephones

ZNBG3210

ZNBG3211

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.6V to 12V	Power Dissipation ($T_{amb}=25^{\circ}\text{C}$)	
Supply Current	100mA	QSOP20	500mW
Input Voltage (V_{POL})	25V Continuous		
Drain Current (per FET) (set by R_{CAL})	0 to 15mA		
Operating Temperature	-40 to 70°C		
Storage Temperature	-50 to 85°C		

ELECTRICAL CHARACTERISTICS. TEST CONDITIONS

(Unless otherwise stated): $T_{amb}=25^{\circ}\text{C}$, $V_{CC}=5\text{V}$, $I_D=10\text{mA}$ ($R_{CAL}=33\text{k}\Omega$)

SYMBOL	PARAMETER	CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
V_{CC}	Supply Voltage		5		10	V
I_{CC}	Supply Current	I_{D1} to $I_{D3}=0$ $I_{D1}=0, I_{D2}$ to $I_{D3}=10\text{mA}$, $V_{POL}=14\text{V}$ $I_{D2}=0, I_{D1}$ to $I_{D3}=10\text{mA}$, $V_{POL}=15.5\text{V}$ I_{D1} to $I_{D3}=0$, $I_{LB}=10\text{mA}$ I_{D1} to $I_{D3}=0$, $I_{HB}=10\text{mA}$		6 25 25 16 16	15 35 35 25 25	mA mA mA mA mA
V_{SUB}	Substrate Voltage	(Internally generated) $I_{SUB}=0$ $I_{SUB}=-200\mu\text{A}$	-3.5	-3.0	-2.5 -2.4	V V
E_{ND} E_{NG}	Output Noise Drain Voltage Gate Voltage	$C_G=4.7\text{nF}$, $C_D=10\text{nF}$ $C_G=4.7\text{nF}$, $C_D=10\text{nF}$			0.02 0.005	Vpkpk Vpkpk
f_O	Oscillator Frequency		200	350	800	kHz

ZNBG3210 ZNBG3211

SYMBOL	PARAMETER	CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	

GATE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
I_{GO}	Output Current Range		-30		2000	μA
		I_{Dx} V_{POL} I_{GOx} (mA) (V) (μA)				
V_{G1O} V_{G1L} V_{G1H}	Output Voltage Gate 1 Off Low High	$I_{D1}=0$ $V_{POL}=14$ $I_{GO1}=0$ $I_{D1}=12$ $V_{POL}=15.5$ $I_{GO1}=-10$ $I_{D1}=8$ $V_{POL}=15.5$ $I_{GO1}=0$	-0.05 -2.7 0.4	0 -2.4 0.75	0.05 -2.0 1.0	V V V
V_{G2O} V_{G2L} V_{G2H}	Output Voltage Gate 2 Off Low High	$I_{D2}=0$ $V_{POL}=15.5$ $I_{GO2}=0$ $I_{D2}=12$ $V_{POL}=14$ $I_{GO2}=-10$ $I_{D2}=8$ $V_{POL}=14$ $I_{GO2}=0$	-0.05 -2.7 0.4	0 -2.4 0.75	0.05 -2.0 1.0	V V V
V_{G3L} V_{G3H}	Output Voltage Gate 3 Low High	$I_{D3}=12$ $I_{GO3}=-10$ $I_{D3}=8$ $I_{GO3}=0$	-3.5 0.4	-2.9 0.75	-2.0 1.0	V V

DRAIN CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	8	10	12	UNITS
I_D	Current					mA
ΔI_{DV} ΔI_{DT}	Current Change with V_{CC} with T_j	$V_{CC}=5$ to $10V$ $T_j=-40$ to $+70^\circ C$		0.5 0.05		%/V %/°C
V_{D1}	Drain 1 Voltage: High ZNBG3210 ZNBG3211	$I_{D1}=10mA$, $V_{POL}=15.5V$ $I_{D1}=10mA$, $V_{POL}=15.5V$	2.0 1.8	2.2 2.0	2.4 2.2	V V
V_{D2}	Drain 2 Voltage: High ZNBG3210 ZNBG3211	$I_{D2}=10mA$, $V_{POL}=14V$ $I_{D2}=10mA$, $V_{POL}=14V$	2.0 1.8	2.2 2.0	2.4 2.2	V V
V_{D3}	Drain 3 Voltage: High ZNBG3210 ZNBG3211	$I_{D3}=10mA$ $I_{D3}=10mA$	2.0 1.8	2.2 2.0	2.4 2.2	V V
ΔV_{DV} ΔV_{DT}	Voltage Change with V_{CC} with T_j	$V_{CC}=5$ to $10V$ $T_j=-40$ to $+70^\circ C$		0.5 50		%/V ppm
I_{L1} I_{L2}	Leakage Current Drain 1 Drain 2	$V_{D1}=0.5V$, $V_{POL}=14V$ $V_{D2}=0.5V$, $V_{POL}=15.5V$			10 10	μA μA

ZNBG3210

ZNBG3211

SYMBOL	PARAMETER	CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	

tone DETECTION CHARACTERISTICS

I_B	Filter Amplifier Input Bias Current	$R_{F1}=150k\Omega$	0.02	0.07	0.25	μA
V_{OUT}	Output Voltage ⁵	$R_{F1}=150k\Omega$	1.75	1.95	2.05	V
I_{OUT}	Output Current ⁵	$V_{OUT}=1.96V, V_{FIN}=2.1V$	400	520	650	μA
G_V	Voltage Gain	$f=22kHz, V_{IN}=1mV$		46		dB
f_R ⁸	Rejection Frequency	$V_{(AC)in}=1V$ p/p sq.w ⁶	1.0	7.5		kHz
V_{LOV}	Output Stage L_{OV} Volt. Range	$I_L=50mA(L_B$ or $H_B)$	-0.5		$V_{CC}-1.8$	V
I_{LOV}	L_{OV} Bias Current	$V_{LOV}=0$	0.02	0.15	1.0	μA
V_{LBL}	L_B Output Low	$V_{LOV}=0$ $I_L=-10\mu A$ Enabled ⁶ $V_{LOV}=3V$ $I_L=0$ Enabled ⁷	-3.5 -0.01	-2.75 0	-2.5 0.01	V V
V_{LBH}	L_B Output High	$V_{LOV}=0$ $I_L=10mA$ Disabled ⁶ $V_{LOV}=3V$ $I_L=50mA$ Disabled ⁷	-0.025 2.9	0 3.0	0.025 3.1	V V
V_{HBL}	H_B Output Low	$V_{LOV}=0$ $I_L=-10\mu A$ Disabled ⁶ $V_{LOV}=3V$ $I_L=0$ Disabled ⁷	-3.5 -0.01	-2.75 0	-2.5 0.01	V V
V_{HBH}	H_B Output High	$V_{LOV}=0$ $I_L=10mA$ Enabled ⁶ $V_{LOV}=3V$ $I_L=50mA$ Enabled ⁷	-0.025 2.9	0 3.0	0.025 3.1	V V

POLARITY SWITCH CHARACTERISTICS

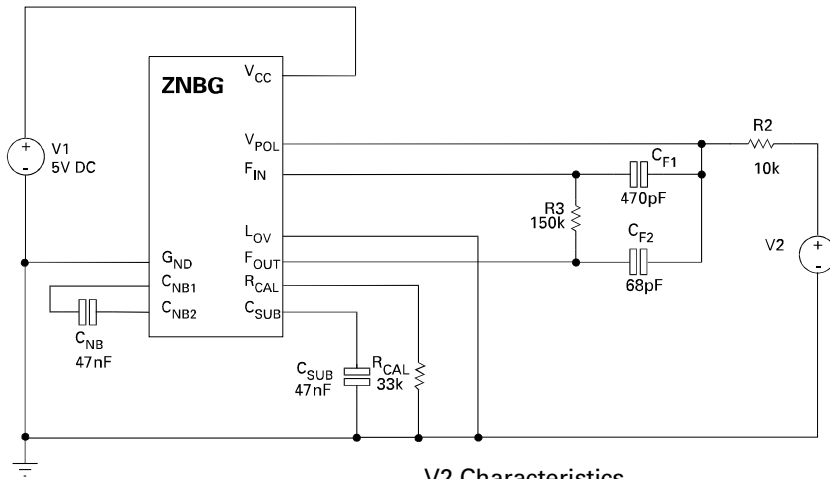
I_{POL}	Input Current	$V_{POL}=25V$ (Applied via $R_{POL}=10k\Omega$)	10	20	40	μA
V_{TPOL}	Threshold Voltage	$V_{POL}=25V$ (Applied via $R_{POL}=10k\Omega$)	14	14.75	15.5	V
T_{SPOL}	Switching Speed	$V_{POL}=25V$ (Applied via $R_{POL}=10k\Omega$)			100	ms

NOTES:

1. The negative bias voltages specified are generated on-chip using an internal oscillator. Two external capacitors, C_{NB} and C_{SUB} , of 47nF are required for this purpose.
2. The characteristics are measured using an external reference resistor R_{CAL} of value 33k wired from pins R_{CAL} to ground.
3. Noise voltage is not measured in production.
4. Noise voltage measurement is made with FETs and gate and drain capacitors in place on all outputs. C_G , 4.7nF, are connected between gate outputs and ground, C_D , 10nF, are connected between drain outputs and ground.
5. These parameters are linearly related to V_{CC} .
6. These parameters are measured using Test Circuit 1
7. These parameters are measured using Test Circuit 2
8. The ZNBG32 series will also reject DiSeqC™ and other common switching bursts.

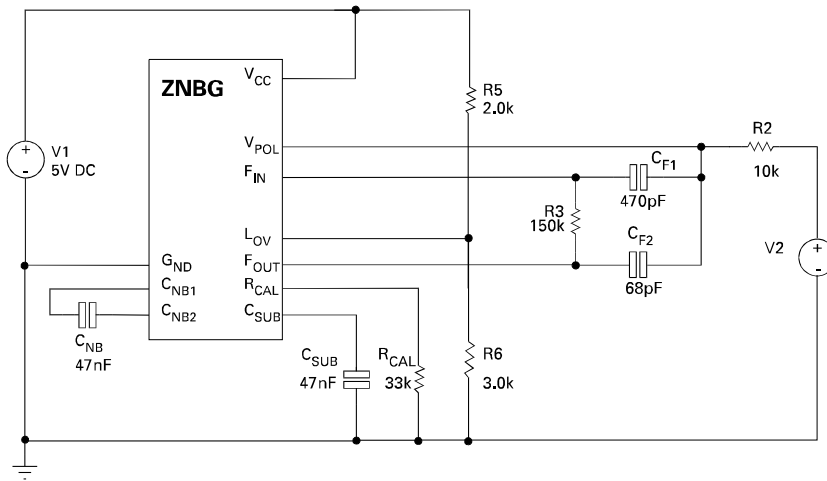
ZNBG3210 ZNBG3211

TEST CIRCUIT 1



V2 Characteristics
 Type AC source
 Frequency 22kHz
 Voltage 350mV p/p enabled
 100mV p/p disabled

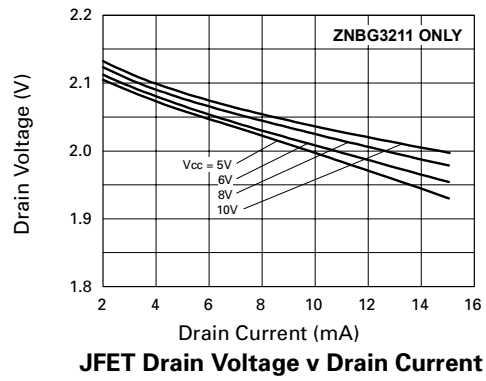
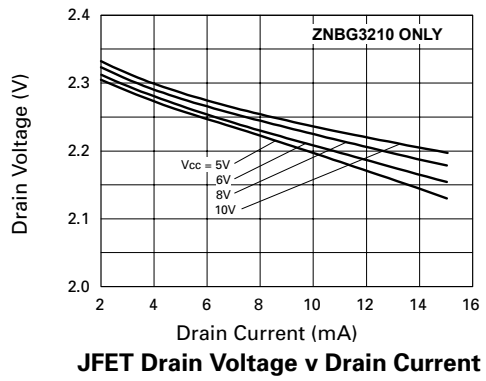
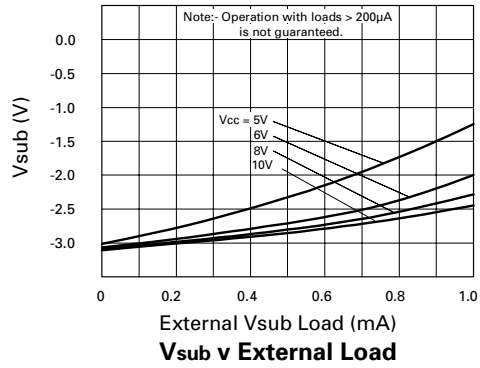
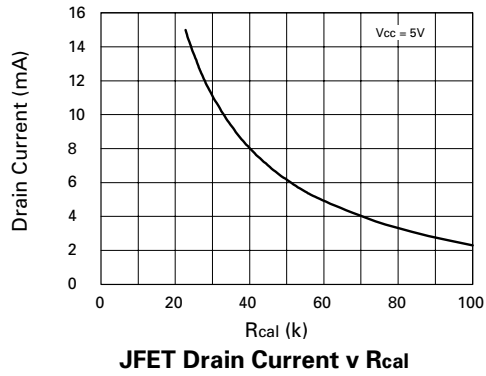
TEST CIRCUIT 2



V2 Characteristics
 Type AC source
 Frequency 22kHz
 Voltage 350mV p/p enabled
 100mV p/p disabled

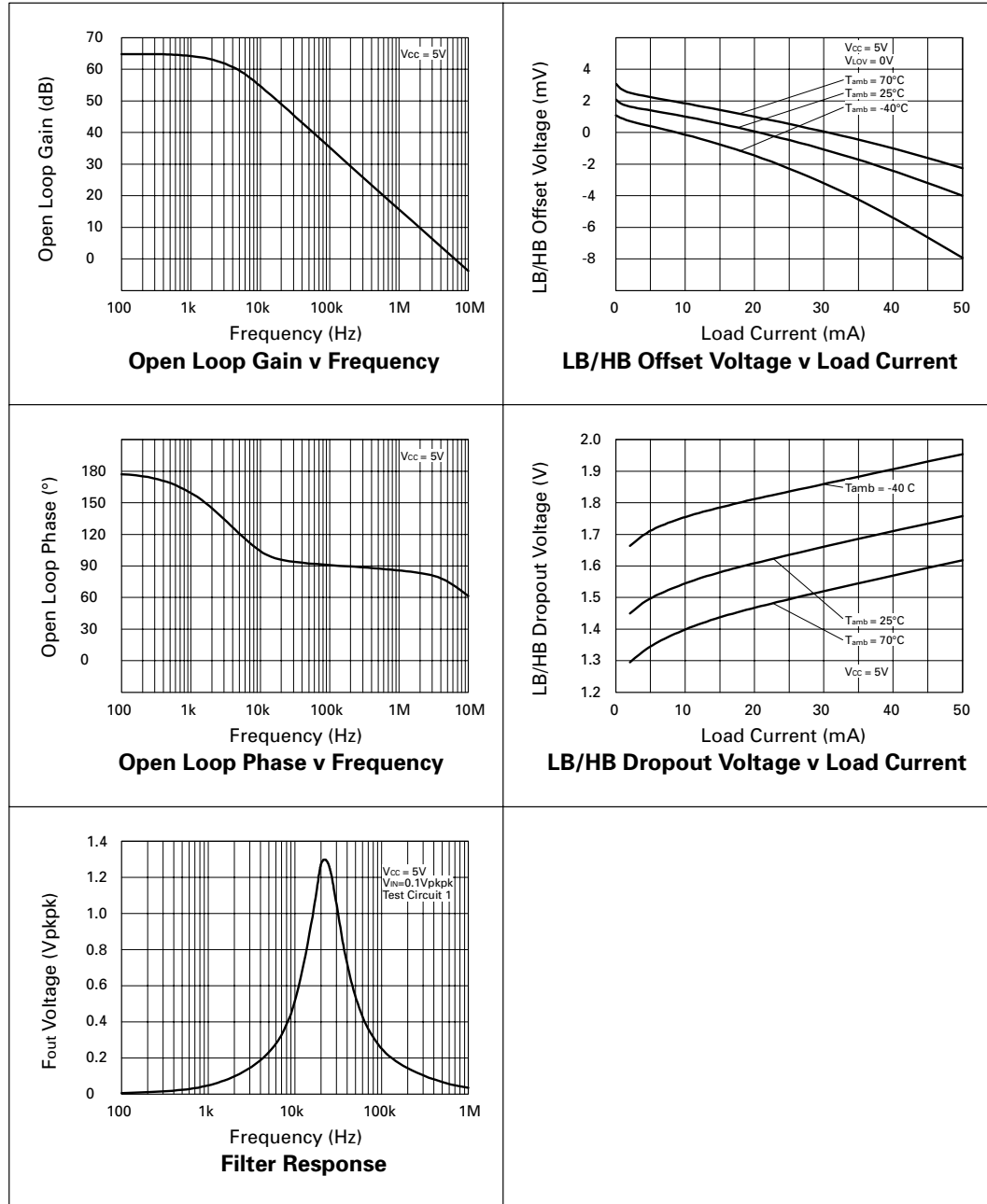
ZNBG3210 ZNBG3211

TYPICAL CHARACTERISTICS



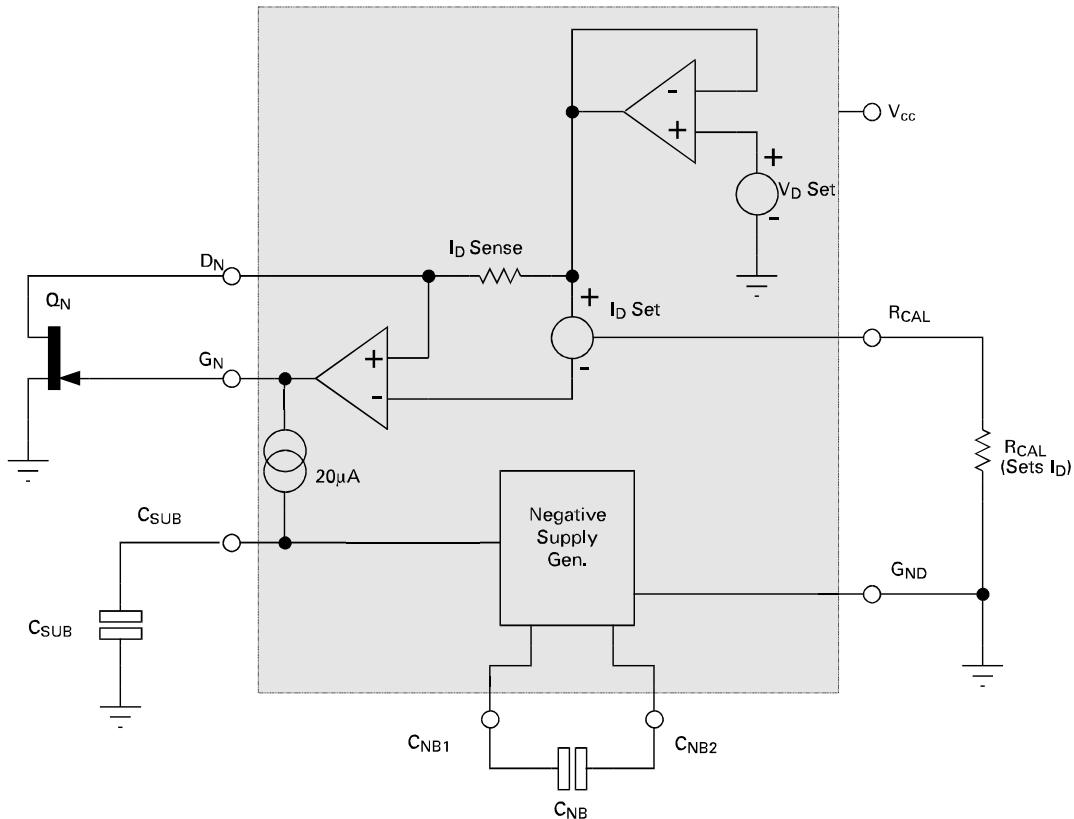
ZNBG3210 ZNBG3211

TYPICAL CHARACTERISTICS



ZNBG3210 ZNBG3211

FUNCTIONAL DIAGRAM



FUNCTIONAL DESCRIPTION

The ZNBG devices provide all the bias requirements for external FETs, including the generation of the negative supply required for gate biasing, from the single supply voltage. The diagram above shows a single stage from the ZNBG series. The ZNBG3210/11 contains 3 such stages. The negative rail generator is common to all devices.

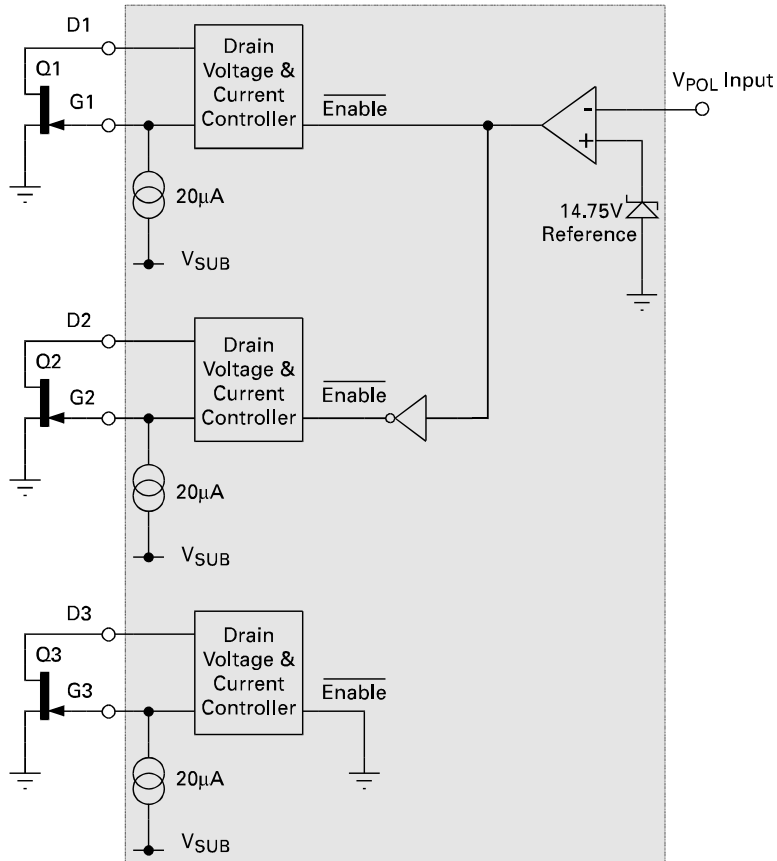
The drain voltage of the external FET Q_N is set by the ZNBG device to its normal operating voltage. This is determined by the on board V_D Set reference, for the ZNBG3210 this is nominally 2.2 volts whilst the ZNBG3211 provides nominally 2 volts.

The drain current taken by the FET is monitored by the low value resistor I_D Sense. The amplifier driving the gate of the FET adjusts the gate voltage of Q_N so that the drain current taken matches the current called for by an external resistor R_{CAL} .

Since the FET is a depletion mode transistor, it is often necessary to drive its gate negative with respect to ground to obtain the required drain current. To provide this capability powered from a single positive supply, the device includes a low current negative supply generator. This generator uses an internal oscillator and two external capacitors, C_{NB} and C_{SUB} .

ZNBG3210 ZNBG3211

The following schematic shows the function of the V_{POL} input. Only one of the two external FETs numbered Q1 and Q2 are powered at any one time, their selection is controlled by the input V_{POL} . This input is designed to be wired to the power input of the LNB via a high value (10k) resistor. With the input voltage of the LNB set at or below 14V, FET Q2 will be enabled. With the input voltage at or above 15.5V, FET Q1 will be enabled. The disabled FET has its gate driven to 0V and its drain terminal is switched open circuit. FET number Q3 is always active regardless of the voltage applied to V_{POL} .

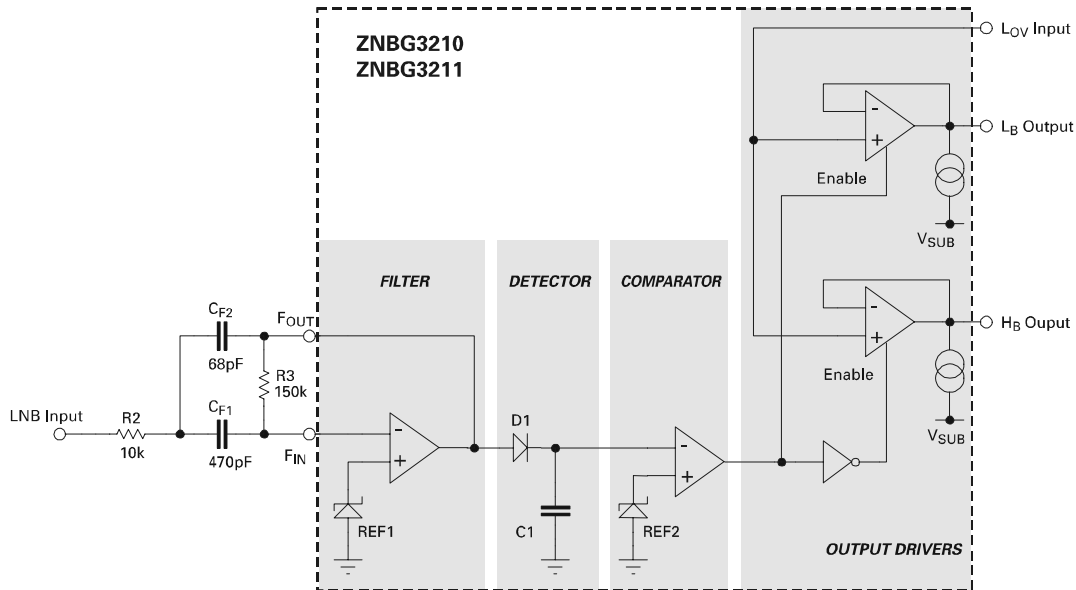


Control Input Switch Function

Input Sense	Polarisation	Select
$\ll \leq 14$ volts	Vertical	FET Q2
≥ 15.5 volts	Horizontal	FET Q1

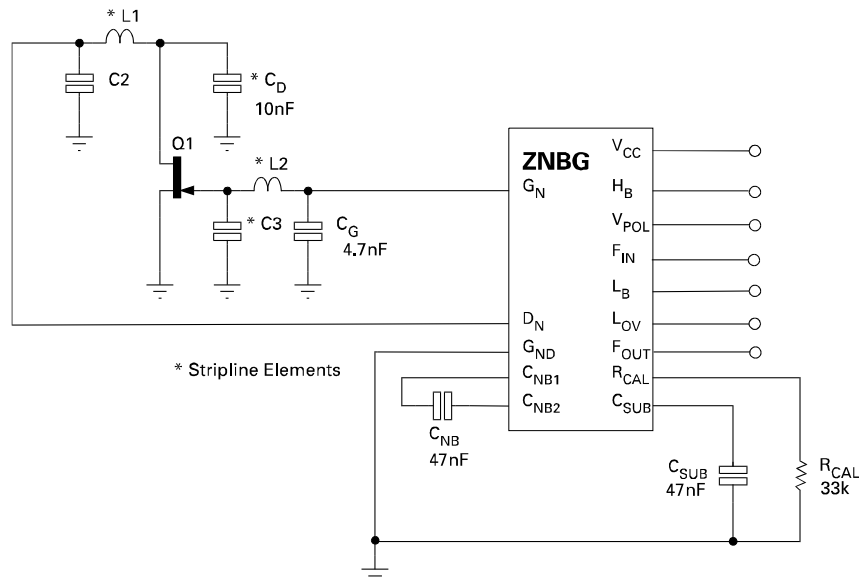
ZNBG3210 ZNBG3211

For many LNB applications tone detection and band switching is required. The ZNBG3210/11 includes the circuitry necessary to detect the presence of a 22kHz tone modulated on the supply input to the LNB. Referring to the following schematic diagram, the main elements of this detector are an op-amp enabling the construction of a Sallen Key filter, a rectifier/smoother and a comparator. Full control is given over the centre frequency and bandwidth of the filter by the selection of two external resistors and capacitors (one of these resistors, R2, shares the function of overvoltage protection of pin V_{POL}). The detector used in the ZNBG32 series has been specifically designed to reject low frequency signals, DiSEqC™ tone bursts and other common interference signals that may be present on the LNB supply input. This has been achieved without the need for any additional external components.



ZNBG3210 ZNBG3211

APPLICATIONS CIRCUIT



APPLICATIONS INFORMATION

The above is a partial application circuit for the ZNBG series showing all external components required for appropriate biasing. The bias circuits are unconditionally stable over the full temperature range with the associated FETs and gate and drain capacitors in circuit.

Capacitors C_D and C_G ensure that residual power supply and substrate generator noise is not allowed to affect other external circuits which may be sensitive to RF interference. They also serve to suppress any potential RF feedthrough between stages via the ZNBG device. These capacitors are required for all stages used. Values of 10nF and 4.7nF respectively are recommended however this is design dependent and any value between 1nF and 100nF could be used.

The capacitors C_{NB} and C_{SUB} are an integral part of the ZNBGs negative supply generator. The negative bias voltage is generated on-chip using an internal oscillator. The required value of capacitors C_{NB} and C_{SUB} is 47nF. This generator produces a low current supply of approximately -3 volts. Although this generator is intended purely to bias the external FETs, it can be used to power other external circuits via the C_{SUB} pin.

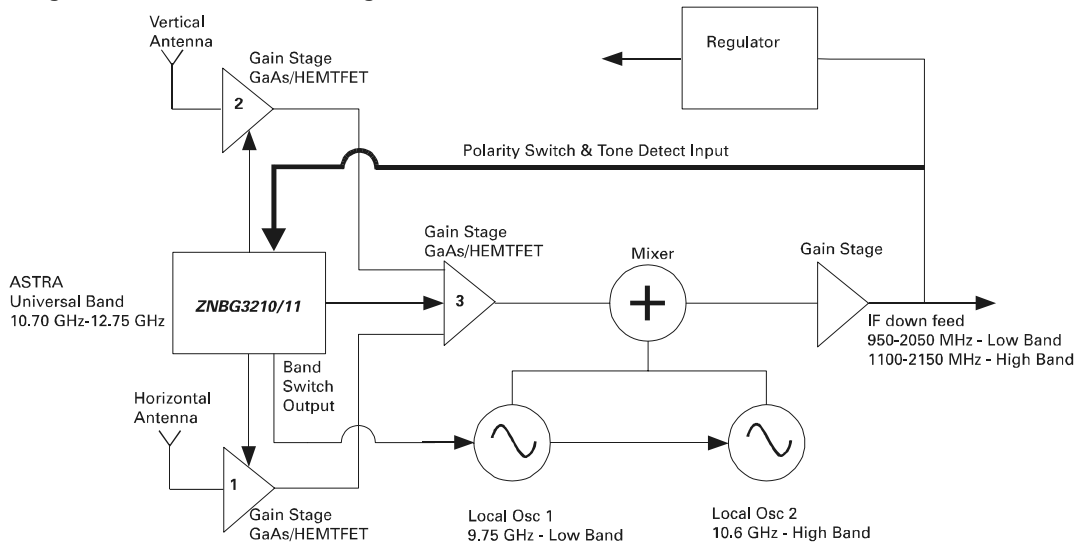
Resistor R_{CAL} sets the drain current at which all external FETs are operated. If any bias control circuit is not required, its related drain and gate connections may be left open circuit without affecting the operation of the remaining bias circuits.

The ZNBG devices have been designed to protect the external FETs from adverse operating conditions. With a JFET connected to any bias circuit, the gate output voltage of the bias circuit can not exceed the range -3.5V to 1V under any conditions, including powerup and powerdown transients. Should the negative bias generator be shorted or overloaded so that the drain current of the external FETs can no longer be controlled, the drain supply to FETs is shut down to avoid damage to the FETs by excessive drain current.

ZNBG3210 ZNBG3211

The following block diagram shows the main section of an LNB designed for use with the Astra series of satellites. The ZNBG3210/11 is the core bias and control element of this circuit. The ZNBG provides the negative rail, FET bias control, polarisation switch control, tone detection and band switching with the minimum of external components. Compared to other discrete component solutions the ZNBG circuit reduces component count and overall size required.

Single Universal LNB Block Diagram



Tone detection and band switching is provided on the ZNBG3210/11 devices. The following diagrams describes how this feature operates in an LNB and the external components required. The presence or absence of a 22kHz tone applied to pin F_{IN} enables one of two outputs, L_B and H_B . A tone present enables H_B and tone absent enables L_B . The L_B and H_B outputs are designed to be compatible with both MMIC and discrete local oscillator applications, selected by pin L_{OV} . Referring to Figure 1 wiring pin L_{OV} to ground will force L_B and H_B to switch between -2.6V (disabled) and 0V (enabled). Referring to Figure 2 wiring pin L_{OV} to a positive voltage source (e.g. a potential divider across V_{CC} and ground set to the required oscillator supply voltage, V_{OSC}) will force the L_B and H_B outputs to provide the required oscillator supply, V_{OSC} , when enabled.

Tone Detection Function

L_{OV}	F_{IN}	L_B	H_B	L_B	H_B
G_{ND}	22kHz	Disabled	Enabled	-2.6 volts	G_{ND}
	—	Enabled	Disabled	G_{ND}	-2.6 volts
V_{OSC}	22kHz	Disabled	Enabled	Note 1	V_{OSC}
	—	Enabled	Disabled	V_{OSC}	Note 1

Note 1: 0 volts in typical LNB applications but dependent on external circuits.

ZNBG3210 ZNBG3211

APPLICATIONS INFORMATION(cont)

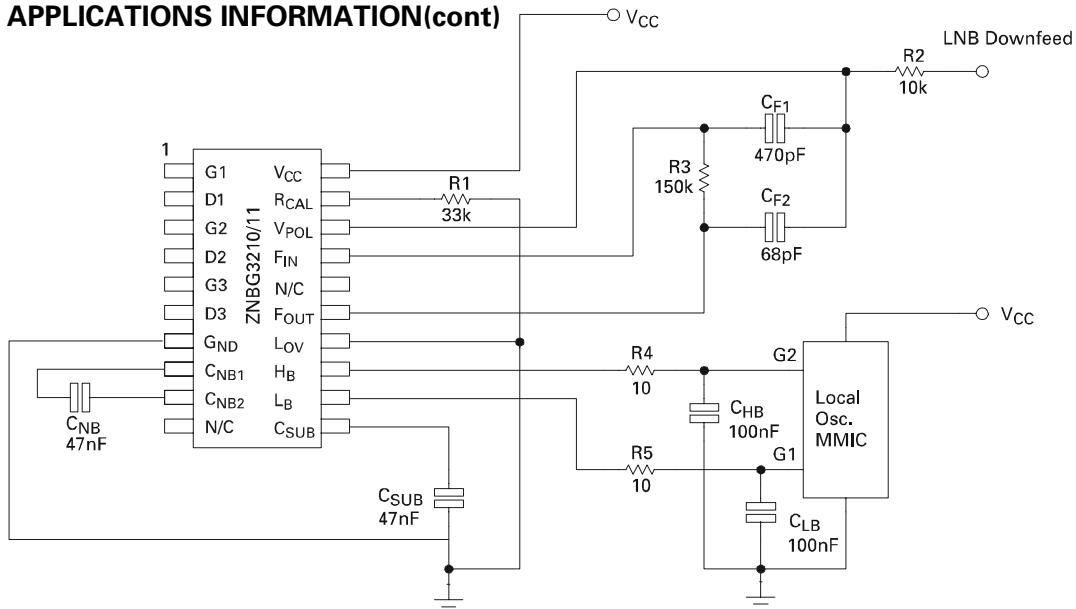


Figure 1
LOV grounded

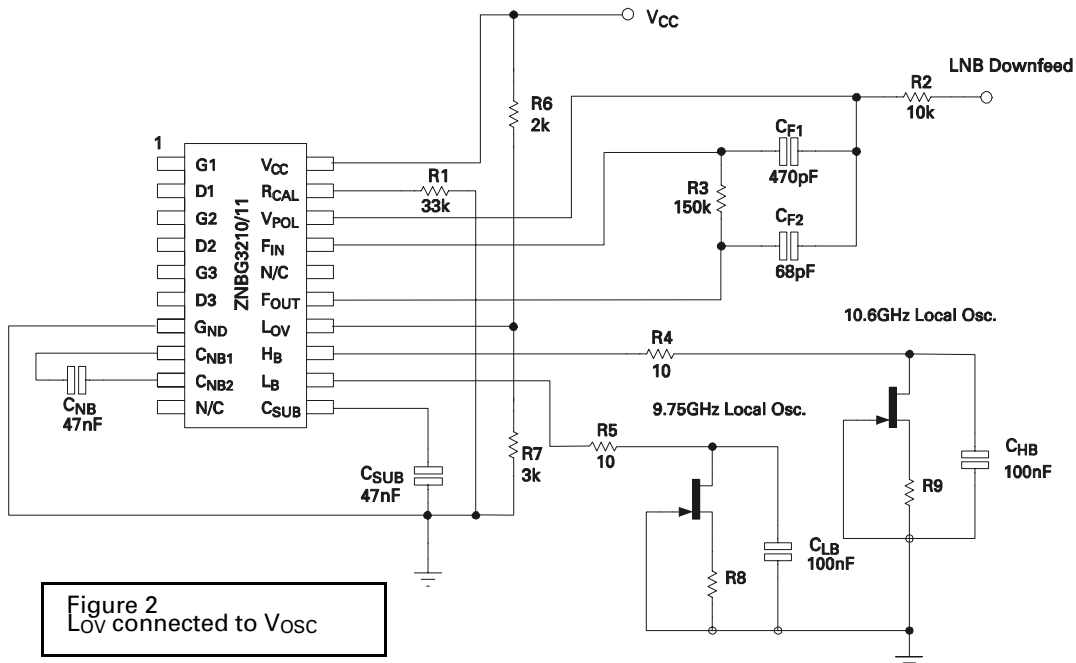
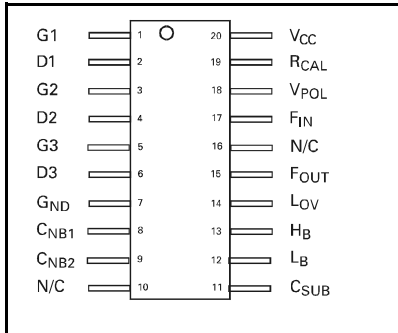


Figure 2
LOV connected to Vosc

ZNBG3210 ZNBG3211

CONNECTION DIAGRAM

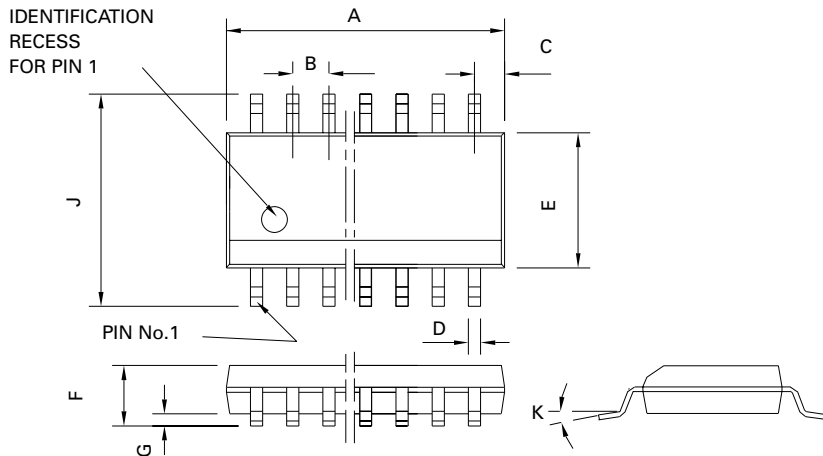


ORDERING INFORMATION

Part Number	Package	Part Mark
ZNBG3210Q20	QSOP20	ZNBG3210
ZNBG3211Q20	QSOP20	ZNBG3211

ZNBG3210 ZNBG3211

PACKAGE DIMENSIONS



PIN	Millimetres		Inches	
	MIN	MAX	MIN	MAX
A	8.55	8.74	0.337	0.344
B	0.635		0.025 NOM	
C	1.42	1.52	0.056	0.06
D	0.20	0.30	0.008	0.012
E	3.81	3.99	0.15	0.157
F	1.35	1.75	0.053	0.069
G	0.10	0.25	0.004	0.01
J	5.79	6.20	0.228	0.244
K	0°	8°	0°	8°



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ZNBG3210
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