NEMO Bluetooth Radio Module

Unigen Corp. Wireless Module Products

NEMO Bluetooth Radio Modules
UGWC621RSMA133

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Revision History

Rev. No.	History	Issue Date	Remarks
1.0	Draft	Dec. 5, 2008	Advanced information; Author: Allen B. Cabreros
1.1	Revision	Aug. 18, 2009	Added dimensional drawings.

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PRODUCT INTRODUCTION

The Nemo Bluetooth radio module enables Bluetooth functionality to any hosted system. Nemo supports Bluetooth version 2.1 with Enhanced Data Rate mode for up to 3Mbps throughput. Nemo's small module footprint and low power consumption makes it attractive for small, handheld, battery powered devices for short range wireless communications. Bluetooth is a cable replacement radio technology. The advanced Bluetooth protocol stack adds seamless, secure, adhoc, point to multi-point communications between other Bluetooth enabled devices regardless of manufacturer. Bluetooth enables personal area networks and short range communications between devices such as portable handhelds, personal computers, embedded devices and industrial communication devices.

FEATURES AND BENEFITS

- Bluetooth v2.1+EDR compliant
- CSR BlueCore 6 ROM
- 2.40-2.480 GHz FHSS Radio
- Max Data Rate 3Mbps
- ±10PPM Crystal Oscillator Included
- 4Mbit High Speed UART Interface
- Single 3.3V Power Supply
- Bluetooth Co-existence Support with 802.11
- Deep Sleep Mode of 40µA With Fast Wake-up

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Applications

- Short Range Radio Systems
- Point-to-Point Systems
- Point-to-Multi-Point Systems
- Cable Replacement
- Portable Devices
- Mobile Phones
- Headsets
- Hand Free Kits
- Personal Computers
- Laptops
- Personal Hand Handhelds
- Remote Controls
- Mouse
- Keyboards
- Human Interface Devices (HID)
- Embedded Devices
- Asset Tracking
- Barcode Scanners
- Data Acquisition Devices

PRODUCT DESCRIPTION

NEMO Module

The Nemo module is a complete 2.4GHz radio transceiver operating in the license free ISM (Industrial, Scientific and Medical) band. The Nemo module has CSR's BlueCore 6 ROM Bluetooth solution. The CSR BlueCore 6 ROM is a single-chip radio and baseband IC for Bluetooth 2.4GHz systems including enhanced data rate (EDR) to 3Mbps. With the on-chip CSR Bluetooth software stack, it provides a fully compliant Bluetooth v2.1 + EDR specification system for data and voice communications. The module dimensions measure 6.5mm x 5.5mm x 1.5mm. A single 3.3V power supply input, single ended RF output/input, and a low 26 pin count makes the NEMO module easy to interface with.

CSR BlueCore 6 ROM Transceiver IC

BlueCore™6-ROM is a single-chip radio and baseband IC for Bluetooth 2.4 GHz systems including enhanced data rates (EDR) to 3Mbits/s. With the on-chip CSR Bluetooth software stack, it provides a fully compliant Bluetooth system to v2.1 of the specification for data and voice communications.

BlueCore6-ROM has been designed to reduce the number of external components required which ensures production costs are minimized. BlueCore6-ROM includes the AuriStream baseband CODEC, which offers significant power reduction over the CVSD based system when used at both ends of the link. The device incorporates auto-calibration and built-in self-test (BIST) routines to simplify development, type approval and production test. All hardware and device firmware is fully compliant with the Bluetooth v2.1 +EDR specification (all mandatory and optional features). To improve the performance of both Bluetooth and 802.11b/g co-located systems a wide range of coexistence features are available including a variety of hardware signaling: basic activity signaling and Intel WCS activity and channel signaling.

Functional Block Diagrams

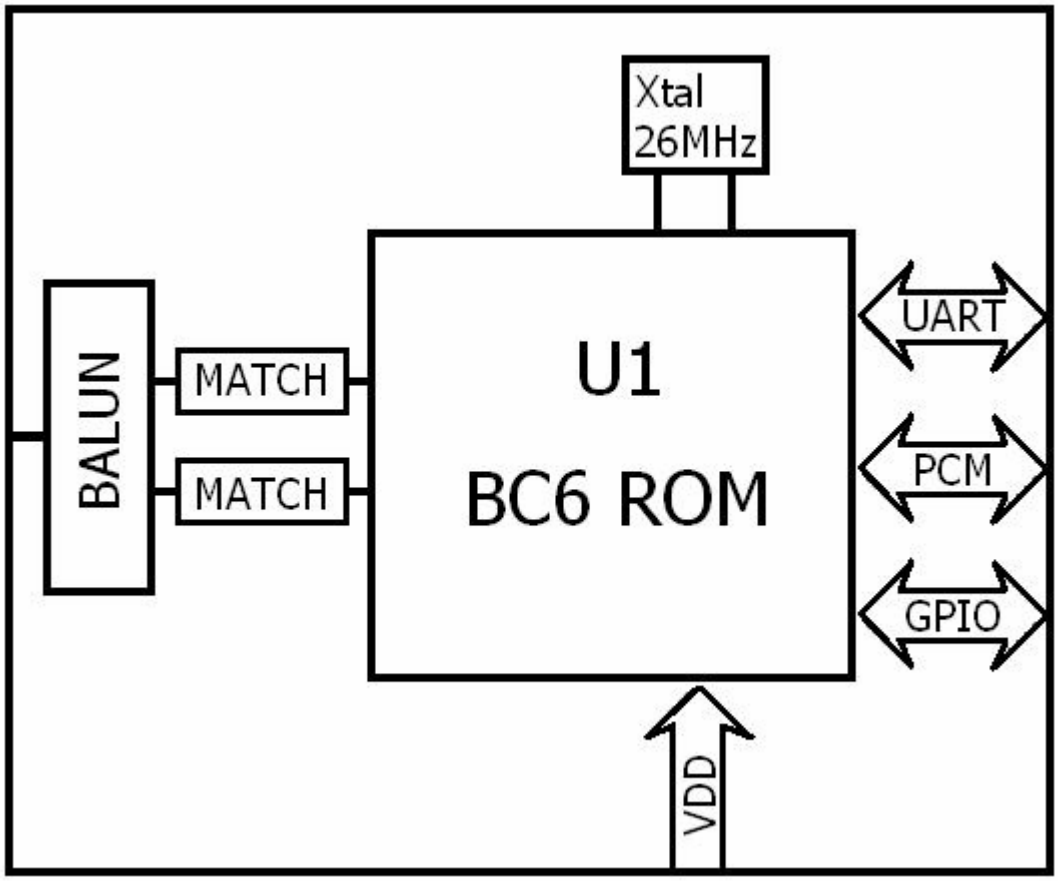

Figure 1: NEMO Module Block Diagram

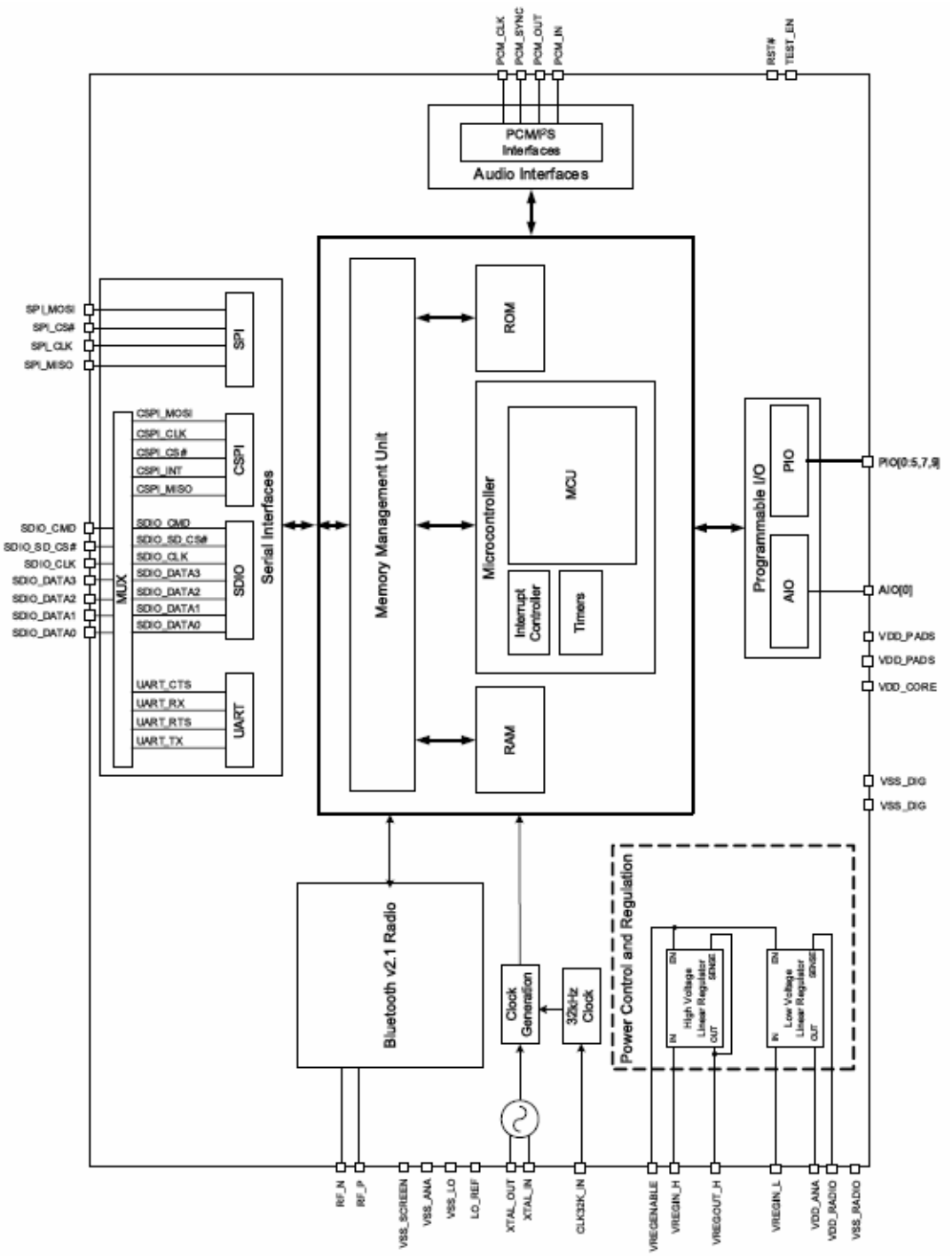

Figure 2: CSR BlueCore 6 ROM Block Diagram

PIN ASSIGNMENT

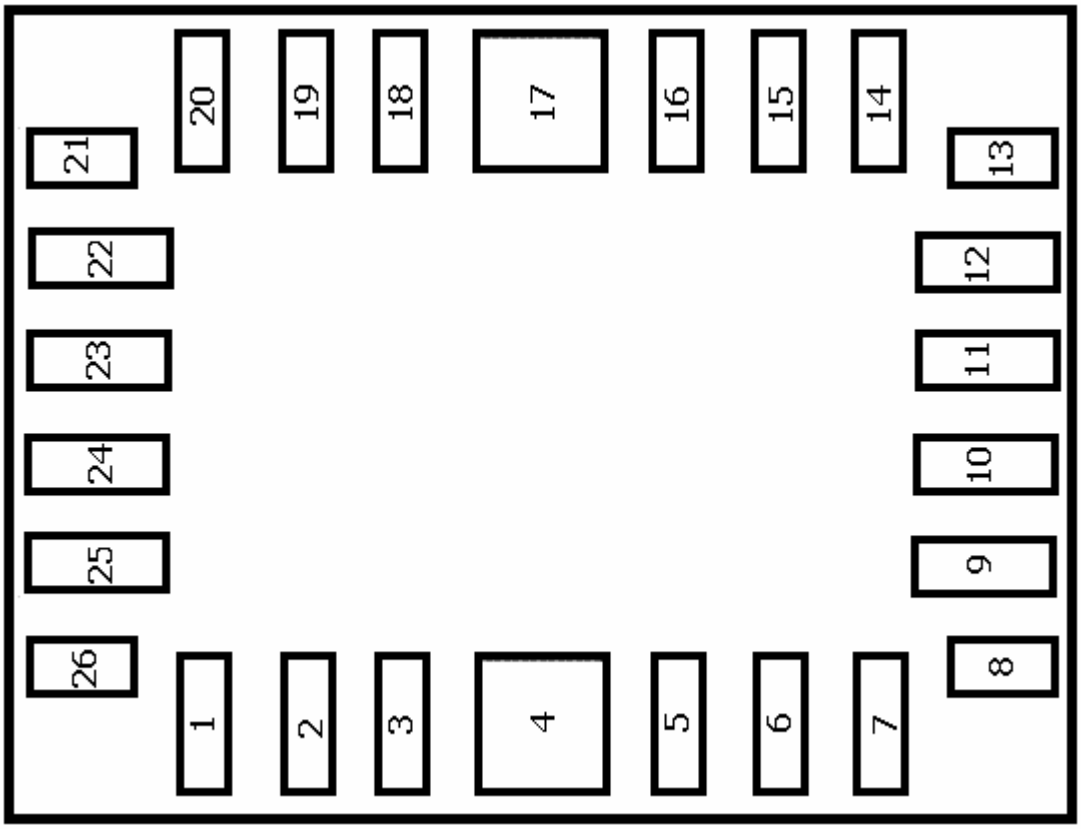

Figure 3: NEMO Module Pin Locations

PIN FUNCTIONS

Table 1: NEMO Pin Functions

Pin	Signal Name	Type	Description
1	BT_CTRL_RTS_N	Output	UART RTS
2	BT_WAKE_P	Input	Module wakeup
3	HOST_WAKE_P	Output	Host device wakeup
4	GND	--	Ground Reference
5	BT_CTRL_RXD_N	Input	UART RXD
6	BT_CTRL_TXD_N	Output	UART TXD
7	BLUETOOTH_TX_CONFIRM	Input	Wi-Fi Coexistence signal
8	BLUETOOTH_TX_REQUEST	Output	Wi-Fi Coexistence signal
9	BLUETOOTH_STATUS	Output	Wi-Fi Coexistence signal
10	GND	--	Ground Reference
11	ANT_OUT	Output	Antenna Output
12	GND	--	Ground Reference
13	BT_PCM_CLK_P	Input	PCM_CLK
14	BT_PCM_RXD_P	Input	PCM RXD serial input
15	BT_PCM_TXD_P	Output	PCM TXD serial output
16	BT_PCM_SYNC_P	Input	PCM SYNC
17	GND	--	Ground Reference
18	BLUETOOTH_LPO_IN	Input	32.768kHz low power clock input
19	BLUETOOTH_RESET_N	Input	Module Reset
20	BT_REG_CTRL_P	Input	Internal regulator enable/disable
21	GND	--	Ground Reference
22	+VBT_IO	Input	I/O Power Supply
23	+VBT	Input	Main supply input
24	+VRF	--	Bypass Capacitor connection for RF VDD.
25	GND	--	Ground Reference
26	BT_CTRL_CTS_N	Input	UART CTS
Note: Active Low signals are designated with an '_N' suffix, and Active High signals are designated with an '_P' suffix.			

ABSOLUTE MAXIMUM RATINGS

Table 2: Absolute Maximum Ratings

Symbol	Definition	Min	Max	Unit
+VBT	Supply Voltage	-0.4	4.9	VDC
+VBT_IO	IO Supply Voltage	-0.4	3.7	VDC
TS	Storage Temperature	-40	+85	°C

These are stress ratings only. Exposure to stresses beyond these maximum ratings may cause permanent damage to, or affect the reliability of this module. Avoid using the module outside the recommended operating conditions defined below. This module is ESD sensitive and should be handled and/or used in accordance with proper ESD mitigation.

RECOMMENDED OPERATING CONDITIONS

Table 3: Recommended Operating Conditions

Symbol	Description	Value			
		Min	Typ	Max	Unit
+VBT	Supply Voltage	2.4	3.3	4.9	VDC
TOC	Operating Temp. Range	-40*	25	85	°C
GND	Ground Voltage	-0.4	0	+0.4	VDC

*Unigen and CSR do not guarantee EDR receiver sensitivity 8DPSK performance below -30ºC.

RF CHARACTERISTICS

Table 4: RF Characteristics

Parameter	Specifications	Units
RF output power	**+ 7**	dBm
Receiver sensitivity	**- 89**	dBm

EXTERNAL SLOW CLOCK SOURCE CHARACTERISTICS

Table 5: External Slow Clock Characteristics

32kHz External Reference Clock	Min	Typ	Max	Units
Frequency	32748	32768	32788	Hz
Frequency deviation at 25ºC	-	-	±20	ppm
Frequency deviation at -30°C to 85°C	-	-	±150	ppm
Input high level, square wave	0.625 x +VBT	-	-	V
Input low level, square wave	-	-	0.425 x +VBT	V
Duty cycle square wave	30	-	70	%
Rise and fall time	-	-	50	ns

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AGENCY CERTIFICATIONS (PRE-SCAN)

TBD

REGULATORY COMPLIANCE STATEMENT

TBD

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FUNCTIONAL OVERVIEW

NEMO Hardware Functional Description

The NEMO is a complete Radio Transceiver Module operating in the license free ISM (Industrial Scientific and Medical) 2.4GHz band. The Nemo module is equipped an external 26MHz crystal oscillator and BALUN for a single ended RF input and output path. NEMO incorporates CSR BlueCore 6 ROM WLCP chipset that is fully compliant to the Bluetooth 2.1 specification with Enhanced Data Rate (EDR) radio for transfers up to 3Mbit throughput.

The Nemo module has uses CSR's BlueCore 6 built in voltage regulator for powering the radio and digital circuitry. The separate IO supply line give the option of running the digital interfaces such as the high speed UART and PCM port at different signal voltages to match the external host MCU's digital interfaces. The built in CSR voltage regulators supplies the 1.8V supply to the radio and digital MCU blocks of the CSR chip.

The module converts CSRs differential RF output and input into a single ended RF path for transmit and receive. Matching circuitry is in line between the CSR device and the BALUN for optimized transmit output and receive sensitivity.

The high speed UART interface, PCM port, GPIO along with WLAN co-existence interface lines are all brought outside of the module. The UART interface communicates with an external host running the upper Bluetooth stack and using the BlueCore Serial Protocol over the Bluetooth defined Host Controller Interface (HCI) layer. The UART is used to send HCI commands and events to and from the external host to the NEMO module.

Asynchronous and Synchronous data is sent between the module and external host via the UART interface as well. Asynchronous data sent and received over an Asynchronous packet switched RF link defined by the Bluetooth specification as "Asynchronous ConnectionLess" (ACL). Synchronous data such as audio data uses "Synchronous Connection Oriented" (SCO) circuit switched RF links defined by the Bluetooth specification. ACL data links can retransmit lost or corrupted data continuously due to the packet switched connection. SCO data can provide fast reliable continuous synchronous data over the circuit-switched RF link.

Synchronous audio data received or transmitted over the air via a Bluetooth SCO connection can be immediately decoded over the air and passed directly through CSR's digital PCM port for audio applications. The module also support I2S digital formats through the same physical PCM port for systems supporting I2S interfaces.

A slow clock 32.768kHz input is brought out for support for Deep Sleep and Standy By low power modes in between radio transmissions. This is used to keep the CSR radio from drifting out of

sync from the remote Bluetooth device during an active connection with “dead silence” and allows BlueCore to enter Deep Sleep low power mode during “dead silence” to conserve power consumption.

NEMO Firmware Functional Description

The Nemo module incorporates the CSR BlueCore 6 ROM chipset and ROM Bluetooth firmware. The firmware controls the CSR internal MCU, IO handling, radio control and also incorporates the lower Bluetooth protocol stack. The lower stack includes the Link Controller (LC), Link Manager or Link Manager Protocol (LM, LMP), Bluetooth radio Baseband (BB). These Bluetooth protocol stack components are all qualified to the Bluetooth v2.1+ EDR specification supporting all features such as Adaptive Frequency Hopping “AFH”, low power mode link modes (Hold, Sniff, Park) end Extended Synchronous Connection Oriented (eSCO) links.

The lower stack is a prequalified Bluetooth component. This means that the lower stack and baseband has already been tested and recognized by the Bluetooth Special Interest Group (SIG) as a working qualified software stack. No further testing of these lower stack components are necessary when seeking Bluetooth qualification. Protocol Implementation Conformance Statement (PICS) can be obtained from CSR or the Bluetooth SIG and submitted for these particular test cases and bypassed.

The firmware is burned into ROM within the CSR BlueCore 6 chipset. There is no need to load the firmware from an external memory device or from the host via a communication interface. The Nemo module and CSR chipset is initialized via a small subset of registers (PSKEYS) that can easily be programmed via the UART interface. These PSKEYS configure and control the radio behavior, interfaces (UART baud rate, PCM settings, etc), and holds information such as the Bluetooth address and country code of operation. Detailed descriptions of the necessary PSKEY that need to be set are discussed later in this document.

CSR BLUETOOTH SOFTWARE STACK

NEMO is supplied with the CSR BlueCore 6 ROM chip. CSR's BlueCOre 6 ROM contains the lower layers of the Bluetooth stack. The stack is Bluetooth v2.1+EDR compliant and runs on the internal RISC microcontroller within BlueCore. The implementation shown below illustrates the internal processor of BlueCore running the Bluetooth stack up to the Host Controller Interface (HCI). The external host processor, external to NEMO, must provide all the upper layers of the Bluetooth stack including the application.

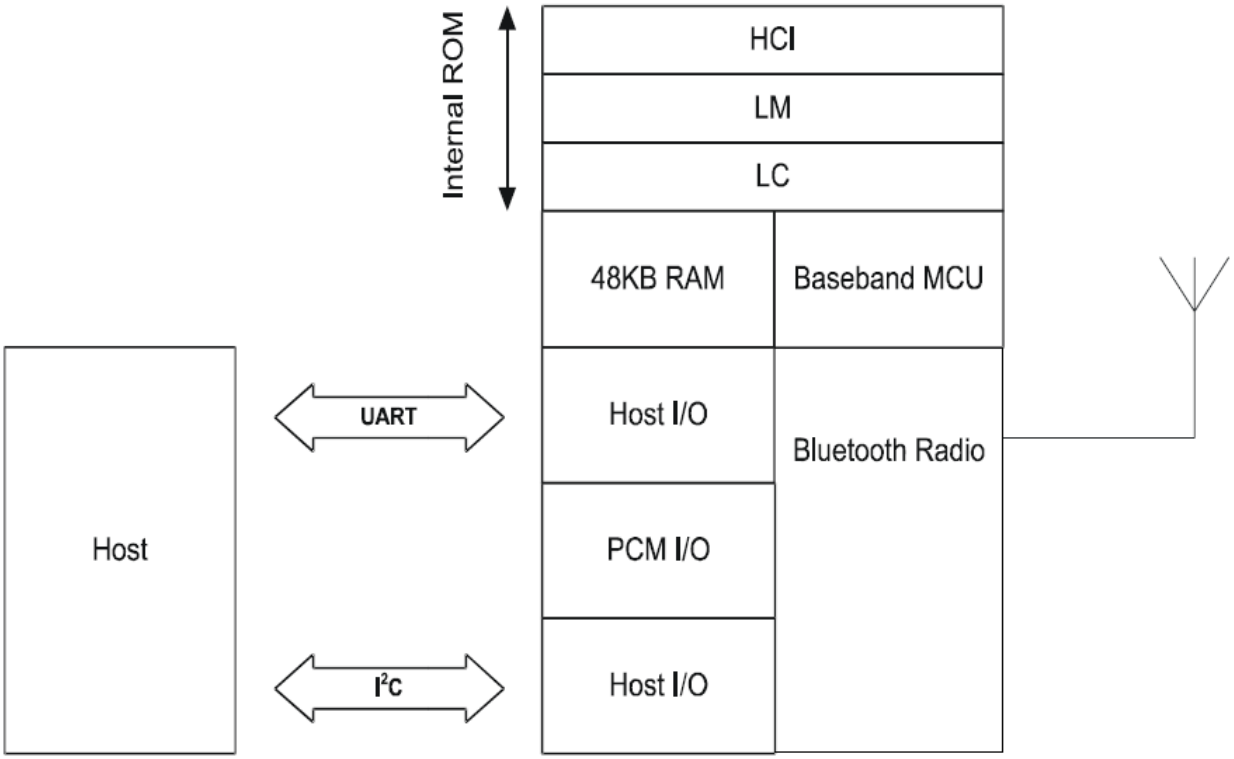

Figure 4: BlueCore Bluetooth HCI Stack

Key Features of the HCI Stack: Standard Bluetooth Functionality

CSR supports the following Bluetooth v2.1 + EDR functionality:

- Secure simple pairing
- Sniff subrating
- Encryption pause resume
- Packet boundary flags
- Encryption
- Extended inquiry response

CSR supports the following Bluetooth v2.0 + EDR mandatory functionality:

- Adaptive frequency hopping (AFH), including classifier
- Faster connection - enhanced inquiry scan (immediate FHS response)
- LMP improvements
- Parameter ranges

Optional Bluetooth v2.0 + EDR functionality supported:

- Adaptive Frequency Hopping (AFH) as Master and Automatic Channel Classification
- Fast Connect - Interlaced Inquiry and Page Scan plus RSSI during Inquiry
- Extended SCO (eSCO), eV3 +CRC, eV4, eV5
- SCO handle
- Synchronization

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The firmware was written against the Bluetooth v2.0+EDR specification.

- Bluetooth components:
  - Baseband (including LC)
  - LM
  - HCI
- Standard UART HCI Transport Layers
- All standard Bluetooth radio packet types
- Full Bluetooth data rate, enhanced data rates of 2 and 3Mbps
- Operation with up to seven active slaves
- Scatternet v2.5 operation
- Maximum number of simultaneous active ACL connections: 7
- Maximum number of simultaneous active SCO connections: 3
- Operation with up to three SCO links, routed to one or more slaves
- All standard SCO voice coding, plus transparent SCO
- Standard operating modes: Page, Inquiry, Page-Scan and Inquiry-Scan
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power saving mechanisms: Hold, Sniff and Park modes, including Forced Hold
- Dynamic control of peers' transmit power via LMP
- Master/Slave switch
- Broadcast
- Channel quality driven data rate
- All standard Bluetooth test modes

The firmware's supported Bluetooth features are detailed in the standard Protocol Implementation Conformance Statement (PICS) documents, available from http://www.csr.com.

Key Features of the HCI Stack: Extra Functionality

The firmware extends the standard Bluetooth functionality with the following features:

- Supports BlueCore Serial Protocol (BCSP), a proprietary, reliable alternative to the standard Bluetooth UART Host Transport
- Provides a set of approximately 50 manufacturer-specific HCI extension commands. This command set, called BlueCore Command (BCCMD), provides:
  - Access to the chip's general-purpose PIO port
  - The negotiated effective encryption key length on established Bluetooth links
  - Access to the firmware's random number generator
  - Controls to set the default and maximum transmit powers; these can help minimize interference between overlapping, fixed-location piconets
  - Dynamic UART configuration
  - Bluetooth radio transmitter enable/disable. A simple command connects to a dedicated hardware switch that determines whether the radio can transmit.
- A block of BCCMD commands provides access to the chip's Persistent Store (PS) configuration database. The database sets the device's Bluetooth address, Class of Device, Bluetooth radio (transmit class) configuration, SCO routing, LM, constants, etc.
- A UART break condition can be used in three ways:
  - Presenting a UART break condition to the chip can force the chip to perform a hardware reboot
  - Presenting a break condition at boot time can hold the chip in a low power state, preventing normal initialization while the condition exists
  - With BCSP, the firmware can be configured to send a break to the host before sending data. (This is normally used to wake the host from a Deep-Sleep state.)
- A block of Bluetooth radio test or BIST commands allows direct control of the chip's radio. This aids the development of modules' radio designs, and can be used to support Bluetooth qualification.
- Hardware low power modes: Shallow Sleep and Deep-Sleep. The chip drops into modes that significantly reduce power consumption when the software goes idle.
- SCO channels are normally routed via HCI (over BCSP). However, up to three SCO channels can be routed over the chip's PCM ports (at the same time as routing any remaining SCO channels over HCI).

For more details on the CSR Bluetooth stack, limitations and firmware refer to CSR's firmware release note "BlueCore Unified 23c Release Note (CS-116212-RNP3).pdf"

DIGITAL INTERFACES

High Speed UART Interface

NEMO uses a standard UART interface for communicating to other serial devices. Four signals from NEMO implement the UART function. The signal operation amplitude can be varied with the external +VBT_IO supply pin. This is useful for different systems that support different digital communication amplitudes such as 3.3V or 1.8V. When NEMO is connected to another digital device, BT_CTRL_RXD_N and BT_CTRL_TXD_N transfer data between the two devices. The other two remaining UART pins, BT_CTRL_RTS_N and BT_CTRL_CTS_N, can be used as hardware flow control signal as used in RS232 communications.

The high speed UART can support up to 4Mbits in throughput which is needed for data transfers using EDR RF link payloads with 3Mbit over the air throughput. The baud rate and other configuration parameters can be set via the firmware and PSKEYs during bootup and initialization.

BlueCore Serial Protocol (BCSP)

This document only describes CSR's BlueCore Serial Protocol overview and does not go into detail on BCSP implementation, packet structure and stack elements. Please refer to CSR's "BlueCore Serial Protocol (bcore-sp-012Pb).pdf" document for more a detailed explanation and implementation. BCSP must be implemented on the Host to communicate to the NEMO module.

BlueCore Serial Protocol (BCSP) is a protocol used to carry data that flow through a reliable UART link. The Bluetooth stack has been designed to transfer data between a Bluetooth Host and a Host Controller (NEMO). The Bluetooth stack is intended to be used to carry the Bluetooth HCI (Host Controller Interface) protocols plus several others. BCSP is intended to be used with CSR based Host Controllers (NEMO), which provides hardware to support much of the Bluetooth stack functionality.

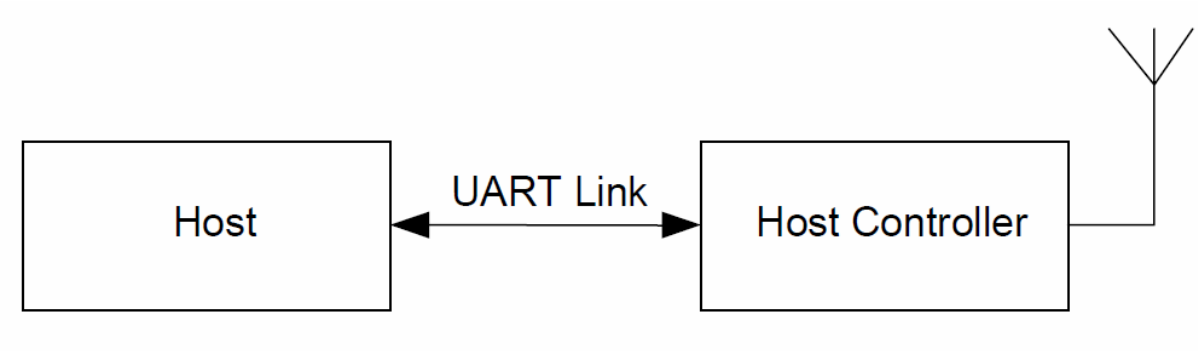

Figure 5: UART Host Connection

BCSP is used to control and format information that flows between the Bluetooth Host and the NEMO modules. The Bluetooth stack carries a set of parallel information that flows between the two process entities, multiplexing them over the single UART link.

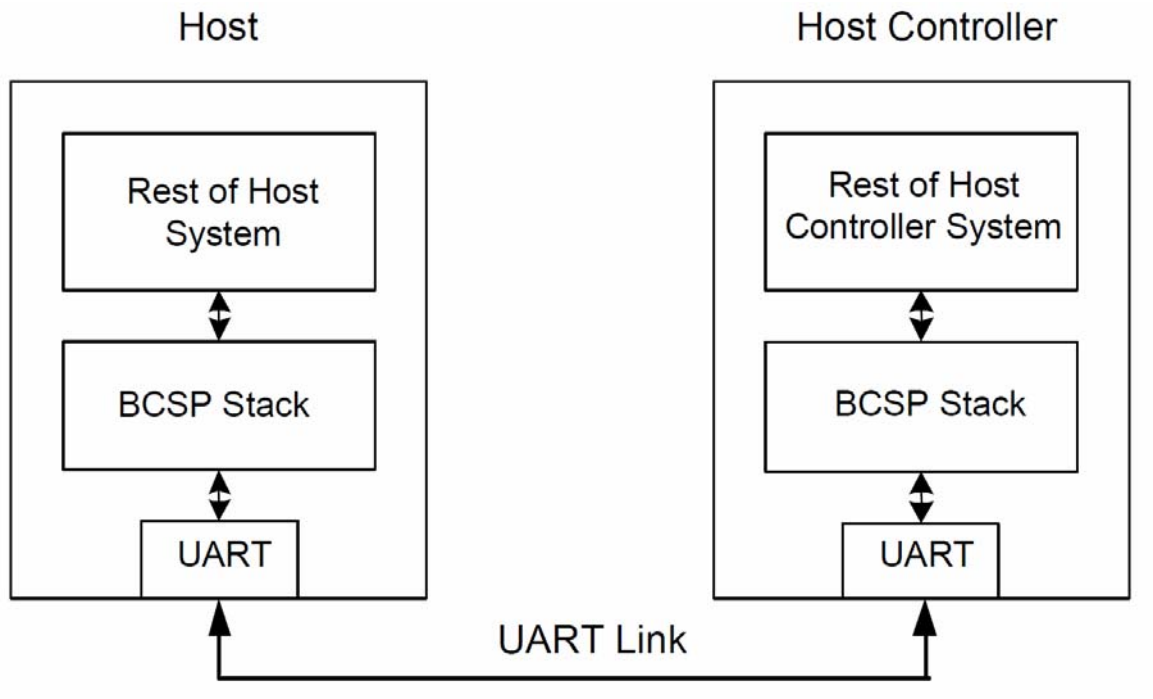

Figure 6: BCSP Context

An instance of the BCSP stack runs on both the Host and the Host Controller (NEMO). The BCSP stack is layered above the UART on each side.

The top of the BCSP stack presents:

- One bidirectional reliable datagram service
- One bidirectional unreliable datagram service

The BCSP protocol is defined to run on a 3-wire UART connection (TXD, RXD, & GND). However, BCSP can also run on a 5 wire UART connection (TXD, RXD, GND, CTS, RTS) which is common for higher baud rates.

BLUECORE COMMAND (BCCMD) PROTOCOL

This document only gives an overview of CSR's BCCMD Protocol overview and does not go into detail on BCCMD implementation, command set and events. The BlueCore Command Protocol (BCCMD) is used to configure parameters such as UART Baud Rate, Bluetooth address and initiate NEMO's radio. BCCMD and BCSP are protocols that need to be implemented on the Host connected to NEMO via the UART interface. For detailed information and implementation of CSR's BCCMD Protocol please refer to CSR's "BCCMD Protocol (bcore-sp-002Pc).pdf" document.

BCCMD describes a software interface to a command interpreter on a CSR BlueCore Bluetooth device, in this case the BlueCore 6 ROM chip inside NEMO. The command interpreter presents commands and events that allow monitoring and control of specific CSR ship functions outside of the Bluetooth stack protocol. The command set is not part of the Bluetooth protocol.

BCCMD allows the software on the Bluetooth Host to control and monitor the CSR BlueCore ship and flows alongside the normal Host Controller Interface (HCI) channels. The BCCMD protocol is carried over the UART link over a BCSP channel.

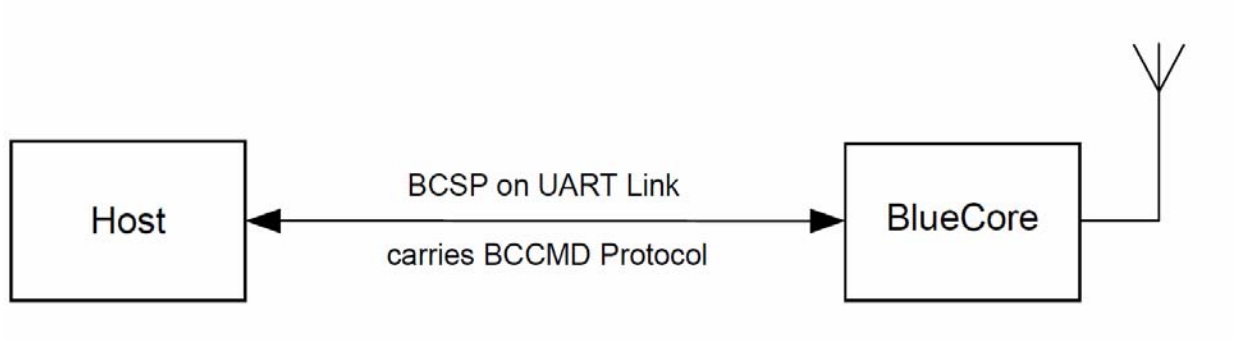

Figure 7: BCCMD Interface

Audio PCM and I2S Interfaces

The NEMO module has a Pulse Code Modulation (PCM) audio port and I2S interface. These interfaces are intended to be used for quick transfer of synchronous audio date transmitted or received over Bluetooth SCO audio links for voice applications such as headsets and hands free kits. These signals can also vary in operation amplitude based on the +VBT_IO supply pin.

PCM is a standard method for digitizing audio (particularly voice) for transmission over digital communications channels. The dedicated PCM port reduces overhead processing power for battery powered devices. The PCM port bi-directional digital audio interface is routed directly into the CSR radio baseband for fast encoding/decoding. The audio is not passed through the UART/HCI layer. The digitized audio through the baseband is sent and received via Bluetooth defined RF SCO links.

The PCM port can operate as a the PCM master generating an output clock of 128, 256, 512, 1536, and 2400kz. When configured as a PCM slave, NEMO can support a master input clock up to 2400kHz. A variety of clock formats are supported including, Long Frame Sync, Short Frame Sync, and GCI timing environments.

It supports 13-bit or 16-bit linear. 8-bit µ-law or A-law companded sample formats at 8ksamples/s. These samples can be received and transmitting through any selection of the first 3 out of the 4 timing slots following BT_PCM_SYNC_P.

PCM Interface Master/Slave

When NEMO is configured as a PCM master, NEMO generates BT_PCM_CLK_P and BT_PCM_SYNC signals

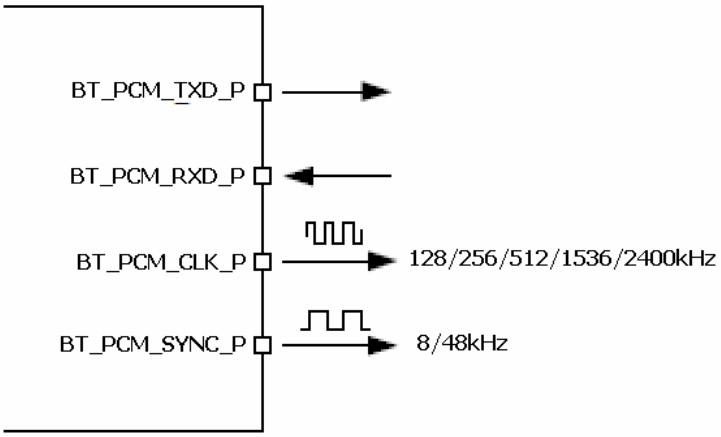

Figure 8: PCM Interface Master

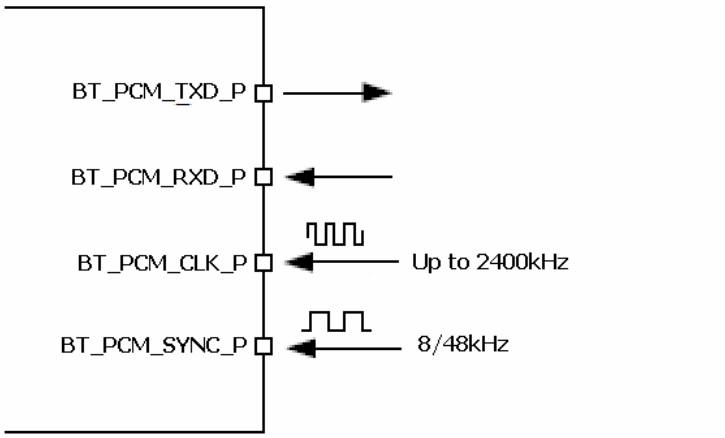

Figure 9: PCM Interface Slave

PCM Long Frame Sync

Long Frame Sync is a clocking format that controls data transfer for PCM data words or sample between two devices. The rising edge of BT_PCM_SYNC_P indicates the start of a PCM word in Long Frame Sync. When NEMO is configured as a PCM master, generating BT_PCM_SYNC_P and BT_PCM_CLK_P, the BT_PCM_SYNC_P is 8-bits long. As a PCM slave, BT_PCM_SYNC_P may be from two consecutive falling edges of BT_PCM_SYNC_P to half of the BT_PCM_SYNC_P rate, i.e 62.5us long.

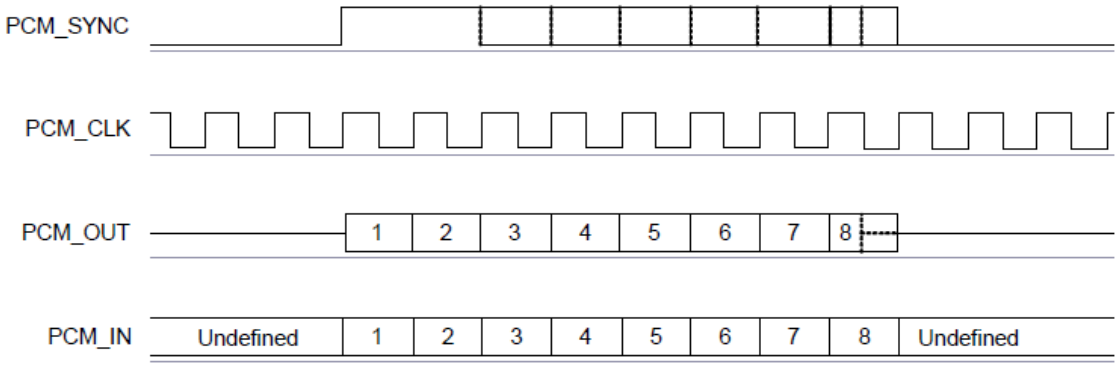

Figure 10: Long Frame Sync (Shown with 8-bit Companded Sample)

NEMO samples BT_PCM_RXD_P on the falling edge of BT_PCM_CLK_P and transmits BT_PCMTXD_P on the rising edge of BT_PCM_CLK_P. The BT_PCM_TXD_P signal maybe configured to be high impedance on the falling edge of BT_PCM_CLK_P in the LSB position or on the rising edge.

Short Frame Sync

In Short Frame Sync, the falling edge of BT_PCM_SYNC_P indicates the start of the PCM word. BT_PCM_SYNC_P is always one clock cycle long.

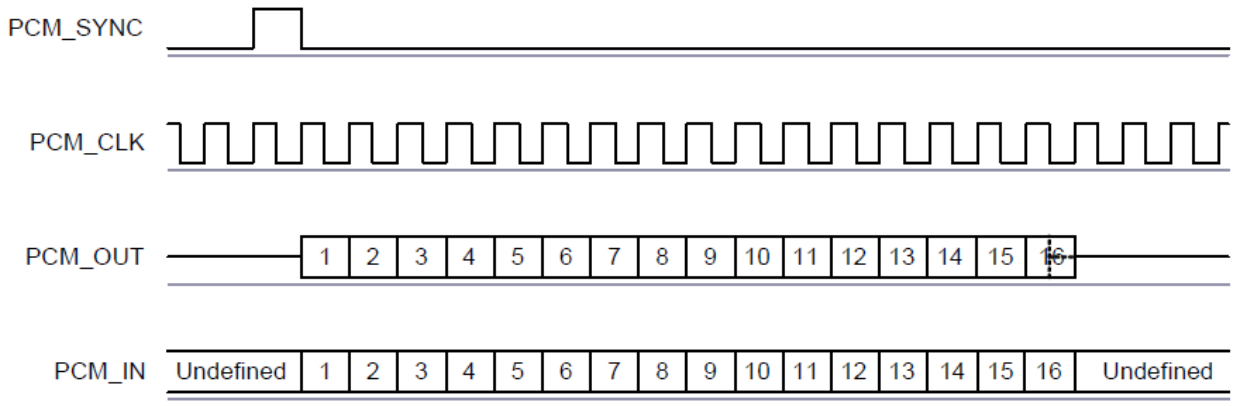

Figure 11: Short Frame Sync (Shown with 16-bit Sample)

Like with Long Frame Sync, NEMO samples BT_PCM_RXD_P on the falling edge of BT_PCM_CLK_P and transmits BT_PCM_TXD_P on the rising edge. BT_PCM_TXD_P maybe configured to be high impedance on the falling edge of BT_PCM_CLK_P in the LSB position or on the rising edge.

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Multi-slot Operation

More than one audio Bluetooth SCO connection over the PCM interface is supported using multiple slots as more than one Bluetooth SCO connection can exist simultaneously. Up to three Bluetooth SCO connections can be handled simultaneously and can be carried over any of the first three out of the four slots of the PCM port.

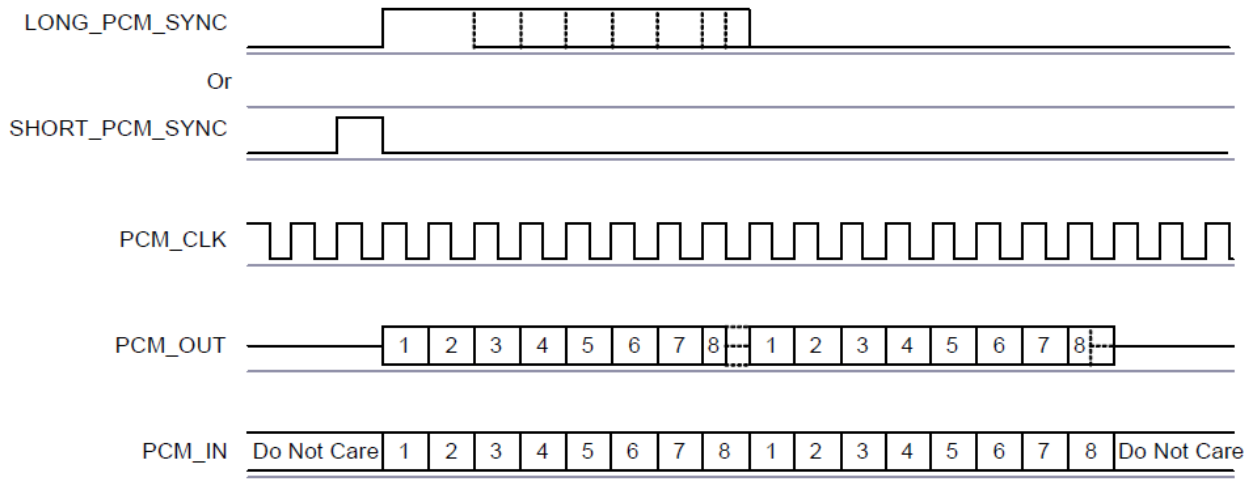

Figure 12: Multi-slot Operation with Two Slots and 8-bit Companded Samples

GCI Interface

NEMO is compatible with General Circuit Interface (GCI), a standard synchronous 2B+D ISDN timing interface. The two 64kbps B channels can be accessed when this mode is configured.

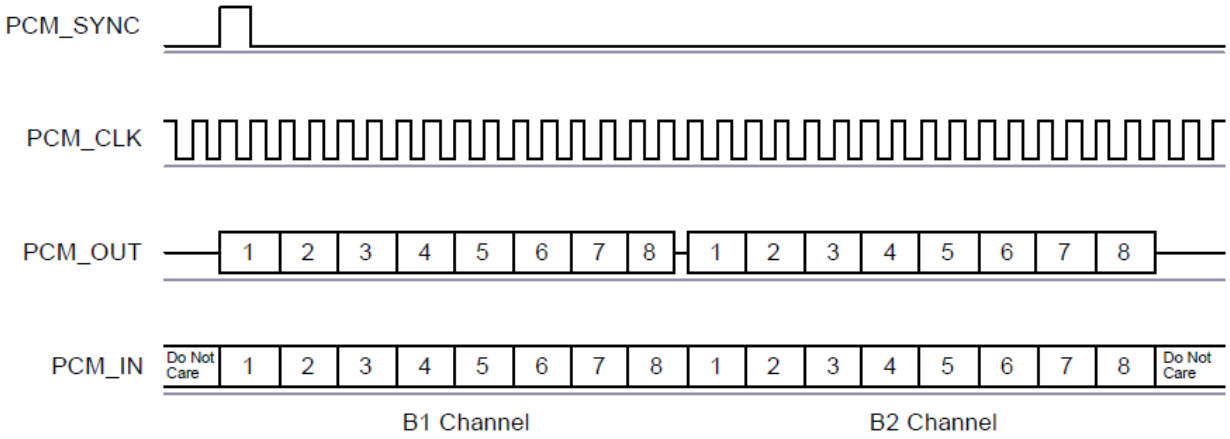

Figure 13: GCI Interface

The start of frame is indicated by the rising edge of BT_PCM_SYNC_P and runs at 8kHz. With NEMO in slave mode, the frequency of BT_PCM_CLK can be up to 4.096MHz.

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PCM Slots and Sample Formats

NEMO can receive and transmit on any selection of the first four slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Durations of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8-bit, 13-bit or 16-bit sample formats. NEMO supports 13-bit linear, 16-bit linear and 8-bit μ-law or A-law sample formats.

The sample rate is 8ksamples/s. The bit order may be little or big endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola CODECs.

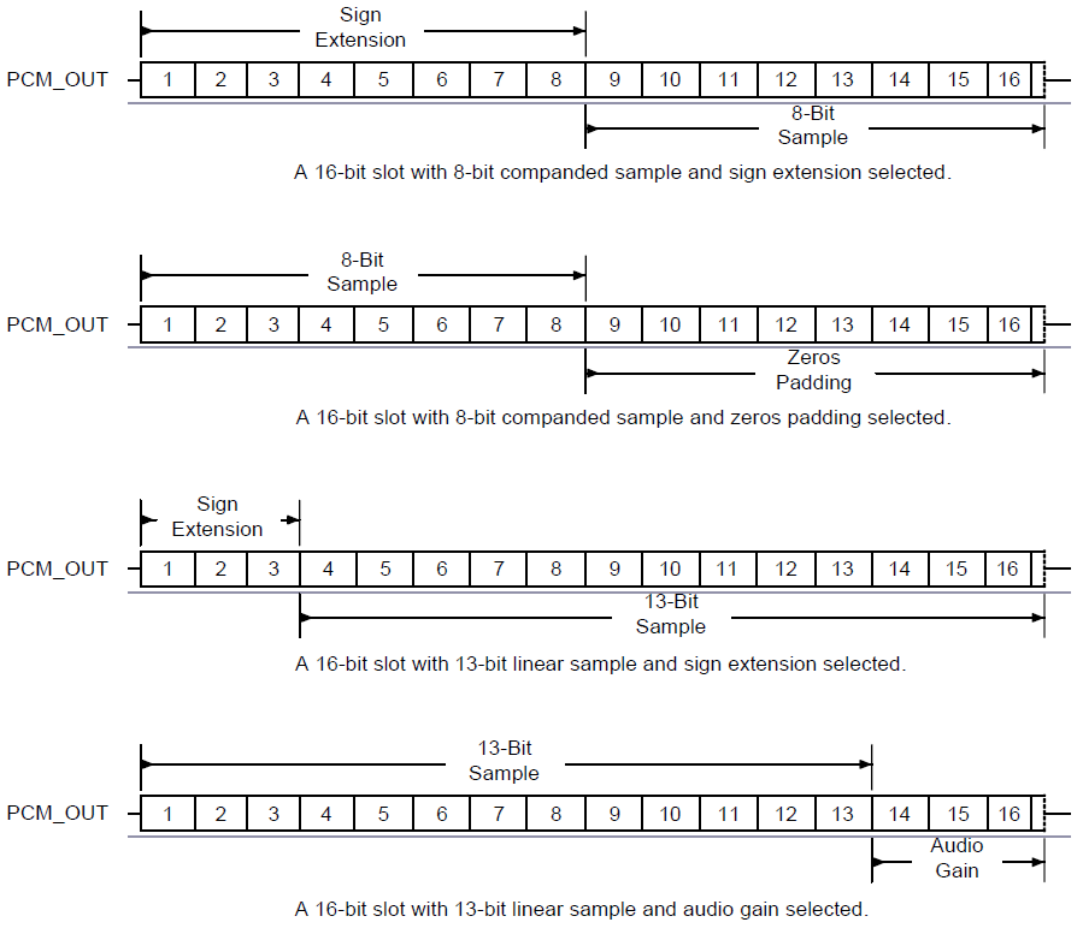

Figure 14: 16-Bit Slot Length and Sample Formats

PCM Timing Information

Table 6: PCM Timing Table

Symbol	Parameter		Min	Typ	Max	Unit
fmclk	BT_PCM_CLK_P frequency	4MHz DDS generation. Selection of frequency is programmable. See Table XXXX	-	128	-	kHz
				256		
				512		
		48MHz DDS generation. Selection of frequency is programmable. See Table XXXX.	2.9	-	-	kHz
-	BT_PCM_SYNC_P Frequency for SCO		-	8	-	kHz
tmclkh	BT_PCM_CLK_P high	4MHz DDS generation	980	-	-	Ns
tmclkl	BT_PCM_CLK_P low	4MHz DDS generation	730	-	-	Ns
-	BT_PCM_CLK_P jitter	48MHz DDS generation.	-	-	21	ns pk-pk
tdmclksynch	Delay time from BT_PCM_CLK_P high to BT_PCM_SYNC high		-	-	20	Ns
tdmclkpout	Delay time from BT_PCM_CLK_P high to valid BT_PCM_TXD_P		-	-	20	Ns
tdmclklsyncl	Delay time from BT_PCM_CLK_P low to BT_PCM_SYNC_P low (Long Frame Sync only)		-	-	20	Ns
tdmclkhsyncl	Delay time from BT_PCM_CLK_P high to BT_PCM_SYNC low		-	-	20	Ns
tdmclklpoutz	Delay time from BT_PCM_CLK_P low to BT_PCM_TXD high impedance		-	-	20	Ns
tdmclkhpoutz	Delay time from BT_PCM_CLK_P high to BT_PCM_TXD_P high impedance		-	-	20	Ns
tsupinclkl	Set-up time for BT_PCM_RXD_P vaid to BT_PCM_CLK low		30	-	-	Ns
thpinclkl	Hold time for BT_PCM_CLK low to BT_pCM_RXD_P invalid		10	-	-	Ns

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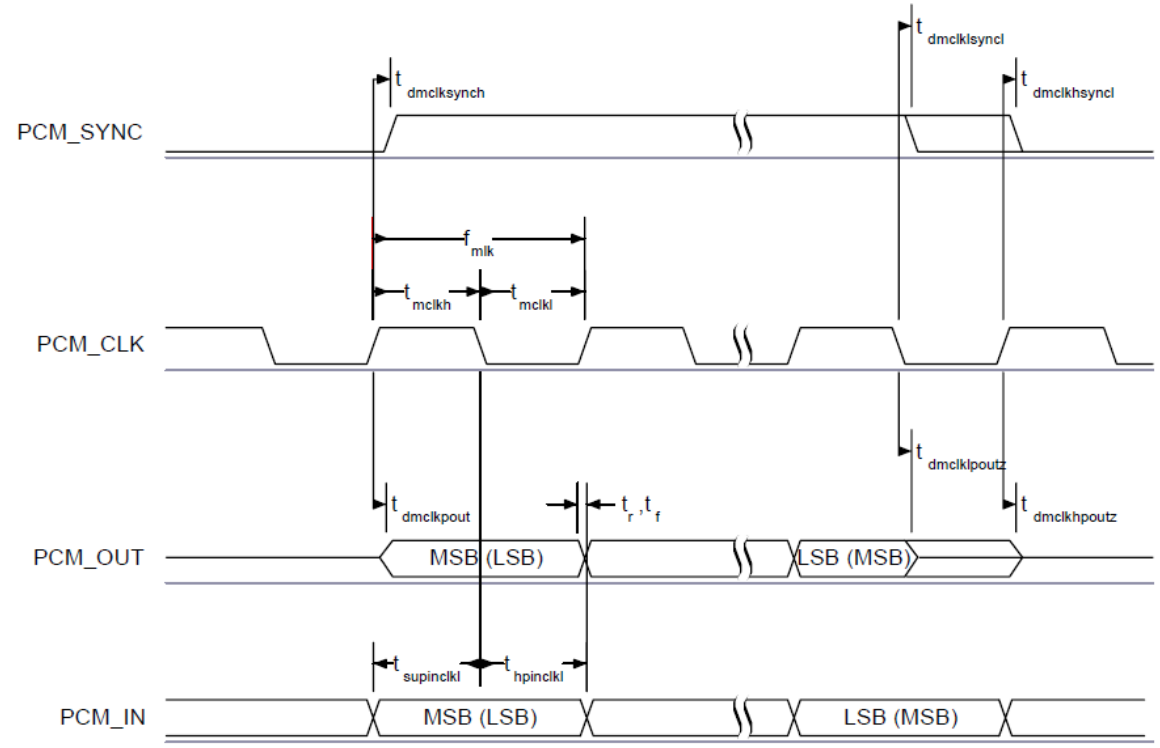

Figure 15: PCM Master Timing Long Frame Sync

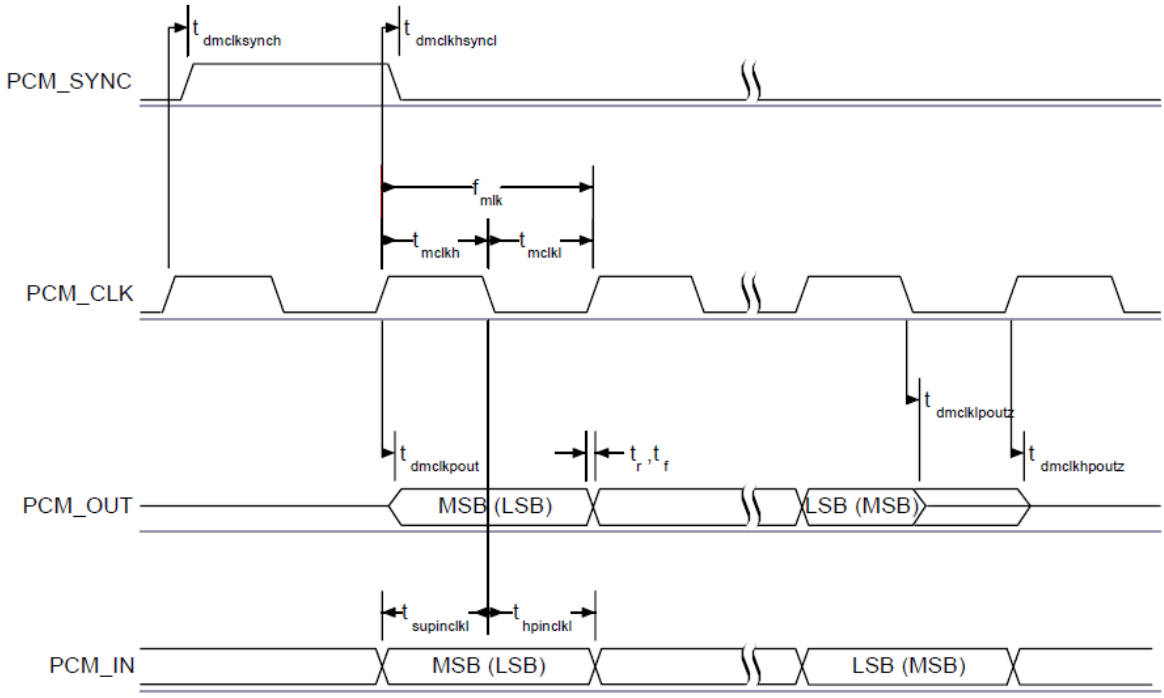

Figure 16: PCM Master Timing Short Frame Sync

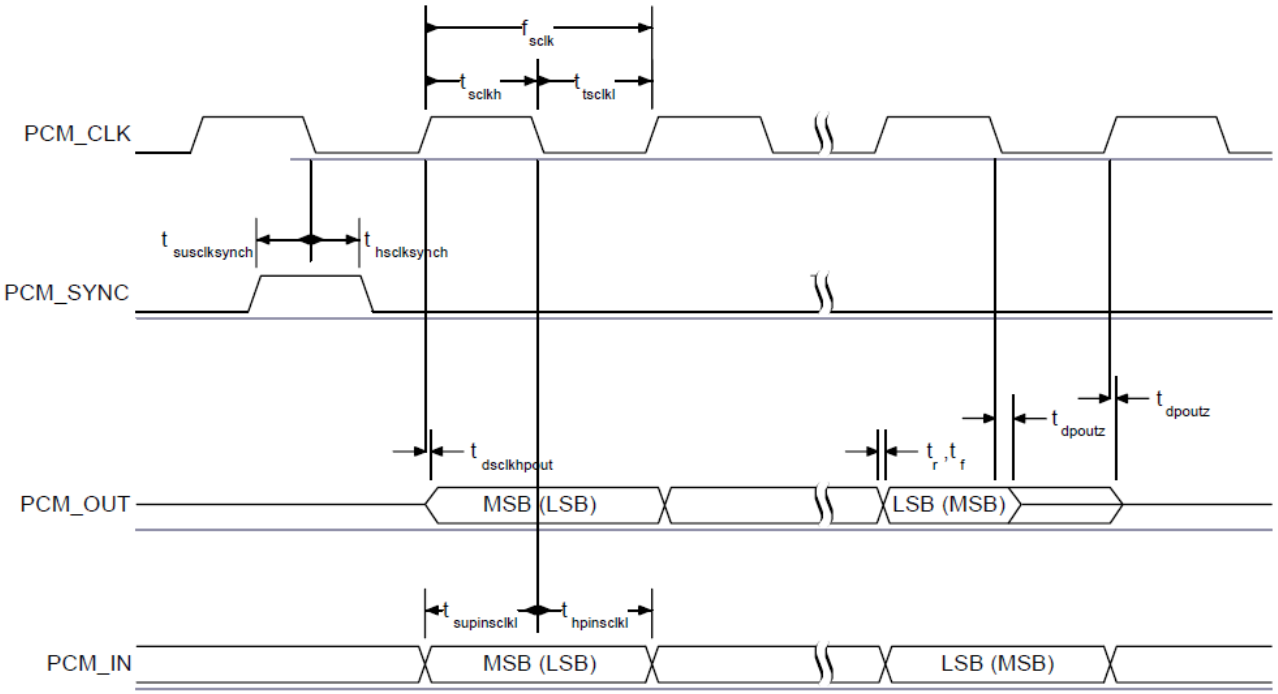

Figure 17: PCM slave Timing Short Frame Sync

PCM CLK and PCM SYNC Generation

NEMO has two methods of generating the PCM CLK and PCM SYNC in master mode:

- Generating signals by Direct Digital Synthesis (DDS) from internal 4MHz clock. Using this mode limits BT_PCM_CLK_P to 126, 256 or 512kHz, and BT_PCM_SYNC_P to 8kHz.

- Generating these signals by DDS from an internal 48MHz clock (which allows greater range of frequencies to be generated with low jitter but consumes more power). This method is selected by setting bit 48M_PCM_CLK_GEN_EN in the PSKEY_PCM_CONFIG32 key. When in this mode and with long frame sync, the length of the BT_PCM_SYNC_P can either be8 or 16 cycles of BT_PCM_CLK_P, determined by LONG_LENGTH_SYNC_EN bit in the PSKEY_PCM_CONFIG32 key.

The equation below describes the PCM CLK frequency when being generated using the internal 48MHz clock:

$$f = \frac{CNT\_RATE}{CNT\_LIMIT} \times 24MHz$$

The frequency of the PCM SYNC relative to the PCM CLK is set using either of the two equations below by setting the value of PCM_SYNC_MULT (see Table 10.4):

$$f = \frac{PCM\_CLK}{SYNC\_LIMIT \times 8}$$

$$f = \frac{PCM\_CLK}{SYNC\_LIMIT}$$

CNT_RATE, CNT_LIMIT and SYNC_LIMIT are set using PSKEY_PCM_LOW_JITTER_CONFIG. As an example, to generate BT_PCM_CLK_P at 512kHz with BT_PCM_SYNC_P at 8kHz, set PSKEY_PCM_LOW_JITTER_CONFIG to 0x08080177.

PCM Configuration

The PCM configuration is set using the PS Keys, PSKEY_PCM_CONFIG32 described in Table 10.4 and PSKEY_PCM_LOW_JITTER_CONFIG in Table 10.3. The default for PSKEY_PCM_CONFIG32 is 0x00800000, i.e., first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tri-state of PCM_OUT. For more information in regards to PS keys and their usage refer to the Persistent Store section of this document.

Table 7: PSKEY_PCM_LOW_JITTER_CONFIG Description

Name	Bit Position	Description
CNT_LIMIT	[12:0]	Sets the PCM CLK counter limit
CNT_RATE	[23:16]	Sets the PCM CLK count rate
SYNC_LIMIT	[31:24]	Sets the PCM SYNC division relative to PCM CLK

Table 8: PSKEY_PCM_CONFIG32 Description

Name	Bit Position	Description
	0	Set to 0
SLAVE_MODE_EN	1	0 = Master mode with internal generation of the BT_PCM_CLK_P and BT_PCM_SYNC_P. 1 = Slave mode requiring externally generated PCM CLK and the PCM SYNC signals.
SHORT_SYNC_EN	2	0 = Long Frame Sync mode (rising edge indicates start of frame). 1 = Short Frame Sync mode (falling edge indicates start of frame).
	3	Set to 0
SIGN_EXTENDED_EN	4	0 = Padding of 8 or 13-bit voice sample into a 16-bit slot by inserting extra LSBs. When padding is selected with 13-bit voice sample, the 3 padding bits are the audio gain setting; with 8-bit sample the 8 padding bits are zeroes. 1 = Sign-extension.
LSB_FIRST_EN	5	0 = MSB first of transmit and receive voice samples. 1 = LSB first of transmit and receive voice samples.
TX_TRISTATE_EN	6	0 = Drive PCM_OUT continuously. 1 = Tri-state BT_PCM_TXD_P immediately after falling edge of BT_PCM_CLK_P in the last bit of an active slot, assuming the next slot is not active.
TX_TRISTATE_RISING_EDGE_EN	7	0 = Tri-state BT_PCM_TXD_P immediately after falling edge of BT_PCM_CLK_P in last bit of an active slot, assuming the next slot is also not active. 1 = Tri-state BT_PCM_TXD after rising edge of BT_PCM_CLK_P.

SYNC_SUPPRESS_EN	8	0 = enable PCM_SYNC output when master. 1 = suppress PCM_SYNC while keeping PCM_CLK running. Some CODECS use this to enter a low power state.
GCI_MODE_EN	9	1 = enable GCI mode.
MUTE_EN	10	1 = force BT_PCM_TXD_P to 0.
48M_PCM_CLK_GEN_EN	11	0 = set PCM_CLK and PCM_SYNC generation via DDS from internal 4MHz clock. 1 = set PCM_CLK and PCM_SYNC generation via DDS from internal 48MHz clock.
LONG_LENGTH_SYNC_EN	12	0 = set PCM_SYNC length to 8 PCM_CLK cycles. 1 = set length to 16 PCM_CLK cycles. Only applies for long frame sync and with 48M_PCM_CLK_GEN_EN set to 1.
PCM_SYNC_MULT	13	0 = Sync limit = SYNC_LIMIT x 8. 1 = SYNC_LIMIT.
	[20:16]	Set to 0b00000
MASTER_CLK_RATE	[22:21]	Selects 128 (0b01), 256 (0b00), 512 (0b10) kHz BT_PCM_CLK+P frequency when master and 48M_PCM_CLK_GEN_EN (bit 11) is low.
ACTIVE_SLOT	[26:23]	Default is 0001. Ignored by firmware.
SAMPLE_FORMAT	[28:27]	Selects between 13 (0b00), 16 (0b01), 8 (0b10) bit sample with 16-cycle slot duration or 8 (0b11) bit sample with 8-cycle slot duration.

Digital Audio Interface (I²S)

The digital audio interface supports the industry standard formats for I²S, left-justified (LJ) or right-justified (RJ). The interface shares the same pins as the PCM interface, which means each audio bus is mutually exclusive in its usage. Table 7 lists these alternative functions.

Table 9: Alternative Functions of the Digital Audio Bus Interface on the PCM Interface

PCM Interface	I²S Interface
BT_PCM_TXD_P	SD_OUT
BT_PCM_RXD_P	SD_IN
BT_PCM_SYNC_P	WS
BT_PCM_CLK_P	SCK

Table 8 describes the values for the PS Key (PSKEY_DIGITAL_AUDIO_CONFIG) that is used to set-up the digital audio interface. For example, to configure an I²S interface with 16-bit SD data set PSKEY_DIGITAL_CONFIG to
0x0406.

Table 10: PSKEY_DIGITAL_AUDIO_CONFIG

Bit	Mask	Name	Description
D[0]	0x0001	CONFIG_JUSTIFY_FORMAT	0 for left justified, 1 for right justified.
D[1]	0x0002	CONFIG_LEFT_JUSTIFY_DELAY	For left justified formats: 0 is MSB of SD data occurs in the first SCLK period following WS transition. 1 is MSB of SD data occurs in the second SCLK period.
D[2]	0x0004	CONFIG_CHANNEL_POLARITY	For 0, SD data is left channel when WS is high. For 1 SD data is right channel.
D[3]	0x0008	CONFIG_AUDIO_ATTEN_EN	For 0, 17 bit SD data is rounded down to 16 bits. For 1, the audio attenuation defined in CONFIG_AUDIO_ATTEN is applied over 24 bits with saturated rounding. Requires CONFIG_16_BIT_CROP_EN to be 0.
D[7:4]	0x00F0	CONFIG_AUDIO_ATTEN	Attenuation in 6 dB steps.

D[9:8]	0x0300	CONFIG_JUSTIFY_RESOLUTION	Resolution of data on SD_IN, 00=16 bit, 01=20 bit, 10=24 bit, 11=Reserved. This is required for right justified format and with left justified LSB first.
D[10]	0x0400	CONFIG_16_BIT_CROP_EN	For 0, 17 bit SD_IN data is rounded down to 16 bits. For 1 only the most significant 16 bits of data are received.

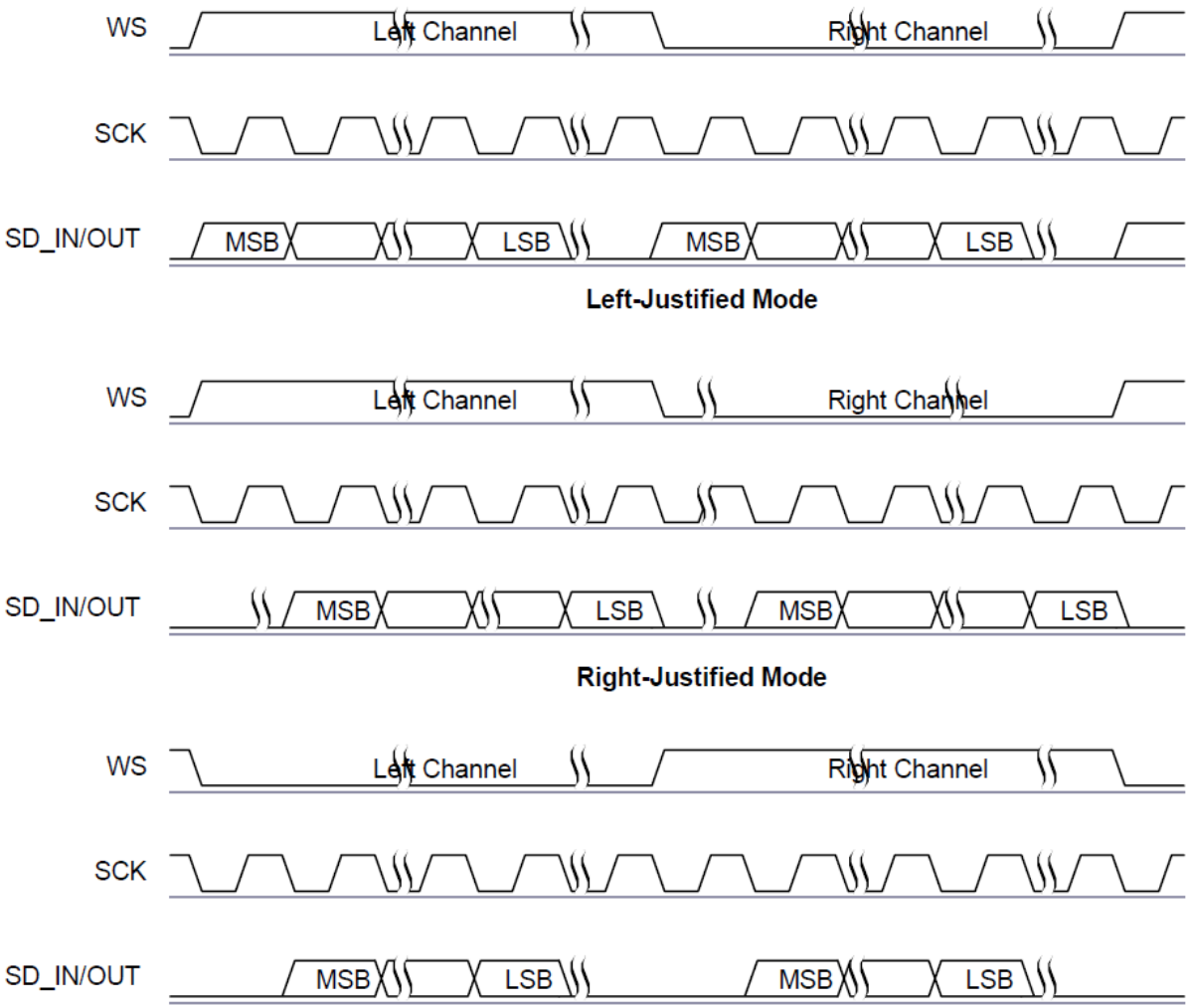

Figure 18: I²S Mode Digital Audio Interface

Table 11: Digital Audio Interface Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz
tch	SCK high time	80	-	-	ns
tcl	SCK low time	80	-	-	ns
topd	SCK to SD_OUT delay	-	-	20	ns
tssu	WS to SCK set-up time	20	-	-	ns
tsh	WS to SCK hold time	20	-	-	ns
tisu	SD_IN to SCK set-up time	20	-	-	ns
tih	SD_IN to SCK hold time	20	-	-	ns

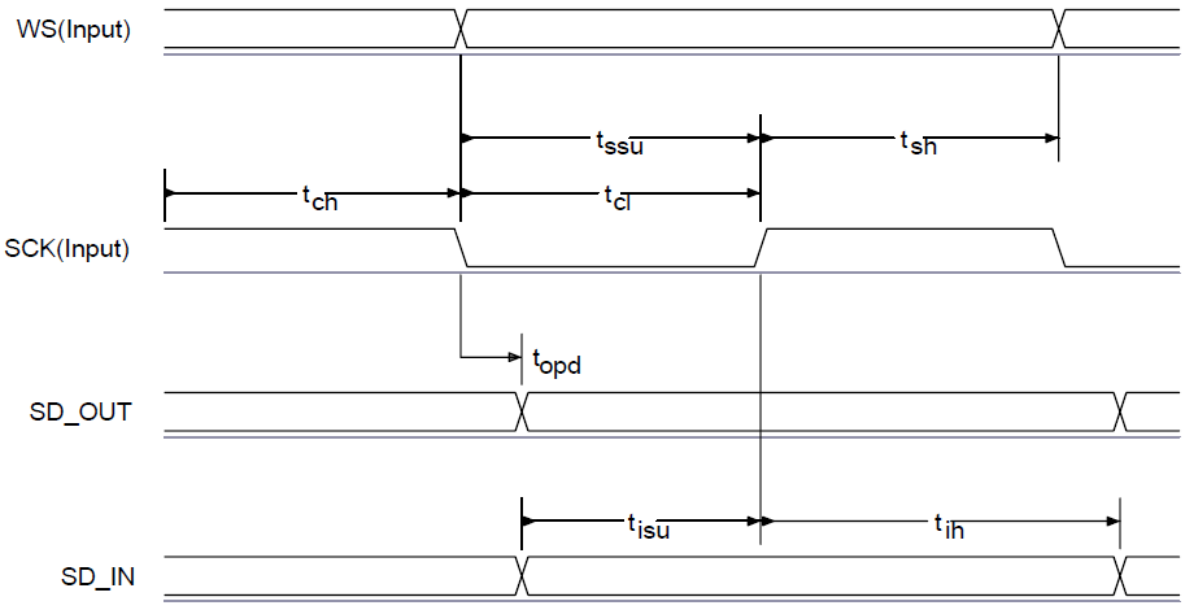

Figure 19: Digital Audio Interface Slave Timing

Table 12: Digital Audio Interface Master Timing

Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz
topd	SCK to SD_OUT delay	-	-	20	ns
tspd	SCK to WS delay	-	-	20	ns
tisu	SD_IN to SCK set-up time	20	-	-	ns
tih	SD_IN to SCK hold time	10	-	-	ns

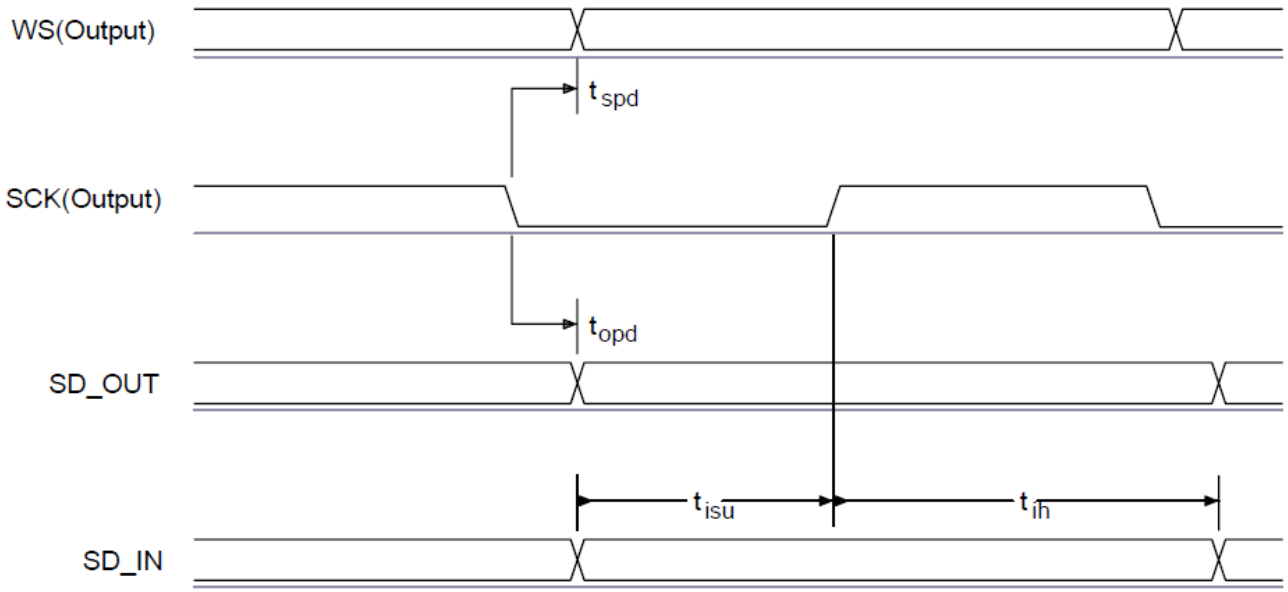

Figure 20: Digital Audio Interface Master Timing

POWER CONSUMPTION

Table 13: Operating Power Consumption Figures

Operation Mode	Connection Type	Average	Unit
Page scan, time interval 1.28s	-	0.4	mA
Inquiry and page scan, time interval 1.28s	-	0.8	mA
ACL no traffic	Master	4	mA
ACL with file transfer	Master	9	mA
ACL 40ms sniff	Master	2	mA
ACL 1.28s sniff	Master	0.2	mA
eSCO EV5	Master	12	mA
eSCO EV3	Master	18	mA
eSCO EV3 - hands-free - setting S1	Master	18.5	mA
SCO HV1	Master	37	mA
SCO HV3	Master	17	mA
SCO HV3 30ms sniff	Master	17	mA
ACL no traffic	Slave	14	mA
ACL with file transfer	Slave	17	mA
ACL 40ms sniff	Slave	1.6	mA
ACL 1.28s sniff	Slave	0.2	mA
eSCO EV5	Slave	19	mA
eSCO EV3	Slave	23	mA
eSCO EV3 - hands-free - setting S1	Slave	23	mA
SCO HV1	Slave	37	mA
SCO HV3	Slave	23	mA
SCO HV3 30ms sniff	Slave	16	mA
Standby host connection (Deep-Sleep)	-	40	µA
Reset (active low)	-	39	µA

Note Conditions: 20ºC, +VBT = 3.15V, +VBT = 3.15V, UART BAUD rate = 115.2kbps.

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Table 14: Peak Current

Typical Peak Current @ 20°C	
Device Activity/State	**Current (mA)**
Peak current during cold boot	45
Peak TX current Master	45
Peak RX current Master	40
Peak TX current Slave	45
Peak RX current Slave	45
Conditions	
VREGIN_H, VDD_PADS	3.15
Host Interfaces	UART
UART Baud rate	115200
RF output power	0dBm

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BOOTING NEMO ROM

The NEMO module contains the CSR BlueCore 6 ROM device. The firmware is loaded from BlueCore's internal ROM. The NEMO module is boot-strapped to use the UART interface upon power up. The BCSP communication protocol along with the BCCMD protocol is used over the UART. PIO 4 must be held low in order to boot into BCSP over the UART successfully.

Configuration of NEMO is handled through the UART interface and BCCMD protocol. The Bluetooth address, UART baud rate, PCM configuration and country code are all parameters that can be configured on the ROM device upon power up. These parameters are programmed into Persistent Store Keys in RAM and are loaded into firmware after a soft reset.

NEMO Boot Process

1. Power up NEMO with PIO4 pulled low.
2. Initialize BCSP communications over the UART link.
3. Load and program the PSKEYS via BCCMD commands necessary for the initialization
4. Issue BCCMD warm_reset command
5. Re-initialize BCSP communications
6. Module is ready for operation

This process needs to be performed during every cold boot or hard reset on NEMO.

UART Auto Baud Rate

The NEMO module can support booting into UART mode without pre-configuration of the baud rate, and clock reference. Although a 26MHz internal crystal oscillator is built into the module, the CSR BlueCore device needs to be configured to use the clock reference for radio and UART communication purposes. The CSR device support an "AUTOBAUD" adaption algorithm where the Host can communicate over the UART link to load configuration PSKEYS into RAM and perform initialization of the module.

The AUTOBAUD UART baud rate adaption mechanism starts by treating the UARTS RXD data line as a simple PIO input, and it records the hosts initial UART traffic in a buffer. The mechanism then examines the recorded data stream to determine the times between signal level transitions and, from this, derives the baud rate the host is using. The mechanism then matches the measured baud rate.

The BCSP stack is used on the host to send sync messages from the host to the NEMO module. The Sync message packet is a reasonably good data set for the analysis to complete, though at high baud rates several sync messages from the BCSP stack may need to be sent.

This AUTOBAUD mechanism must complete before any normal UART traffic is passed to or from the host transport. For example, the BCSP Link Establishment messages described in CSR's BlueCore Serial Protocol document are neither transmitted or responded to until the UART's baud rate has been set by this mechanism.

The mechanism is designed to operate between 38.4 kbaud and 691.2 kbaud. However, testing from CSR has only been concentrated on operation between 56 kbaud and 115.2 kbaud. Implementers are therefore advised to choose a bootup baud rate within these ranges.

During cold boot, the CSR BlueCore device can operate where the systems clock frequency is unknown. This causes BlueCore to run more slowly than normal. Consequently, the range of acceptable baud rates is shifted down pro-rata. The radio is not operational until the external system clock is defined in the PSKEY setting. This is due to the PLL not locking to a known external clock frequency. Therefore, the system clock must be programmed upon boot-up via the PSKEY_ANA_FREQ persistent store key in order for the radio to operate.

Operation with an unknown system clock implies dual-boot initialization of NEMO. The approach is for the host to use a safe tested baud rate at the during cold boot (115.2 kbaud), then to set the external clock frequency to 26MHz and the actual baud rate via PSKEYS then issue a "warm reset" command to NEMO over the same UART interface.

For more details on AUTOBAUD rate of the CSR device, please refer to the "UART Baud Rate Adaption (bcore-me-019Pd).pdf" document available from CSR directly.

Persistent Store Keys (PSKEYS)

Persistent Store Keys are configuration settings that are used to configure and initiate the CSR BlueCore 6 device within NEMO. These PSKEYS are written using the BCCMD protocol to send commands to the CSR BlueCore devices. PSKEY are written using BCCMD write commands that are interpreted by the CSR device within NEMO.

PSKEYS configure the CSR chips behavior from its interfaces to radio performance. Data such as Bluetooth address, product ID and country code is also stored in PSKEYS and are necessary information in some cases. Programming these various PSKEYS are vital to initializing NEMO upon cold boot. PSKEYS are address locations with specific values. The values are used for configuration of different systems of the NEMO.

The following are PSKEYS needs to be written and programmed during a cold boot of NEMO

Table 15: Boot PSKEY List

PSKEY Name	PSKEY Address	Value	Description
PSKEY_ANA_FREQ	0x01FE	0x6590	This sets CSRs BlueCore to use a 26MHz reference clock built into NEMO.
PSKEY_HOST_INTERFACE	0x01f9	0x0001	Sets the Host interface to use BCSP over the UART interface
PSKEY_UART_BAUDRATE	0x01be	-	When the system is configured to use a UART-based host transport, i.e. if PSKEY_HOST_INTERFACE selects BCSP, H4, H5 or User (VM access to the UART), then the UART's Baud rate is set to the value of this PS key when the firmware boots. The PS key's value is: Baud rate = pskey_value/0.004096 Some common values are: 38k4 baud - 157 (0x009d) 57k6 baud - 236 (0x00ec) 115k2 baud - 472 (0x01d8) 230k4 baud - 944 (0x03b0) 460k8 baud - 1887 (0x075f) 921k6 baud - 3775 (0x0ebf) 1382k4 baud - 5662 (0x161e)
PSKEY_BDADDR	0x0001	-	This is the local device's Bluetooth address. This should be unique to this device and allocated by the manufacturer. Bluetooth addresses are distributed by IEEE in the same manner as MAC addresses.

PSKEY_COUNTRYCODE	0x0002	-	North America and most of Europe use a particular block of 79 radio frequencies for Bluetooth, but not all countries allow use of these frequencies. Some countries allow the use of different blocks of frequencies. This key selects the frequency blocks used by these exceptional countries. 0 North America and Europe 1 France 2 Spain 3 Japan
PSKEY_DEEP_SLEEP_ EXTERNAL_CLOCK_SOURCE	0x03c3		Enable the use of an external 32kHz clock source for more reliable low power mode and radio synchronization.
PSKEY_PCM_CONFIG32	0x01b3		See Table 6 for more description of this PSKEY.

TYPICAL APPLICATION CIRCUITS

NEMO with out external 32kHz slow clock source:

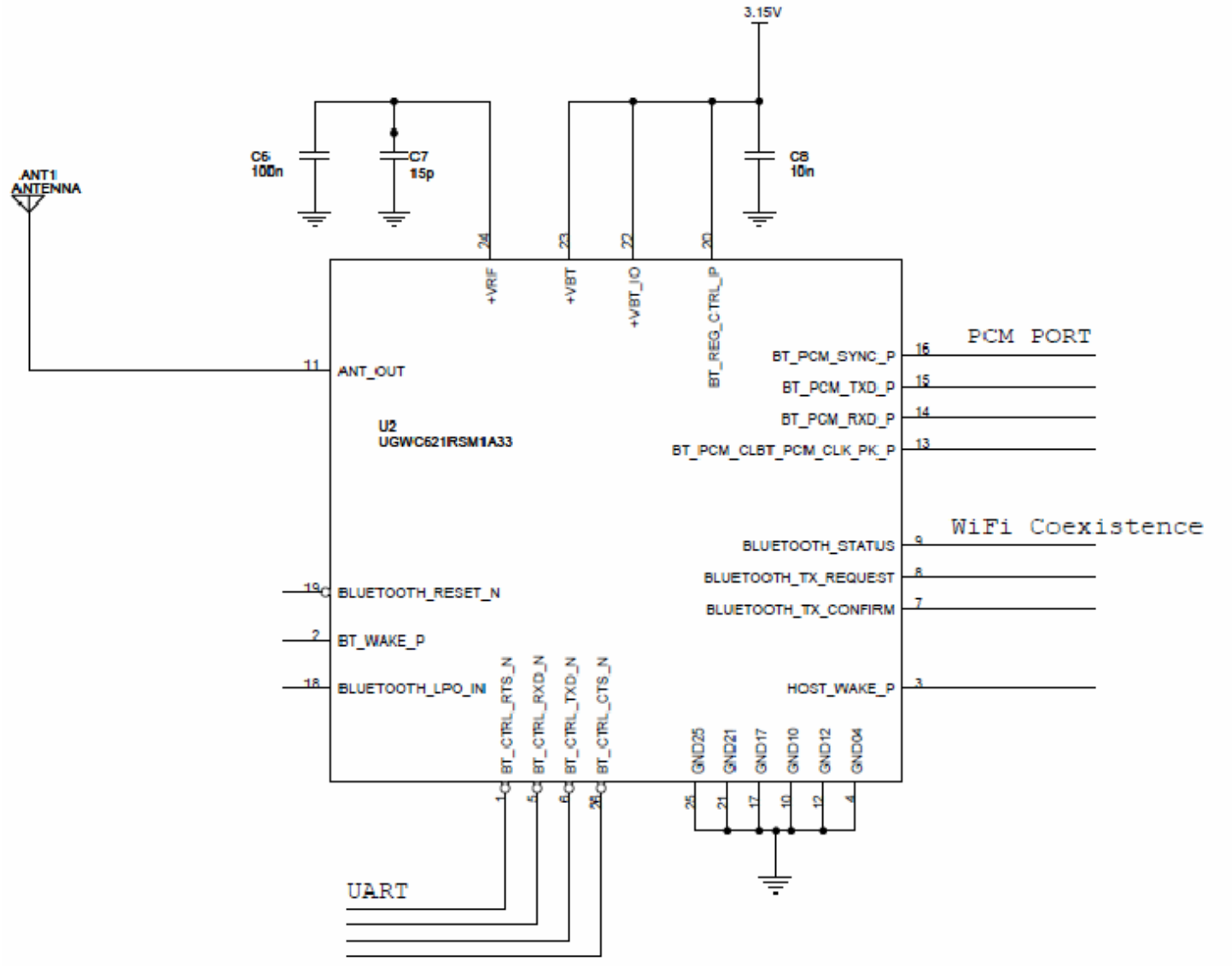

Figure 21: NEMO Example Application Circuit; No External Slow Clock Source

NEMO with external 32kHz slow clock source:

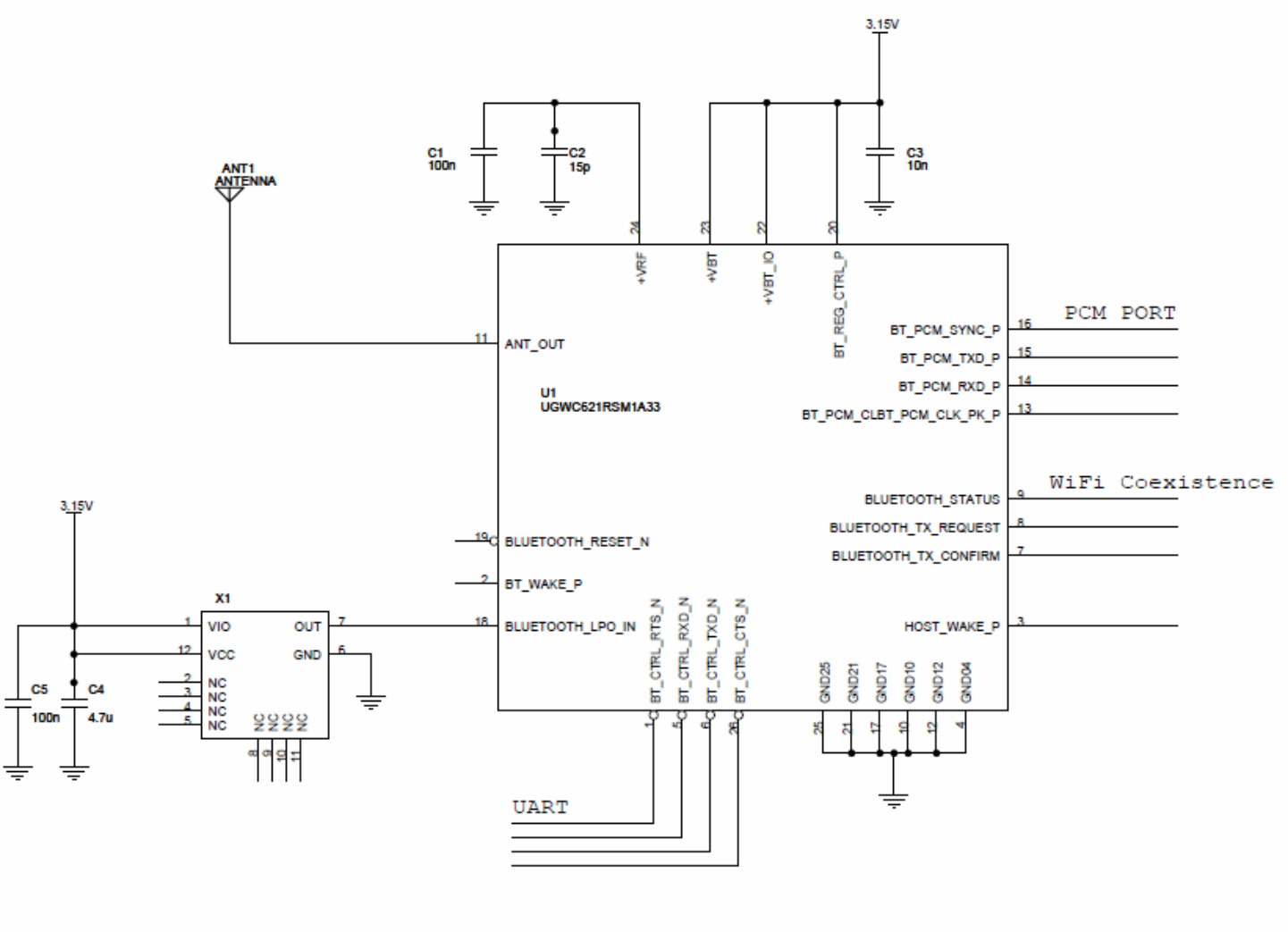

Figure 22: NEMO Example Application Circuit; External Slow Clock Source

MECHANICAL DRAWINGS

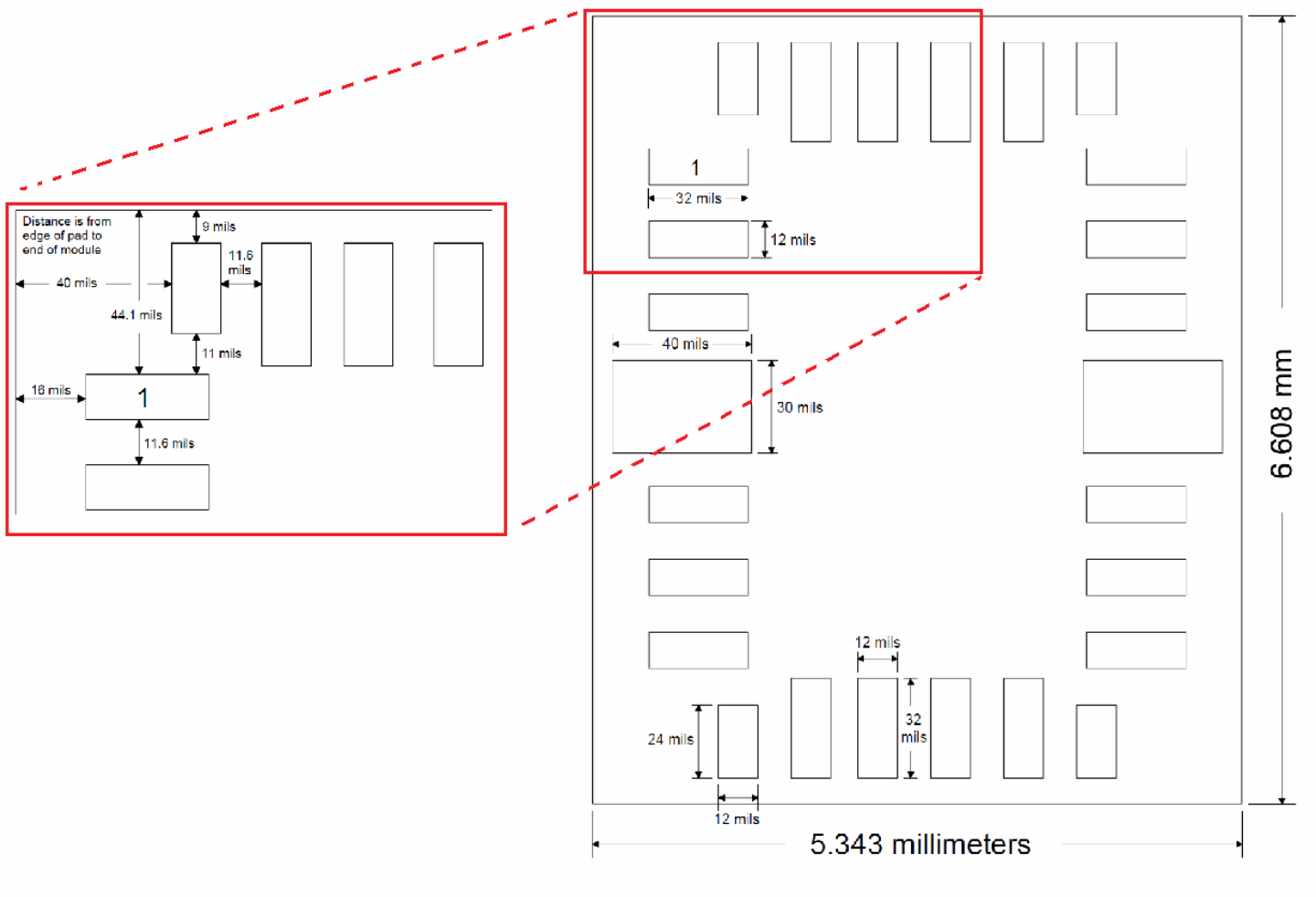

Figure 23: NEMO Mechanical Drawing

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REFERENCE DOCUMENTATION

Table 16: Reference Documentation

Document	Name	Rev/Date	Source
CSR BlueCore 6 ROM Datasheet	"BC6ROM_WLCSP_CS-113960-DSP12.pdf"	Issue 12	CSR
Firmware Release Note	"BlueCore Unified 23c Release Note (CS-116212-RNP3).pdf"	Issue 3	CSR
AUTOBAUD rate adaption	"UART Baud Rate Adaption (bcore-me-019Pd).pdf"	Jun-05	CSR
BCSP	"BlueCore Serial Protocol (bcore-sp-012Pb).pdf"	Jul-04	CSR
BCCMD	"BCCMD Protocol (bcore-sp-002Pc).pdf"	Jul-04	CSR

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