# TRC102 Development Kit User Guide



### **General Overview**

The TRC102 Development Kits are available as:

- DR-TRC102-433-DK (430-439 MHz)
- DR-TRC102-868-DK (860-879 MHz)
- DR-TRC102-915-DK (900-929 MHz)

The TRC102 Development kits allows for complete evaluation and application development of RFM's SRR (Short Range Radio) line of RFIC's. A communication link or Range Test can be executed with the Data Terminal to evaluate system performance.

#### **Kit Includes:**

- 2 RS-232 Cables
- 2 "AAA" battery packs
- 4 "AAA" batteries
- RFDA 2.0 software
- 2 tuned, SMA antennas
- 2 DR-TRC102 DR Board
- Quick Start Guide
- Example assembly code

# **Key Features:**

- Full development with Silicon Labs C8051F330 IDE (sold separately)
- Comprehensive Evaluation of RFIC's
- Individual parameter configuration
- 115.2 kbps serial communication setup
- Example Code
- RFDA 2.0 software
- 2-way communication link
- Range Test
- Up to 50 kbps data rate
- Data Terminal Program
- Diagnostic LED's
- "Out of the box" operation
- 32 byte packet handling



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# **Overview**

The TRC102 Lead Free development board is designed to allow for testing of critical functions of the transmitter and receiver as well as develop custom firmware for any design. All functions of the transmitter and receiver may be enabled by configuration through the RFDA software. A 2-way communication link is possible through the RFDA software by bringing up the Data Terminal program. A Range Test is also possible through the Data Terminal with use of one of the included battery packs for roaming capability.



Figure 1. TRC102 Development Board

# **Descriptions**

# **Test Points**

Test points are provided to monitor signals in real time from the TRC102. In addition there are accessible vias that may be used to apply an oscilloscope probe to monitor a signal that is not brought to an accessible pin. The following test points are provided:

SDI: Serial Data In to the RFIC

SDO: Serial Data Out from the RFIC

nCS: Chip Select to enable the SPI port for commands

SCLK: Serial Clock Input to the RFIC for the SPI port.

- **IRQ:** Interrupt Request Output. The receiver will generate an active low interrupt request for the microcontroller on the following events:
  - The TX register is ready to receive the next byte
  - · The FIFO has received the preprogrammed amount of bits
  - · Power-on reset
  - · FIFO overflow/TX register underrun
  - · Wake-up timer timeout
  - · Negative pulse on the interrupt input pin nINT
  - · Supply voltage below the preprogrammed value is detected

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**DATA:** Transmit Data In/Receive Data Out when internal FIFO not used. Use in conjunction with DCLK.

DCLK: Recovered Data Clock Output

**CLK:** Output Clock. Configurable from 1MHz to 10MHz.

**RSSI:** Analog RSSI Output. This is the raw DC value of the received signal strength.

**INT:** Interrupt Request Input - This pin may be configured as an active low external interrupt to the chip. When a logic '0' is applied to this pin, it causes the nIRQ pin (5) to toggle, signaling an interrupt to an external processor. Reading the first four (4) bits of the status register tells the source of the interrupt. This pin may be used as a wake-up event from sleep.

Valid Data Detector Output– This pin may also be configured to indicate Valid Data when the synchronous pattern recognition circuit indicates potentially real incoming data. The pin's function is configured within the RFDA software.

#### **Microcontroller Programming Header**



The dual row, 10-pin header is used to program the Silicon Labs C8051F330 microcontroller IC. This is available if the user wishes to develop their code for the TRC102 and use the TRC102 development board as a bench trial. The development board can be used as a development platform or as an development tool for IC performance. Pin one is orientated to the red ribbon stripe.

#### **Development Board Operation**

#### Antennas

Two monopole antennas are included that are matched for performance to the ground plane area of the DR boards. The antennas are a critical part of the performance of the communication link, thus, a monopole antenna requires a good ground plane for proper performance. **Power Supply** 

Two pins are provided for connection of an external power supply or a portable battery pack. Note the polarity of the connections before connecting any power source.

The TRC102 development board may operate up to +3.6V. Although the TRC102 IC may operate at a higher supply voltage, the microcontroller is only rated to +3.6V.

#### **LEDs**

The on-board LED's are provided for visual confirmation of programming data sent and received from the software. On power-up the Green LED will illuminate indicating the board is powered and working. When

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a command is sent to the TRC102, the yellow LED will flash indicating a successful command send. When a command is received from the TRC102, such as a Status Read, the red LED will flash indicating a successful receive of the packet.

The LED's also indicate the success or failure of a communication packet when using the Data Terminal/Range Test associated with the RFDA software. When a packet is sent and received successfully a green LED will flash on both boards to indicate successful reception and acknowledgement. If the packet received contains a checksum error then a red LED will flash on both boards indicating a packet error.

#### RS232 Port

The RS232 connection may be used with a straight thru cable. There is no flow control so DTS, CTS, RTS, etc.., signals are not used. Make sure that the TX and RX lines are not swapped at either end of the cable. Use a DB9 Male to Female cable for correct gender match to the PC and development board.

#### **Current Monitor (J6)**

J6 allows power to flow to the TRC102 ONLY! This enables the current consumption of the TRC102 to be monitored without the additive effect of the microcontroller and RS232 converter IC's current usage. For normal operation the Jumper at J6 must be installed. To monitor the current usage of the TRC102, simply remove the Jumper and apply an ammeter between the two pins.

#### 2-way Comm Header (J3)

Installation of J3 allows the DR board to power-up in comm link mode. J3 must be installed first before power applied to the board in order for the board to initialize in comm link mode. After power-up, follow the Quick Start Guide configuration for comm. link setup.

#### **PCB Layout**

The most critical portion of the layout is the output and matching section of the TRC102. If using a single ended antenna, such as a monopole, the matching is critical to get maximum output power delivered to the antenna. All components should be placed as close as possible to each other and as close to the TRC102 chip as possible.

Since the TRC102 is capable of 3 different bands of operation, the output matching for each band will be different, except for the 868MHz and 915MHz bands, where the matching is optimized for both and separate matching for each band is not necessary.





# **Communication Link**

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TXC101 RXC101 TRC102			Enable Disable
TRC102 Transceiver Design Assis	tant		
RF Monolithics, Inc.	A STATE	Wire	🚏 RFICDA Data Terminal
Enable the receiver     Enable the receiver     Enable receiver baseband     Enable the woke-up timer     Enable the olive wattery detector     Dasable the clock output     Enable the structure     Enable the structure     Enable the transmitter     Enable the transmitter     Enable TX Register     Enable TX Register     Enable TX Register     Dasable the Structure     Conta Detector output     Ail Low Power on     PLL Differing     DUFFLE Detect of Office	Center frequency 433.92 MHz Crystal load 12.0 pF - LNA gain: max DRSSS: -103 dBm - Baseband bandwith: 67 kHz - Valid Data Detector Slow - FSK Deviation (df) 45 kHz - Pout: Pmax - Pout: Pmax - Pout: pfar: D4 Clock Buffer Stew: >5 MHz -	Band Selection 868 MHz 915 MHz 7 915 MHz 7 0 915 MHz 7 0 915 MHz 7 0 915 MHz 8 007 8	HELLO WORLD!
Wake-Up Timer   Duty-Cycle   Batt. De ↓ Enable AFC Mod ↓ Enable fine mode AFC	ttect/Clock AFA Data Rate Baseband Filter FIFO/Re e Auto, drop Folfset ▼ Strobe C +15/-16 Fres ▼ ✓ Output Enable	set AFC Command: C497	Clear
Read Status FFIT POR Status register: FIFEMP RSSI	Jpdate Carrier	alibrate Synthesizer receiver carrier frequency offset: 2 OFF1 OFF0 kHz	nSS = 1 //Slave select high nSS = 0 //Slave select low SPIODATA = 98H SPIOdone() //wait for spio SPIODATA = 20H SPIOdone() //wait for spio nSS = 1 //Slave select high Write File
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A 2-way communication link may be established by opening the Data Terminal Window within the RFDA software. The board must be configured through the RFDA software before a link can be established.

# **Communication Link Packet**

The packet structure for the comm link and range test is given below. The packet demonstrates the use of



the preamble for data recovery and the synchronization bytes for valid data recognition. The synch byte (word) is 0x2DD4. Synch byte recognition is enabled through the *FIFO Buffer* tab of the RFDA. The preamble sets the data timing and the RXC101 receiver locks on to this signal in order to recover the data. The clock/data recovery time of the receiver may be set in the RFDA for fast (1 byte preamble) or slow (2 byte preamble). Regardless of the clock/data recovery setting of the receiver, the TXC102 sends a 2 byte preamble.

Configure both boards as follows:

Enable Receiver
Enable TX Register
Enable RX FIFO
Crystal Load = 12pF
LNA Gain = max
Baseband BW = 67kHz
Valid Data Detect = Slow
FSK Deviation = 45kHz
Polarity of Mod = fo + df
AFC:
Enable AFC
Enable Fine Mode
Output Enable
Mode = Auto, drop Foffset
AFC = +15/-16*Fres
Data Rate:
Enable Prescalar
R = 17 (2.4kbps)
Data Filter: (use defaults)
FIFO Buffer:
Enable Synch Latch
Disable Sensitive Reset
FIFO Fill Start = Synch pattern
FIFO IT level = 8

#### **Range Test**

A range test can be performed by configuring both DR boards for a comm link as above and clicking on the "Enable Range Test" button at the top of the Data Terminal Window. When the range test is activated it will send a default message of "<TX> Range Test Data" and the enable button will flash red. At this point the serial cable may be disconnected for free movement around the area of interest.

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File View Help Data Terminal Window			
TXC101 RXC101 TXC102			Enable Disable
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RF Monolithics, Inc.		Wire	RFICDA Data Terminal
Enable the receiver     Enable the receiver backband     Enables the wake-up time     Enables the look battery detector     Deable the clock output     Enable the optimizer     Enable the optimizer     Enable the constitutor     Enable the transmitter     Enable TX Register     Enable TX Register     Enable TX Register     Cata Detector output     Cata Detector output     Tal Detector output     Enable RX BIFO     Pnd function     Fail Detector output     Tal Detector output     Elifered     PLL Dethering     FLI Dethering	Center frequency 433.92 MHz Crystal load 12.0 pF LN4 gata. max. DRSSE 103 dBm Basebard boundwrit: [57 kHz Valid Data Detector Slow PSK Deviation (df) 45 kHz Pout: [max. Pout: [max. Pout: [max. Cock Baffer Slev: [55 MHz Cock Baffer Sl	Band Selection 688 MHz 7915 MHz Tuning Resolution 25 kHz Cogfiguration Register: 8007 Prequency Setting Register: 8209 Receiver Control Register: 9200 Transmitter Configuration: 9620 Janch Char Command. EED4 PLL Command. ECD6	CTO Range Text Data CTO Range Text Data
Wake-Up Timer   Duty-Cycle   Batt. D	etect/Clock AFA Data Rate Baseband Filter FIFO/Re.	sat	<ul> <li>X</li> <li>X</li> </ul>
I Enable AFC Mov I Enable fine mode AF	le (Auto, drop Folfset ▼	AFC Command: C497	Clear
Read Status FFIT POR Status register FIFEMP RSSI	Jpdate CCC FFOV WKINT INTRST LB Drammitter- GDQD CRLCK AFATGL OFFSGN OFF3 OFF3 TRC102	librate Synthesiser receiver carrier frequency afflet: 2 DFF1 OFF0 kHz	nSS = 1 //Slave select high nSS = 0 //Slave select low SPIODATA = 38H SPIOdone[] //wait for spio SPIODATA = 20H SPIOdone[] //wait for spio nSS = 1 //Slave select high Write Pile
🛃 start 🔰 🙆 🖉 🖼 🖿 🗹	🚺 🧔 🧐 🦉 👔 🐚 Novell Gro 🔛 TXC102	D 🐺 RFIC Desi 🔮 TRC101	D 🖻 TRC102_D 🔇 🚱 🔀 🦻 9:43 AM

A custom range test message of up to 32 bytes may be sent by simply typing in the message desired and pressing the "Enable Range Test" button.

🗰 RFIC Design Assistant			
File View Help Data Terminal Window			
REM REM REM			COM1 - Sent
TXC101 RXC101 TRC102			Enable Disable
TRC102 Transceiver Design Assis			
		Aline	🍸 RFICDA Data Terminal 📃 🗖 🔀
RF Monolithics, Inc.		vvire	Enable IX Bange Test
Enable the receiver	Center frequency 433.92 MHz	Band Selection	CUSTOM MESSACE-TYN CUSTOM MESSA
Enable the wake-up timer	Crystal load 12.0 pF	○ 868 MHz ● 433 MHz	<tx>CUSTOM MESSAGE</tx>
Enable the low battery detector	LNA gain: max. 🗾 Update	C 915 MHz	<tx>CUSTOM MESSAGE</tx>
✓ Disable the clock output ✓ Enable the synthesizer	DRSSI: -103 dBm 🗨	Tuning Resolution 2.5 kHz	<tx>CUSTOM MESSAGE</tx>
Enable the oscillator	Baseband bandwith: 67 kHz 🚽	Configuration Register: 80D7	<tx>CUSTOM MESSAGE</tx>
Enable the transmitter	Valid Data Detector Slow	Frequency Setting Register: A620	<tx>CUSTOM MESSAGE</tx>
✓ Enable RX FIFO	FSK Deviation (df) 45 kHz	Power Management Register: 82D9	<tx>CUSTOM MESSAGE <tx>CUSTOM MESSAGE</tx></tx>
- Pin8 function	Pout: Pmax	Receiver Control Register: 9200	
C Data Detector output	Polarity of mod: to + df	Transmitter Configuration: 9820	
Tal Low Power on	Synch Char. Byte: D4	Synch Char Command: CED4	
✓ PLL Dithering DL DW/Data Data + 00//b.	Clock Buffer Slew: >5 MHz 👻	PLL Command: CC06	
FLL DWILAU RUE >90K05		1	
Wake-Up Timer   Duty-Cycle   Batt. De	ttect/Clock AFA   Data Rate   Baseband Filter   FIFO/Re.	set	
✓ Enable AFC Mod	e Auto, drop Foffset	170.0 1	Clear
✓ Enable fine mode AFY	7 +15/-16 Fres ▼ Qutnut Enable	AFC Commana:	
		1	
			nSS = 1 //Slave select high
L	Jpdate a	ulibrate Synthesizer	nSS = 0 //Slave select low
Read Status FEIT POB	FERV WKINT INTEST I B Transmitter-	receiver carrier frequency offset:	SPIODATA = 36H SPIOdone() //wait for spio
Status register: FIFEMP RSSI	GDQD CRLCK AFATGL OFFSGN OFF3 OFF3	2 OFF1 OFF0 kHz	SPIODATA = 20H
ter alter alter	TDC102		nSS = 1 //Slave select high
	TRC102		Write File
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During a range test or general comm link, each time a packet is sent and verified, the green LED will flash on both the originating board and destination board to indicate a successful transmit and acknowledge. If there was an error detected in the packet, the red LED will flash on both boards. This is a useful verification tool when performing a range test. As one board moves out of visual range, the LED's indicate success or failure of packets. As the red LED begins to occur more frequently, this indicates that the outer limit of the range is being reached.

When performing a range test one board must remain connected to a computer in order to transmit the data stream from the RFDA. The other board may either be disconnected and allowed to roam freely around a given area, or may be installed on another computer at a remote location to view the actual data that is received. The actual data received is displayed in the Data Terminal window with an "OK" indicating successful reception, or "ERROR" indicating a packet error.

#### **Battery Packs**

The kit includes four "AAA" batteries and two battery packs that hold 2 "AAA" batteries each. One pack may be connected and used to free-roam an area for range test.



**TRC102** Evaluation Board Schematic

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ITEM	DESCRIPTION	QTY	REF
	COMPONENT NOT USED IN ASSY	10	S1,D5-D8,L4,R1-R4
	IND,0603,47NH,10%	1	L3*
	IND,CHIP,0603CS,390 nH,5%,COILCRAFT	1	L2*
	IND,0603,36 nH,+/- 10%	1	L1*
	RES,CHIP,0603,1.0K OHM,+/-5%, TIN TERMINATIONS	2	R13,14
	RES,CHIP,0603,10K OHM,+/-5%, TIN TERMINATIONS	1	R8
	RES,CHIP,0603,470 OHM,+/-5%, TIN TERMINATIONS	3	R5,6,7,12
	CAP,CHIP,0603,COG,2.7 pF,50V,SOLDER MNT	1	C2*
	CAP,CHIP,0603,COG,5.1 pF,50V,SOLDER MNT	1	C1*
	CAP,CHIP,0603,COG,10 pF,50V,SOLDER MNT	1	C7
	CAP,CHIP,0603,COG,100 pF,50V,SOLDER MNT	2	C4,C14
	CAP,CHIP,0603,X7R,1000 pF,50V,SOLDER MNT	3	C3,5,6
	CAP,CHIP,0603,X7R, .1 uF,16V,SOLDER MNT	7	C9,10,11,12,13,14,15
	CAP,CHIP,0603,X5R,1.0 uF,10V,SOLDER MNT	1	C8
	CAP,CHIP,TAN,22 uF,+/-10%,6V,B CASE	1	C16
	LED,SM,RED,0603	1	D1
	LED,SM,YELLOW,0603	1	D3
	LED,SM,GREEN,0603	1	D2
	LED,SM,AMBER,0603	1	D4
	CONN,HDR,MALE,.100"CTRS, SQ POST,3 POS	1	J5
	CONN,HDR,MALE,.100"CTRS, SQ POST,2 POS W/SHUNT	1	J6
	CRYSTAL,10 MHZ	1	Y1
	C8051F330 SILICON LABS MICROCONTROLLER, 20-QFN	1	U3
	DB-9 CONNECTOR	1	J4
	HDR,2-PIN	2	J1,3
	CONN,HEADER,DUAL ROW,5 PIN	1	J2
	CONN,SMA,STRAIGHT VERTICAL,PCB JACK	1	ANT1
	IC,XCVR W/AUTO SHUTDOWN,RS-232,120 kbps,16 TSSOP	1	U2
	TRC102 RFIC, TSSOP-16	1	U1

# Bill of Material for DR-TRC102-433

\*Matching Circuit Values

ITEM	DESCRIPTION	QTY	REF
	COMPONENT NOT USED IN ASSY	10	S1,D5-D8,L4,R1-R4
	IND,0603,22 nH,10%, COILCRAFT	1	L3*
	IND,CHIP,0603CS,100 nH,5%,COILCRAFT	1	L2*
	IND,0603,8.7 nH,+/- 10%, COILCRAFT	1	L1*
	RES,CHIP,0603,1.0K OHM,+/-5%, TIN TERMINATIONS	2	R13,14
	RES,CHIP,0603,10K OHM,+/-5%, TIN TERMINATIONS	1	R8
	RES,CHIP,0603,470 OHM,+/-5%, TIN TERMINATIONS	3	R5,6,7,12
	CAP,CHIP,0603,COG,1.2 pF,50V,SOLDER MNT	1	C2*
	CAP,CHIP,0603,COG,2.7 pF,50V,SOLDER MNT	1	C1*
	CAP,CHIP,0603,COG,10 pF,50V,SOLDER MNT	1	C7
	CAP,CHIP,0603,COG,100 pF,50V,SOLDER MNT	2	C4,C14
	CAP,CHIP,0603,X7R,1000 pF,50V,SOLDER MNT	3	C3,5,6
	CAP,CHIP,0603,X7R, .1 uF,16V,SOLDER MNT	7	C9,10,11,12,13,14,15
	CAP,CHIP,0603,X5R,1.0 uF,10V,SOLDER MNT	1	C8
	CAP,CHIP,TAN,22 uF,+/-10%,6V,B CASE	1	C16
	LED,SM,RED,0603	1	D1
	LED,SM,YELLOW,0603	1	D3
	LED,SM,GREEN,0603	1	D2
	LED,SM,AMBER,0603	1	D4
	CONN,HDR,MALE,.100"CTRS, SQ POST,3 POS	1	J5
	CONN,HDR,MALE,.100"CTRS, SQ POST,2 POS W/SHUNT	1	J6
	CRYSTAL,10 MHZ	1	Y1
	C8051F330 SILICON LABS MICROCONTROLLER, 20-QFN	1	U3
	DB-9 CONNECTOR	1	J4
	HDR,2-PIN	2	J1,3
	CONN,HEADER,DUAL ROW,5 PIN	1	J2
	CONN,SMA,STRAIGHT VERTICAL,PCB JACK	1	ANT1
	IC,XCVR W/AUTO SHUTDOWN,RS-232,120 kbps,16 TSSOP	1	U2
	TRC102 RFIC, TSSOP-16	1	U1

# Bill of Material for DR-TRC102-868/915

\*Matching Circuit Values



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