

NEC's LOW POWER GPS RF RECEIVER

UPB1008K

FEATURES

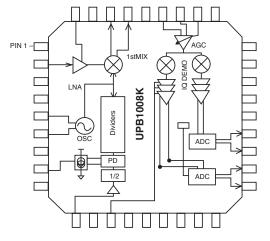
- LOW POWER CONSUMPTION: 52 mW
- DUAL-CONVERSION IQ DOWN CONVERTER¹: Reference frequency: REFin = 27 MHz
- PSEUDO-BASEBAND WITH 2-BIT DIGITIZED OUTPUT
- ON-CHIP LNA, ON-CHIP FREQUENCY SYNTHESIZER, IF AGC AMPLIFIER:

with 45 dB typical range of adjustable gain

SMALL 36 PIN QFN PACKAGE:
 Flat lead style for better RF performance
 Note:

1. Based on eRide's proprietary GPS DSP architecture

BLOCK DIAGRAM



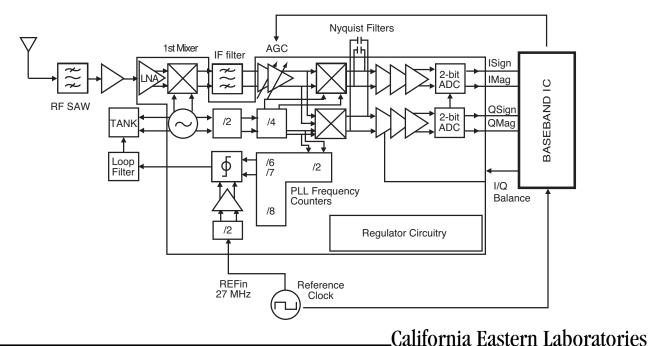
APPLICATIONS

- E911 ENABLED MOBILE PHONE
- IN-VEHICLE NAVIGATION SYSTEMS
- LOW POWER HANDHELD GPS RECEIVER
- PC/PDA+GPS INTEGRATION
- ASSET TRACKING

DESCRIPTION

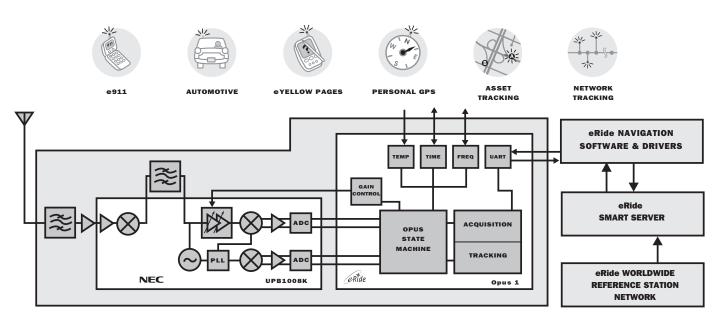
NEC's UPB1008K is a Silicon RFIC especially designed for handheld low power/low cost GPS receivers. The IC combines an LNA, followed by a double-conversion RF/IF downconverter block and a PLL frequency synthesizer on one chip. The second IF Freqency is a pseudo- baseband signal into a on-chip 2-bit A/D converters. The device can operate on a supply voltage as low as 2.7 V, and is a housed in a small 36 pin QFN (Quad, Flat, No-lead) package, resulting in a very low power consumption and reduced board space.

NEC's stringent quality assurance and test procedures ensure the highest reliability and performance.



RF APPLICATION DIAGRAM

ADVANCED GPS COMPLETE SOLUTION



ADVANCED GPS COMPLETE SOLUTION

"NEC Corporation and eRide, Inc. have teamed to provide an advanced positioning solution delivering high GPS performance, accuracy, integration and architecture flexibility. The chip set combines CEL's **UPB1008K** receiver IC with eRide's **Opus One** SOC (System-on-a-Chip) Baseband ASIC and is suitable for standard GPS products as well as Cellular Handset applications. Also provided are scalable client navigation software and drivers, plus location-aiding data from eRide's Smart Server. Together, they offer a complete hardware/infrastructure solution.

The chip set's design allows it to operate independently of wireless interface standards - and independently of the host product's CPU and Operating System. This unique approach to system integration makes it easy to deploy the chip set into an wireless application, in any wireless network. A "Universal Hardware" solution, the design promises lower manufacturing costs and, ultimately lower cost to the consumer.

The chip set's advanced positioning architecture offers unmatched sensitivity providing fast, accurate positioning architecture offers unmatched sensitivity providing fast and accurate position fixes, even when indoors or in deep in urban canyons."

HIGH PERFORMANCE GPS OMNI MODE

LI, C/A code receiver

Performance	Indoor	Outdoor
Time to First Fix w/ aiding	5-7sec	1-3sec
Time to First Fix w/o aiding	10-20sec	3-5sec
Accuracy	10-25m cep	2-5m cep
Sensitivity	-155dBm	-142dBm
	in 1sec dwells	in two 10msec dwells

Superior performance in high reflection indoor environments and in urban canyon types of outdoor environments

POWER DISSIPATION

First Fix	400 mW
Tracking	200-300 mW
Stand By	30 mW

ELECTRICAL CHARACTERISTICS (TA = 25°C, Vcc = 3.0 V, unless otherwise specified)

SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	ТҮР	MAX
lcc	Total Circuit Current, No Signals	mA	14	18	23.5
Vcc	Supply Voltage	V	2.7	3.0	3.3
ICC_PD	Power down current, PIN 13 = VIL	μΑ	-	1	10
Icc rf	RF Block Circuit Current (pin 3), No signal	μΑ	0.4	0.5	0.7
lcc lo	VCO Block Circuit Current (pin 7), No signal	mA	4.1	5.6	7.2
ICC pll	PLL Block Circuit Current (pin 9), No signal	mA	2.7	3.6	4.7
ICC bb	Baseband Block Circuit Current (pin 23), No signal,	mA	2.5	3.4	4.3
	open load				
ICC if	IF Block Circuit Current (pin 28), No signal	mA	2.7	3.7	4.7
ICC Ina	Pre-Amplifier Open Connector Current (pin 36), No signal	mA	1.0	1.4	1.8

LNA/RF DOWNCONVERTER

(fRFin = 1575.42 MHz, f1stLoin = 1400 MHz, PLO = -10 dBm, f1stIF = 175 MHz, Pin 13: VIL = 3 V, ZL differential = 32Ω & Zs = Γopt)

SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	ТҮР	МАХ
CGLNA_MIX	Power conversion gain from 2nd LNA/mixer to 1st IF, $P_{RFin} = -50 \text{ dBm}$	dB	18	23	28
NFlna_mix	Noise Figure of 2nd LNA/mixer(SSB), Input matched	dB	-	5	-
P1dBLNA_MIX	1 dB Compression refer to source, Input matched	dBm	-	-38	-
ZLNAin	RF Input Impedance of LNA	Ohm	-	31	-
ZMIXout	IF Output Impedance of Mixer	Ohm		32	
Alo-IF	Local Signal Leak to IF, f1stLOin=1400 MHz, PLO = 0 dBm	dBm	_	-35	_
Alo-RF	Local Signal Leak to RF, f1stLOin=1400 MHz, PLO = 0 dBm	dBm	_	-50	-

PLL

SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	ТҮР	MAX
Ісрон	PLL Charge Pump High Side Current @ VCPout = VCC/2	μA	-	200	-
ICPOL	PLL Charge Pump Low Side Current @ VCPout = VCC/2	μΑ	-	-200	-
fpd	Phase Comparison Frequency	MHz	-	13.5	-

CRYSTAL OSCILLATOR/REVERENCE AMPLIFIER BLOCK

SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	ТҮР	MAX	
VREFin	Reference input minimum level	mVpp	50	200	-	
fref	Input Frequency of Reference Input	MHz	_	27	_	
VT	VCO Control Voltage, PLL Locked	V	0.8	1.5	2.2	
C/N	VCO C/N, \triangle 1kHz, Loop band width = 5 kHz	dBc/Hz	57	62	_	

AGC AMPLIFIER, I-Q DEMODULATOR, and ADC BLOCK(f1stlFin = 175 MHz, Zin = 600Ω)

			,		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
CGAGC/MIX	Maximum voltage conversion gain of AGC amplifier/ I-Q mixer, Pin = -60 dBm, VAGC = 0.5 V, Unmatched	dB	_	30	-
	Minimum voltage conversion gain of AGC amplifier/ I-Q mixer, Pin = -60 dBm, VAGC = 2.0 V, Unmatched	dB	_	-15	-
AAGC/MIX	AGC control range, VAGC = 0.5 V to 2 V	dB	25	45	_
P1dBAGC	1 dB compression input to AGC amplifier, set voltage gain = 30 dB	dBm	_	-45	-
VAGC	AGC control voltage	V	0.5	-	2.0
BW	3dB Mixer Bandwidth	MHz	-	10	-
VIQ-C	IQ BalanceControl Voltage, Gain(Ich) = Gain (Qch)	V	_	2.1	2.8
AlQ-C	IQ Balance Control Gain Range, VIQ-C = 0 to 3 V	dB	4.0	6.5	-
Duty Ich	Ich Mag Bit Output Pulse Duty, P1stlFin = -84 dBm VAGC = 0.5 V , VIQ-C = 0 V	%	50	-	-
Duty Qch	Qch Mag Bit Output Pulse Duty, PIF2in = -88 dBm VAGC = 0.5 V, VIQ-C = 0 V	%	50	-	-
BASEBA	ND AMPLIFIER BLOCK (Zs = $2k\Omega \& ZL = 2 k\Omega$)				
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	ТҮР	MAX
Vввон	Baseband output logic high, CL = 10 pF	V	2.0	-	-
Vbbol	Baseband output logic low, CL = 10 pF	V	0	-	0.5

ABSOLUTE MAXIMUM RATINGS^{1,2} (TA = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
Vcc	Supply Voltage ⁴	Vcc	3.6
PD	Total Power Dissipation ³	mW	361
Тор	Operating Temperature	°C	-40 to +85
Тѕтс	Storage Temperature	°C	-55 to +150
ICC_total	Total Circuit Current ⁴		

Notes:

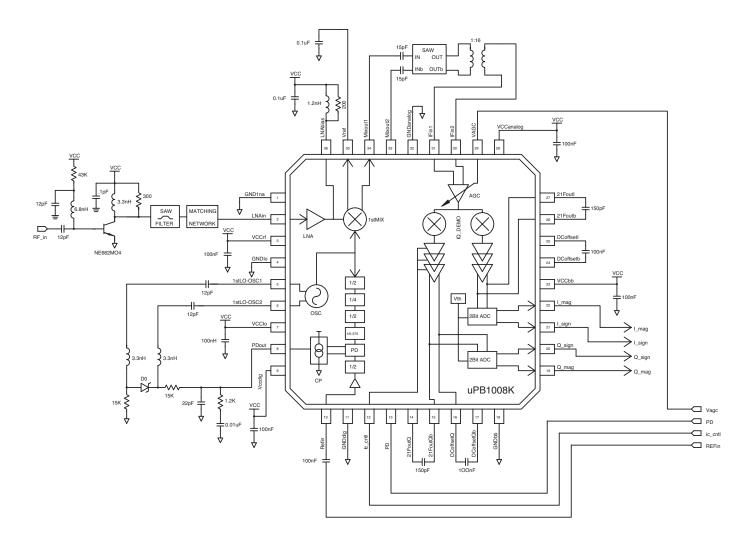
1. Operation in excess of any one of these parameters may result in permanent damage.

- 2. More than two items must not be reached simultaneously.
- 3. TA = $+85^{\circ}$ C, mounted on a 50 x 50 x 1.6 mm double-sided copper clad epoxy glass PWB.
- 4. TA = 25°C

RECOMMENDED OPERATING CONDITIONS

SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
Vcc	Supply Voltage	V	2.7	3.0	3.3
Тор	Operating Temperature	°C	-40	+25	+85
fRFin	RF Input Frequency	MHz		1575	
fREFin	Reference Frequency	MHz		27	
f1stLO	1st LO Oscillating				
	Frequency	MHz		1400	
f1stlFin	1st IF Input Frequency	MHz		175	
f2ndLOin	2nd LO Input Frequency	MHz		175	
Vih	Power Down Control				
	Voltage "High"	V	2		Vcc
VIL	Power Down Control				
	Voltage "Low"	V	0		0.5

APPLICATION CIRCUIT



UPB1008K

Pin No.	Symbol	Function and Application	Internal Equivalent Circuit
1	GNDIna	Ground pin of LNA	30
2	LNAin	Input pin of low noise amplifier. It is a single-ended open collector design. Capacitive coupling is required; external matching will improve gain or NF.	
3	VCCrf	Supply voltage pin of LNA, RF mixer and VCO voltage regulator.	70
4	GNDlo	Ground pin of 1st LO Oscillator circuit and RF Mixer.	3 0 1 = 200 2 = 200 2 = 200 2 = 200 2 = 200
5	1stLO-OSC1	Pin 5 & 6 are base pins of the differential	
6	1stLO-OSC2	amplifier for 1st LO oscillator. These pins require an LC (varacator) tank circuit to oscillate at around 1400 MHz.	
7	VCClo	Supply voltage pin of oscillator circuit for 1st LO Oscillator and RF mixer	Regulator GND 4
8	PDout	This is a current mode charge pump output. For connection to a passive RC loop filter for driving external varactor diode of 1stLO-OSC.	Source Control
9	VCCdig	Supply voltage pin of digital portion of the chip.	GLA WOUL Sink Control
10	REFin	Input pin of reference frequency buffer. This pin should be equipped with external 27 MHz oscillator (e.g. TCXO).	P ↓ ESD r=20k ↓ r=20k ↓ r=20k ↓ r=20k
11	GNDdig	Ground pin of digital portion of the chip.	10 10 10 10 10 10 10 10 10 10

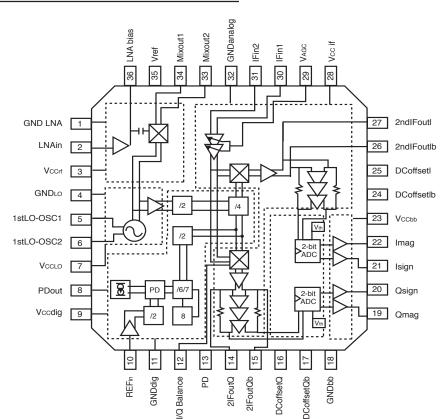
Pin No.	Symbol	Function and Application	Internal Equivalent Circuit
12	I/Q Balance Control	The voltage on this pin controls the Q channel IF Amplifier Gain. Gain control of ±2 dB can be achieved for 0~3 V. Leave open-circuited if not used. Qgain $\int_{0}^{\frac{1}{2}} \int_{0}^{\frac{1}{2}} \int_{0}^{\frac{1}{2}}$	
13	PD1	Standby mode control. Low=whole chip OFF & High=Whole chip ON.	
<u>14</u> 15	2IFout-Q 2IFout-Qb	Differential ouptut pins of quadrature demodulator Q output. Adding a lowpass shunt capacitor between these pins will define the IF Bandwidth.	Aur province of the second sec
16	DC offset Q	DC offset compensation pin for C arm. A low pass capacitor shunt to Pin 17 is required. DC offset compensation pin for Q-bar arm. A low pass capacitor shunt to Pin 16 is required.	Track risk track to be a constrained of the constra

UPB1008K

18 GNDbb Ground pin of CMOS output driver. 20 Gaign Digitized Q signal. Signit of 2-bit ADC output. 21 Isign Digitized Q signal. Signit of 2-bit ADC output. 22 Imag Digitized Q signal. Signit of 2-bit ADC output. 23 VCCbb Supply voltage pin of CMOS output driver. 24 ISignal. Signit of 2-bit ADC output. Digitized 1 signal. Magnitude bit of 2-bit ADC output. 25 VCCbb Supply voltage pin of CMOS output driver. See pin 16 & 17 schematic 26 DCoffsetd DC offset compensation pin for I am. See pin 16 & 17 schematic 26 DCoffsetd Offset compensation pin for I am. See pin 16 & 17 schematic 27 21Four-b Differential output pins of tart IF as outgate. See pin 16 & 17 schematic 28 VCC1 Gain control voltage pin of IF amplifier. See pin 16 & 17 schematic 29 VVcC Gain control voltage pin of 1 st. IF AGC amplifier See pin 14 & 15 schematic 29 VVcC Gain control voltage pin of 1 st. IF AGC amplifier See pin 14 & 15 schematic 30 IF-int Differential output pins of 1st. IF AGC amplifier See pin 16 & 17 schematic	Pin No.	Symbol	Function and Application	Internal Equivalent Circuit
19 Orage Digitized C Signal. Magnitude bit d 2-bit ACC output. 22 Digitized C Signal. Sign bit of 2-bit ACC output. Isign Digitized Signal. Sign bit of 2-bit ACC output. 23 VCCbb Supply voltage pin of CMOS output driver. Image: signal digital bit of 2-bit ACC output. 24 DCoffsetIb DC offset compensation pin for 1-bar arm. A low pass capacitor shunt to Pin 25 is required. See pin 16 & 17 schemalic 25 DCoffsetIb DC offset compensation pin for 1-bar arm. A low pass capacitor shunt to Pin 25 is required. See pin 16 & 17 schemalic 26 DCoffsetIb DC offset compensation pin for 1-bar arm. A low pass capacitor shunt to Pin 25 is required. See pin 14 & 15 schemalic 28 VCC if Supply voltage pin of analog portion of the chip. See pin 14 & 15 schemalic 28 VCC if Supply voltage pin of analog portion of the chip. See pin 14 & 15 schemalic 29 VAcc Supply voltage pin of analog portion of the chip. See pin 14 & 15 schemalic 29 VAcc Supply voltage pin of analog portion of the chip. See pin 14 & 15 schemalic 29 VAcc Supply voltage pin of analog portion of the chip. See pin 14 & 15 schemalic 30 IF-in1 Differential input pins of 1st	18	GNDbb	Ground pin of CMOS output driver.	230
20 Caigin Digitized C aignal. Sign bit of 2-bit ADC output. 21 Isign Digitized I signal. Sign bit of 2-bit ADC output. 22 Imag Digitized I signal. Magnitude bit of 2-bit ADC output. 23 VCCbb Supply voltage pin of CMOS output driver. 24 DCoffsetIb DC offset compensation pin for I-bar arm. A low pass capacitor shunt to Pin 2-bit required. See pin 16 & 17 schemalic 25 DCoffsetI DC offset compensation pin for I-bar arm. A low pass capacitor shunt to Pin 2-bit required. See pin 16 & 17 schemalic 26 21Fourb Differential output pin of characterize and and an advector shunt to Pin 2-bit required. See pin 14 & 15 schematic 27 21Fourb Differential output pin sof for I arm. A low pass capacitor shunt to Pin 2-bit required. See pin 14 & 15 schematic 28 VCC if Surgiv voltage pin of analog potion of the chip. See pin 14 & 15 schematic 29 VGC if Surgiv voltage pin of analog potion of the chip. See pin 14 & 15 schematic 29 VGC if Surgiv voltage pin of analog potion of the chip. See pin 14 & 15 schematic 30 IF-in1 Differential nput pins of 1st IF AGC amplifier See pin 14 & 15 schematic 31 IF-in2 D				
1 Isign Digitized I signal. Sign to 12-bit ADC output. 22 Image Digitized I signal. Magnitude bit of 2-bit ADC output. 23 VCCbb Supply voltage pin of CMOS output driver. 24 DCoffsettlb DC offset compensation pin for I-bar arm. A low pass capacitor shunt to Pin 25 is required. 25 DCoffsettl DC offset compensation pin for I arm. A low pass capacitor shunt to Pin 25 is required. 26 D2/foot Differential output pins of quadrature democulator I output. Adding a lowpass shunt in E-bandwidth. 26 21/four-bit Differential output pins of quadrature democulator I output. Adding a lowpass shunt in E-bandwidth. 28 VCC if Supply voltage pin of an adding a lowpass shunt in E-bandwidth. 29 VAcc Gain control voltage pin of I fe millier. This voltage adding a lowpass shunt in this default at maximum gain. 30 IE-in1 Differential input pins of 1st IF AGC amplifier 31 IE-in2 Offserential output pins of 1st IF AGC amplifier 32 ONDanalog Ground pin of analog portion of the chip. 33 IE-in2 Differential output pins of RF mixer. This is an emitter 34 Mixout1 Difforential output pins of RF mixer. This is an emitter 34				
22 Image Digitized 1 signal. Magnitude bit of 2-bit ADC output. 23 VCCbb Supply voltage pin of CMOS output driver. 24 DCoffsettb DC offset compensation pin for I-bar arm. A low pass capacitor shunt to Pin 25 is required. 25 DCoffsett DC offset compensation pin for I-bar arm. A low pass capacitor shunt to Pin 25 is required. 26 21Foul-H Deferrential output not of quadrature capacitor between these pin swill define the 1 27 21Foul-H Differential output not of quadrature capacitor between these pin swill define the 1 28 VCC bf Supply voltage pin of ranking portion of the chip. 29 VAcC Gain control voltage pin of 1 arm (gain dawn), if this pin sleft open, then it is default at moximum gain. 30 IF-in1 Differential input pins of 1 st IF AGC amplifier 31 IF-in2 Ground pin of analog portion of the chip. 32 GNDanalog Ground pin of analog portion of the chip. 33 IF-in1 Differential input pins of 1st IF AGC amplifier 34 Mixoul1 Differential output pins of RF mixor. This is an emitter follower output buffer, provide a 502 output load.			Digitized L signal. Sign bit of 2-bit ADC output	F=21.5
23 VCCbb Supply voltage pin of CMOS output driver. 24 DCoffsetIb DC offset compensation pin for Hbar arm. A low pass capacitor shunt to Fin 25 is required. 26 DCoffsetI DC offset compensation pin for Hbar arm. A low pass capacitor shunt to Fin 25 is required. 26 2/Foul-Ho DT offset compensation pin for Hbar arm. A low pass capacitor shunt to Fin 25 is required. 27 2/Foul-Ho DT offset compensation pin for I arm. Capacitor between these pins will define the HE bandwidth. See pin 14 & 15 schematic 28 VCC if Supply voltage in of analog portion of the chip. See pin 14 & 15 schematic 29 VAcc Gain Response of the input pins of 1st IF AGC amplifier See pin 14 & 15 schematic 30 IF-in1 Differential input pins of 1st IF AGC amplifier If Fin2 31 IF-in2 Ground pin of analog portion of the chip. If find ping find analog portion of the chip. 31 IF-in2 Differential input pins of 1st IF AGC amplifier If find ping find analog portion of the chip. 32 GNDanalog Ground pin of analog portion of the chip. If find ping find analog portion of the chip. 33 Mixout1 Differential output pins of FF mixer. This is an emitter follower output buffer, provide a 500 output load.				
24 DCoffsetIb DC offset compensation pin for 1-bar arm. A low pass capacitor shunt DP in 25 is required. See pin 16 & 17 schematic 25 DCoffsetI DC offset compensation pin for 1-bar arm. A low pass capacitor shunt DP in 25 is required. See pin 16 & 17 schematic 26 2iFoul-I demods/dbn 10 Pin 24 is required. See pin 16 & 17 schematic 27 2iFoul-I demods/dbn 10 Pin 24 is required. See pin 14 & 15 schematic 28 VAcC Gan control voltage pin of macip proton of the chip. See pin 14 & 15 schematic 29 VAcC Gan control voltage pin of analog proton of the chip. See pin 14 & 15 schematic 30 IF-in1 Differential input pins of 1st IF AGC amplifier See pin 14 & 15 schematic 31 IF-in2 Ground pin of analog portion of the chip. See pin 14 & 15 schematic 31 IF-in2 Differential input pins of 1st IF AGC amplifier See pin 14 & 15 schematic 32 GNDanalog Ground pin of analog portion of the chip. See pin 14 & 15 schematic 33 Mixout1 Differential input pins of 1st IF AGC amplifier See pin 14 & 15 schematic 34 Mixout1 Differential output pins of RF mixer. This is an emitter See pin 14 & 15 schematic		VCCbb	Supply voltage pin of CMOS output driver.	
A low pass capacitor shunt to Pin 25 is required. 25 DCoffset 26 21Fout-10 27 21Fout-10 28 VCC if 29 VAcc 29 VAcc 29 VAcc 20 15 20 16 21 5 21 5 21 5 22 VAcc 23 VAcc 24 VAcc 25 0 26 16 27 21 28 VCC if 29 VAcc 20 Gain control voltage pin of analog portion of the chip. 21 Typical AGC 22 VAcc 30 IF-in1 31 IF-in2 32 GNDanalog 31 IF-in2 32 GNDanalog 33 Mixout1 34 Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 502 output load.				
A low pass capacitor shunt to Pin 24 is required. 26 21Foult-b 27 21Foult-b 28 VCC if 29 VAcc 29 VAcc 20 21Foult-b 21 Supply voltage pin of analog portion of the chip. 28 VCC if 29 VAcc 20 Gain control voltage pin of 1F amplifier. This voltage performs reverse control (i.e., VAcc up → gain down). If this pin is left open, then it is default at maximum gain. 30 IF-in1 31 IF-in2 32 GNDanalog Ground pin of analog portion of the chip. 33 Mixout1 34 Mixout1			A low pass capacitor shunt to Pin 25 is required.	See pin 16 & 17 schematic
27 2IFoul-I demodulator I output. Adding a lowpass shurt IF bandwitch. 28 VCC if Supply voltage pin of analog portion of the chip. 29 Vacc Gain control voltage pin of IF amplifier. This voltage performs reverse control, (i.e., Vacc up → gain down). If this pin is left open, then it is default at maximum gain. 			A low pass capacitor shunt to Pin 24 is required.	
27 2IFoul-I demodulator I output. Adding a lowpass shurt IF bandwitch. 28 VCC if Supply voltage pin of analog portion of the chip. 29 Vacc Gain control voltage pin of IF amplifier. This voltage performs reverse control, (i.e., Vacc up → gain down). If this pin is left open, then it is default at maximum gain. 		2IFout-Ib	Differential output pins of quadrature	See pin 14 & 15 schematic
28 VCC if Supply voltage pin of analog portion of the chip. 29 Vacc Gain control voltage pin of 1 analog portion of the chip. 29 Vacc Gain control voltage pin of 1 analog portion of the chip. 30 IF-in1 Differential input pins of 1st IF AGC amplifier. 31 IF-in2 Ground pin of analog portion of the chip. 32 GNDanalog Ground pin of analog portion of the chip. 33 Mixout2 Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50Ω output load.	27		demodulator I output. Adding a lowpass shunt capacitor between these pins will define the IF bandwidth.	
29 VASC Gain control voltage pin of IF amplifier. This voltage proforms reverse control (i.e., VASC up → gain down). If this pin is left open, then it is default at maximum gain. If this pin is left open, then it is default at maximum gain. 30 IF-in1 0 <td></td> <td>VCC if</td> <td>Supply voltage pin of analog portion of the chip.</td> <td>00 P</td>		VCC if	Supply voltage pin of analog portion of the chip.	00 P
30 IF-in1 31 IF-in2 32 GNDanalog Ground pin of analog portion of the chip. 33 Mixout2 34 Mixout1 Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 500 output load.			Gain control voltage pin of IF amplifier. This voltage	28
30 IF-in1 31 IF-in2 32 GNDanalog Ground pin of analog portion of the chip. 33 Mixout2 34 Mixout1				
and maximum gain. and for the constraints of the constraint				
30 IF-in1 31 IF-in2 32 GNDanalog 33 Mixout2 34 Mixout1 Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50£0 output load.				Ŷ
30 IF-in1 31 IF-in2 32 GNDanalog 34 Mixout2 34 Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50Ω output load.			g	L Ľ
30 IF-in1 Differential input pins of 1st IF AGC amplifier 31 IF-in2 32 GNDanalog Ground pin of analog portion of the chip. 33 Mixout2 34 Mixout1 Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50:2 output load.				Å ESD Å r=300
30 IF-in1 Differential input pins of 1st IF AGC amplifier 31 IF-in2 32 GNDanalog Ground pin of analog portion of the chip. 33 Mixout2 34 Mixout1 Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50:2 output load.			30	t ¥ man → To AGC Amp
30 IF-in1 31 IF-in2 32 GNDanalog 33 Mixout2 34 Mixout1 Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50Ω output load.				
30 IF-in1 31 IF-in2 32 GNDanalog Ground pin of analog portion of the chip. 4 Mixout2 33 Mixout1 Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50Ω output load.				29 D
30 IF-in1 Differential input pins of 1st IF AGC amplifier 31 IF-in2 32 GNDanalog Ground pin of analog portion of the chip. 4 Mixout2 33 Mixout1 Mixout1 Differential output pins of RF mixer. This is an emilter follower output buffer, provide a 50Ω output load.			Gain Response	
30 IF-in1 Differential input pins of 1st IF AGC amplifier 31 IF-in2 32 GNDanalog Ground pin of analog portion of the chip. 4 Mixout2 33 Mixout1 Mixout1 Differential output pins of RF mixer. This is an emilter follower output buffer, provide a 50Ω output load.				
30 IF-in1 Differential input pins of 1st IF AGC amplifier 31 IF-in2 32 GNDanalog Ground pin of analog portion of the chip. 4 Mixout2 33 Mixout1 Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50Ω output load.			0	
30 IF-in1 Differential input pins of 1st IF AGC amplifier 31 IF-in2 32 GNDanalog Ground pin of analog portion of the chip. 4 Mixout2 33 Mixout1 Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50Ω output load.				
30 IF-in1 Differential input pins of 1st IF AGC amplifier 31 IF-in2 32 GNDanalog Ground pin of analog portion of the chip. 4 Mixout2 33 Mixout1 Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50Ω output load.			-15	
30 IF-in1 Differential input pins of 1st IF AGC amplifier 31 IF-in2 32 GNDanalog GNDanalog Ground pin of analog portion of the chip. image: state s			$\downarrow \qquad \vdots \qquad \vdots \qquad \vdots \qquad \rightarrow$	32
31 IF-in2 32 GNDanalog Ground pin of analog portion of the chip. 33 Mixout2 34 Mixout1 Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50Ω output load.			0.5 1.5 2 VAGC (V)	
31 IF-in2 32 GNDanalog Ground pin of analog portion of the chip. 33 Mixout2 34 Mixout1 Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50Ω output load.	30	IF-in1	Differential input pins of 1st IF AGC amplifier	28 0
 32 GNDanalog 32 GNDanalog 33 Mixout2 34 Mixout1 Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50Ω output load. 				
33 Mixout2 34 Mixout1 Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50Ω output load.			Ground nin of analog portion of the chin	r=4k r=2k r=2k r=4k
33 Mixout2 34 Mixout1 Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50Ω output load.	52	CINDanalog		
33 Mixout2 34 Mixout1 Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50Ω output load.				
33 Mixout2 34 Mixout1 Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50Ω output load.				│ <u></u> ≱×q+K ≯+-∔+K ≯+- │
33 Mixout2 34 Mixout1 Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50Ω output load.				
33 Mixout2 34 Mixout1 Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50Ω output load.				Regulator =
33 Mixout2 34 Mixout1 Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50Ω output load.				ESD - r=4k ESD
33 Mixout2 34 Mixout1 Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50Ω output load.				
33 Mixout2 34 Mixout1 Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50Ω output load.				
33 Mixout2 34 Mixout1 Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50Ω output load.				
33 Mixout2 34 Mixout1 Mixout1 Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50Ω output load.				r=1.42k r=1.42k
33 Mixout2 34 Mixout1 Mixout1 Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50Ω output load.				32 🔁
34 Mixout1 follower output buffer, provide a 50Ω output load.				
34 Mixout1 follower output buffer, provide a 50Ω output load.				
34 Mixout1 follower output buffer, provide a 50Ω output load.				
34 Mixout1 follower output buffer, provide a 50Ω output load.				
	34	Mixout1	tollower output buffer, provide a 50 Ω output load.	
				[#] [#] ⁺ [−] ^{=1.67p} _{r=111} [±] [±] [±] ^{ESD}
				│ └┉┉┉┋┈┉┟╣╴┇╴┇
				r=111 🚆
۵ ^۰				
				40

Pin No.	Symbol	Function and Application	Internal Equivalent Circuit	
35	Vref	Base-emitter junction voltage wth respect to ground. May be used for biasing an external discrete transistor. Regulation will develop PTAT current.	Regulator GND 4 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	
36	LNAbias	LNA output pin. External bias (Vcc) and matching for gain is required.	See pin 2 schematic	

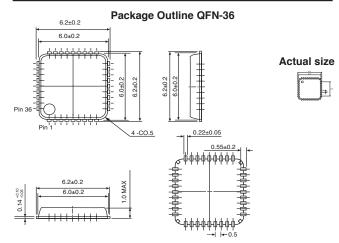
INTERNAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package
UPB1008K-A	36 Pin plastic QFN

OUTLINE DIMENSIONS (Units in mm)



Caution:

The island pins located on the corners are needed to fabricate products in our plant, but do not serve any other function.

Consequently the island pins should not be soldered and should remain non-connection pins.

Life Support Applications

These NEC products are not intended for use in life support devices, appliances, or systems where the malfunction of these products can reasonably be expected to result in personal injury. The customers of CEL using or selling these products for use in such applications do so at their own risk and agree to fully indemnify CEL for all damages resulting from such improper use or sale.

California Eastern Laboratories, Your source for NEC RF, Microwave, Optoelectronic, and Fiber Optic Semiconductor Devices. 4590 Patrick Henry Drive • Santa Clara, CA 95054-1817 • (408) 988-3500 • FAX (408) 988-0279 • www.cel.com DATA SUBJECT TO CHANGE WITHOUT NOTICE



Subject: Compliance with EU Directives

CEL certifies, to its knowledge, that semiconductor and laser products detailed below are compliant with the requirements of European Union (EU) Directive 2002/95/EC Restriction on Use of Hazardous Substances in electrical and electronic equipment (RoHS) and the requirements of EU Directive 2003/11/EC Restriction on Penta and Octa BDE.

CEL Pb-free products have the same base part number with a suffix added. The suffix –A indicates that the device is Pb-free. The –AZ suffix is used to designate devices containing Pb which are exempted from the requirement of RoHS directive (*). In all cases the devices have Pb-free terminals. All devices with these suffixes meet the requirements of the RoHS directive.

This status is based on CEL's understanding of the EU Directives and knowledge of the materials that go into its products as of the date of disclosure of this information.

Restricted Substance per RoHS	Concentration Limit per RoHS (values are not yet fixed)	Concentration contained in CEL devices	
Lead (Pb)	< 1000 PPM	-A Not Detected	-AZ (*)
Mercury	< 1000 PPM	Not Detected	
Cadmium	< 100 PPM	Not Detected	
Hexavalent Chromium	< 1000 PPM	Not Detected	
РВВ	< 1000 PPM	Not Detected	
PBDE	< 1000 PPM	Not Detected	

If you should have any additional questions regarding our devices and compliance to environmental standards, please do not hesitate to contact your local representative.

In no event shall CEL's liability arising out of such information exceed the total purchase price of the CEL part(s) at issue sold by CEL to customer on an annual basis.

See CEL Terms and Conditions for additional clarification of warranties and liability.

Important Information and Disclaimer: Information provided by CEL on its website or in other communications concerting the substance content of its products represents knowledge and belief as of the date that it is provided. CEL bases its knowledge and belief on information provided by third parties and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. CEL has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. CEL and CEL suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.