Bluetooth™ Front-end IC T7024 Design Guide

General Information

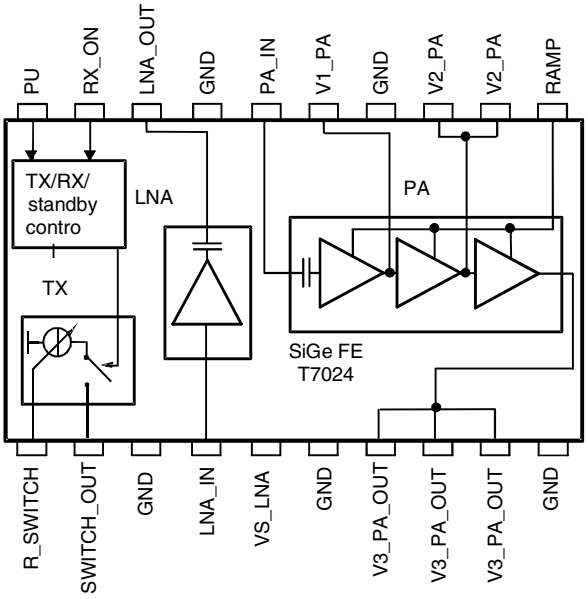
The T7024 is a single supply front-end IC especially designed for applications in the 2.4 GHz to 2.5 GHz frequency band. The front end consists of a Power Amplifier (PA), a Low-Noise Amplifier (LNA) and a switch driver for a PIN diode antenna switch.

The T7024 is compliant with TDMA systems such as Bluetooth™, WDCT.

Since the LNA and the PA can be operated at the same time, the T7024 is also open to other modulation systems when the antenna switch is not needed.

The block diagram of the T7024 is shown in Figure 1.

Figure 1. Block Diagram



The PA is designed as a three-stage amplifier with analog input control (RAMP) for a simplified control of the output power. This control is also used to switch the PA to power-down mode. The PA delivers +23 dBm (200 mW) output power with a high Power Added Efficiency (PAE) of typically 35%. However, power added efficiencies of about 45% can be reached with the QFN20 package.

The LNA is a two-stage amplifier in the 2.4 GHz to 2.5 GHz frequency range with a typical noise figure of 2.1 dB. The LNA has two digital controls. One control toggles between the LNA and the PIN diode switch, the other control switches the LNA and the antenna switch from current-saving standby mode to active mode.

The PIN diode switch activates an external antenna switch. The current consumption of the antenna switch can be controlled by an external resistor.

Bluetooth Front-end IC T7024

Design Guide

Rev. 4549D–BLURF–06/04

Reference Design for PSSO20 Package

The typical application board that supports circuitry of the T7024 in a PSSO20 package is shown in Figure 2, Figure 3 on page 3 and Figure 4 on page 3.

The reference design consists of a four-layer FR4 printed circuit board. The upper layer contains the RF lines and most DC connections. The internal layers are used for ground connections. Some DC connections are made on the backside of the application board. The RF lines for the LNA and PA inputs as well as outputs are 50 Ω lines and a width of 1 mm and a distance of 0.5 mm to the ground layer. A Gerber file with information of the printed circuit is available on request.

The application board consists of 4 layers:

1. Top layer: RF-signals, 35 µm Cu. Spacing: 490 µm FRY
2. Second layer: GND, 35 µm Cu. Spacing: 550 µm FRY
3. Third layer: GND (optional) 35 µm Cu. Spacing: 490 µm FRY
4. Bottom layer: DC connections (optional), 35 µm Cu

Figure 2. T7024 Application Board Photo (PSSO20 Package)

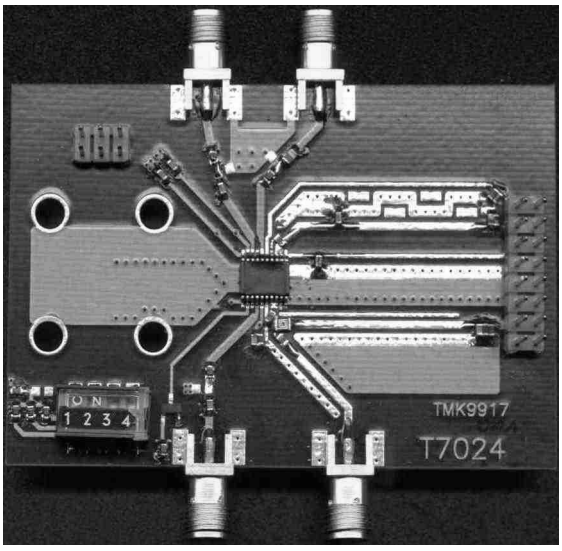


Figure 3. T7024 Application Board Layout (PSSO20 Package)

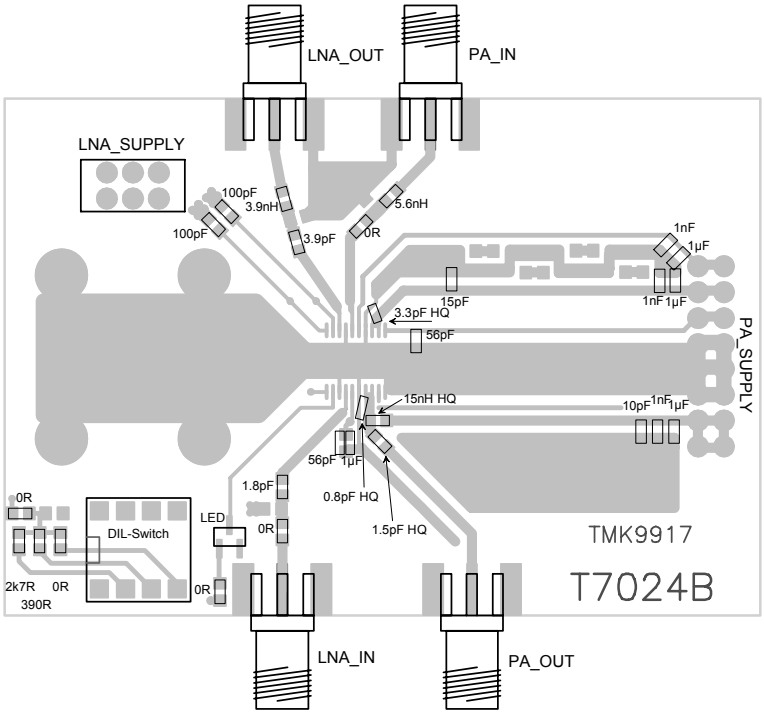
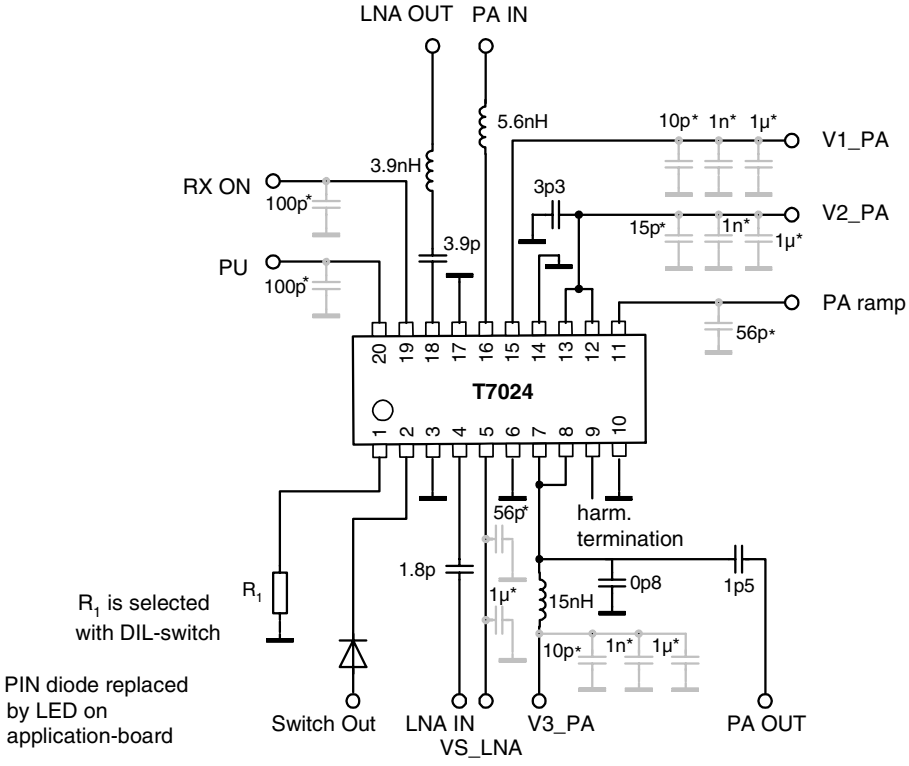


Figure 4. T7024 Application Board Schematic (PSSO20 Package)



*: Only necessary for unstabilized DC supply, depending on application

Reference Design for QFN20 Package

The typical application module support circuitry of the T7024 in a QFN20 package is shown in Figure 6 on page 5, Figure 7 on page 5 and Figure 8 on page 8.

The reference design consists of a four-layer FR4 printed circuit board where the upper layer contains the RF lines and most DC connections. The internal layers are used for ground connections. Some DC connections are made on the backside of the application board. The RF lines for the LNA and PA input and output are 50 Ω lines with a width of 1 mm and a spacing of 0.5 mm to the ground layer. A Gerber file with information of the printed circuit is available on request.

The application board consists of 4 layers:

1. Top layer: RF-signals, 35 µm Cu. Spacing: 490 µm FRY
2. Second layer: GND, 35 µm Cu. Spacing: 550 µm FRY
3. Third layer: GND (optional), 35 µm Cu. Spacing: 490 µm FRY
4. Bottom layer: DC connections (optional), 35 µm Cu

Figure 5. T7024 Application Board Photo (QFN20 Package)

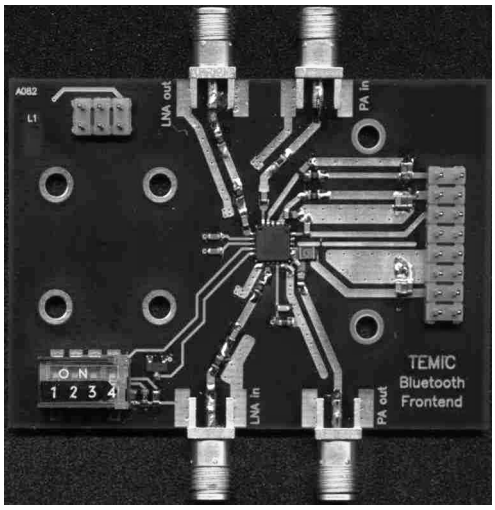


Figure 6. T7024 Application Board Layout (QFN20 Package)

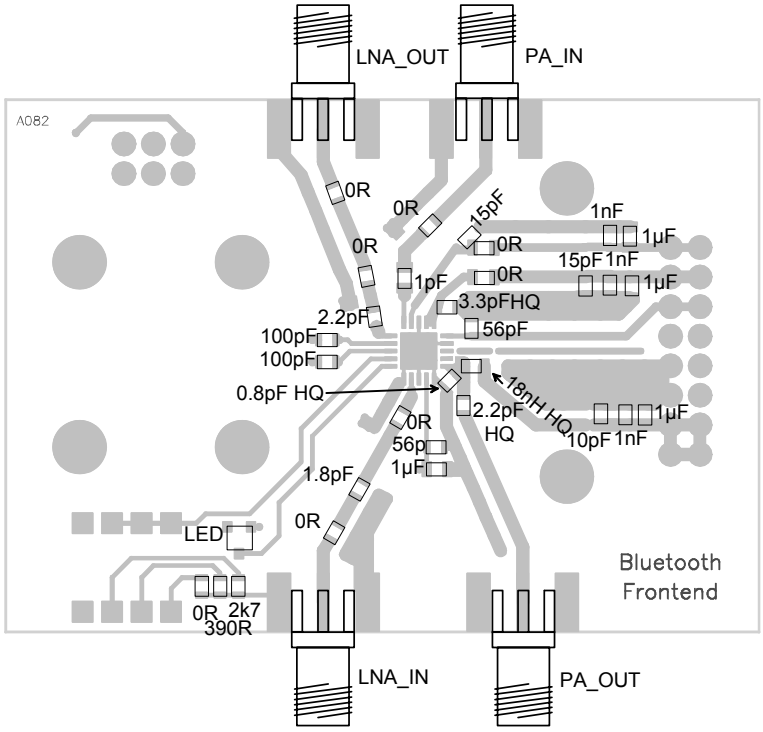
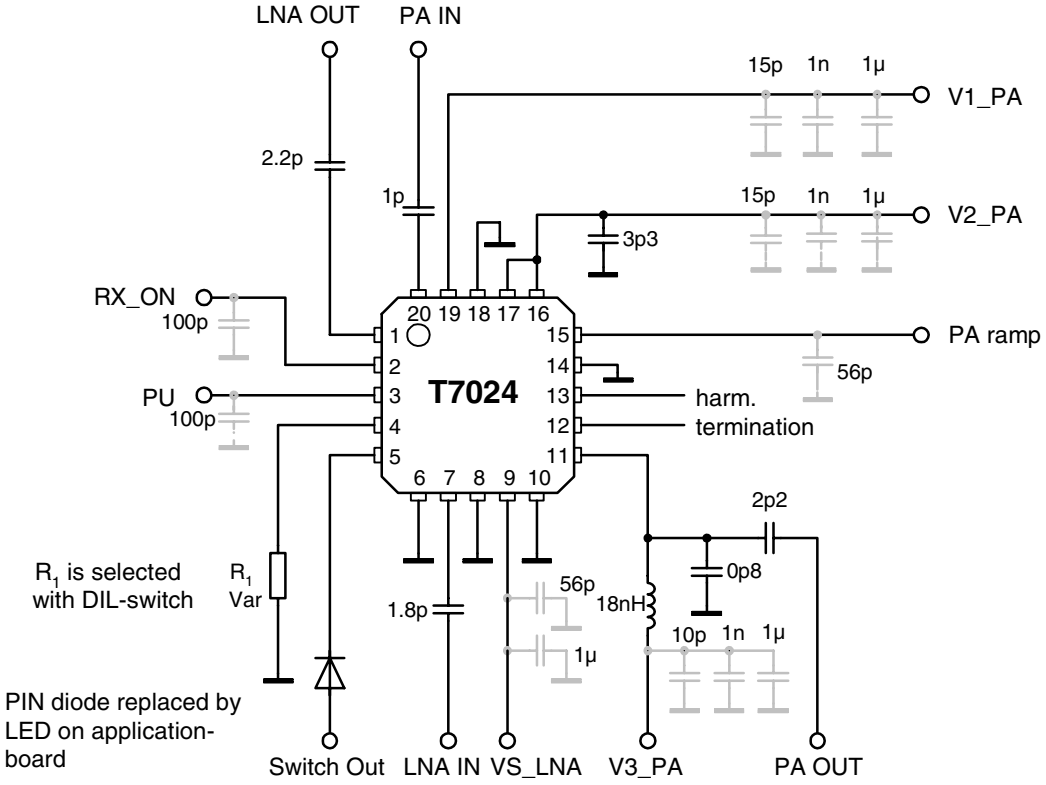


Figure 7. T7024 Application Board Schematic (QFN20 Package)



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Power Amplifier

The power amplifier of the T7024 is designed as a three-stage amplifier. The input stage of the amplifier is AC-coupled to PA_IN. Therefore, a DC blocking capacitor is not necessary at the input port. An external matching circuit should however be designed for optimum performance of the power amplifier. The power amplifier has a nominal input power of 0 dBm. It is therefore recommended that the input circuit should be designed at this value. This has been done for the matching circuits on the application boards. The difference between the input matching circuits for the T7024 in PSSO20 package and the T7024 in QFN20 package result from the fact that the RF performance changes with the different packages.

The power amplifier of the T7024 is turned on and off with the ramp input signal.

It is very important that the slug on the backside of the IC has a good connection to RF ground.

The supply voltage for the collector of the first amplifier stage is connected via V1_PA. Since the collector is internally matched to simplify the handling, an additional matching is recommended. The supply line for the matching is not very sensitive in terms of output power and PAE.

The supply voltage for the collector of the second stage is fed using a 50 Ω transmission line. In both reference designs, a capacitor of 3.3 pF with a high Q value should be placed close to the two IC pins. The RF blocking of this stage with the 15 pF capacitor is done after a length of approximately 10 mm to 15 mm using a 50 Ω transmission line. The matching for the second stage is sensitive. The blocking capacitors should be placed with some distance to the matching capacitor of 3.3 pF, otherwise output power and PAE will drop. Since the matching capacitor (and its resonant frequency) has great influence on the output power, it may be useful to consider using slightly different values (3.0 pF to 3.6 pF), since the exact capacitance and the parasitic influence vary depending on manufacturer and size.

Finally, the third stage uses three output connectors for the open collector. In the reference design for the PSSO20 package, it is recommended that one short stub with a length of 1 mm should be used as a harmonic termination. This harmonic termination is not necessary to achieve the output power, however, a shorting of the second harmonic reduces RF losses in the output transistor and therefore increases the power added efficiency (PAE). The other two output connectors (pin 7 and pin 8) are connected to each other. For the output matching, a capacitor of 0.8 pF to ground and a DC blocking capacitor of 1.5 pF should be used. Make sure that the capacitor to ground is placed very close to the RF output pins. The DC feeding inductor of 15 nH should also be placed near the RF output.

For the output matching, a capacitor of 0.8 pF to ground and a DC blocking capacitor of 2.2 pF should be used. Make sure that the capacitor to ground and the DC blocking capacitor are placed very close to the RF output connector. Finally, the DC feeding inductor of 18 nH should also be placed near the RF output pin 11.

Since the two capacitors play the major role for a good match to 50 Ω for both reference designs, it is recommended that capacitors with a high Q factor are used.

As harmonic terminations, the reference design for the QFN20 package uses actually two short stubs with 1 mm length.

For the design of the output matching circuit, an S-parameter test set or network analyzer may not be used. The measurement of the output matching with a network analyzer results in wrong values since the measurement is done without RF input for the output stage. Moreover, the output stage is sensitive to RF input power and bias, which also changes with the RF input power. The output matching can only be designed using a load pull setup, with which it is possible to measure the output power versus load impedance. If a load pull setup is not available, the described matching with two capacitors can be used to match the impedance of approximately 15 Ω + j17 Ω at load 2.4 GHz (at the output pins) for the PSSO20 package. The load impedance at the output pin 11 for the QFN20 package is approximately 22 Ω + j29 Ω at 2.4 GHz.

The measured load pull data is summarized in Figure 19 on page 15 and Figure 20 on page 15.

The output matching of the power amplifier includes loads which are used as harmonic termination. In Figure 4 on page 3, these lines are called harmonic termination. The harmonic termination consists of an open IC pin, which is internally connected to the PA output. By using this harmonic terminations, the power added efficiency of the PA will be increased. This effect, which influences the PA's output impedance, is included in the reported reference designs.

Please note, that it is important not only to design optimum input and output matching, but also to design the right RF termination at the DC supplies to achieve optimum stability against parasitic oscillations, output power and power added efficiency from the PA.

On the application board, all three stages of the amplifier are separated, allowing access to each collector stage. Blocking capacitors are needed on each stage. In a final design they can be combined to reduce space and costs.

The PA's output power and the current consumption are regulated by the ramp pin, which is also used to switch the PA to standby mode with a low quiescent current of typically below 10 µA. A ramp voltage between 1.3 V and 1.75 V is the usual operating mode of the power amplifier. A higher ramping voltage results in a higher output power of the PA. The operating point of 23 dBm output power is reached at approximately 1.75 V ramp signal.

The ramp control circuit for the T7024 is designed to operate with a control voltage as input signal at the ramp input. However, it is also possible to use a current as an input signal. This has advantages regarding the temperature behavior of the PA. The relation of output power in dependence of ramp current is shown in Figure 8

The temperature compensation of the power amplifier should be done externally, e.g., with a processor with temperature sensor and D/A output which drives the ramp pin of the PA. However, if this circuitry is not available, it is possible to use a solution for a simple temperature compensation, which is sufficient for most needs. This temperature compensation uses the possibility to drive the ramp input with voltage or current simultaneously. Since the temperature behavior of the power amplifier is different for these two modes, it is possible to select an optimum impedance to drive the power amplifier with a specific ramp voltage and ramp current according to the desired output power.

A schematic for this simple temperature compensation is shown in Figure 9 on page 8. The temperature compensation is optimized for different power levels in the range from 1 dBm to 23 dBm at the PA output. The resistors and reference voltages can be adjusted according to different output power levels.

Figure 8. Typical Ramp Curve for T7024 in QFN20 Package (Temperature 20°C)

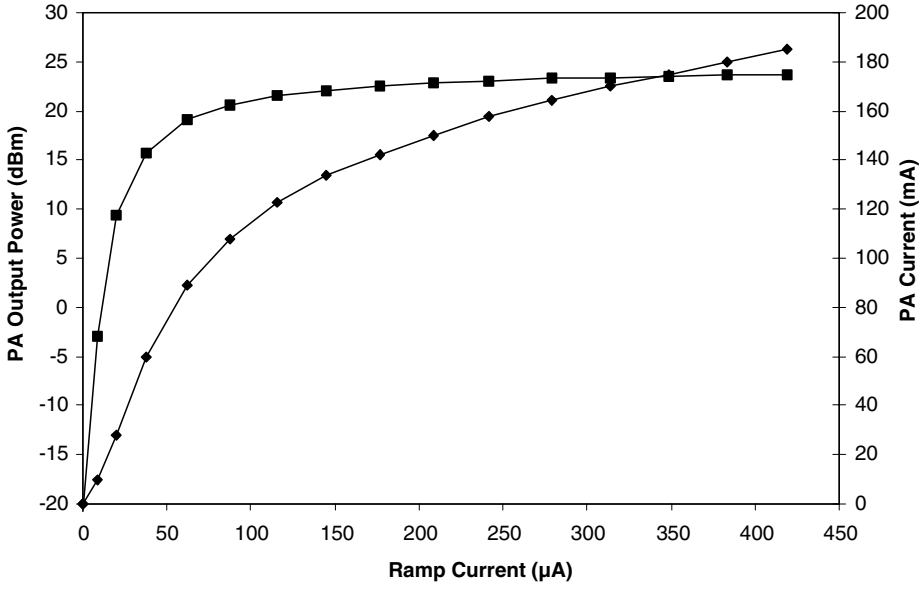
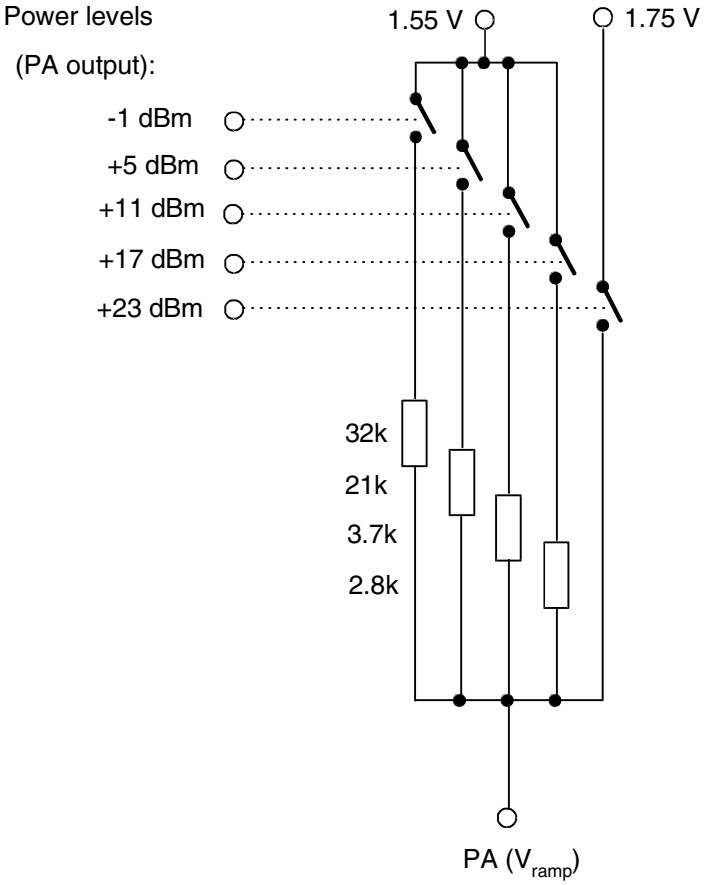


Figure 9. Schematic for Simple Temperature Compensation



Low-noise Amplifier

The Low-Noise Amplifier (LNA) of the T7024 is a two-stage amplifier with an internal matching at 2.45 GHz. The LNA includes DC supply, RF input, RF output, two control signals and ground connections. To achieve good noise figure values, it is recommended that blocking capacitors at the DC supply of the LNA are used.

The RF input is DC-coupled to the internal circuitry. A DC blocking capacitor is therefore necessary at the RF input. This blocking capacitor should also be used for the matching of the input port. A 1.8 pF capacitor is used on the reference designs for matching to 50 Ω and noise matching.

The RF output of the LNA has an internal DC blocking capacitor, therefore, external DC blocking is not necessary. Since the LNA output has only a minor influence on the noise figure, it is sufficient to design an output network with a good match to 50 Ω.

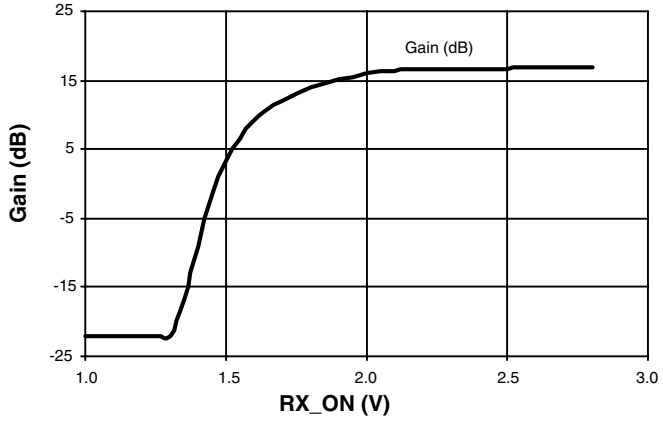
The LNA and the switch driver are controlled by the PU and the RX_ON control pin. A PU high signal switches the LNA from standby mode with low quiescent current to active mode. The RX_ON signal toggles between LNA (RX_ON high) and switch driver (RX_ON low), since the switch driver and the LNA are not used simultaneously, see further design considerations in the next paragraph.

The gain of the integrated LNA may be controlled by an analogue signal at the RX_ON pin. This feature can be used - together with an automatic gain control (AGC) loop in a transceiver - to get optimum signal power level at the receive input of the transceiver. Figure 10 shows the correspondence between RX_ON control voltage and LNA gain.

Please note, that below approximately 1.4 V at RX_ON the LNA/antenna control circuitry switches to transmit mode. Usually, this behavior should be omitted, since a sharp step with additional gain loss of about 15 to 20 dB (depending on antenna switch performance) occurs.

However, if a transceiver can handle this sharp gain step, it may be possible to use this switching as an additional benefit under high power reception.

Figure 10. Gain of T7024 LNA versus RX_ON Voltage

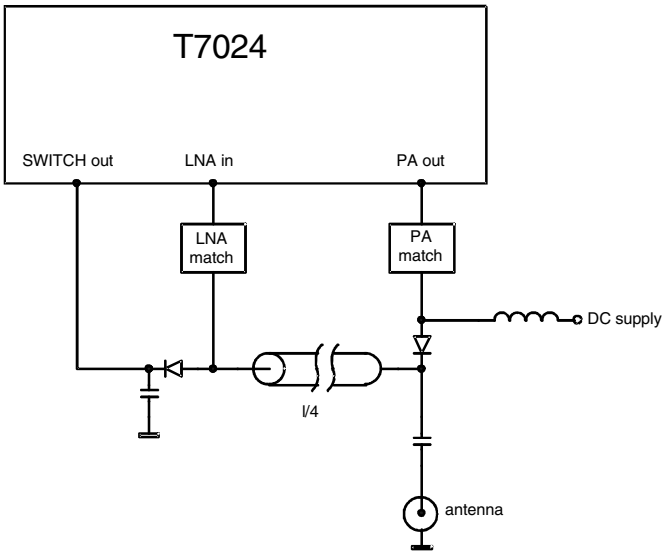


Switch Driver

The switch driver of the T7024 front end is used to realize an antenna switch. A switched current source is used for this purpose. The supply of the LNA is also used for the switch driver. The switch driver is turned on with the control signals PU on high and RX_ON on low.

A typical application of the switch driver is shown in Figure 11.

Figure 11. Antenna Switch with the T7024



The operation of the antenna switch is as follows.

If the LNA and switch driver are in receive mode (RX_ON = high), the switch-out port draws no current. In this case, the diodes can be seen as a high impedance and the LNA input is connected directly to the antenna.

In transmit mode, the RX_ON signal is toggled to low. The switch-out port draws current to ground and the diodes are switched to a low impedance. The PA output is connected directly to the antenna, the quarter wavelength transmission line between the two diodes transforms the short of the capacitor at the switch-out connector to an open at the diode in the PA output line. Therefore, the LNA input is separated from the PA output and the high output power cannot be delivered to the LNA input. The switch-out current is adjusted between approximately 1.7 mA and 19 mA using a reference resistor at the R_SWITCH pin.

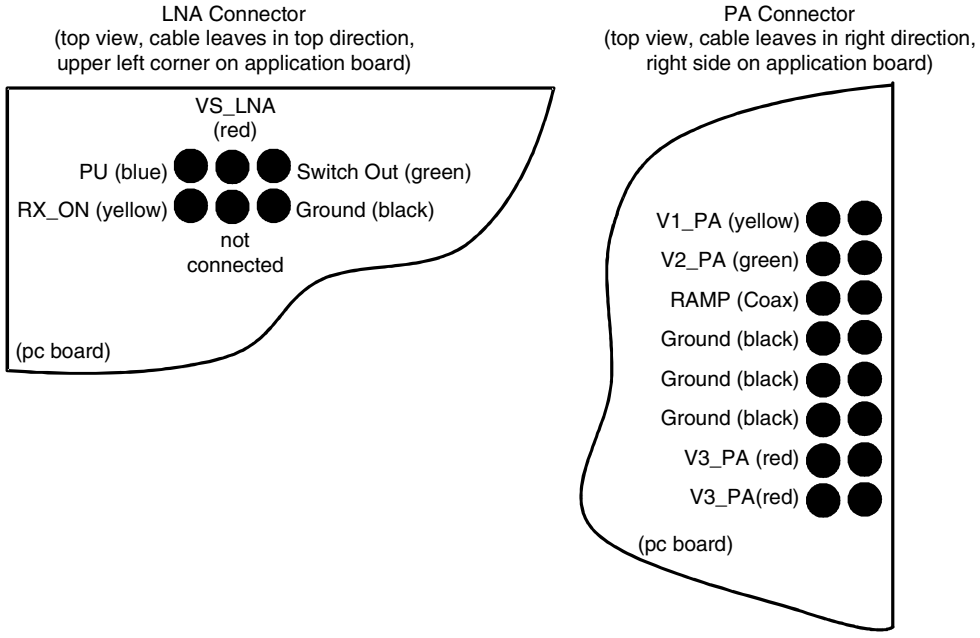
However, the antenna switch is not realized on the application board, thus enabling good access to the LNA input and the PA output. Instead of PIN diodes, the application board is equipped with two LEDs for visualization purposes.

Application Board Connectors

The application uses four SMA female connectors for the RF signals: LNA in, LNA out, PA in, and PA out. The DC connections are realized by two connectors, one for the PA with lines for ramp, ground and the supply voltages for the three-amplifier stages: V1_PA, V2_PA, and V3_PA, and one connector for the LNA with lines for the supply voltage, ground, switch current, PU (power up) and RX_ON.

The two connectors are shown in Figure 12 on page 11.

Figure 12. LNA and PA Connectors for the Application Board



S-parameter Data for the Reference Designs

The following S-parameter diagrams are measured with the described reference designs. However, the reference plane of the calibration is shifted to the input or output pin. The test power for the LNA is -30 dBm, the test power for the PA input is 0 dBm.

Figure 13. Measured S-parameter Data for the LNA Input, QFN20 Package

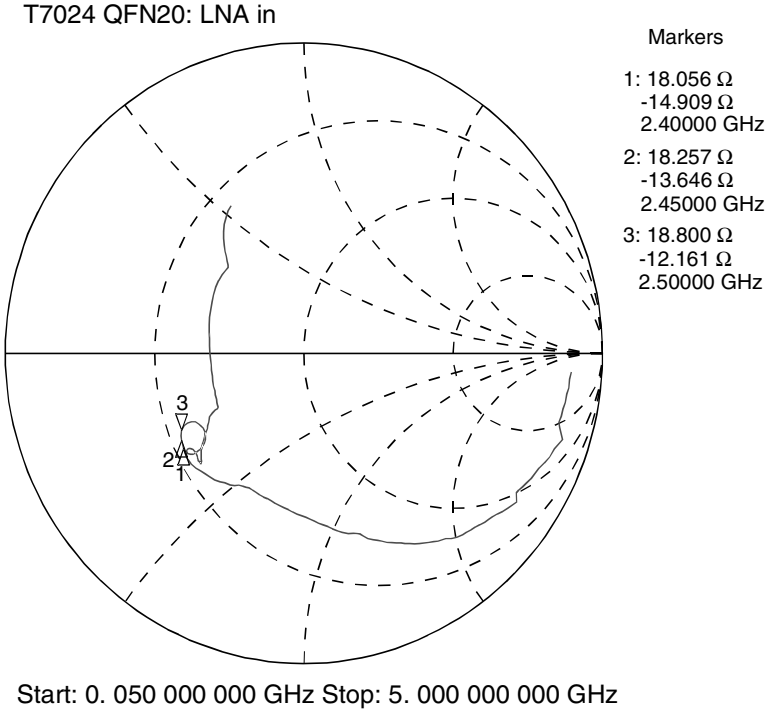


Figure 14. Measured S-parameter Data for the LNA Output, QFN20 Package

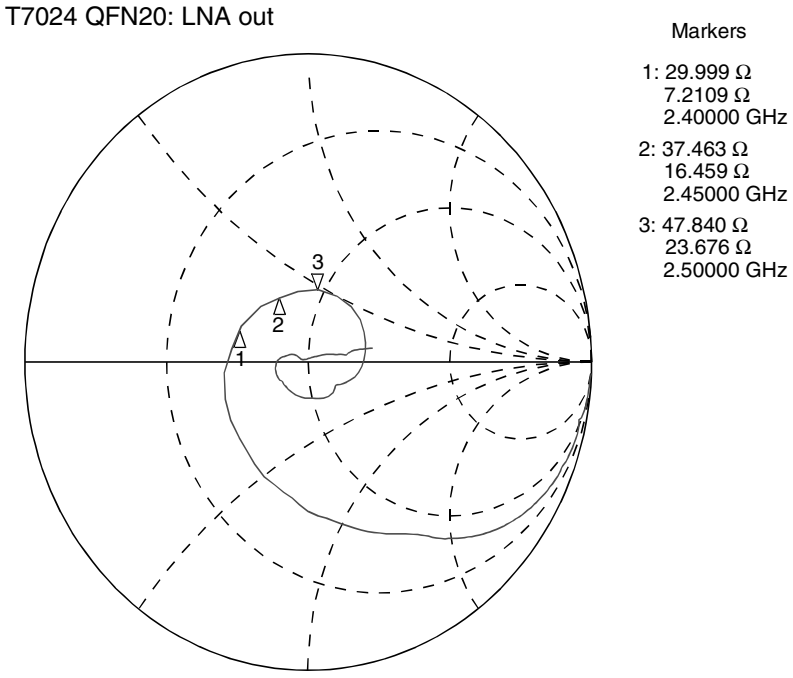


Figure 15. Measured S-parameter Data for the PA Input, QFN20 Package

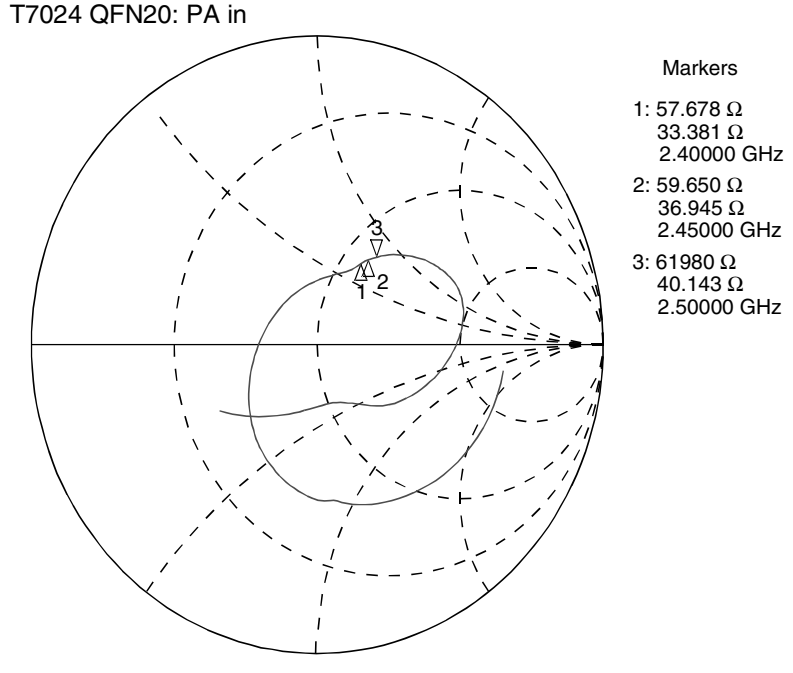


Figure 16. Measured S-parameter Data for the LNA Input, PSSO20 Package

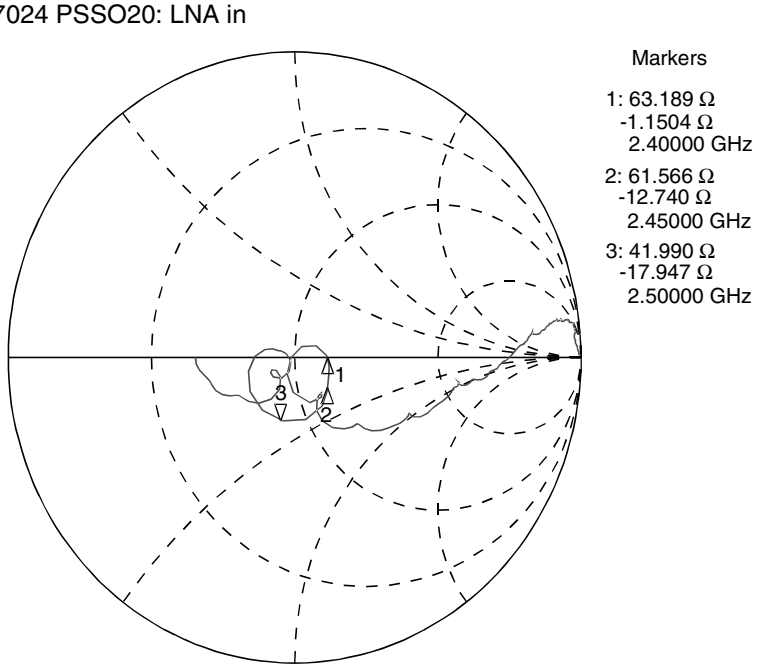


Figure 17. Measured S-parameter Data for the LNA Output, PSSO20 Package

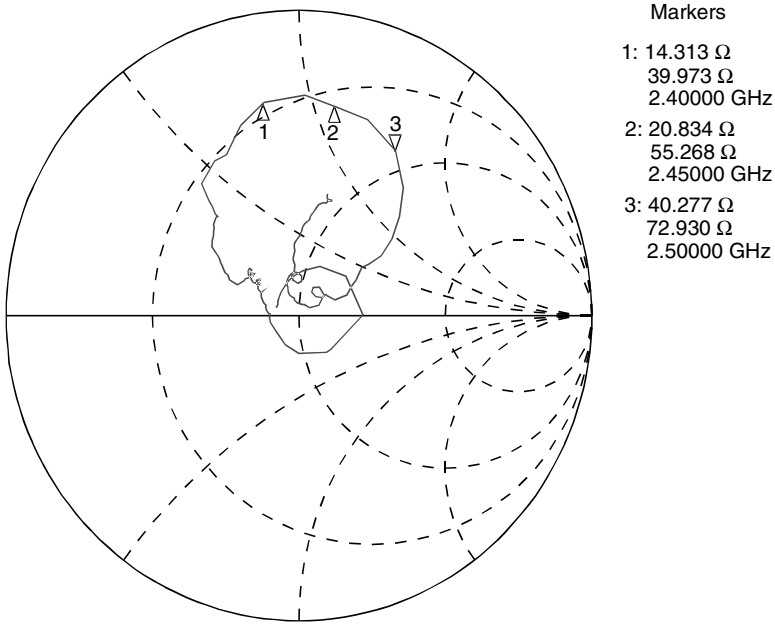
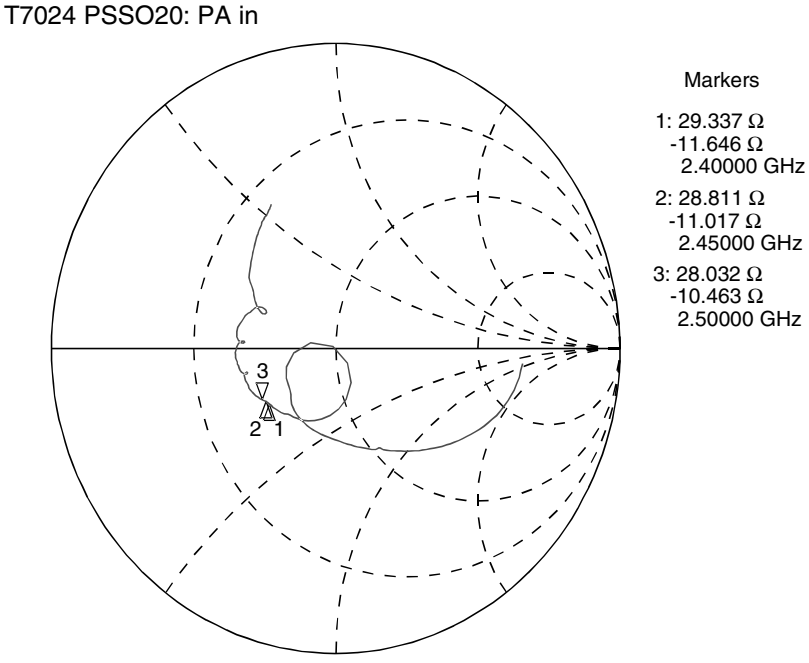


Figure 18. Measured S-parameter Data for the PA Input, PSSO20 Package



Load Pull Data for the Reference Designs

Load pull measurements of the power amplifiers were done by using an ATN load pull system. The measurements were calibrated to the output pins of the power amplifier in order to get the output impedance of the IC. The measurement results are summarized in the Table 1 and in Figure 19 on page 15 and Figure 20 on page 15. The output of the power amplifier uses three pins. However, one pin is used as a harmonic termination. Therefore, during the load pull measurement, the RF load at the two output pins has been changed. The depicted results are the impedances seen by the output transistor for optimum RF power and power added efficiency.

Table 1. Load Impedances for Different Packages and Frequencies

Frequency	Load Impedance PSSO20 Package	Load Impedance QFN20 Package
2.4 GHz	15.0 + j16.8 Ω	22.0 + j28.6 Ω
2.45 GHz	12.7 + j12.8 Ω	19.5 + j28.8 Ω
2.48 GHz	12.0 + j11.7 Ω	16.2 + j21.4 Ω
2.5 GHz	11.9 + j10.3 Ω	14.8 + j24.7 Ω

Figure 19. Measured Load Impedance for the PA Output, PSSO20 Package (Reference: 50 Ω)

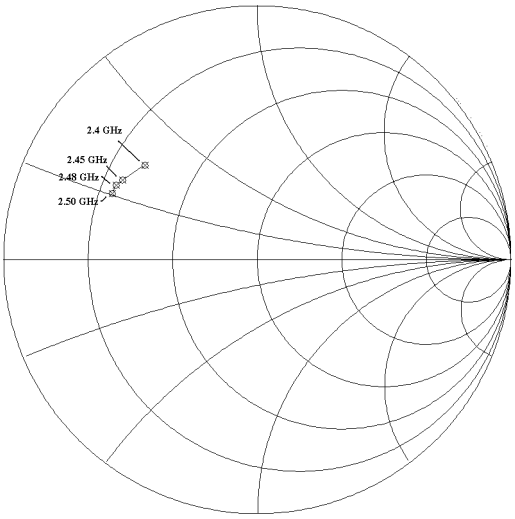
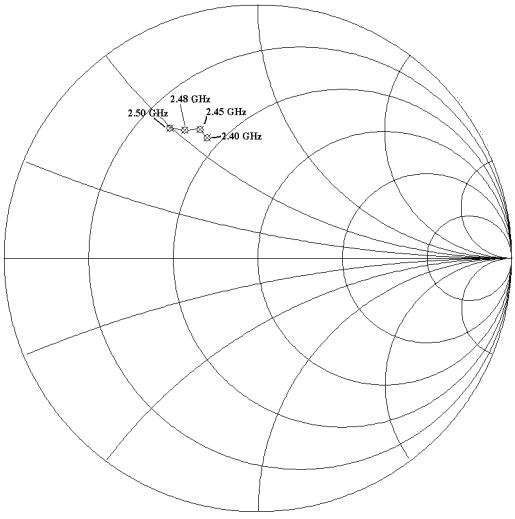


Figure 20. Measured Load Impedance for the PA Output, QFN20 Package (Reference: 50 Ω)



Frequently Asked Questions

1. What is the advantage of SiGe Hetero Junction Transistor Technology?

There are several advantages:

- The silicon material itself has a 3 times higher thermal conductivity compared to GaAs material which leads to a much better thermal dissipation of the heat that is generated in the transistor cells.
- For both bipolar and GaAs transistors an increased beta can be observed with increased device temperature. This leads to higher current and finally to destruction of the transistor. For SiGe devices, there is a decreasing of beta with temperature and therefore a built-in self-stabilization of the transistor cell itself.
- Due to the negligible quiescent current, there is no need for the high side switch transistor normally required by GaAs's even for large transistor structures.
- All necessary circuitry for proper operation of RF power cells (band gap, biasing, ramp voltage generation, temperature compensation a. s. o.) are normally integrated into the main chip.

2. What is the maximum allowed voltage for V_{cbo} and V_{ceo}?

   V_{cbo} (max) = 15 V

   V_{ceo} (max) = 5.5 V

3. What is the typical gain partitioning of three stage power amplifier T7024?

   1^{st} stage: ~12 dB

   2^{nd} stage: ~11 dB

   3^{rd} stage: ~9 dB

   The decreasing gain per stage is due to the size of the stage and the losses in the interstage matching.

4. Is there a chronological order to be obeyed when connecting the PA to power supply?

   Yes, first, make sure that all RF terminals (i.e. RF input and output) are terminated with 50 Ohms. After that, all V_{cc} terminals and grounds need to be connected to the supply and switched on. Then an RF input signal within the frequency range and power range specified in the data sheet has to be applied to the PA input. After that, Vramp can be applied and is used to adjust the RF output power to the desired level.

5. Is it possible to make a short circuit at the RF input or output terminal during operation?

   No, this is strictly forbidden. It is possible to apply a certain mismatch at the output terminal of the PA, but for the exact values and conditions please refer to the data sheet.

6. Is it possible to make a short circuit at the Vcc terminals of the PA during operation or shortly after operation?

   No, we don't recommend to apply a short circuit to the terminals of PA, because - depending on application circuit - there might arise strong voltage peaks due to inductors or other inductive components like feeding lines in the supply chain. These voltages may reach up to 3 times the standard voltage levels and can be measured only with a very fast oscilloscope.

7. What is the purpose of interstage matching?

   The input and output impedance of a single power amplifier stage has to be matched to the impedance of the preceding or following stages respectively. This is done to avoid spurious or unwanted oscillations and to reduce the gain loss due to mismatch.

8. What is the purpose of input and output matching?

- Output matching of PA: the output of the PA device has to be matched to 50 Ohms in order to get maximum output power and efficiency. It normally consists of a transmission line or an inductor and a shunt capacitor to ground.
- Input matching of PA: This is necessary to keep the interaction between PA and preceding stage (i.e. VCO or transceiver circuit) as low as possible. Therefore it is a condition for stable PA operation.
- Input matching of LNA: This matching is necessary to keep the losses and the noise figure low. It has therefore some influence on the sensitivity of the receive path (minimum detectable input power).
- Output matching of LNA: This matching leads to a low loss connection to the transceiver. It also influences the minimum detectable input power.

9. Is it necessary to provide the PU signal, if the PA is driven?

   No, since the PA is turned on and off with the ramp voltage, it is not necessary to provide an PU signal. The PU signal has no influence on the PA.

10. Is it necessary to use a blocking capacitor as part of the LNA input matching?

    Yes, it is necessary to use a blocking capacitor as a matching component for the LNA input, since the input of the LNA is directly connected to the base of the first amplifier stage in order to keep the noise figure to a minimum.

Glossary

Table 2. Used Abbreviations

Abbreviation	Description
AGC	Automatic Gain Control
BOM	Bill Of Material
CW	Continuous Wave
DC	Direct Current
DECT	Digital Enhanced Cordless Telecommunications
DUT	Device Under Test
GaAs	Gallium Arsenic
IC	Integrated Circuit
ISM	Industrial, Scientific,. Measurement
PA	Power Amplifier
PAE	Power Added Efficiency
PCB	Printed Circuit Board
RF	Radio Frequency
SIGE	Silicon Germanium
TDMA	Time Division Multiple Access
VCO	Voltage Controlled Oscillator
WDCT	Worldwide Digital Cordless Telecommunications

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