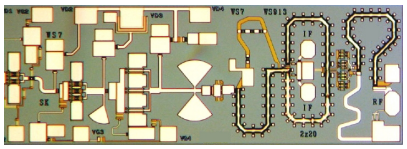
AMMC-3040

18 - 36 GHz Double-Balanced Mixer with Integrated LO Amplifier/Multiplier

Data Sheet



Chip Size: 2520 x 760 µm (99.2 x 29.9 mils)
Chip Size Tolerance: ± 10 µm (± 0.4 mils)
Chip Thickness: 100 ± 10 µm (4 ± 0.4 mils)
Pad Dimensions: 75 x 75 µm (3 ± 0.4 mils)

Description

The AMMC-3040 is a broadband Double-Balanced Mixer (DBM) with an integrated high-gain LO amplifier. This MMIC can be used as either an up converter or down converter in microwave or millimeter wave applications. If desired, the LO amplifier can be biased to function as a frequency multiplier to enable second harmonic mixing of the LO input. The mixer section ofthe AMMC-3040 is fabricated using a suspended metal system to create a unique, broadside-coupled balun structure (patent pending) to achieve exceptional bandwidth. The MMIC provides repeatable conversion loss without tuning, making it highly suitable for automated assembly processes. For improved reliability and moisture protection, the die is passivated at the active areas.

AMMC-3040 Absolute Maximum Ratings[1]

Symbol	Parameters/Conditions	Units	Min.	Max.
$V_{D1, 2, 3, 4}$	Positive Drain Voltage	V		5
$V_{G1, 2, 3, 4}$	Gate Voltage	V	-3.0	0.5
I_{dd}	Total Drain Current	mA		550
T_{ch}	Operating Channel Temp.	°C		+160
T_b	Operating Backside Temp.	°C	-55	
T_{stg}	Storage Case Temp.	°C	-65	+165
T_{max}	Maximum Assembly Temp. (60 sec max)	°C		+300

Note:

1. Operation in excess of any one of these conditions may result in permanent damage to this device.

Features

- High IIP3: +23 dBm
- Wide bandwidth
- RF: 18-36 GHz
- LO: 18-36 GHz
- IF: DC-3 GHz
- Fundamental or subharmonic mixing
- Up or down converter
- Conversion loss: 9.5 dB
- P1dB: +17 dBm
- Low LO drive power: +2 dBm
- Usable to 42 GHz

Applications

- Point-to-point radio
- LMDS
- SATCOM

Note: These devices are ESD sensitive. The following precautions are strongly recommended:
Ensure that an ESD approved carrier is used when dice are transported from one destination to another.
Personal grounding is to be worn at all times when handling these devices.

AMMC-3040 DC Specifications/Physical Properties[1]

Symbol	Parameters and Test Conditions	Units	Min.	Typical	Max.
$V_{D1, 2, 3, 4}$	Drain Supply Operating Voltage	V	2	3.5	5
I_{d1}	First Stage Drain Supply Current, V_{dd} = 3.5 V, V_{g1} = -0.5 V	mA		50	
$I_{D2, 3, 4}$	Total Drain Supply Current for Stages 2, 3 and 4 (V_{dd} = 3.5 V, V_{gg} = -0.5 V)	mA		225	
$V_{G1, 2, 3, 4}$	Gate Supply Operating Voltages (I_{dd} = 250 mA)	V		-0.5	
V_p	Pinch-Off Voltage (V_{dd} = 3.5 V, I_{dd} < 10 mA	V		-1.5	
θ_{ch-b}	Thermal Resistance[2] (Backside Temp. T_b = 25°C)	°C/W		49	

Notes:
1. Measured in wafer form with T_{chuck} = 25°C. (Except θch-bs.)
2. Channel-to-backside Thermal Resistance (θch-b) = 58°C/Ω at Tchannel (Tc)=150°C as measured using the liquid crystal method. Thermal Resistance at backside temperature (T_b) = 25 °C calculated from measured data.

AMMC-3040 RF Specifications

Zo = 50 Ω, Tb = 25°C, IF Output = 2 GHz, LO Input Power = +2 dBm, RF Input Power = -20 dBm, except as noted.

			Vdd = 3.5 V, Idd = 250 mA		Vdd = 4.5 V, Idd = 150 mA
Symbol	Parameters and Test Conditions	Units	Typ.	Max.	Typ.
Lc	Conversion Loss, Down Conversion[1]	dB	9.5	12	10
Lc	Conversion Loss, Up Conversion[2]	dB	10		10.5
$ISOL_{L-R}$	LO - RF Isolation at RF Frequency = 22 GHz[3]	dB	31		32
$P_{-1\ dB}$	Input Power at 1 dB Conversion Loss Compression, Down Conversion	dBm	17		17
IIP3	Input 3rd Order Intercept Point, Down Conversion at RF Frequency = 22 GHz[4]	dBm	23		22

Notes:
1. 100% on-wafer RF testing is done at RF frequency = 18, 22, and 32 GHz.
2. IF Input = 2 GHz, RF Input Power = -20 dBm, RF freq = LO + IF.
3. Does not include LO amplifier gain of ~20 dB.
4. Δf = 2 MHz, RF Input Power = -5 dBm.

AMMC-3040 Typical Performance

Zo = 50 Ω, Tb = 25°C, IF = 2 GHz, LO Input Power = +2 dBm, RF Input Power = -20 dBm, except as noted.

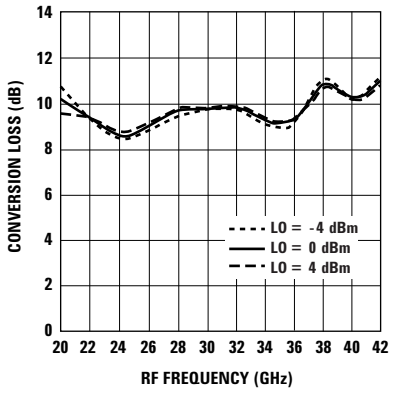


Figure 1. Conversion loss, up conversion. V_d = 3.5 V, I_d = 250 mA, LO freq = RF + IF

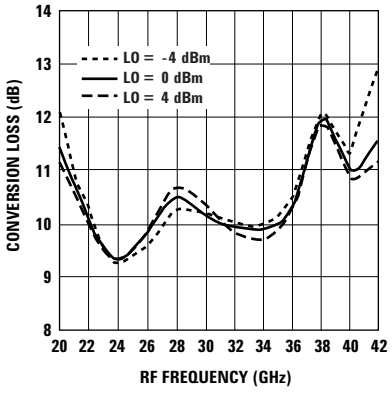


Figure 2. Conversion loss, down conversion. V_d = 3.5 V, I_d = 250 mA, LO freq. = RF – IF

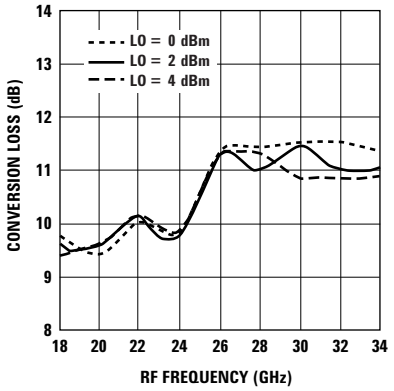


Figure 3. Conversion loss, up conversion. V_d = 4.5 V, I_d = 150 mA, LO freq = RF + IF

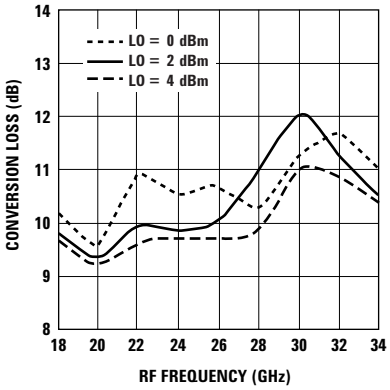


Figure 4. Conversion loss, down conversion. V_d = 4.5 V, I_d = 150 mA, LO freq = RF - IF

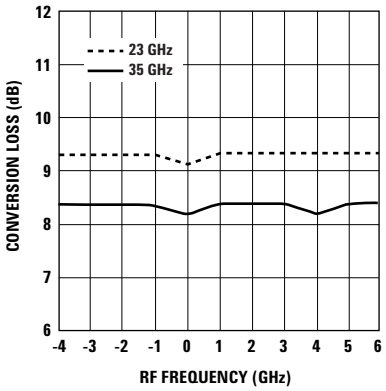


Figure 5. Conversion loss vs. LO input power, up conversion. V_d = 3.5 V, I_d = 250 mA, LO freq = RF + IF

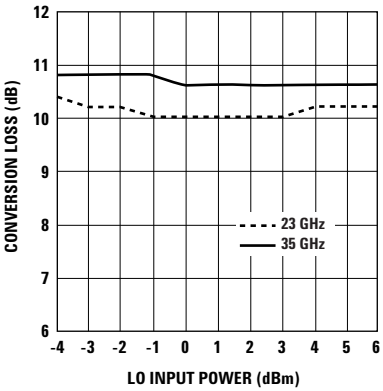


Figure 6. Conversion loss vs. LO input power, down conversion. V_d = 3.5 V, I_d = 250 mA, LO freq = RF - IF

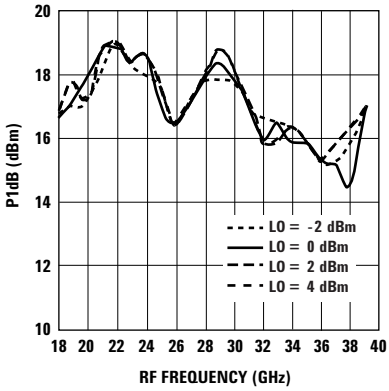


Figure 7. Input power at 1 dB conversion loss compression, down conversion. V_d = 3.5 V, I_d = 250 mA, LO freq = RF - IF

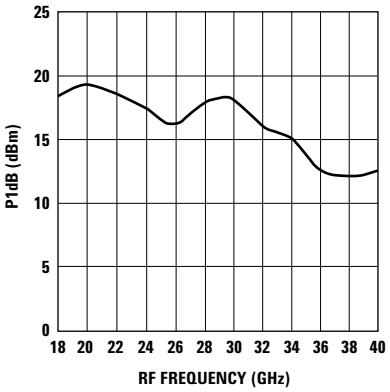


Figure 8. Input power at 1 dB conversion loss compression, up conversion. V_d = 3.5 V, I_d = 250 mA, LO freq = RF + IF

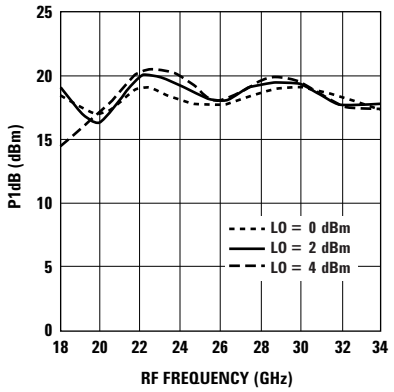


Figure 9. Input power at 1 dB conversion loss compression, down conversion. V_d = 4.5 V, I_d = 150 mA, LO freq = RF - IF

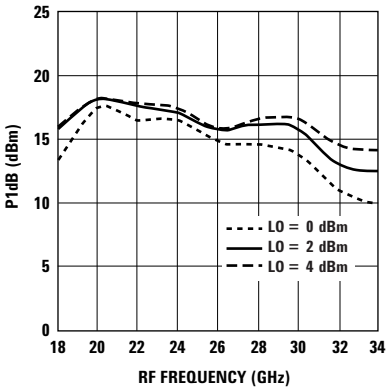


Figure 10. Input power at 1 dB conversion loss compression, up conversion. V_d = 4.5 V, I_d = 150 mA, LO freq = RF + IF

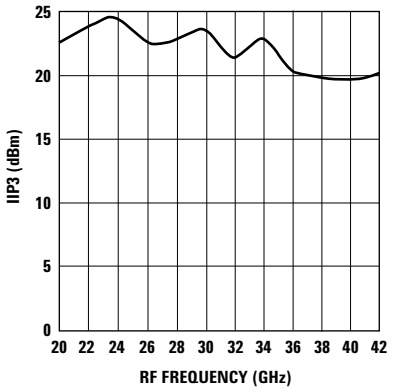


Figure 11. Input 3rd order intercept point, down conversion. V_d = 3.5 V, I_d = 250 mA, LO freq = RF - IF

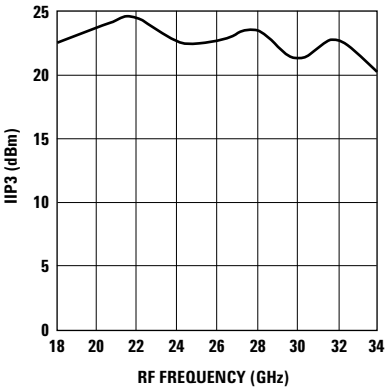


Figure 12. Input 3rd order intercept point, down conversion. V_d = 4.5 V, I_d = 150 mA, LO freq = RF – IF

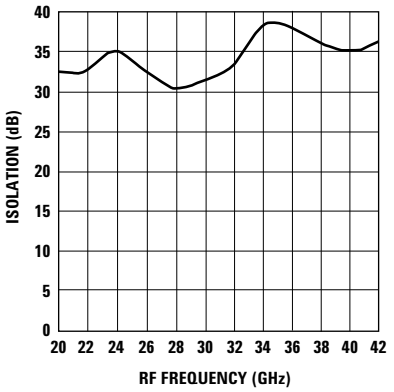


Figure 13. LO-RF isolation, down conversion. V_d = 3.5 V, I_d = 250 mA. Note: Does not include LO buffer amplifier gain of ~ 20 dB, LO freq = RF - IF

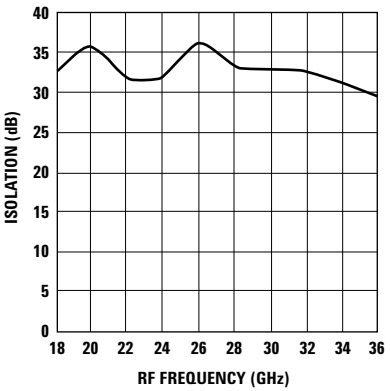


Figure 14. LO-RF isolation, down conversion. V_d = 4.5 V, I_d = 150 mA. Note: Does not include LO buffer amplifier gain of ~ 18 dB, LO freq = RF – IF

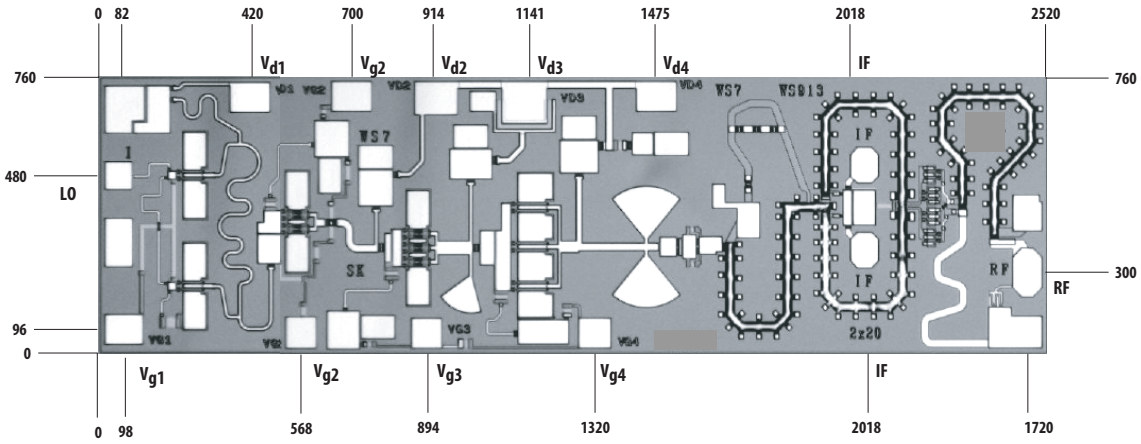
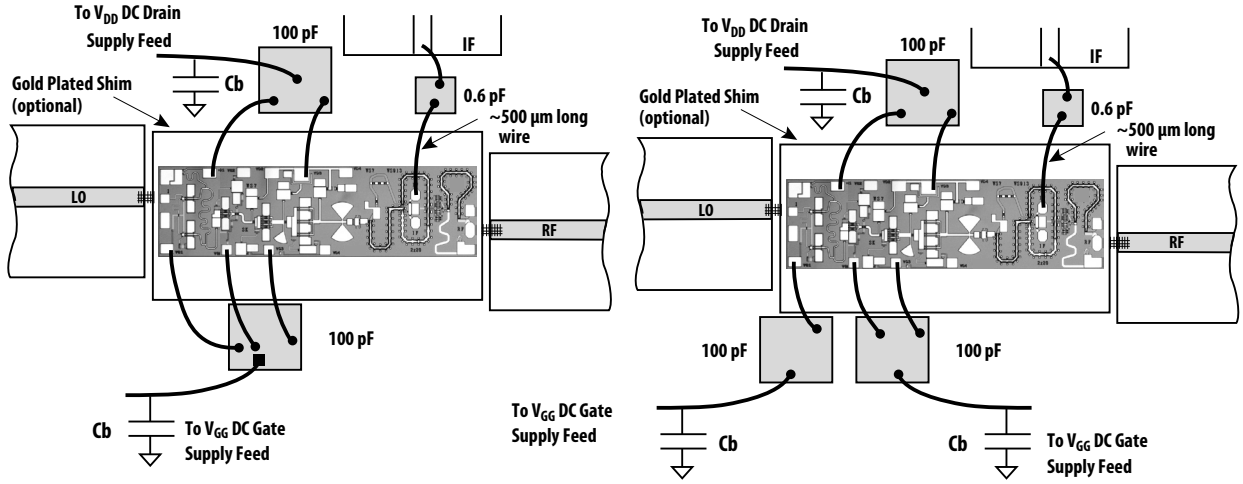


Figure 15. AMMC-3040 Bond pad locations, dimensions in microns



(a) Fundamental LO. Single drain and single gate supply assembly for using the LO amplifier in fundamental frequency mixer applications.

(b) Sub-harmonic LO. Separate first-stage gate bias supply to use the LO amplifier as a multiplier for application as a sub-harmonic mixer.

Figure 16. AMMC-3040 assembly diagram

(**Note:** To assure stable operation bias supply feeds should be bypassed to ground with a capacitor, Cb ≥ 100 pF typical.)

Biasing for Fundamental Mixing

The recommended DC bias condition for the AMMC-3040 LO amplifier when used as a fundamental frequency mixer is with all four drains connected to a single 3.5 to 4.5 V supply and all four gates connected to an adjustable negative supply voltage as shown in Figure 16(a). The gate voltage is adjusted for a total drain supply current of typically 150 to 250 mA.

The second, third, and fourth stage DC drain bias lines are connected internally and therefore require only a single bond wire. A separate bond wire is needed for the first stage DC drain bias, V_{d1}.

The third and fourth stage DC gate bias lines are connected internally. A total of three DC gate bond wires are required: one for V_{g1}, one for V_{g2}, and one for the V_{g3}/V_{g4} connection. The internal matching circuitry at the RF input creates a 50-ohm DC and RF path to ground. Any DC voltage applied to the RF input must be maintained below 1 volt, otherwise, a blocking capacitor should be used. The RF output is AC coupled.

No ground bond wires are needed since the ground connection is made by means of plated through via holes to the backside of the chip.

Biasing for Sub-Harmonic Mixing

The LO amplifier in the AMMC-3040 can also be used as a frequency doubler. Optimum conversion efficiency as a doubler is obtained with an input power level of 3 to 8 dBm.

Frequency multiplication is achieved by reducing the bias on the first stage FET to efficiently generate harmonics. The remaining three stages are then used to provide amplification.

While many bias methods could be used to generate and amplify the desired harmonics within the AMMC-3040's LO amplifier, the following information is suggested as a starting point for subharmonic mixing applications.

Frequency doubling is accomplished by biasing the first stage FET at pinch-off by setting $V_{g1} = V_p \approx -1.1$ volts. The remaining three stages are biased for normal amplification, e.g., V_{gg} is adjusted such that $I_{d2} + I_{d3} + I_{d4} \approx 250$ mA. The drain voltage, Vdd, for all four stages should be 3.5 to 4.5 volts. The assembly diagram shown in Figure 16(b) can be used as a guideline.

In all cases, Cb $\geq$ 100 pF to assure stability.

IF Output Port

The IF output port is located near the middle of the die, allowing this connection to be made from either side of the chip for maximum layout flexibility.

The LO and RF signals are reflectively terminating at the IF port by connecting a 20-mil (500 µm) long bond wire from the IF output pad on the MMIC to a shunt 0.6 pF chip capacitor mounted off- chip as indicated in Figure 16.

Assembly Techniques

The backside of the AMMC-3040 chip is RF ground. For microstripline applications, the chip should be attached directly to the ground plane (e.g., circuit carrier or heatsink) using electrically conductive epoxy [1,2].

For best performance, the topside of the MMIC should be brought up to the same height as the circuit surrounding it. This can be accomplished by mounting a gold plated metal shim (same length and width as the MMIC) under the chip, which is of the correct thickness to make the chip and adjacent circuit coplanar.

The amount of epoxy used for chip and or shim attachment should be just enough to provide a thin fillet around the bottom perimeter of the chip or shim. The ground plane should be free of any residue that may jeopardize electrical or mechanical attachment.

For use on coplanar circuits, the chip can be mounted directly on the topside ground plane of the circuit as long as care is taken to ensure adequate heat sinking. Multiple vias underneath the chip will significantly improve heat conduction.

The location of the RF, LO, and IF bond pads is shown in Figure 15. Note that all RF input and output ports are in a Ground-Signal-Ground configuration. The IF port is located near the middle of the die, which allows for maximum layout flexibility since the IF connection can be made from either side of the chip.

RF connections should be kept as short as reasonable to minimize performance degradation due to series inductance. A single bond wire is sufficient for all signal connections. However, double-bonding with 0.7 mil gold wire or the use of gold mesh is recommended for best performance, especially near the high end of the frequency range.

Thermosonic wedge bonding is the preferred method for wire attachment to the bond pads. Gold mesh can be attached using a 2 mil round tracking tool and a tool force of approximately 22 grams with an ultrasonic power of roughly 55 dB for a duration of 76 ± 8 mS. A guided wedge at an ultrasonic power level of 64 dB can be used for the 0.7 mil wire. The recommended wire bond stage temperature is 150 ± 2°C.

Caution should be taken to not exceed the Absolute Maximum Ratings for assembly temperature and time.

The chip is 100 µm thick and should be handled with care. This MMIC has exposed air bridges on the top surface and should be handled by the edges or with a custom collet (do not pick up die with vacuum on die center.)

This MMIC is also static sensitive and ESD handling precautions should be taken.

Notes:

1. Ablebond 84-1 LM1 silver epoxy is recommended.
2. Eutectic attach is not recommended and may jeopardize reliability of the device.

Ordering Information:

AMMC-3040-W10 = 10 devices per tray
AMMC-3040-W50 = 50 devices per tray

For product information and a complete list of distributors, please go to our website: **www.avagotech.com**

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