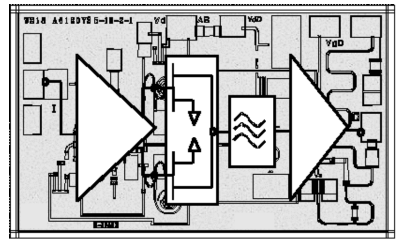
AMMC-6120

8-20 GHz Output x2 Active Frequency Multiplier

Data Sheet



Chip Size: 1600 x 1000 µm (64 x 40 mils)
Chip Size Tolerance: ± 10 µm (± 0.4 mils)
Chip Thickness: 100 ± 10 µm (4 ± 0.4 mils)
Pad Dimensions: 120 x 80 µm (5x3 ± 0.4 mils)

Description

Avago Technologies' AMMC-6120 is an easy-to-use x2 active frequency multiplier MMIC designed for commercial communication systems. Though capable of doubling to 24 GHz with reduced fundamental suppression, the MMIC is designed to take a 4 to 10 GHz input and double it to 8 to 20 GHz. It has integrated output amplifier, matching harmonic suppression, and bias networks. The input/output are matched to 50 Ω and fully DC blocked. The MMIC is fabricated using PHEMT technology. The backside of this die is both RF and DC ground. This helps simplify the assembly process and reduces assembly related performance variations and costs. For improved reliability and moisture protection, the die is passivated at the active areas. This MMIC is a cost effective alternative to bulky hybrid FET and diode doublers that require high input drive power, have high C.L. and poor fundamental suppression.

Features

- Input frequency range: 4-10 GHz
- Broad input power range: -11 to +5 dBm
- Output power: +14 dBm (Pin = +3 dBm)
- Fundamental Suppression of 25 dBc
- 50 Ω input and output match
- Supply bias of -1.4 V, 5 V and 85 mA

Applications

- Microwave radio systems
- Satellite VSAT, DBS Up/Down Link
- LMDS & Pt-Pt mmW Long Haul
- Broadband Wireless Access (including 802.16 and 802.20 WiMax)
- WLL and MMDS loops

AMMC-6120 Absolute Maximum Ratings[1]

Symbol	Parameters/Conditions	Units	Min.	Max.
V_d	Positive Drain Voltage	V		7
V_g	Gate Supply Voltage	V	-3.0	0.5
I_d	Drain Current	mA		120
P_{in}	CW Input Power	dBm		15
T_{ch}	Operating Channel Temp.	°C		+150
T_{stg}	Storage Case Temp.	°C	-65	+150
T_{max}	Maximum Assembly Temp. (60 sec. max.)	°C		+300

Note:
1. Operation in excess of any one of these conditions may result in permanent damage to this device.

Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model (Class A)
ESD Human Body Model (Class 0)
Refer to Avago Application Note A004R: Electrostatic Discharge Damage and Control.

AMMC-6120 DC Specifications/Physical Properties[1]

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
I_{dq}	Drain Supply Current	mA	80	85	105
V_g	Gate Supply Operating Voltage	V	-1.5	-1.4	-1.0
θ_{ch-b}	Thermal Resistance[2] (Backside Temperature, T_b = 25°C)	°C/W		25	

Notes:
1. Ambient operational temperature T_A = 25°C unless otherwise noted.
2. Channel-to-backside Thermal Resistance (θ_{ch-b}) = 26°C/W at $T_{channel}$ (T_c) = 34°C as measured using infrared microscopy. Thermal Resistance at backside temperature (T_b) = 25°C calculated from measured data.

AMMC-6120 RF Specifications [3,4,5]

T_A = 25°C, V_{dd} = 5 V, V_g=-1.4V, $I_{d(Q)}$ = 85 mA, Z_o = 50 Ω

Symbol	Parameters and Test Conditions	Units	Minimum	Typical	Maximum	Sigma
Fin	Input Frequency	GHz		4 to 10		
Fout	Output Frequency	GHz		8 to 20		
Po	Output Power[4]	dBm	10.5	14		0.6
Fo	Fundamental Isolation (referenced to Po)	dBc	18	25		1.8
3Fo	3rd Harmonic Isolation (referenced to Po)	dBc		25		2.5
P_{-1dB}	Input Power at 1dB Gain Compression	dBm		+1		
RLin	Input Return Loss[6]	dB		-15		
RLout	Output Return Loss[6]	dB		-9		
SSB	Single Sideband Phase Noise (100 KHz offset)	DBc/Hz		-135		

Notes:
3. Small/Large -signal data measured in wafer form T_A = 25°C.
4. 100% on-wafer RF test is done at Pin = +3 dBm, output frequency = 10, 16, and 20 GHz.
5. Specifications are derived from measurements in a 50-Ω test environment. Aspects of the multiplier performance may be improved over a more narrow bandwidth by application of additional matching.

AMMC-6120 Typical Performances

(T_A = 25°C, V_{dd} = 5 V, I_{dq} = 85 mA, V_g = -1.4 V, Z_{in} = Z_{out} = 50 Ω unless otherwise stated)

Note: These measurements are in 50 Ω test environment. Aspects of the amplifier performance may be improved over a narrower bandwidth by application of additional conjugate, linearity or low noise (Γopt) matching.

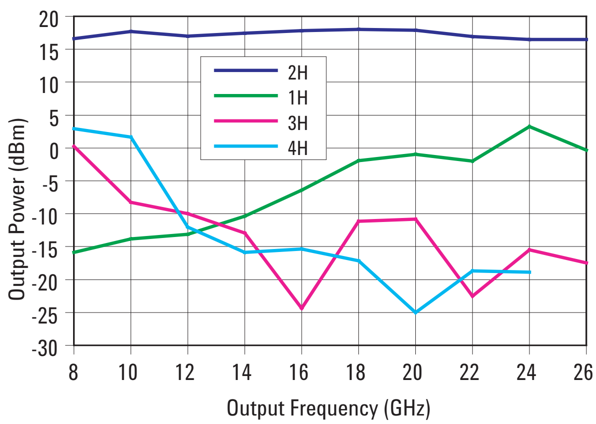


Figure 1. Output Power vs. Output Freq. @ Pin=+3dBm

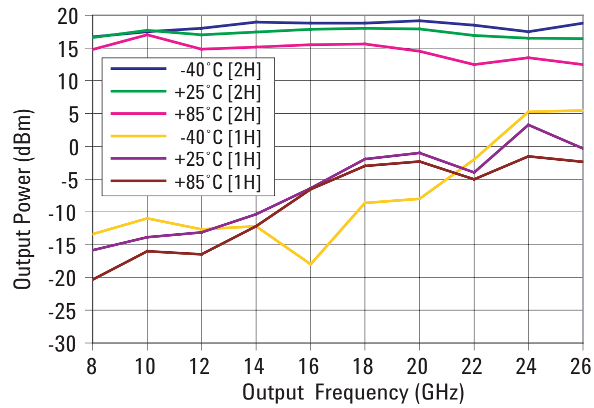


Figure 2. Output Power vs. Output Freq. over temp @ Pin=+3dBm

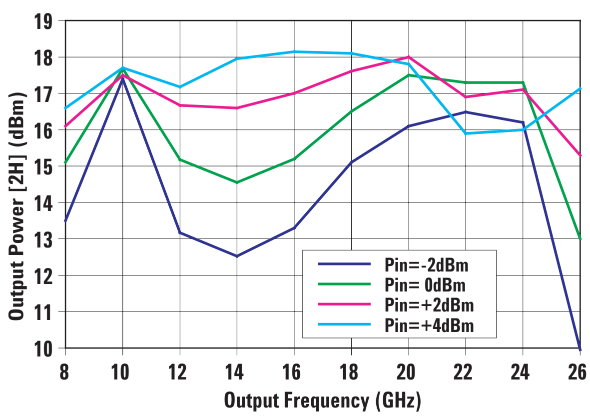


Figure 3. Output Power [2H] vs. Output Freq. at variable Pin

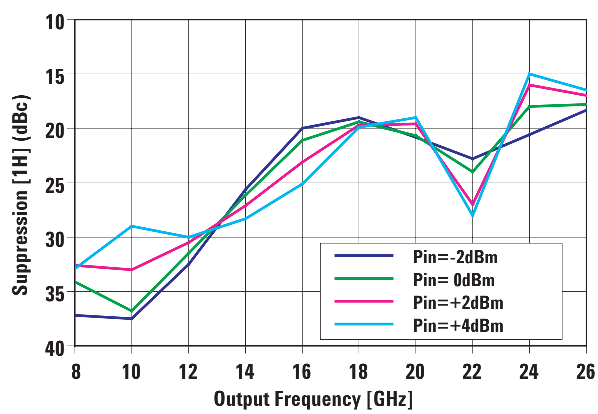


Figure 4. Fundamental Suppression at variable Pin

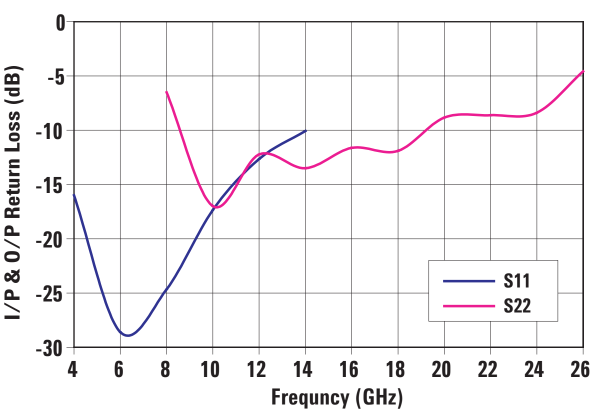


Figure 5. Input and Output Return Loss

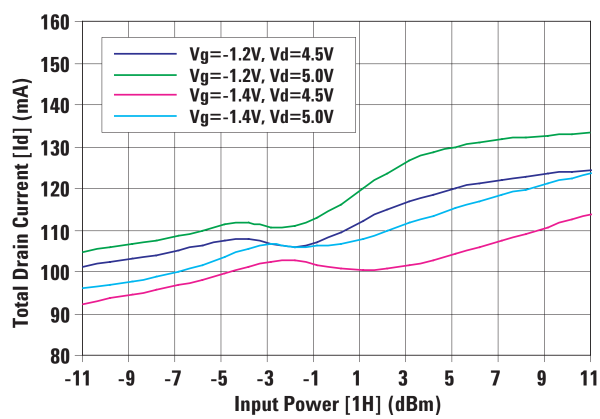


Figure 6. Variation of total drain current with input power

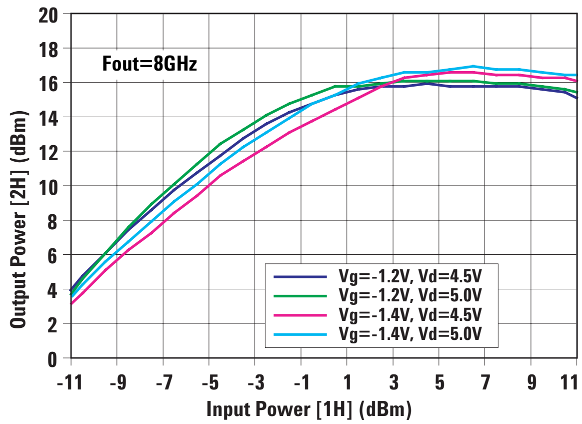


Figure 7. 2H Output Power Vs Input Power @ Fout=8GHz

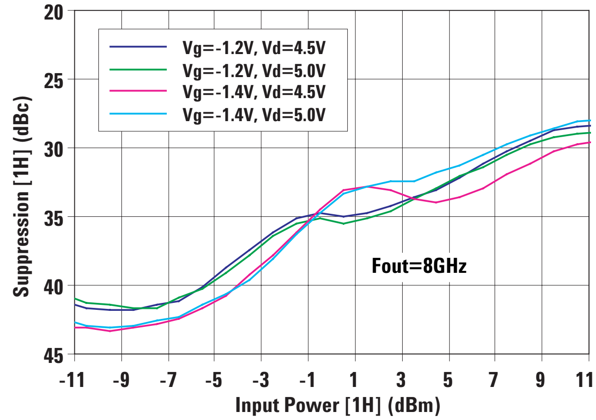


Figure 8. Fundamental Supp. Vs Input Power @ Fout=8GHz

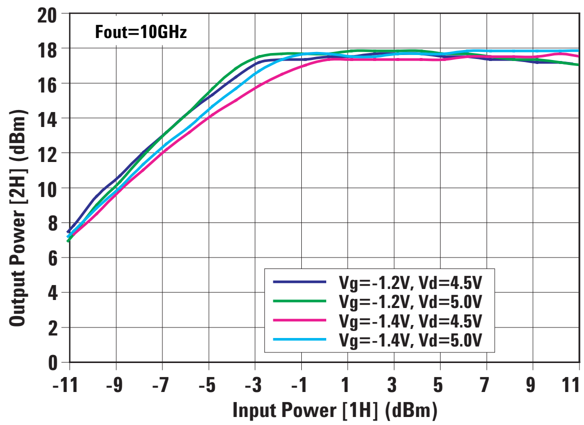


Figure 9. 2H Output Power Vs Input Power @ Fout=10GHz

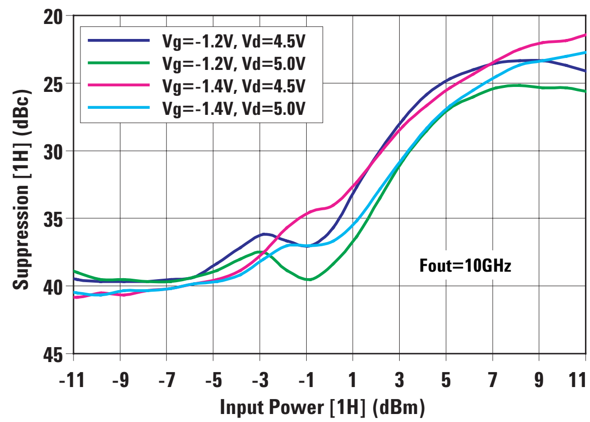


Figure 10. Fundamental Supp. Vs Input Power @ Fout=10GHz

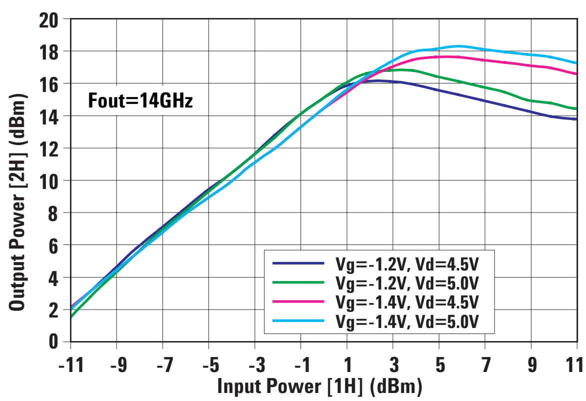


Figure 11. 2H Output Power Vs Input Power @ Fout=14GHz

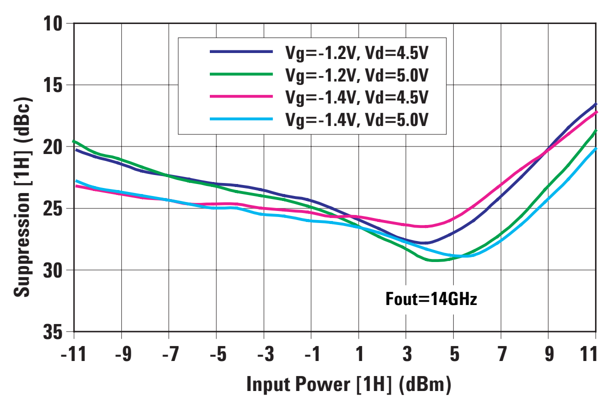


Figure 12. Fundamental Supp. Vs Input Power @ Fout=14GHz

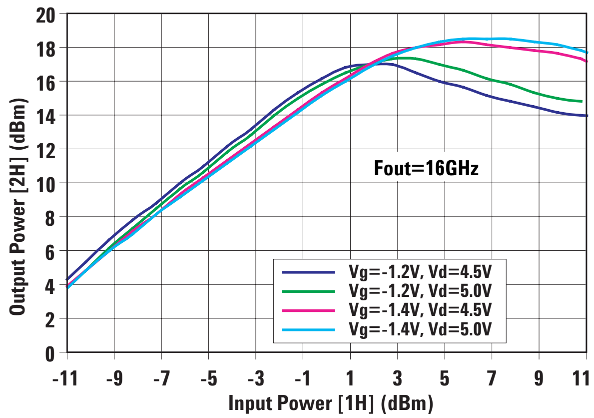


Figure 13. 2H Output Power Vs Input Power @ Fout=16GHz

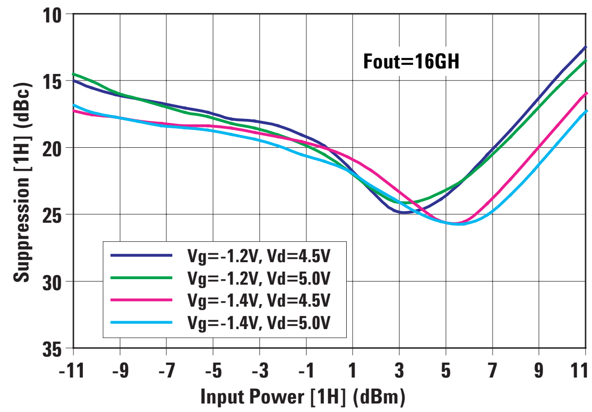


Figure 14. Fundamental Supp. Vs Input Power @ Fout=16GHz

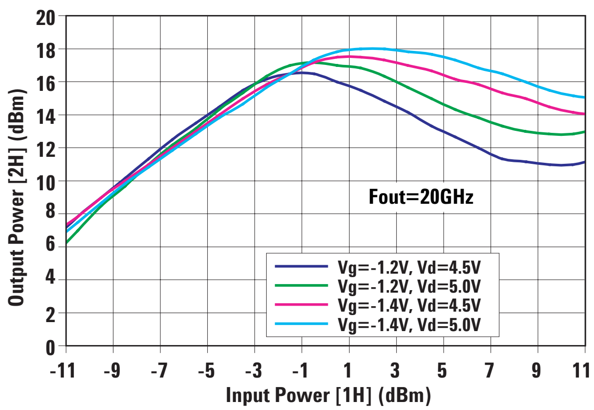


Figure 15. 2H Output Power Vs Input Power @ Fout=20GHz

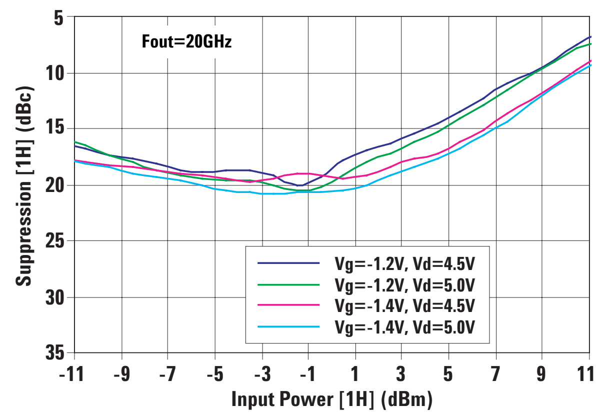


Figure 16. Fundamental Supp. Vs Input Power @ Fout=20GHz

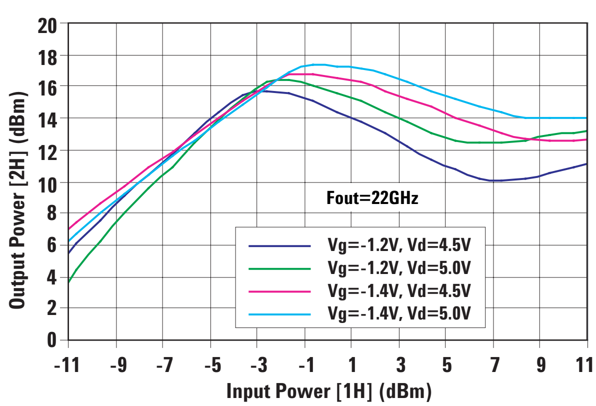


Figure 17. 2H Output Power Vs Input Power @ Fout=22GHz

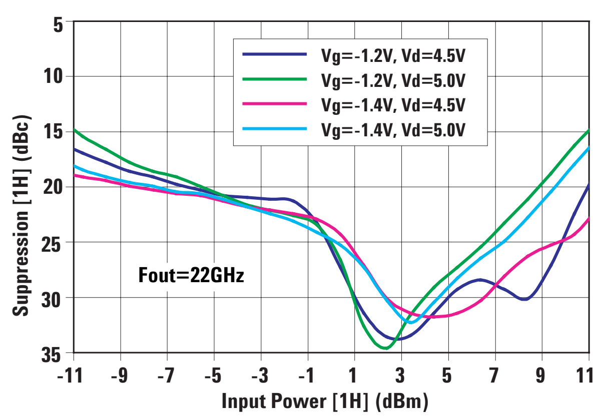


Figure 18. Fundamental Supp. Vs Input Power @ Fout=22GHz

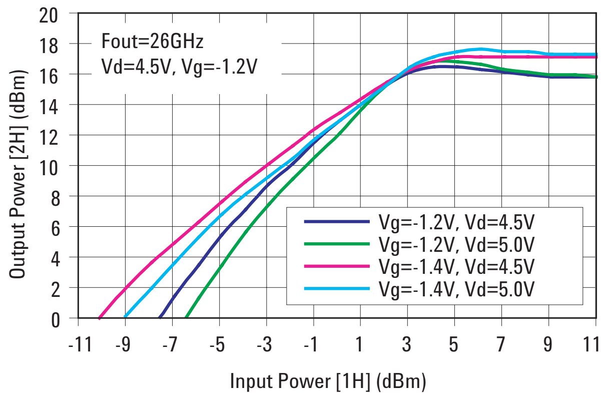


Figure. 19 2H Output Power Vs Input Power @ Fout=26GHz

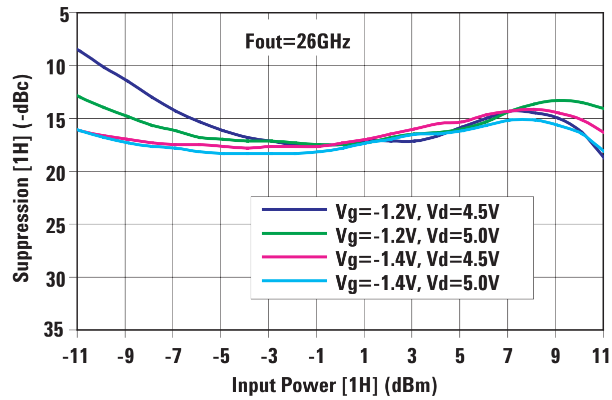


Figure. 20 Fundamental Supp. Vs Input Power @ Fout=26GHz

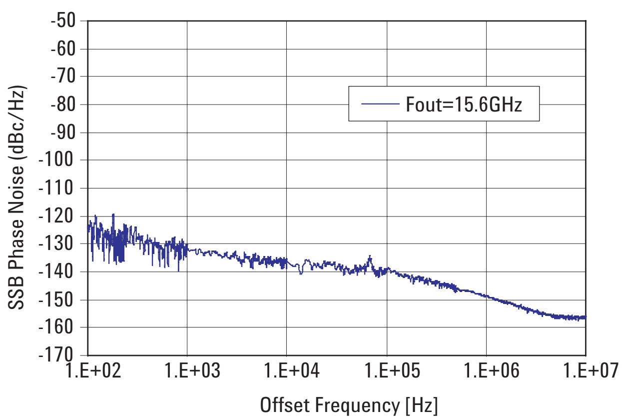


Figure.21 SSB Phase Noise of frequency doubler (Pin=+2dBm, fout=15.6GHz)

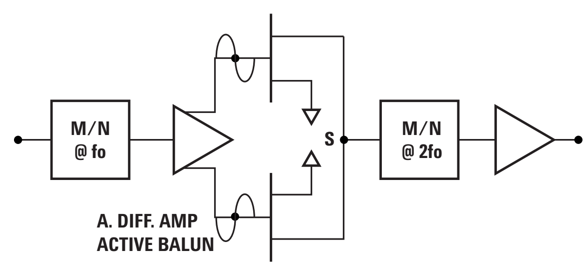


Figure 22.

Biasing and Operation

The frequency doubler MMIC consists of a differential amplifier circuit that acts as an active balun. The outputs of this balun feed the gates of balanced FETs and the drains are connected to form the single-ended output. This results in the fundamental frequency and odd harmonics canceling and the even harmonic drain currents (in phase) adding in superposition. Node 'S' acts as a virtual ground. An input matching network (M/N) is designed to provide good match at fundamental frequencies and produces high impedance mismatch at higher harmonics.

AMMC-6120 is biased with a single positive drain supply and single negative gate supply using separate bypass capacitors. It is normally biased with the drain supply connected to both the VdAB and the Vdd bond pads and the gate supply connected to the VgD bond pad. It is important to bypass both VdAB and Vdd with 100 pF capacitors placed as close to the die as possible. Typical bias connections are shown in Figure 22. For most of the application it is recommended to use a Vg = –1.2 V and Vd = 4.5 V.

The AMMC-6120 performance changes very slightly with Drain (Vd) and Gate bias (Vg) as shown in Figure 8 and 9. Minor improve-ments in performance are possible for output power or fundamental suppression by optimizing the Vg from –1.0 V to –1.4 V and/or Vd from 4.0 to 5.0 V.

The RF input and output port are AC coupled thus no DC voltage is present at either ports. However, the RF output port has a internal output-matching circuit that presents a DC short. Proper care should be taken while biasing sequential circuit to AMMC-6120 as it might cause DC short (use a DC block if sub sequential circuit is not AC coupled). No ground wires are needed since ground connections are made with plated through-holes to the backside of the device.

Refer the Absolute Maximum Ratings table for allowed DC and thermal conditions.

Assembly Techniques

The backside of the MMIC chip is RF ground. For microstrip applications the chip should be attached directly to the ground plane (e.g. circuit carrier or heatsink) using electrically conductive epoxy [1,2].

For best performance, the topside of the MMIC should be brought up to the same height as the circuit surrounding it. This can be accomplished by mounting a gold plate metal shim (same length and width as the MMIC) under the chip which is of correct thickness to make the chip and adjacent circuit the same height. The amount of epoxy used for the chip and/or shim attachment should be just enough to provide a thin fillet around the bottom perimeter of the chip or shim. The ground plan should be free of any residue that may jeopardize electrical or mechanical attachment.

The location of the RF bond pads is shown in Figure 24. Note that all the RF input and output ports are in a Ground-Signal-Ground configuration.

RF connections should be kept as short as reasonable to minimize performance degradation due to undesirable series inductance. A single bond wire is normally sufficient for signal connections, however double bonding with 0.7 mil gold wire or use of gold mesh is recommended for best performance, especially near the high end of the frequency band.

Thermosonic wedge bonding is the preferred method for wire attachment to the bond pads. Gold mesh can be attached using a 2 mil round tracking tool and a tool force of approximately 22 grams and a ultrasonic power of roughly 55 dB for a duration of 76 ± 8 mS. The guided wedge at an ultrasonic power level of 64 dB can be used for 0.7 mil wire. The recommended wire bond stage temperature is 150 ± 2°C.

Caution should be taken to not exceed the Absolute Maximum Rating for assembly temperature and time.

The chip is 100 µm thick and should be handled with care. This MMIC has exposed air bridges on the top surface and should be handled by the edges or with a custom collet (do not pick up the die with a vacuum on die center).

This MMIC is also static sensitive and ESD precautions should be taken.

Notes:
1. Ablebond 84-1 LM1 silver epoxy is recommended.
2. Eutectic attach is not recommended and may jeopardize reliability of the device.

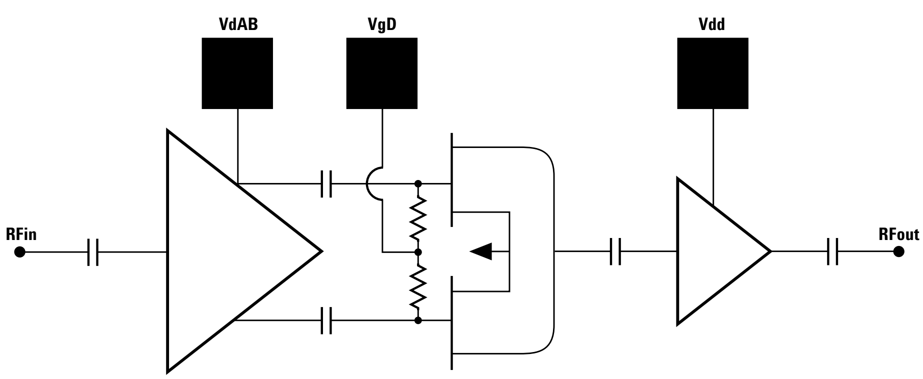


Figure 23. AMMC-6120 simplified schematic.

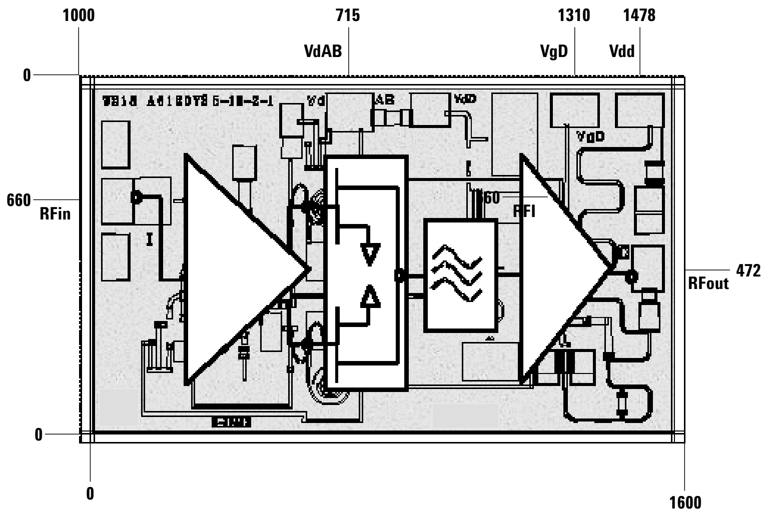


Figure 24. AMMC-6120 bonding pad locations.

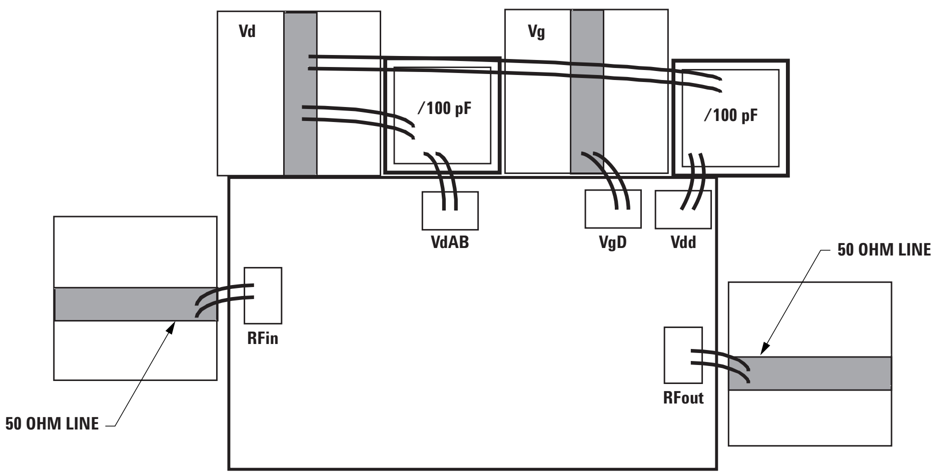


Figure 25. AMMC-6120 assembly diagram.

Ordering Information:

AMMC-6120-W10 = 10 devices per tray

AMMC-6120-W50 = 50 devices per tray

For product information and a complete list of distributors, please go to our website: **www.avagotech.com**

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