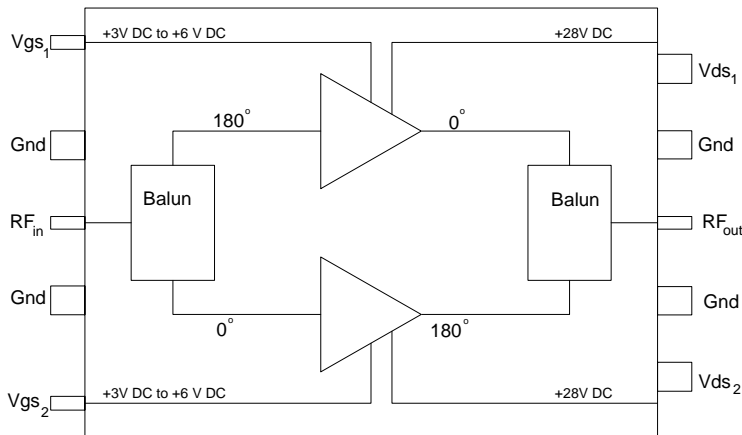




Product Description

Sirenza Microdevices' **SDM-08120** 130W power module is a robust impedance matched, single-stage, push-pull Class AB amplifier module suitable for use as a power amplifier driver or output stage. The power transistors are fabricated using Sirenza's latest, high performance LD MOS process. It is a drop-in, no-tune solution for high power applications requiring high efficiency, excellent linearity, and unit-to-unit repeatability. It is internally matched to 50 ohms.

Functional Block Diagram

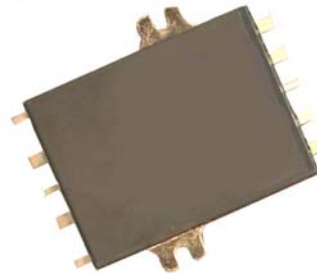


Case Flange = Ground

SDM-08120 SDM-08120Y



869-894 MHz Class AB 130W Power Amplifier Module



Product Features

- Available in RoHS compliant packaging
- 50 Ω RF impedance
- 130W Output P_{1dB}
- Single Supply Operation : Nominally 28V
- High Gain: 16 dB at 880 MHz
- High Efficiency: 42% at 880 MHz

Applications

- Base Station PA driver
- Repeater
- CDMA / GSM / EDGE

Key Specifications

Symbol	Parameter	Units	Min.	Typ.	Max.
Frequency	Frequency of Operation	MHz	869	-	894
P_{1dB}	Output Power at 1dB Compression, 881 MHz	W	120	130	-
Gain	Gain at 12W CDMA Output (Single Carrier IS-95), 881MHz	dB	14	16	-
Gain Flatness	Peak-to-Peak Gain Variation, 869 - 894MHz, 12 Watt	dB	-	0.5	1.0
Efficiency	Drain Efficiency at 120 Watts Output Power, CW 880 MHz	%		42	
Efficiency	Drain Efficiency at 24 Watts Output Power, 869 - 894MHz	%		20	
IRL	Input Return Loss 24W CW Output Power, 869 - 894MHz	dB	-	-15	-12
CDMA ACPR Integrated Bandwidth	IS-95, 9 Ch Fwd, Offset=750kHz, 881MHz, Pout=12W avg	dBc	-	-55	-50
	IS-95, 9 Ch Fwd, Offset=1.98MHz, 881MHz, Pout=12W avg	dBc		-63	-60
	IS-95, 9 Ch Fwd, Offset=750kHz, 881MHz, Pout=24W avg	dBc	-	-46	-
IMD	3rd Order IMD Product, 120W PEP, 880MHz and 881MHz	dBc	-	-34	-30
Delay	Signal Delay from Pin 3 to Pin 8	nS	-	4.0	-
Phase Linearity	Deviation from Linear Phase (Peak-to-Peak)	Deg	-	0.7	-
R_{TH}	Thermal Resistance (Junction-to-Case)	$^{\circ}C/W$		0.7	

Test Conditions $Z_{in} = Z_{out} = 50\Omega$, $V_{DD} = 28.0V$, $I_{DQ1} = I_{DQ2} = 600mA$ $T_{Flange} = 25^{\circ}C$

Quality Specifications

Parameter	Description	Unit	Typical
ESD Rating	Human Body Model	Volts	2000
MTTF	200 $^{\circ}C$ Channel	Hours	1.2 X 10 ⁶

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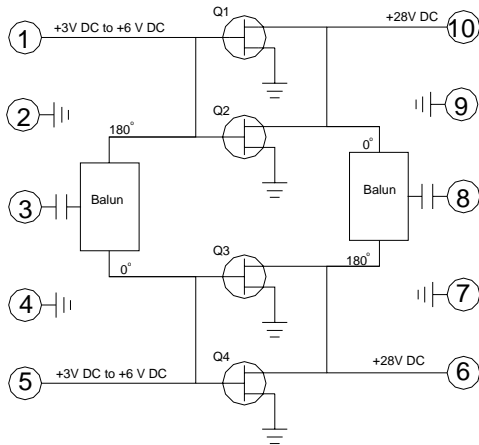
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<http://www.sirenza.com>
EDS-103346 Rev F

Pin Description

Pin #	Function	Description
1	V _{GS1}	LDMOS FET Q1 and Q2 gate bias. V _{GSTH} 3.0 to 5.0 VDC. See Notes 2, 3 and 4
2,4,7,9	Ground	Module Topside ground.
3	RF Input	Internally DC blocked
5	V _{GS2}	LDMOS FET Q3 and Q4 gate bias. V _{GSTH} 3.0 to 5.0 VDC. See Notes 2, 3 and 4
6	V _{D2}	LDMOS FET Q3 and Q4 drain bias. See Note 1.
8	RF Output	Internally DC blocked
10	V _{D1}	LDMOS FET Q1 and Q2 drain bias. See Note 1.
Flange	Ground	Baseplate provides electrical ground and a thermal transfer path for the device. Proper mounting assures optimal performance and the highest reliability. See Sirenza applications note AN-054 Detailed Installation Instructions for Power Modules.

Simplified Device Schematic



Note 1:

Internal RF decoupling is included on all bias leads. No additional bypass elements are required, however some applications may require energy storage on the V_D leads to accommodate modulated signals.

Note 2:

Gate voltage must be applied to V_{GS} leads simultaneously with or after application of drain voltage to prevent potentially destructive oscillations. Bias voltages should never be applied to a module unless it is properly terminated on both input and output.

Note 3:

The required V_{GS} corresponding to a specific I_{DQ} will vary from module to module and may differ between V_{GS1} and V_{GS2} on the same module by as much as ±0.10 volts due to the normal die-to-die variation in threshold voltage. LDMOS transistors.

Note 4:

The threshold voltage (V_{GSTH}) of LDMOS transistors varies with device temperature. External temperature compensation may be required. See Sirenza application notes AN-067 LDMOS Bias Temperature Compensation.

Note 5:

This module was designed to have its leads hand soldered to an adjacent PCB. The maximum soldering iron tip temperature should not exceed 700° F, and the soldering iron tip should not be in direct contact with the lead for longer than 10 seconds. Refer to app note AN054 (www.sirenza.com) for further installation instructions.

Absolute Maximum Ratings

Parameters	Value	Unit
Drain Voltage (V _{DD})	35	V
RF Input Power	+43	dBm
Load Impedance for Continuous Operation Without Damage	5:1	VSWR
Control (Gate) Voltage, VDD = 0 VDC	15	V
Output Device Channel Temperature	+200	°C
Operating Temperature Range	-20 to +90	°C
Storage Temperature Range	-40 to +100	°C

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation see typical setup values specified in the table on page one.

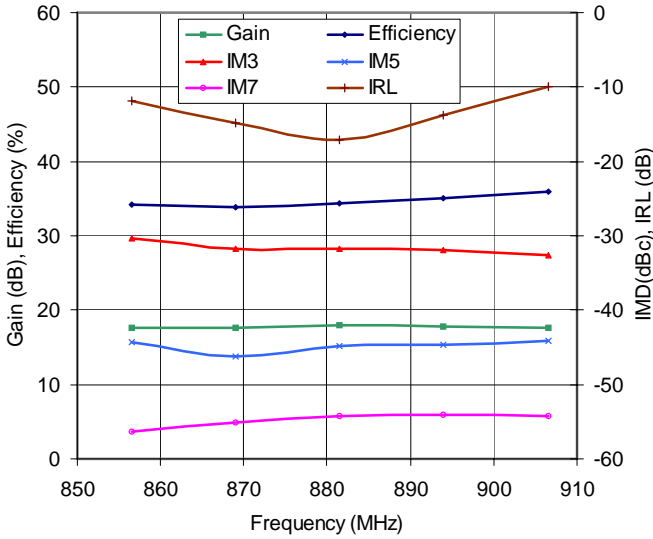


Caution: ESD Sensitive

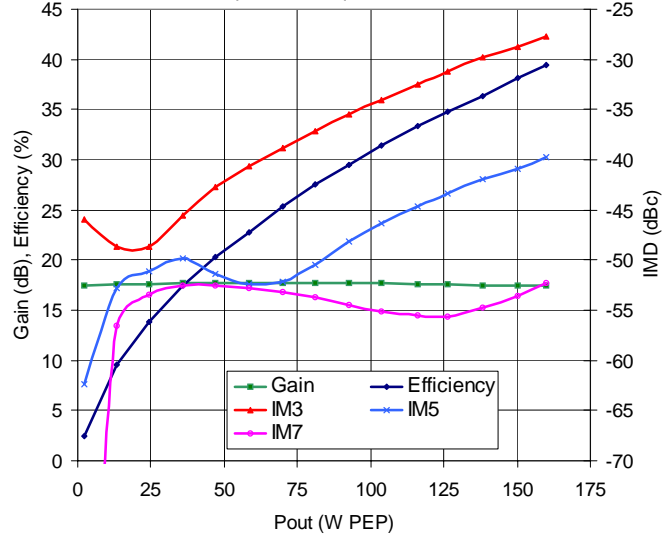
Appropriate precaution in handling, packaging and testing devices must be observed.

Typical Performance Curves

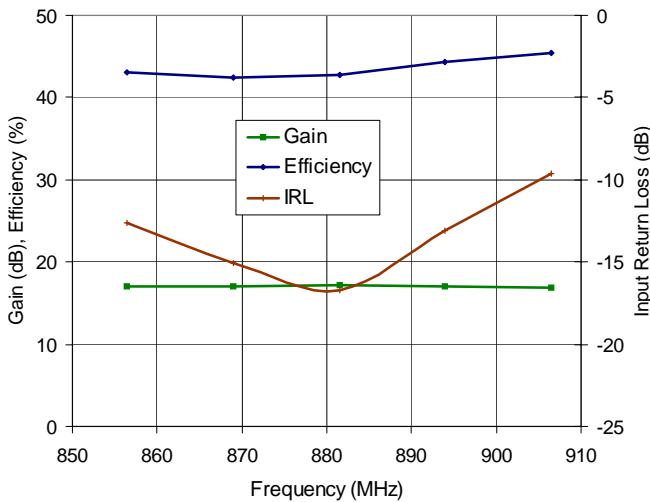
2 Tone Gain, Efficiency, Linearity and IRL vs Frequency
 Vdd=28V, Idq=1.2A, Pout=120W PEP, Delta F=1 MHz



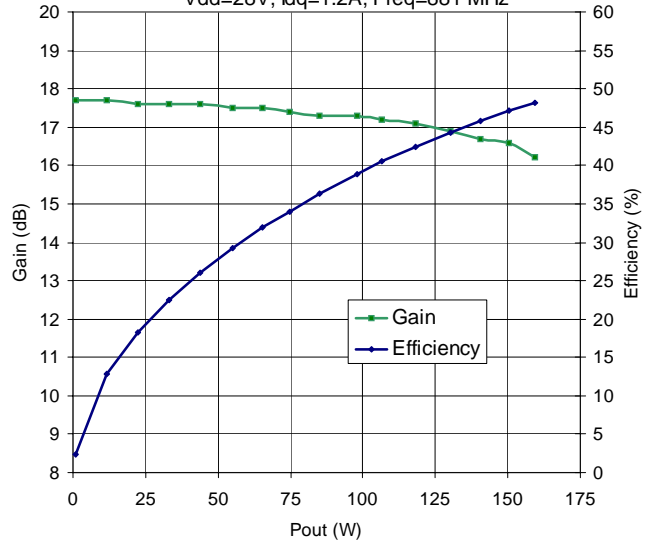
2 Tone Gain, Efficiency, Linearity vs Pout
 Vdd=28V, Idq=1.2A, Freq=881 MHz, Delta F=1 MHz



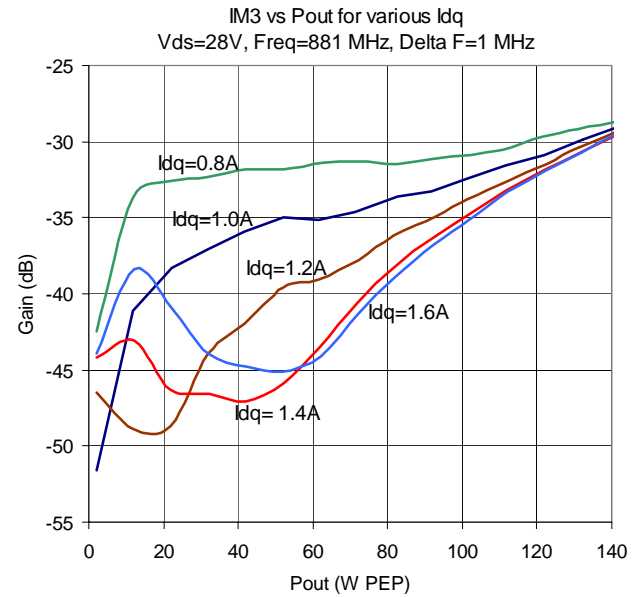
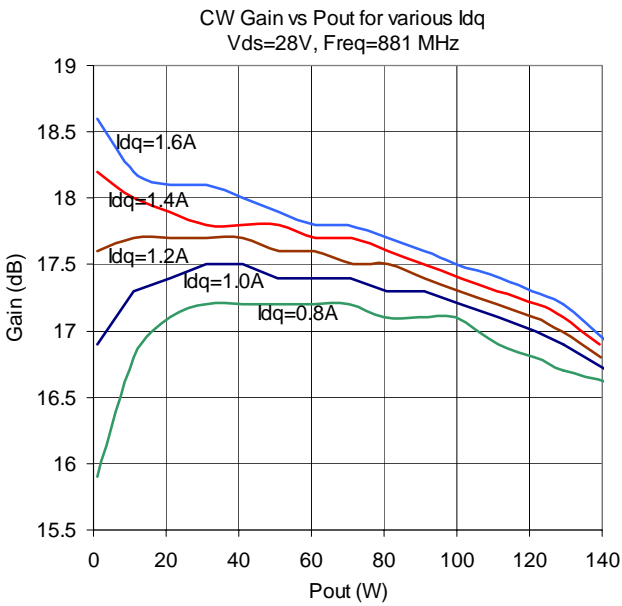
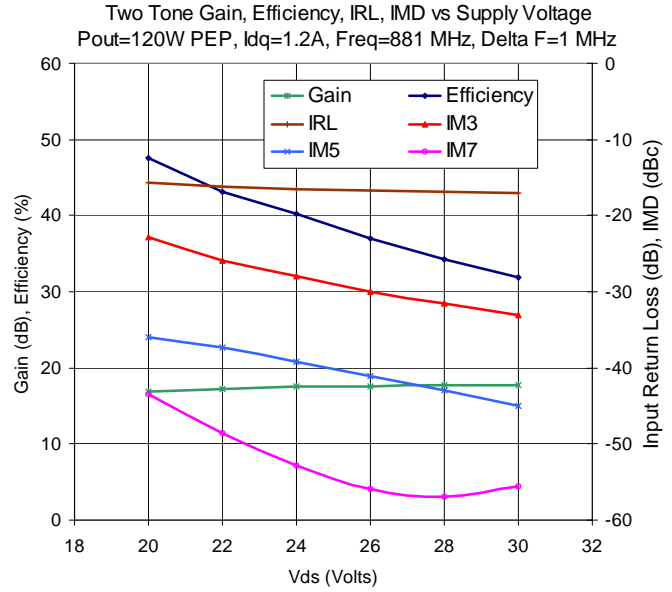
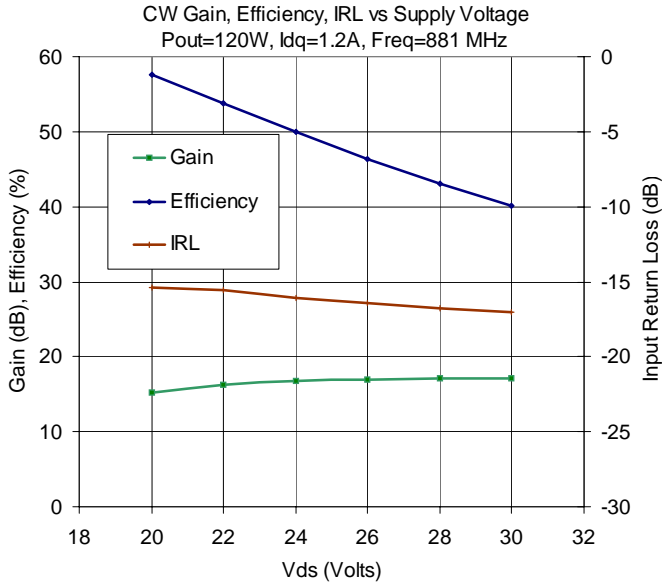
CW Gain, Efficiency, IRL vs Frequency Vdd=28V, Idq=1.2A,
 Pout=120W



CW Gain, Efficiency vs Pout
 Vdd=28V, Idq=1.2A, Freq=881 MHz

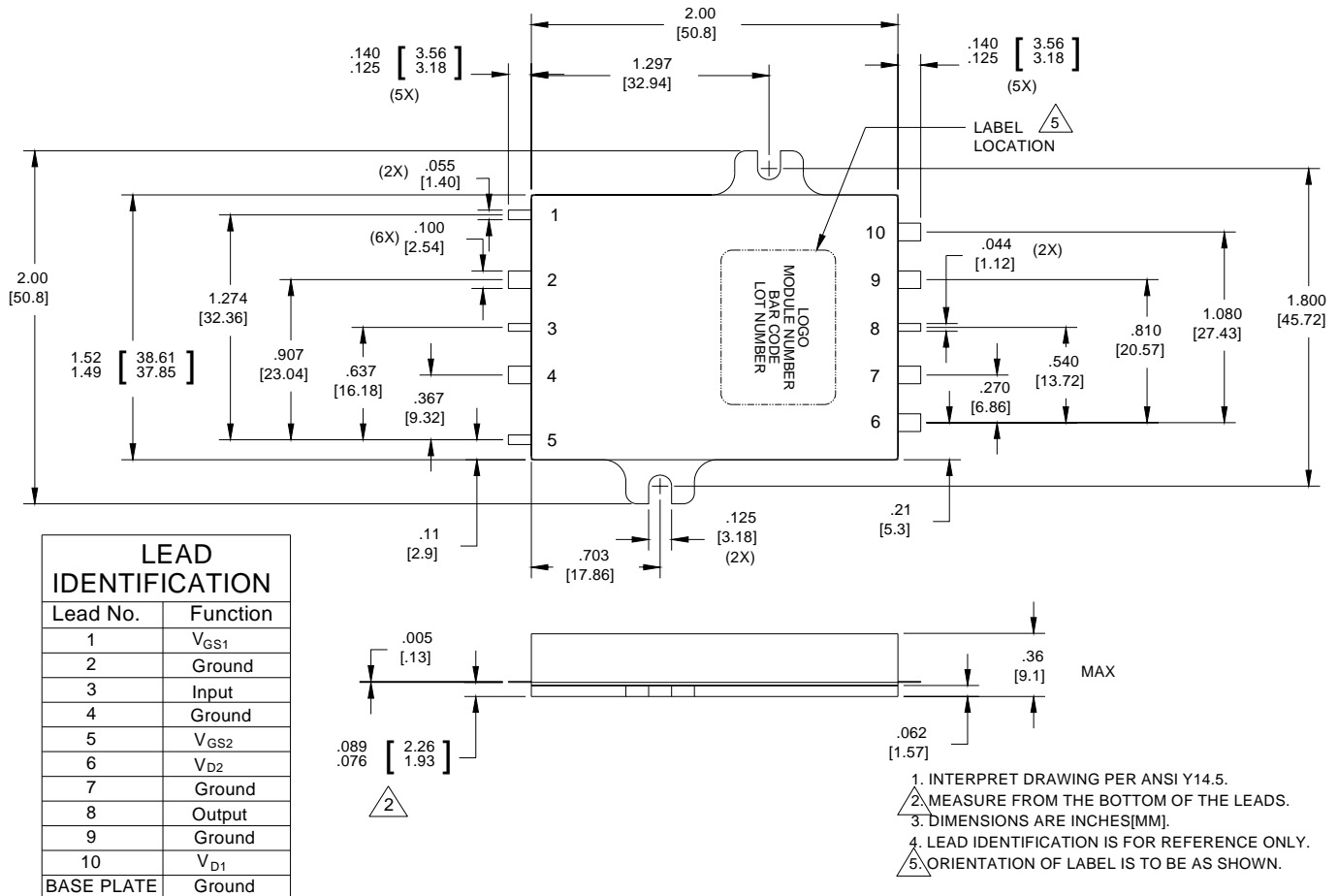


Typical Performance Curves (cont'd)



Note:
Evaluation test fixture information available on Sirenza Website, referred to as SDM-EVAL.

Package Outline Drawing



Note:

Refer to Application note AN054, "Detailed Installation Instructions for Power Modules" for detailed mounting information.