Freescale Semiconductor
Technical Data

Document Number: MWE6IC9100N
Rev. 3, 12/2008

RF LDMOS Wideband Integrated Power Amplifiers

The MWE6IC9100N wideband integrated circuit is designed with on-chip matching that makes it usable from 869 to 960 MHz. This multi-stage structure is rated for 26 to 32 Volt operation and covers all typical cellular base station modulations.

Final Application

- Typical GSM Performance: V_{DD} = 26 Volts, I_{DQ1} = 120 mA, I_{DQ2} = 950 mA, P_{out} = 100 Watts CW, f = 960 MHz
  Power Gain — 33.5 dB
  Power Added Efficiency — 54%

GSM EDGE Application

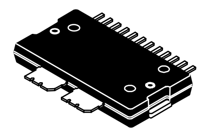
- Typical GSM EDGE Performance: V_{DD} = 28 Volts, I_{DQ1} = 230 mA, I_{DQ2} = 870 mA, P_{out} = 50 Watts Avg., Full Frequency Band (869-960 MHz)
  Power Gain — 35.5 dB
  Power Added Efficiency — 39%
  Spectral Regrowth @ 400 kHz Offset = -63 dBc
  Spectral Regrowth @ 600 kHz Offset = -81 dBc
  EVM — 2% rms
- Capable of Handling 10:1 VSWR, @ 32 Vdc, 960 MHz, 3 dB Overdrive, Designed for Enhanced Ruggedness
- Stable into a 5:1 VSWR. All Spurs Below -60 dBc @ 1 mW to 120 W CW P_{out}.

Features

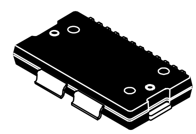
- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source S-Parameters
- On-Chip Matching (50 Ohm Input, DC Blocked)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function (1)
- Integrated ESD Protection
- 225°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.

MWE6IC9100NR1
MWE6IC9100GNR1
MWE6IC9100NBR1

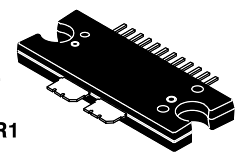
960 MHz, 100 W, 26 V
GSM/GSM EDGE
RF LDMOS WIDEBAND
INTEGRATED POWER AMPLIFIERS



CASE 1618-02
TO-270 WB-14
PLASTIC
MWE6IC9100NR1



CASE 1621-02
TO-270 WB-14 GULL
PLASTIC
MWE6IC9100GNR1



CASE 1617-02
TO-272 WB-14
PLASTIC
MWE6IC9100NBR1

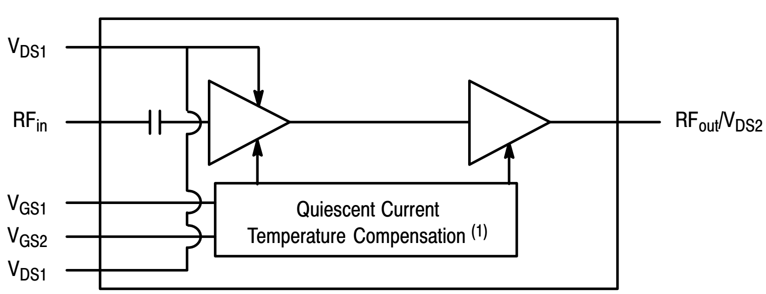
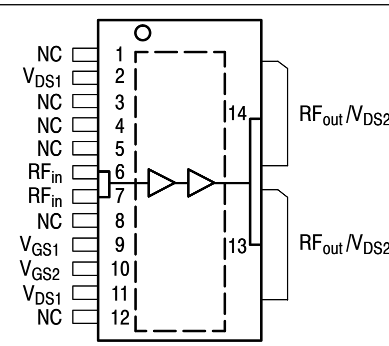


Figure 1. Functional Block Diagram



Note: Exposed backside of the package is the source terminal for the transistors.

Figure 2. Pin Connections

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1977 or AN1987.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +66	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +6	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature [1,2]	T_J	225	°C

Table 2. Thermal Characteristics

Characteristic		Symbol	Value [2,3]	Unit
Thermal Resistance, Junction to Case		$R_{\theta JC}$		°C/W
GSM Application (P_{out} = 100 W CW)	Stage 1, 26 Vdc, I_{DQ1} = 120 mA		1.82	
	Stage 2, 26 Vdc, I_{DQ2} = 950 mA		0.38	
GSM EDGE Application (P_{out} = 50 W Avg.)	Stage 1, 28 Vdc, I_{DQ1} = 230 mA		1.77	
	Stage 2, 28 Vdc, I_{DQ2} = 870 mA		0.44	

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2 (Minimum)
Machine Model (per EIA/JESD22-A115)	B (Minimum)
Charge Device Model (per JESD22-C101)	III (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted)

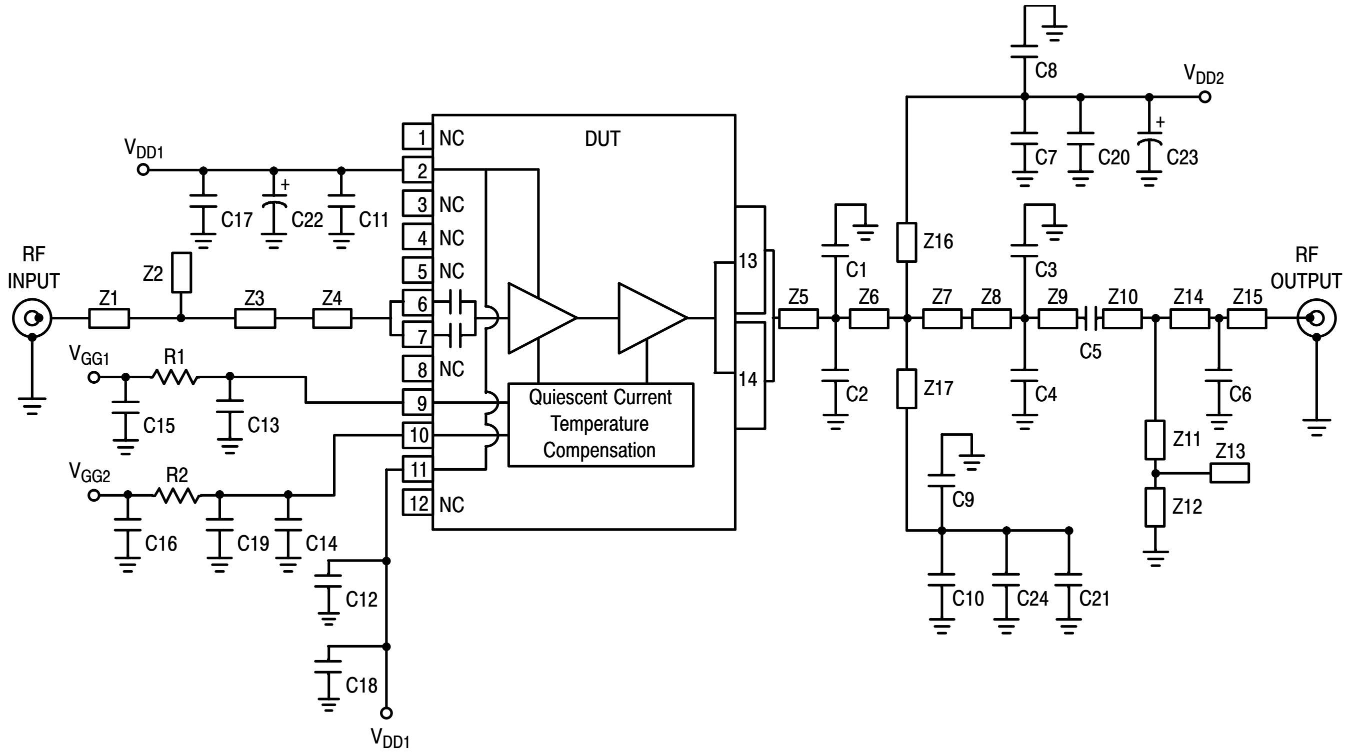
Characteristic	Symbol	Min	Typ	Max	Unit
Stage 1 — Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 66 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	10	μAdc
Stage 1 — On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 35 μAdc)	$V_{GS(th)}$	1.5	2	3.5	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 120 mAdc)	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 26 Vdc, I_D = 120 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	6	9.4	12	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

(continued)

Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Stage 2 — Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 66 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	10	μAdc
Stage 2 — On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 290 μAdc)	$V_{GS(th)}$	1.5	2	3.5	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 950 mAdc)	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 26 Vdc, I_D = 950 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	6	8.6	12	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	0.05	0.4	0.8	Vdc
Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 26 Vdc, P_{out} = 100 W CW, I_{DQ1} = 120 mA, I_{DQ2} = 950 mA, f = 960 MHz					
Power Gain	G_{ps}	31	33.5	36	dB
Input Return Loss	IRL	—	-15	-10	dB
Power Added Efficiency	PAE	52	54	—	%
P_{out} @ 1 dB Compression Point, CW	P1dB	100	112	—	W
Typical GSM EDGE Performances (In Freescale GSM EDGE Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, P_{out} = 50 W Avg., I_{DQ1} = 230 mA, I_{DQ2} = 870 mA, 869-894 MHz and 920-960 MHz EDGE Modulation					
Power Gain	G_{ps}	—	35.5	—	dB
Power Added Efficiency	PAE	—	39	—	%
Error Vector Magnitude	EVM	—	2	—	% rms
Spectral Regrowth at 400 kHz Offset	SR1	—	-63	—	dBc
Spectral Regrowth at 600 kHz Offset	SR2	—	-81	—	dBc



Z1	0.089″ x 0.083″ Microstrip	Z10	0.117″ x 0.083″ Microstrip
Z2	0.157″ x 0.315″ Microstrip	Z11	0.067″ x 0.431″ Microstrip
Z3	0.157″ x 0.397″ Microstrip	Z12	0.067″ x 0.084″ Microstrip
Z4	0.139″ x 0.060″ Microstrip	Z13	0.381″ x 0.067″ Microstrip
Z5	0.024″ x 0.386″ Microstrip	Z14	0.418″ x 0.084″ Microstrip
Z6	0.352″ x 0.902″ Microstrip	Z15	0.421″ x 0.084″ Microstrip
Z7	0.039″ x 0.607″ Microstrip	Z16, Z17	2.550″ x 0.157″ Microstrip
Z8	0.555″ x 1.102″ Microstrip	PCB	Taconic TLX8-0300, 0.030″, ε_r = 2.55
Z9	0.343″ x 0.083″ Microstrip		

Figure 3. MWE6IC9100NR1(GNR1)(NBR1) Test Circuit Schematic

Table 6. MWE6IC9100NR1(GNR1)(NBR1) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2	10 pF Chip Capacitors	ATC100B100GT500XT	ATC
C3, C4, C5	3.9 pF Chip Capacitors	ATC100B3R9BT500XT	ATC
C6	0.5 pF Chip Capacitor	ATC100B0R5BT500XT	ATC
C7, C8, C9, C10, C11, C12, C13, C14	33 pF Chip Capacitors	ATC100B330JT500XT	ATC
C15, C16, C17, C18, C19, C20, C21	6.8 μF Chip Capacitors	C4532X5R1H685MT	TDK
C22, C23	470 μF, 63 V Electrolytic Capacitors, Radial	222212018470	Vishay
C24	330 pF Chip Capacitor	ATC100B331JT200XT	ATC
R1, R2	4.7 kΩ, 1/8 W Chip Resistors	CRCW08054701FKEA	Vishay

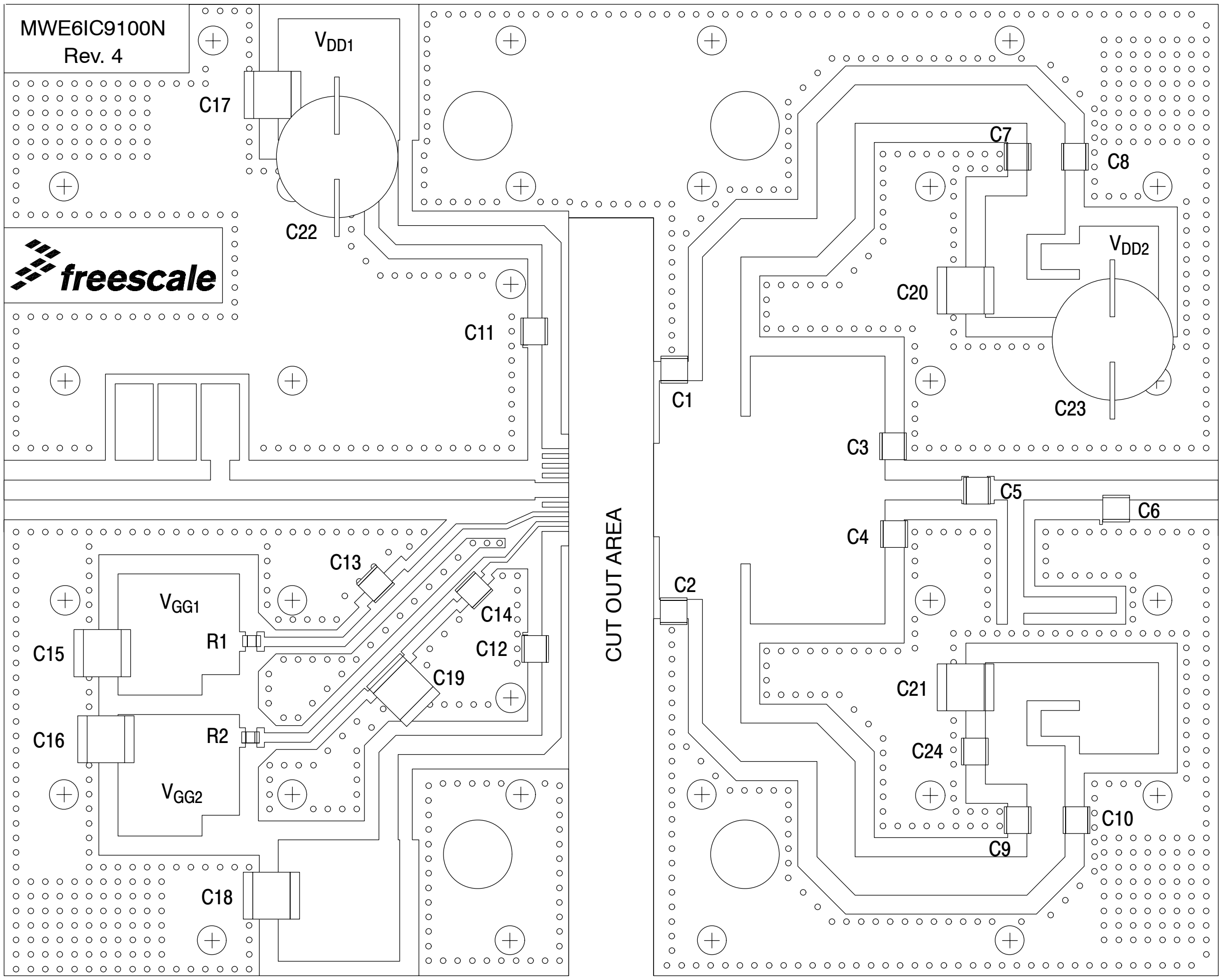


Figure 4. MWE6IC9100NR1(GNR1)(NBR1) Test Circuit Component Layout

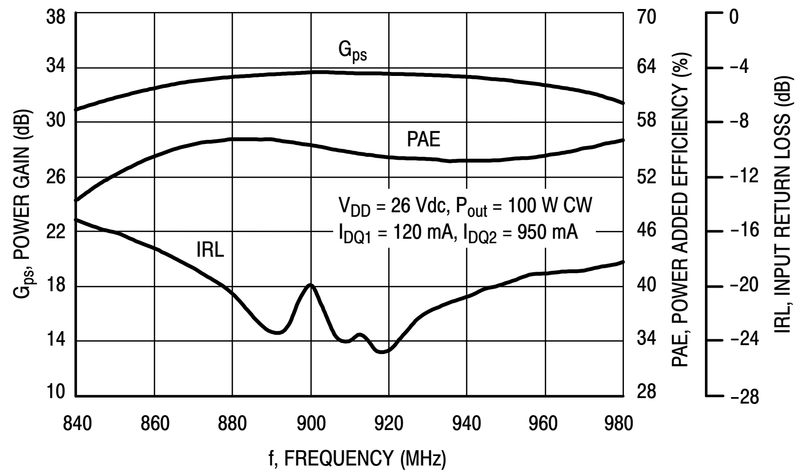


Figure 5. Power Gain, Input Return Loss and Power Added Efficiency versus Frequency @ P_{out} = 100 Watts CW

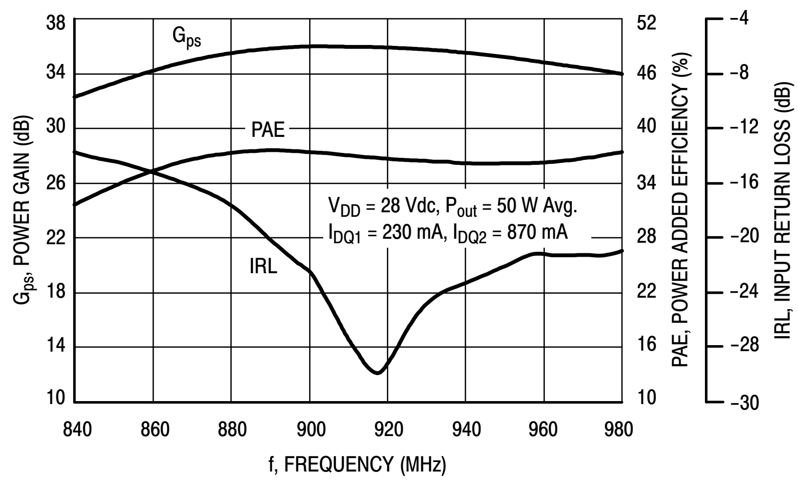


Figure 6. Power Gain, Input Return Loss and Power Added Efficiency versus Frequency @ P_{out} = 50 Watts Avg.

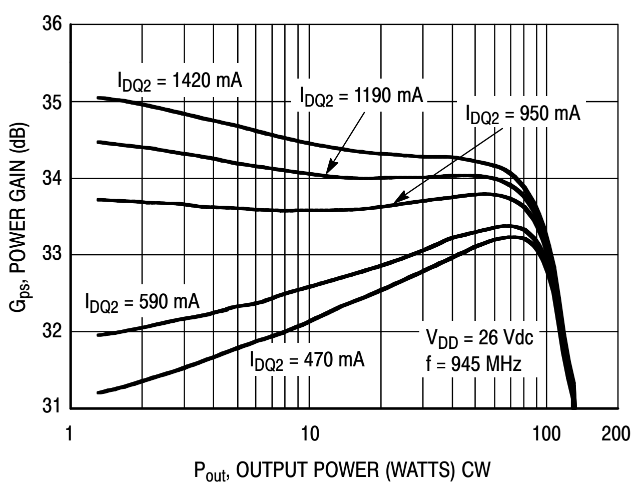


Figure 7. Power Gain versus Output Power @ I_{DQ1} = 120 mA

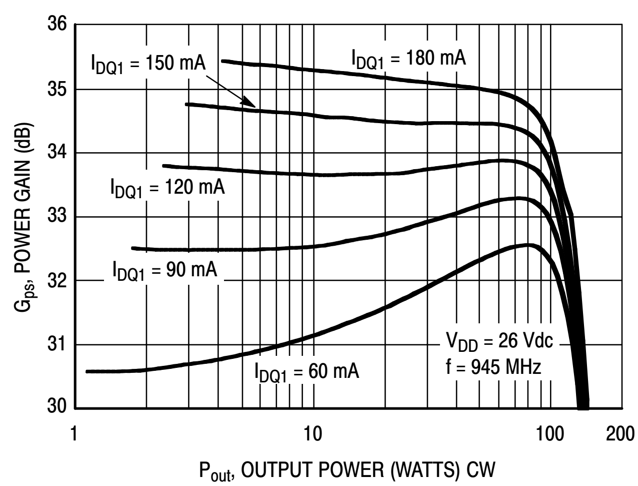


Figure 8. Power Gain versus Output Power @ I_{DQ2} = 950 mA

TYPICAL CHARACTERISTICS

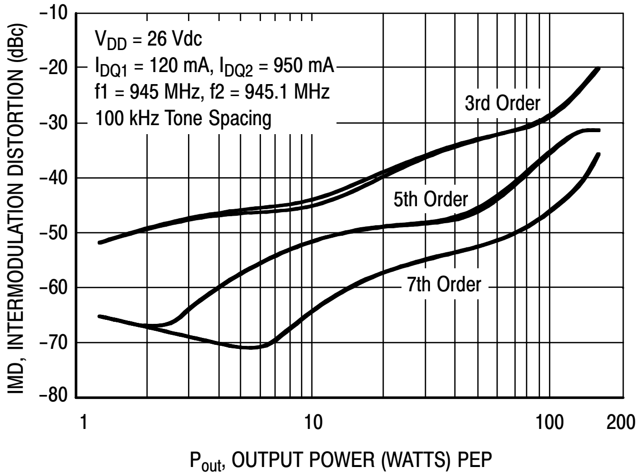


Figure 9. Intermodulation Distortion Products versus Output Power

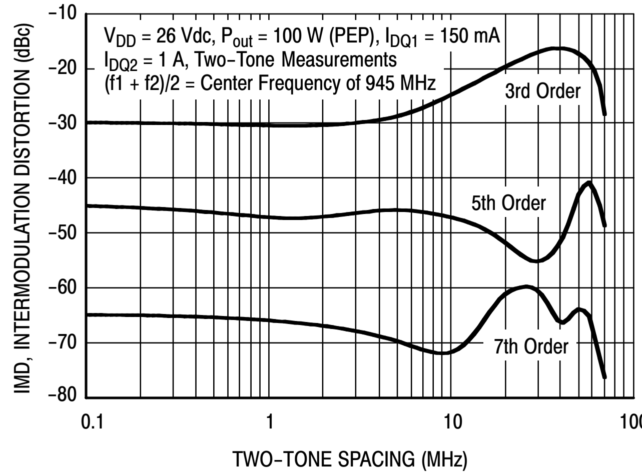


Figure 10. Intermodulation Distortion Products versus Tone Spacing

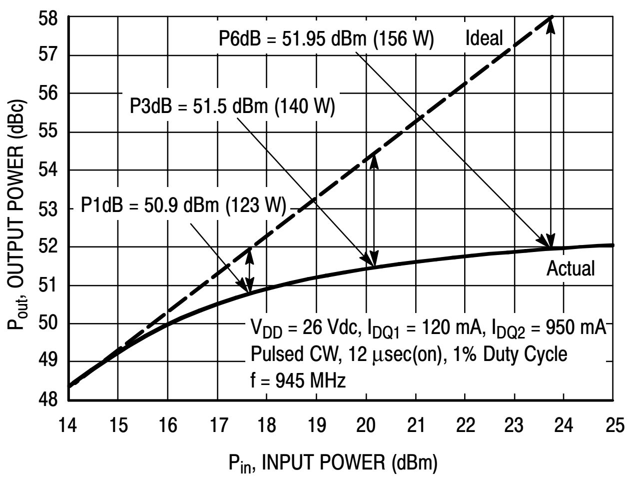


Figure 11. Pulsed CW Output Power versus Input Power

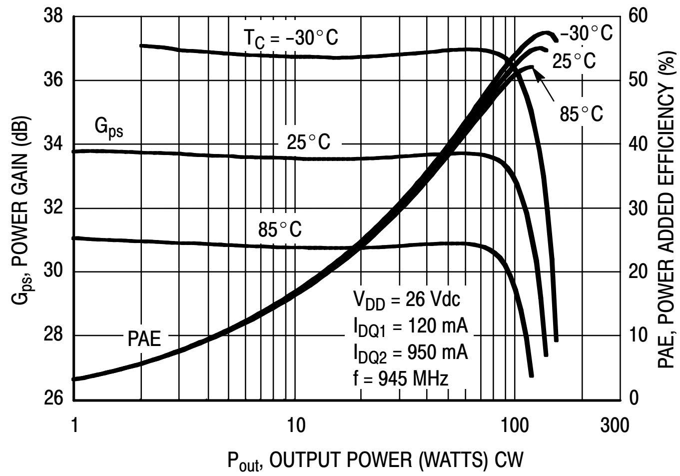


Figure 12. Power Gain and Power Added Efficiency versus Output Power @ 945 MHz

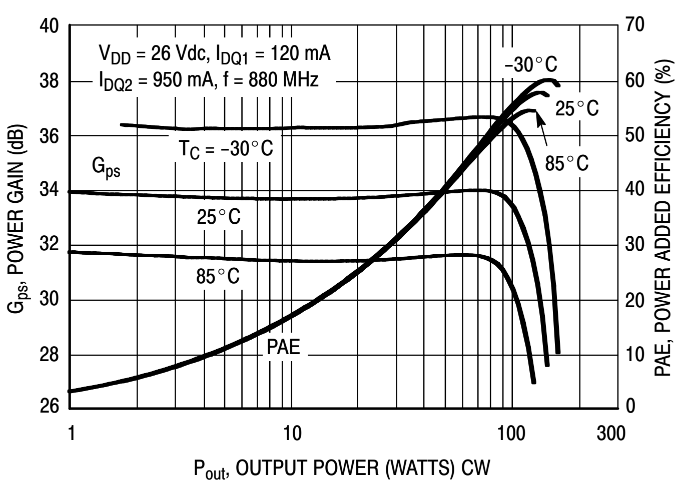


Figure 13. Power Gain and Power Added Efficiency versus Output Power @ 880 MHz

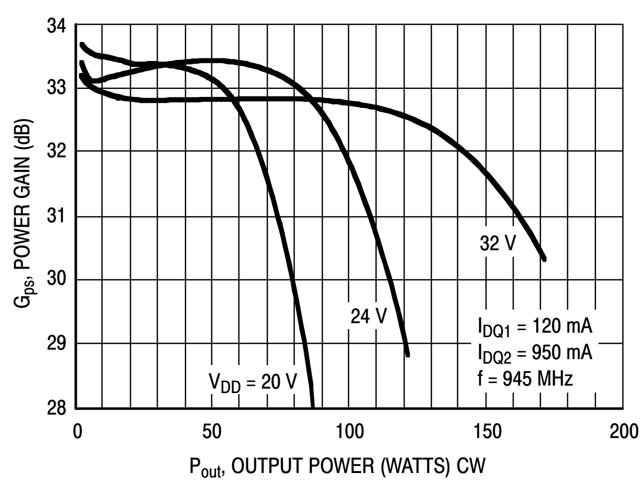


Figure 14. Power Gain versus Output Power

TYPICAL CHARACTERISTICS

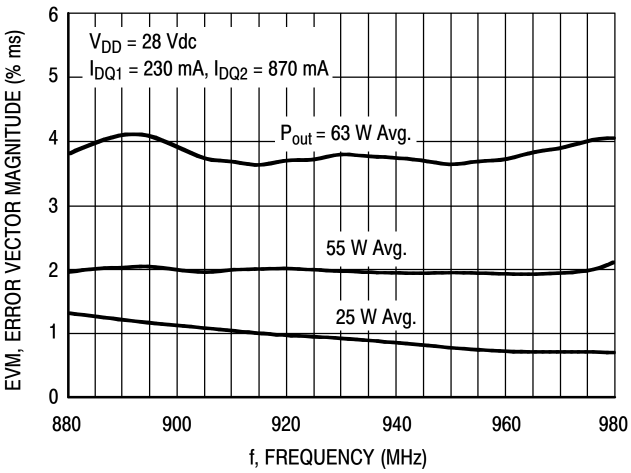


Figure 15. EVM versus Frequency

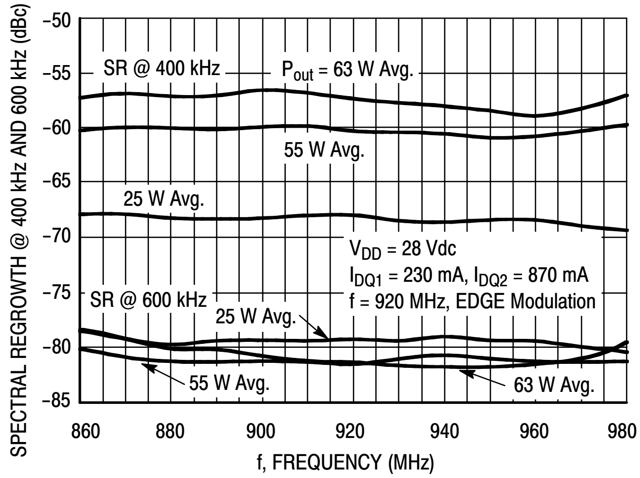


Figure 16. Spectral Regrowth at 400 kHz and 600 kHz versus Frequency

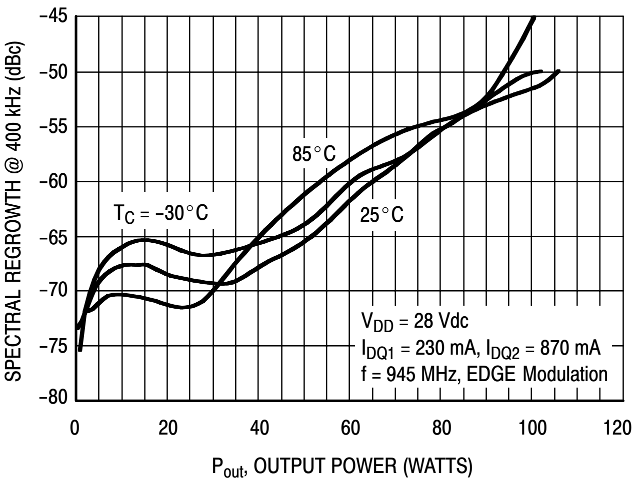


Figure 17. Spectral Regrowth at 400 kHz versus Output Power @ 945 MHz

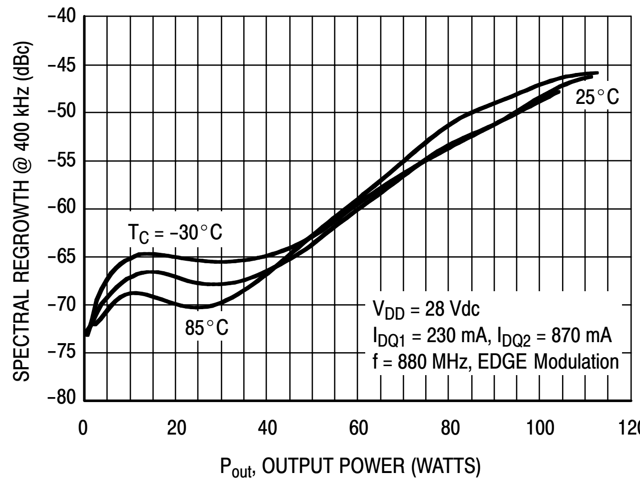


Figure 18. Spectral Regrowth at 400 kHz versus Output Power @ 880 MHz

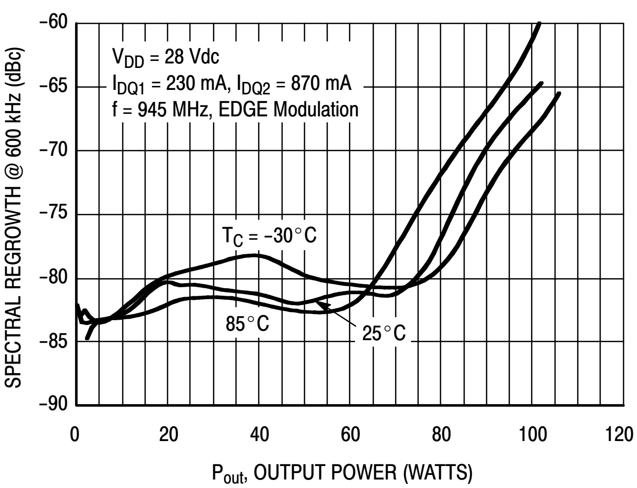


Figure 19. Spectral Regrowth at 600 kHz versus Output Power @ 945 MHz

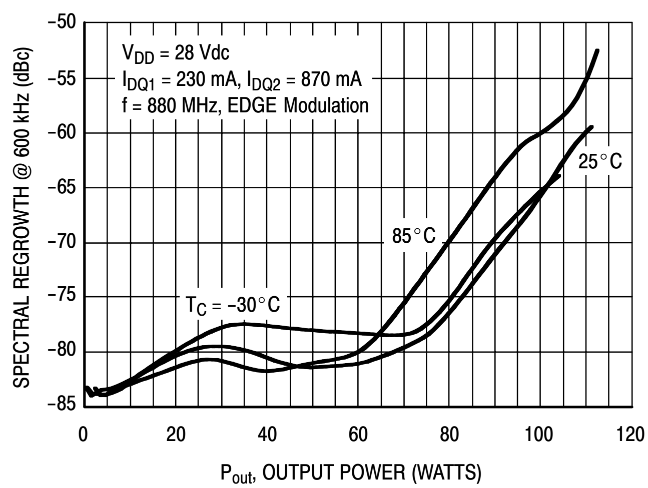


Figure 20. Spectral Regrowth at 600 kHz versus Output Power @ 880 MHz

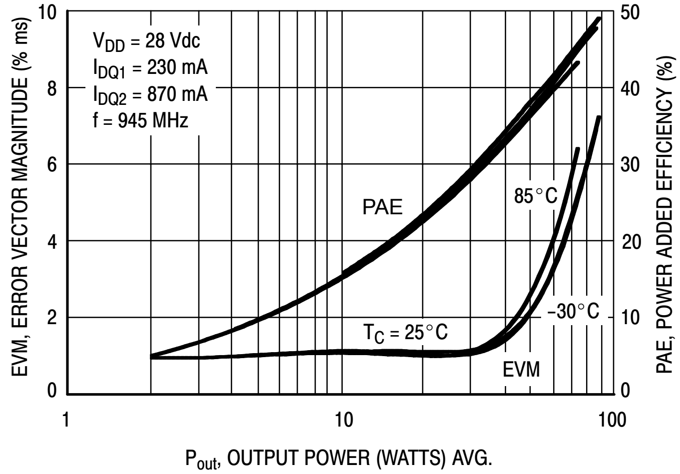


Figure 21. EVM and Power Added Efficiency versus Output Power @ 945 MHz

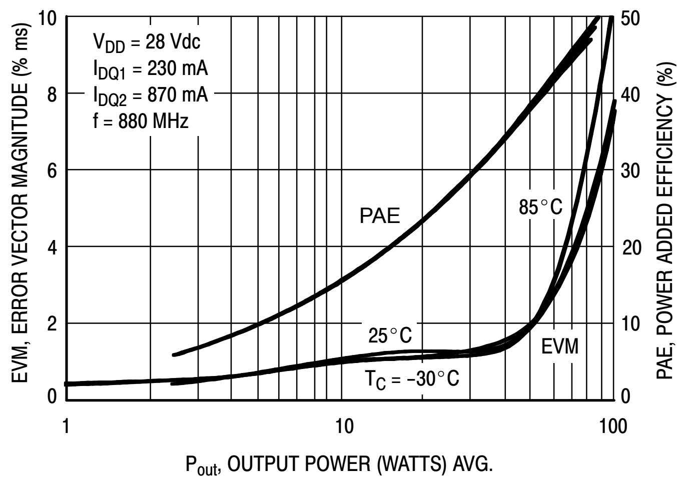


Figure 22. EVM and Power Added Efficiency versus Output Power @ 880 MHz

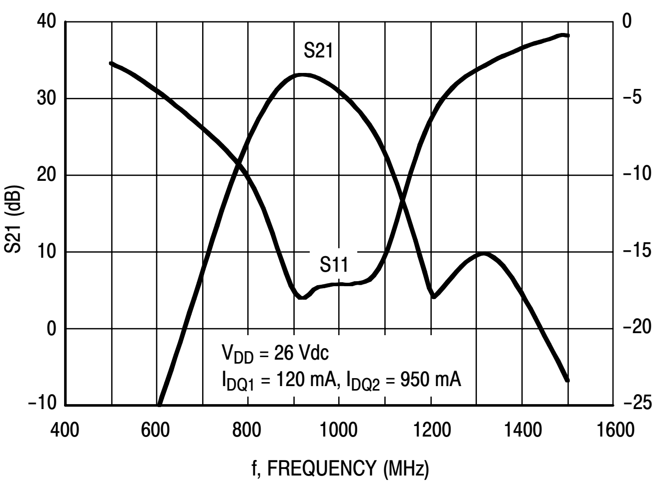


Figure 23. Broadband Frequency Response

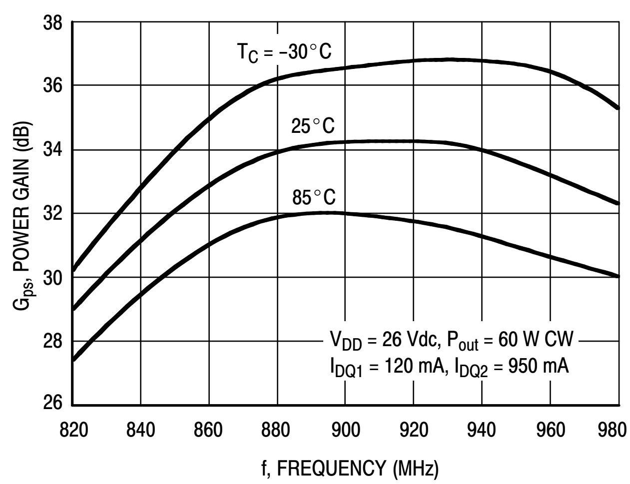
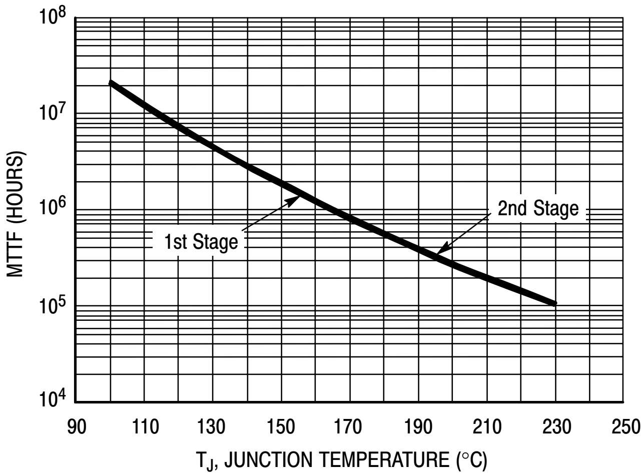


Figure 24. Power Gain versus Frequency



This above graph displays calculated MTTF in hours when the device is operated at V_{DD} = 26 Vdc, P_{out} = 100 W CW, and PAE = 54%.

MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 25. MTTF versus Junction Temperature

GSM TEST SIGNAL

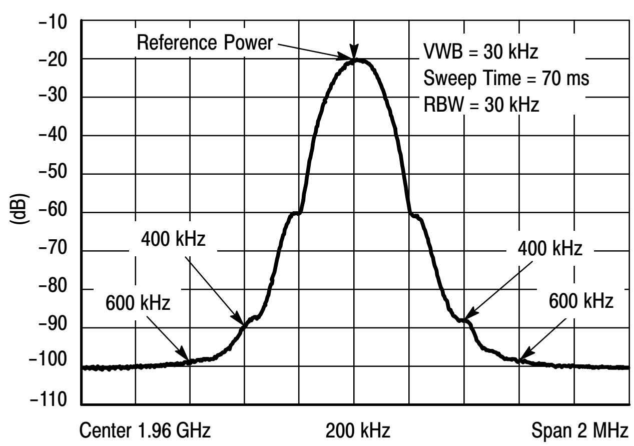
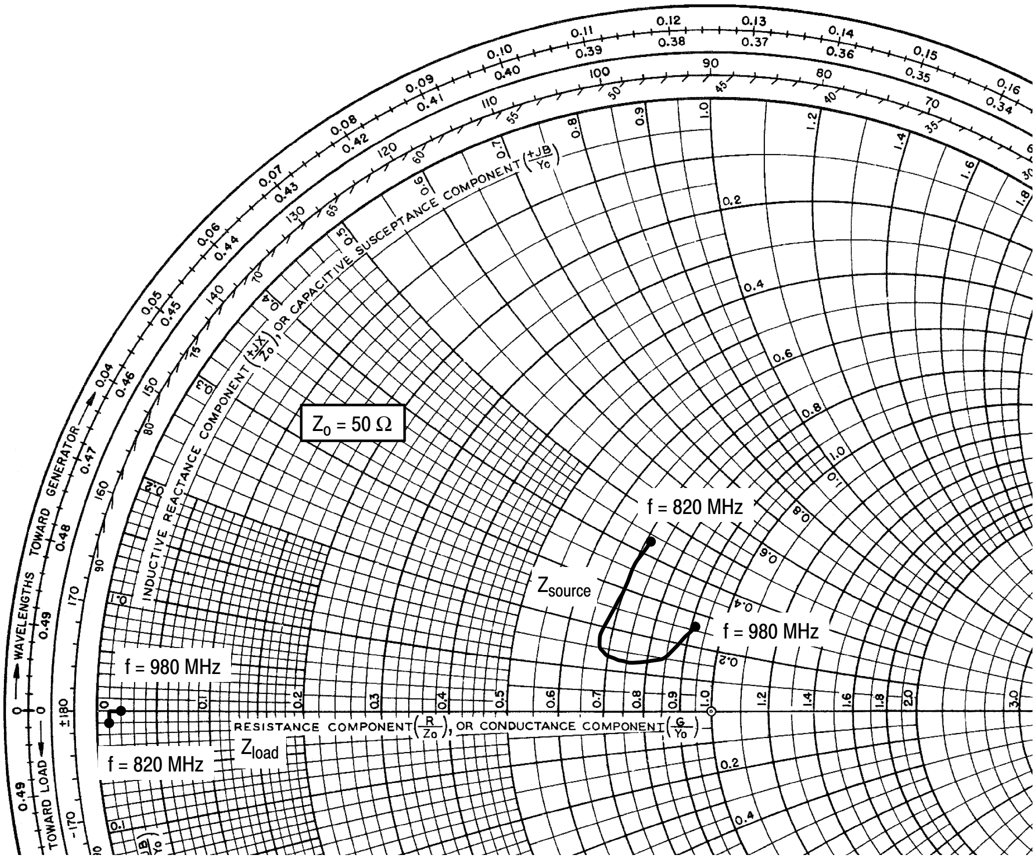


Figure 26. EDGE Spectrum



V_{DD} = 26 Vdc, I_{DQ1} = 120 mA, I_{DQ2} = 950 mA, P_{out} = 100 W CW

f MHz	Z_{source} Ω	Z_{load} Ω
820	35.40 + j21.50	0.516 - j0.365
840	35.00 + j18.00	0.638 - j0.172
860	35.00 + j15.50	0.768 - j0.010
880	34.50 + j12.20	0.874 + j0.071
900	34.00 + j9.00	1.030 + j0.133
920	34.30 + j7.20	1.101 + j0.082
940	38.50 + j6.00	1.088 + j0.037
960	42.00 + j7.40	1.011 + j0.018
980	45.55 + j12.75	0.872 + j0.051

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

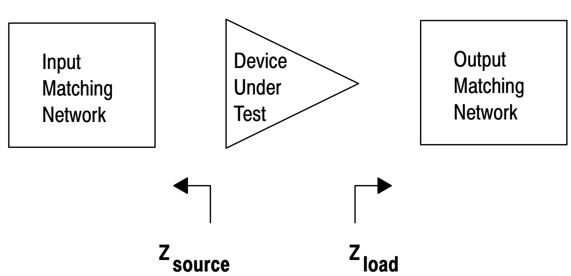
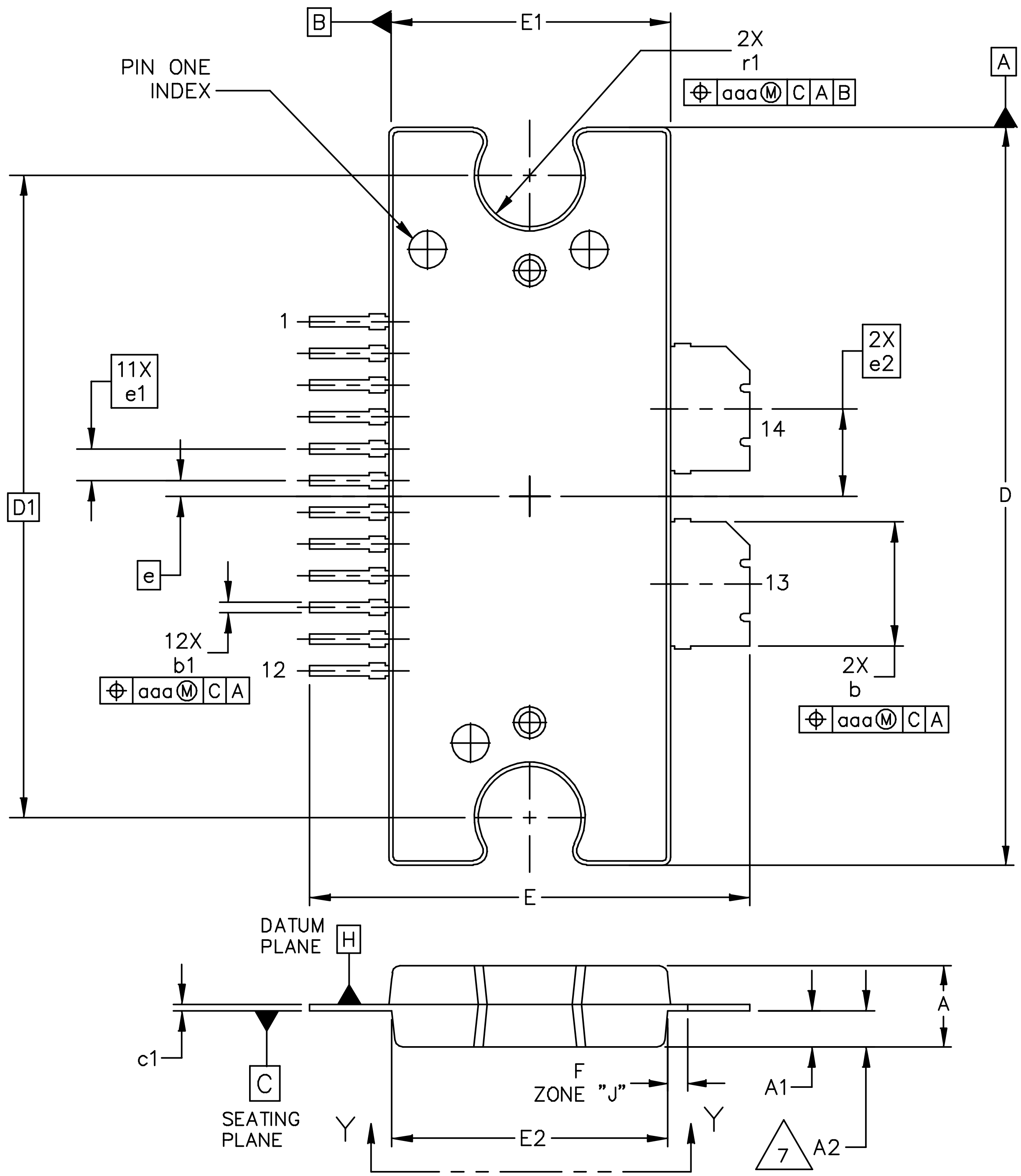


Figure 27. Series Equivalent Source and Load Impedance

Table 7. Common Source Scattering Parameters (V_{DD} = 26 V, 50 ohm system, I_{DQ1} = 120 mA, I_{DQ2} = 950 mA)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
750	0.230	95	5.81	-87	0.0007	-119	0.989	-180
760	0.188	93	6.48	-97	0.0007	-116	0.987	180
770	0.149	92	7.18	-107	0.0007	-111	0.985	180
780	0.114	92	7.88	-117	0.0007	-110	0.983	180
790	0.085	96	8.56	-128	0.0008	-109	0.981	180
800	0.063	104	9.22	-139	0.0008	-108	0.979	180
810	0.047	117	9.82	-150	0.0009	-109	0.978	180
820	0.037	134	10.37	-161	0.0009	-110	0.978	-180
830	0.031	156	10.85	-172	0.0009	-111	0.977	-180
840	0.029	-177	11.27	178	0.0010	-113	0.977	-180
850	0.033	-152	11.60	167	0.0010	-114	0.978	-180
860	0.041	-134	11.87	156	0.0010	-117	0.978	-180
870	0.052	-123	12.07	146	0.0010	-119	0.979	-180
880	0.063	-116	12.20	135	0.0010	-122	0.979	-180
890	0.074	-112	12.25	125	0.0010	-123	0.979	180
900	0.084	-109	12.23	115	0.0010	-126	0.980	180
910	0.094	-106	12.15	106	0.0010	-129	0.979	180
920	0.104	-103	12.01	96	0.0010	-131	0.978	180
930	0.113	-99	11.82	86	0.0009	-133	0.978	180
940	0.125	-95	11.57	77	0.0009	-135	0.977	180
950	0.141	-91	11.28	68	0.0008	-138	0.976	180
960	0.160	-88	10.97	59	0.0008	-136	0.976	180
970	0.183	-86	10.62	50	0.0007	-135	0.976	180
980	0.209	-85	10.23	42	0.0006	-133	0.976	180
990	0.238	-85	9.83	34	0.0006	-130	0.975	180
1000	0.268	-86	9.41	26	0.0006	-125	0.975	180



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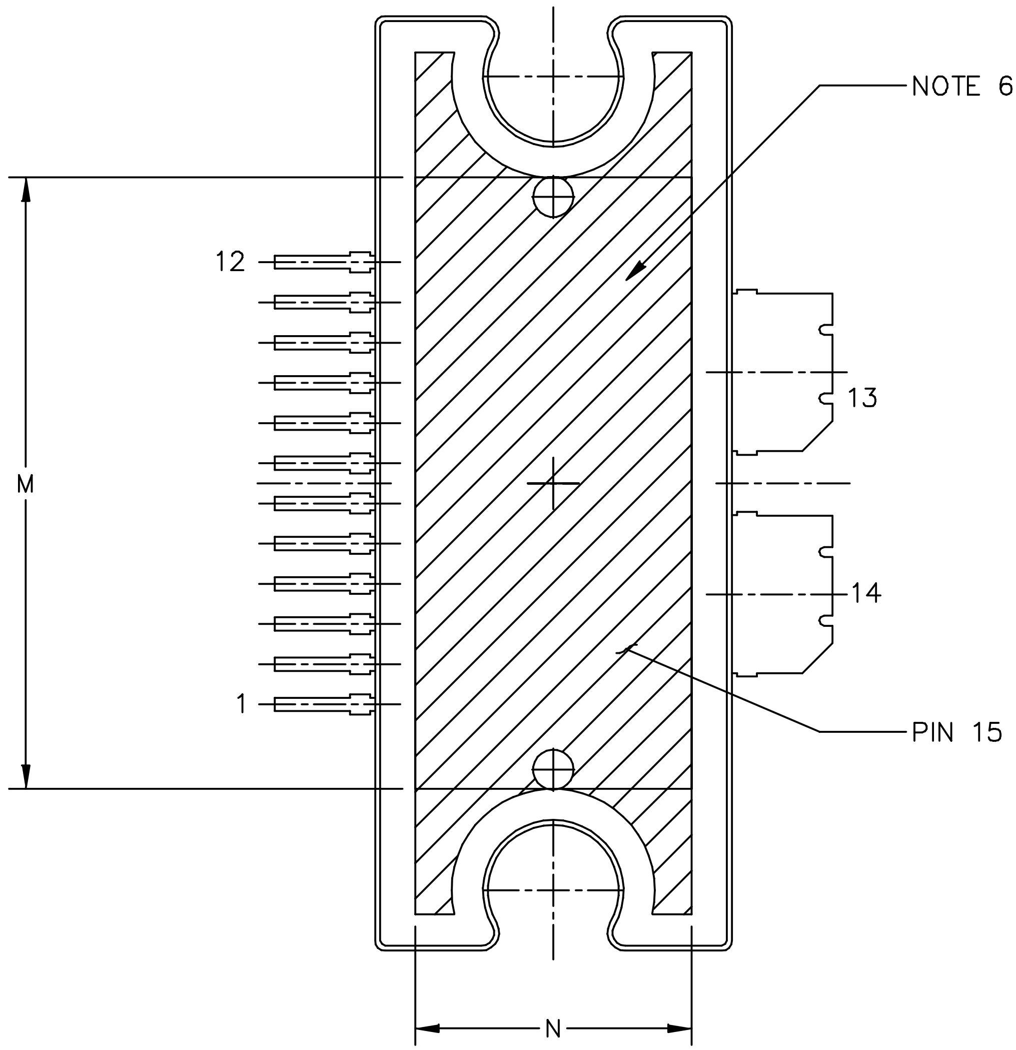
TITLE: TO–272 WIDE BODY 14 LEAD	DOCUMENT NO: 98ASA10649D	REV: A
	CASE NUMBER: 1617–02	27 JUN 2007
	STANDARD: NON–JEDEC	



VIEW Y–Y

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TITLE: TO–272 WIDE BODY 14 LEAD	DOCUMENT NO: 98ASA10649D	REV: A
	CASE NUMBER: 1617–02	27 JUN 2007
	STANDARD: NON–JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.

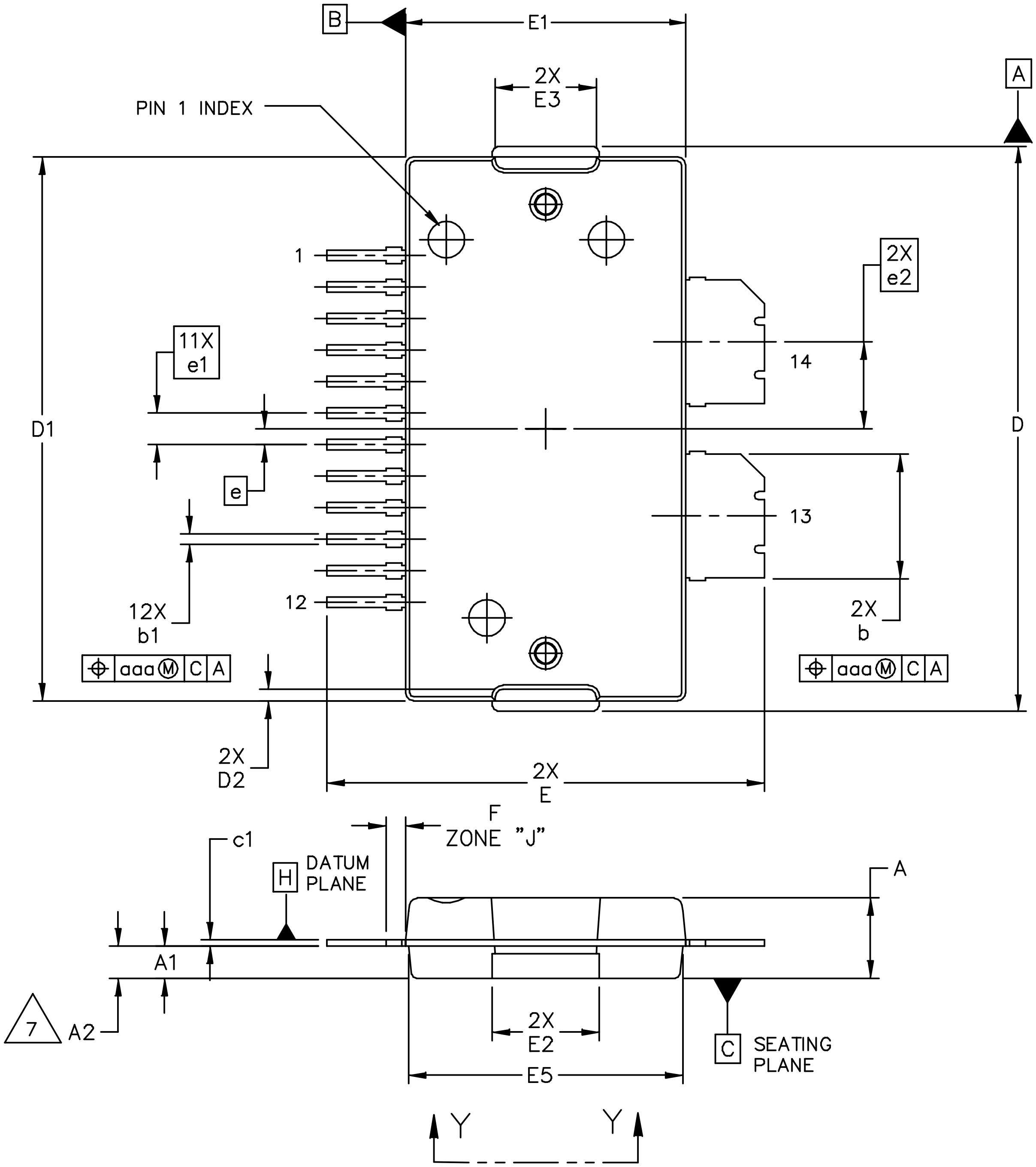
5. DIMENSIONS "b" AND "b1" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. HATCHING REPRESENTS THE EXPOSED AREA OFTHE HEAT SLUG.

7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	b	.154	.160	3.91	4.06
A1	.039	.043	0.99	1.09	b1	.010	.016	0.25	0.41
A2	.040	.042	1.02	1.07	c1	.007	.011	0.18	0.28
D	.928	.932	23.57	23.67	e	.020 BSC		0.51 BSC	
D1	.810 BSC		20.57 BSC		e1	.040 BSC		1.02 BSC	
E	.551	.559	14.00	14.20	e2	.1105 BSC		2.807 BSC	
E1	.353	.357	8.97	9.07	r1	.063	.068	1.6	1.73
E2	.346	.350	8.79	8.89					
F	.025 BSC		0.64 BSC		aaa	.004		0.10	
M	.600	----	15.24	----					
N	.270	----	6.86	----					

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO-272 WIDE BODY 14 LEAD	DOCUMENT NO: 98ASA10649D	REV: A
	CASE NUMBER: 1617-02	27 JUN 2007
	STANDARD: NON-JEDEC	



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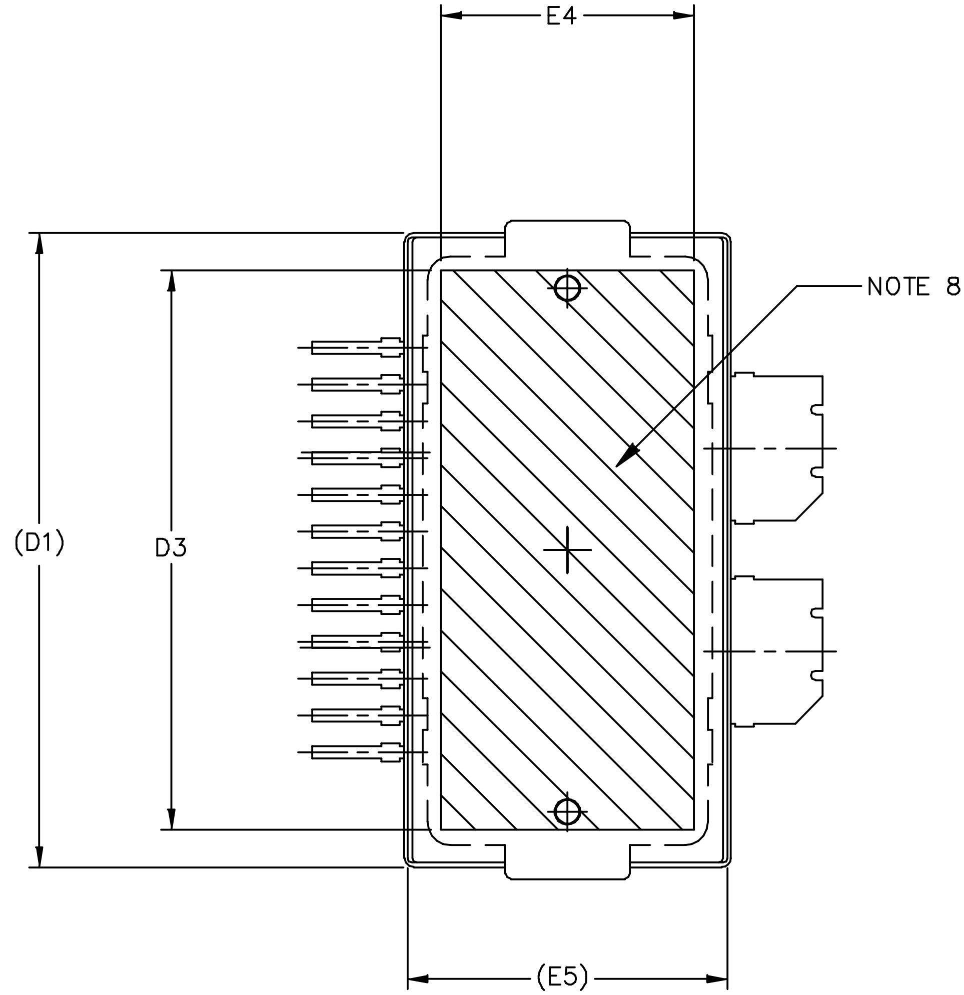
	CASE NUMBER: 1618–02		19 JUN 2007
	STANDARD: NON–JEDEC		



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TITLE: TO–270 WIDE BODY 14 LEAD		DOCUMENT NO: 98ASA10650D	REV: A
		CASE NUMBER: 1618–02	19 JUN 2007
		STANDARD: NON–JEDEC	

NOTES:

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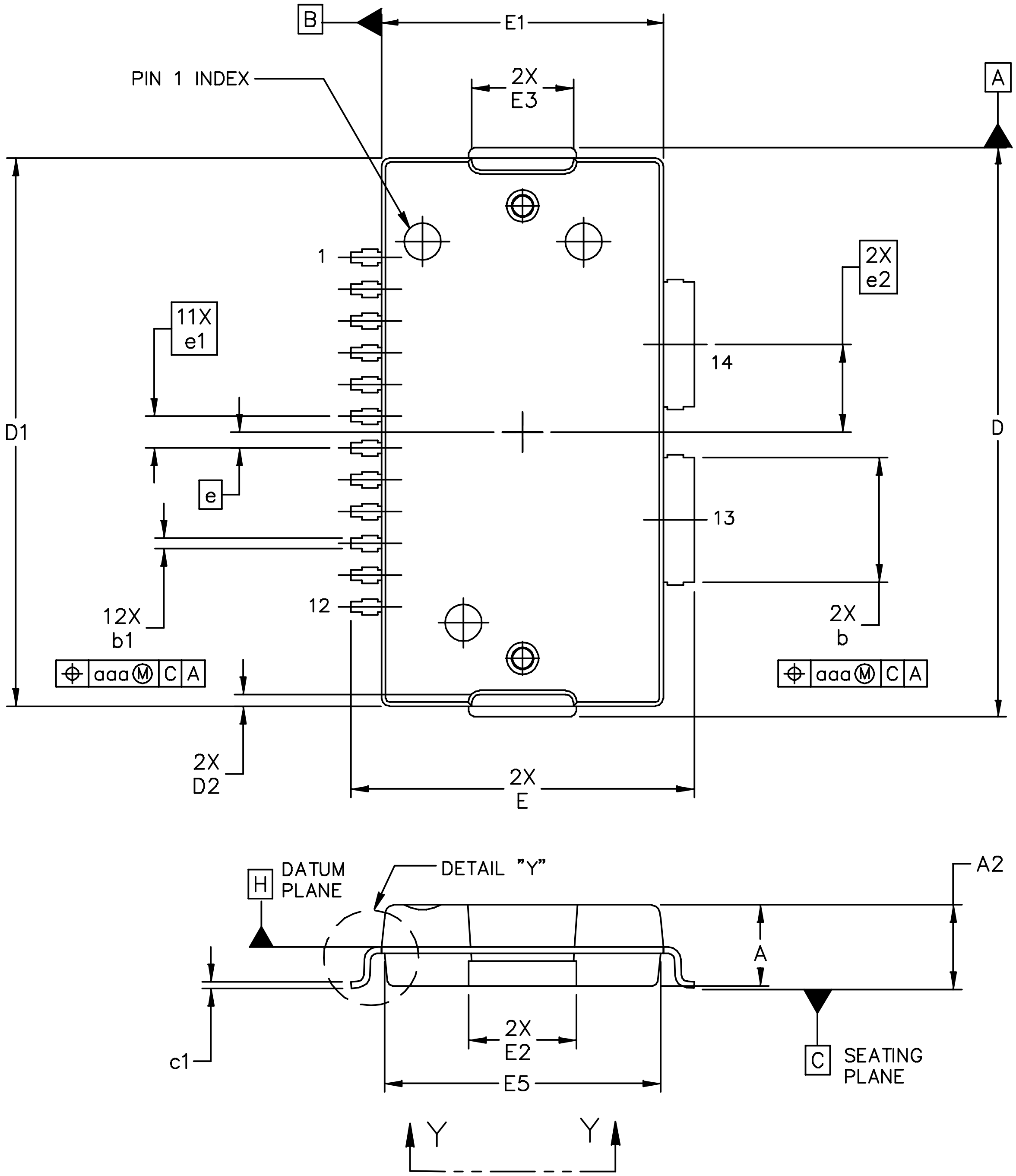
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −H−.
5. DIMENSIONS "b" AND "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS −A− AND −B− TO BE DETERMINED AT DATUM PLANE −H−.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b	.154	.160	3.91	4.06
A2	.040	.042	1.02	1.07	b1	.010	.016	0.25	0.41
D	.712	.720	18.08	18.29	c1	.007	.011	.18	.28
D1	.688	.692	17.48	17.58	e	.020 BSC		0.51 BSC	
D2	.011	.019	0.28	0.48	e1	.040 BSC		1.02 BSC	
D3	.600	−−−	15.24	−−−	e2	.1105 BSC		2.807 BSC	
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07	aaa	.004		.10	
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	−−−	6.86	−−−					
E5	.346	.350	8.79	8.89					

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO−270 WIDE BODY 14 LEAD	DOCUMENT NO: 98ASA10650D	REV: A
	CASE NUMBER: 1618−02	19 JUN 2007
	STANDARD: NON−JEDEC	



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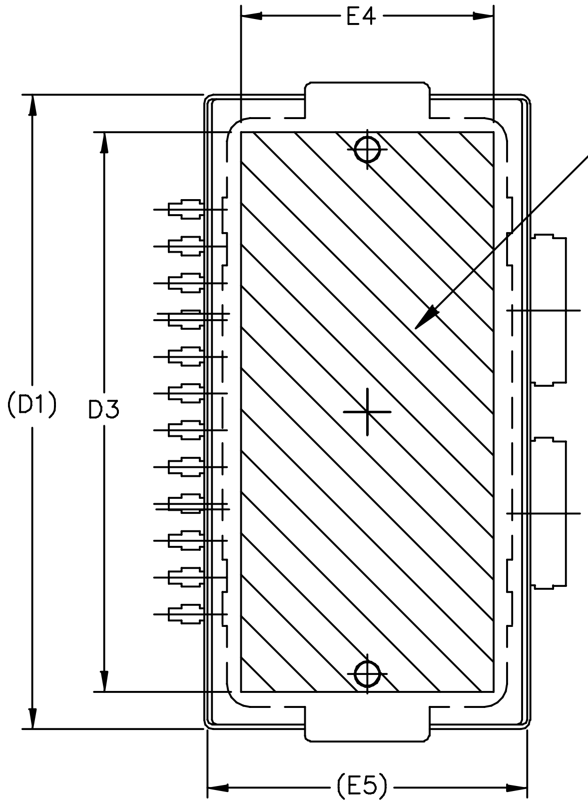
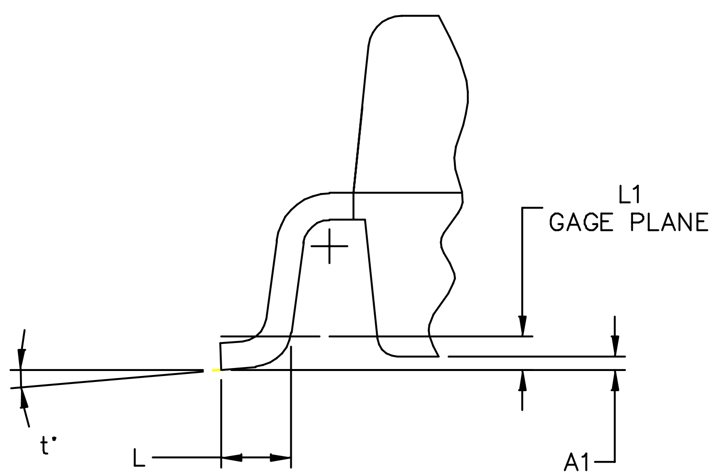
	CASE NUMBER: 1621-02	19 JUN 2007
	STANDARD: NON-JEDEC	



VIEW Y–Y



DETAIL "Y"

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO–270 WIDE BODY 14 LEAD GULL WING	DOCUMENT NO: 98ASA10653D	REV: A
	CASE NUMBER: 1621–02	19 JUN 2007
	STANDARD: NON–JEDEC	

NOTES:

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5. DIMENSIONS "b" AND "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS −A− AND −B− TO BE DETERMINED AT DATUM PLANE −H−.
7. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	L	.018	.024	0.46	0.61
A1	.001	.004	0.02	0.10	L1	.010 BSC		0.25 BSC	
A2	.099	.110	2.51	2.79	b	.154	.160	3.91	4.06
D	.712	.720	18.08	18.29	b1	.010	.016	0.25	0.41
D1	.688	.692	17.48	17.58	c1	.007	.011	.18	.28
D2	.011	.019	0.28	0.48	e	.020 BSC		0.51 BSC	
D3	.600	−−−	15.24	−−−	e1	.040 BSC		1.02 BSC	
E	.429	.437	10.9	11.1	e2	.1105 BSC		2.807 BSC	
E1	.353	.357	8.97	9.07	t	2°	8°	2°	8°
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35	aaa	.004		.10	
E4	.270	−−−	6.86	−−−					
E5	.346	.350	8.79	8.89					

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
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	CASE NUMBER: 1621−02	19 JUN 2007
	STANDARD: NON−JEDEC	

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Feb. 2007	• Initial Release of Data Sheet
1	May 2007	• Changed Device box to 960 MHz to reflect functional test frequency, p. 1 • Added Power Added Efficiency to GSM EDGE Application Typical Performances, p. 1 • Changed “5:1 VSWR, @ 28 Vdc” to “10:1 VSWR, @ 32 Vdc” in the Capable of Handling bullet, p. 1 • Added Footnote (1) to Quiescent Current Thermal Tracking bullet under Features section and to Quiescent Current Temperature Compensation in Fig. 1, Functional Block Diagram, p. 1 • Added top-level, 2-stage block diagram depiction to Fig. 2, Pin Connections; updated Note, p. 1 • Added Case Operating Temperature limit to the Maximum Ratings table and set limit to 150°C, p. 2 • Added Stage 1 and Stage 2 DC Electrical Characteristics tables, p. 2, 3 • In Table 6, Component Designations and Values, corrected Part Number ATC100B331JT500XT to ATC100B331JT200XT for C24 capacitor, p. 4 • Updated Figs. 7 and 8, Power Gain versus Output Power, to remove non-variable I_{DQ} value, p. 6 • Updated Fig. 9, Intermodulation Distortion Products versus Output Power, to show PEP and not CW; corrected frequency value to show 100 kHz Tone Spacing, p. 7 • Updated graphical representation of Ideal/Actual in Fig. 11, Pulsed CW Output Power versus Input Power, to show correct 3 and 6 dB compression points, p. 7
2	June 2007	• Removed Case Operating Temperature from Maximum Ratings table, p. 2. Case Operating Temperature rating will be added to the Maximum Ratings table when parts’ Operating Junction Temperature is increased to 225°C.
3	Dec. 2008	• Changed full frequency band in Typical GSM Performance bullet to f = 960 MHz to match actual production test, p. 1 • Changed Storage Temperature Range in Max Ratings table from -65 to +200 to -65 to +150 for standardization across products, p. 2 • Added Case Operating Temperature limit to the Maximum Ratings table and set limit to 150°C, p. 2 • Operating Junction Temperature increased from 200°C to 225°C in Maximum Ratings table, related “Continuous use at maximum temperature will affect MTTF” footnote added and changed 200°C to 225°C in Capable Plastic Package bullet, p. 1, 2 • Corrected Z10 from 1.17” to 0.117” in the Test Circuit Schematic Z list, p. 4 • Updated Part Numbers in Table 6, Component Designations and Values, to latest RoHS compliant part numbers, p. 4 • Replaced Case Outline 1617-01 with 1617-02, Issue A, p. 1, 13-15. Revised cross-hatched area for exposed heat spreader. Added pin numbers 1, 12, 13, and 14 to Sheets 1 and 2. Corrected mm Min and Max values for dimension A1 to 0.99 and 1.09, respectively. • Replaced Case Outline 1618-01 with 1618-02, Issue A, p. 1, 16-18. Added pin numbers 1, 12, 13, and 14 and Pin 1 Index designation to Sheet 1. Corrected dimensions e and e1 on Sheet 1. Removed Pin 5 designation from Sheet 2. • Replaced Case Outline 1621-01 with 1621-02, Issue A, p. 1, 19-21. Added pin numbers 1, 12, 13, and 14 and Pin 1 Index designation to Sheet 1. Corrected dimensions e and e1 on Sheets 1 and 3. Removed Pin 5 designation from Sheet 2. • Added Product Documentation and Revision History, p. 22

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