Freescale Semiconductor
Technical Data

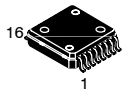
Document Number: MHV5IC2215N
Rev. 3, 1/2007

RoHS

RF LDMOS Wideband Integrated Power Amplifier

MHV5IC2215NR2

**2170 MHz, 23 dBm, 28 V
SINGLE N-CDMA, SINGLE W-CDMA
RF LDMOS WIDEBAND
INTEGRATED POWER AMPLIFIER**



**CASE 978-03
PFP-16**

The MHV5IC2215NR2 wideband integrated circuit is designed for base station applications. It uses Freescale's High Voltage (28 Volts) LDMOS IC technology and integrates a two-stage structure. Its wideband on-chip matching design makes it usable from 1500 to 2200 MHz. The linearity performances cover all modulation formats for cellular applications including TD-SCDMA.

Driver Application

- Typical Single-Carrier N-CDMA Performance: V_{DD} = 28 Volts, I_{DQ1} = 164 mA, I_{DQ2} = 115 mA, P_{out} = 23 dBm, Full Frequency Band (1930-1990 MHz), IS-95 CDMA (Pilot, Sync, Paging, Traffic Codes 8 Through 13) Channel Bandwidth = 1.2288 MHz. PAR = 9.8 dB @ 0.01% Probability on CCDF.
  Power Gain — 27.5 dB
  ACPR @ 885 kHz Offset — -60 dBc in 30 kHz Bandwidth
- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQ1} = 164 mA, I_{DQ2} = 115 mA, P_{out} = 23 dBm, Full Frequency Band (2130-2170 MHz), Channel Bandwidth = 3.84 MHz, PAR = 8.5 dB @ 0.01% Probability on CCDF.
  Power Gain — 24 dB
  ACPR @ 5 MHz Offset — -55 dBc in 3.84 MHz Channel Bandwidth
- Capable of Handling 3:1 VSWR, @ 28 Vdc, 2170 MHz, 15 Watts CW Output Power
- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source Scattering Parameters

Features

- On-Chip Matching (50 Ohm Input, >5 Ohm Output)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function
- On-Chip Current Mirror g_m Reference FET for Self Biasing Application (1)
- Integrated ESD Protection
- RoHS Compliant
- In Tape and Reel. R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel

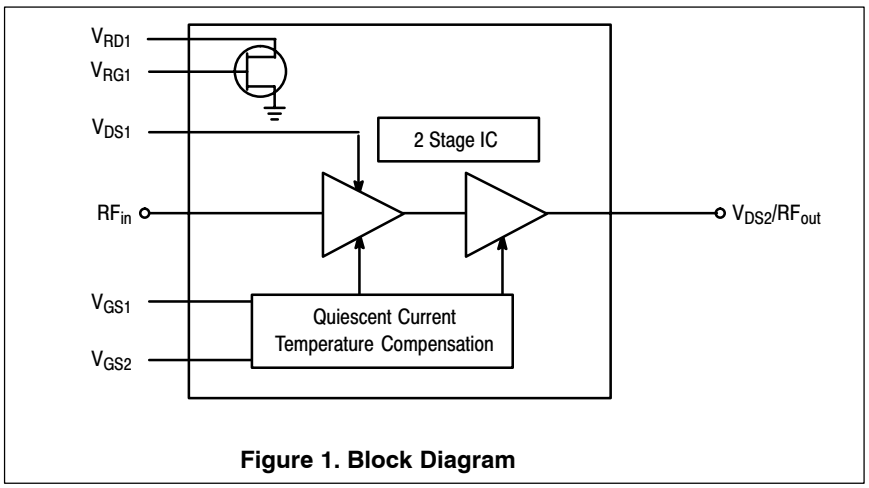
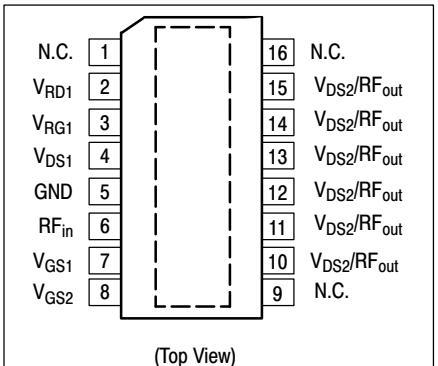


Figure 1. Block Diagram



(Top View)

Note: Exposed backside flag is source terminal for transistors.

Figure 2. Pin Connections

1. Refer to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1987.

freescale semiconductor

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +12	Vdc
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Operating Junction Temperature	T_J	150	°C
Input Power	P_{in}	12	dBm

Table 2. Thermal Characteristics

Characteristic		Symbol	Value (1)	Unit
Thermal Resistance, Junction to Case		$R_{\theta JC}$		°C/W
Driver Application (P_{out} = 23 dBm CW)	Stage 1, 28 Vdc, I_{DQ1} = 164 mA		9.3	
	Stage 2, 28 Vdc, I_{DQ2} = 115 mA		3.5	

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	0 (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	III (Minimum)

Table 4. Moisture Sensitivity Level

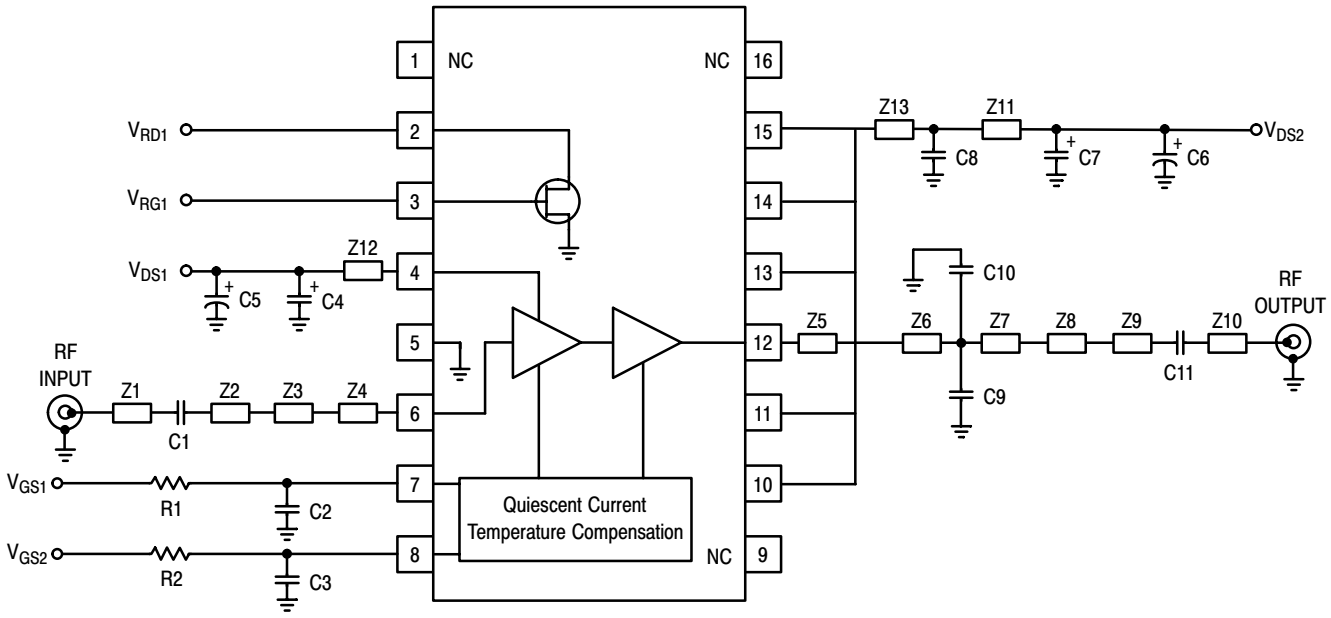
Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
W-CDMA Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1} = 164 mA, I_{DQ2} = 115 mA, P_{out} = 23 dBm, f = 2140 MHz, Single-carrier W-CDMA, 3.84 MHz Channel Bandwidth Carrier. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset. PAR = 8.5 dB @ 0.01% Probability on CCDF.					
Power Gain	G_{ps}	23	24	27	dB
Gain Flatness in 60 MHz Bandwidth @ P_{out} = 23 dBm f = 2110-2170 MHz	G_F	—	0.3	0.5	dB
Adjacent Channel Power Ratio	ACPR	—	-56	-54	dBc
Input Return Loss	IRL	—	-12	-10	dB
Typical N-CDMA Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1} = 164 mA, I_{DQ2} = 115 mA, P_{out} = 23 dBm, f = 1960 MHz, Single-Carrier N-CDMA, 1.2288 MHz Channel Bandwidth Carrier. ACPR measured in 30 kHz Channel Bandwidth @ ±885 kHz Offset. PAR = 9.8 dB @ 0.01% Probability on CCDF					
Power Gain	G_{ps}	25.5	27.5	29	dB
Gain Flatness @ P_{out} = 23 dBm f = 1930-1990 MHz	G_F	—	0.3	—	dB
Adjacent Channel Power Ratio	ACPR	—	-60	—	dBc
Input Return Loss	IRL	—	-12	—	dB
Average Deviation from Linear Phase in 60 MHz Bandwidth @ P_{out} = 23 dBm	Φ	—	0.2	—	°
Average Group Delay @ P_{out} = 23 dBm Including Output Matching	Delay	—	1.5	—	ns

1. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

W-CDMA DRIVER APPLICATION



Z1	0.045″ x 0.1289″ Microstrip	Z8	0.0105″ x 0.1200″ Microstrip
Z2	0.0443″ x 0.0161″ Microstrip	Z9	0.0559″ x 0.1145″ Microstrip
Z3	0.0308″ x 0.0416″ x 0.03″ Taper	Z10	0.045″ x 0.2671″ Microstrip
Z4	0.0161″ x 0.0685″ Microstrip	Z11	0.3319″ x 0.0349″ Microstrip
Z5	0.0838″ x 0.1759″ Microstrip	Z12	0.0027″ x 2.0413″ Microstrip
Z6	0.0503″ x 0.1759″ Microstrip	Z13	0.9151″ x 0.0349″ Microstrip
Z7	0.0922″ x 0.1759″ Microstrip	PCB	Rogers 4350, 0.020″, ε_r = 3.5

Figure 3. MHV5IC2215NR2 Test Circuit Schematic

Table 6. MHV5IC2215NR2 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	22 pF, 50 V Chip Capacitor	06033J220GBS	AVX
C2, C3	6.8 pF, 50 V Chip Capacitors	06035J6R8BBS	AVX
C4, C7	1 μF, 35 V Tantalum Chip Capacitors	TAJA105K035R	AVX
C5, C6	330 μF, 50 V Electrolytic Chip Capacitors	MCR35V337M10X16	Multicomp
C8	0.01 μF, 50 V Chip Capacitor	0805C103K5RACTR	Kemet
C9, C10	2.7 pF, 50 V Chip Capacitors	06035J2R7BBS	AVX
C11	15 pF, 25 V Chip Capacitor	06033J150GBS	AVX
R1, R2	1 kΩ, 1/8 W Chip Resistors	CRCW08051000FKTA	Vishay

W-CDMA DRIVER APPLICATION

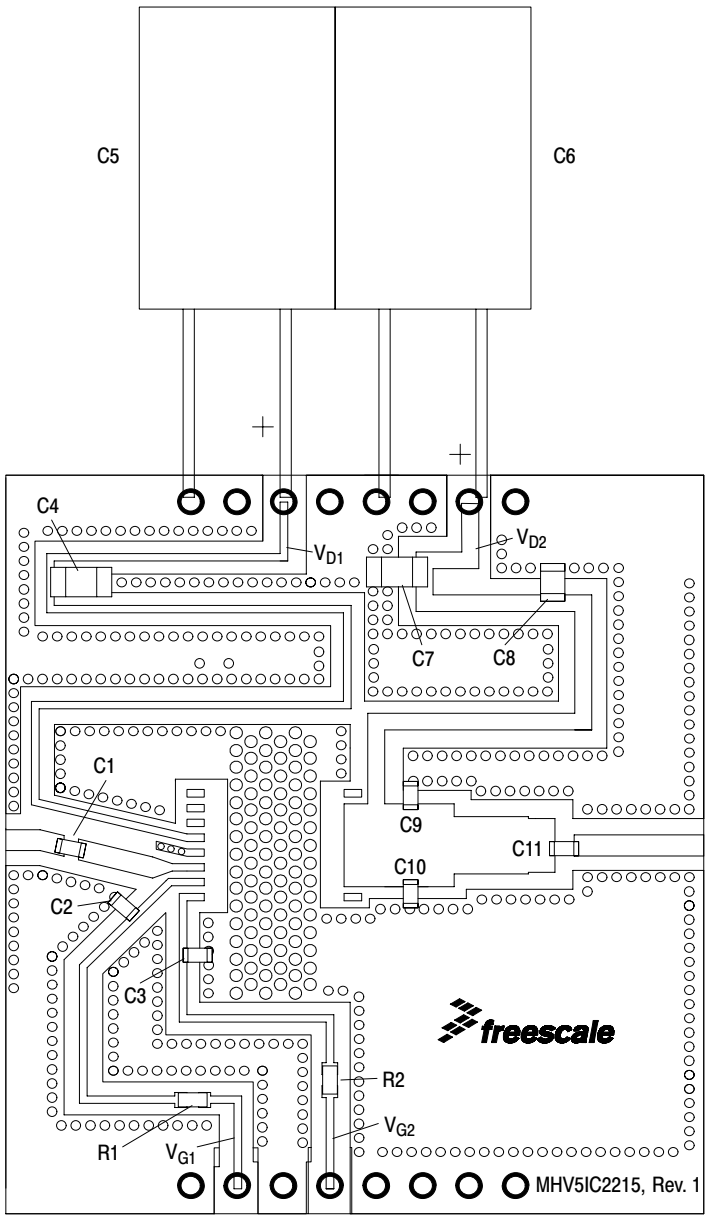


Figure 4. MHV5IC2215NR2 Test Circuit Component Layout

TYPICAL W-CDMA DRIVER APPLICATION CHARACTERISTICS

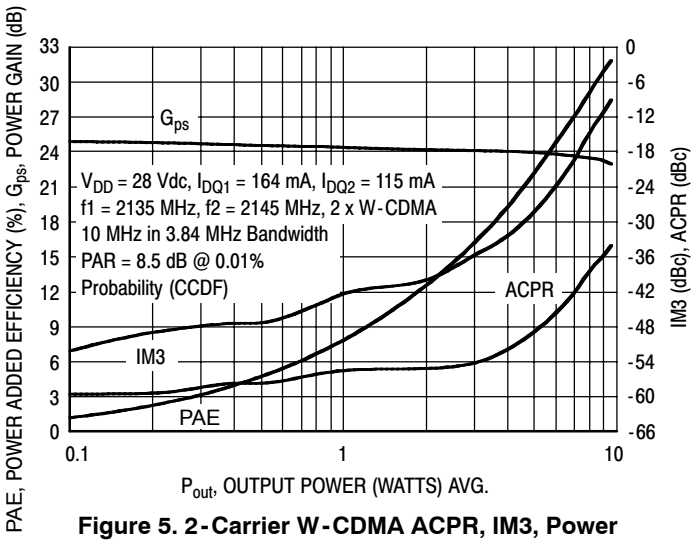


Figure 5. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Power Added Efficiency versus Output Power

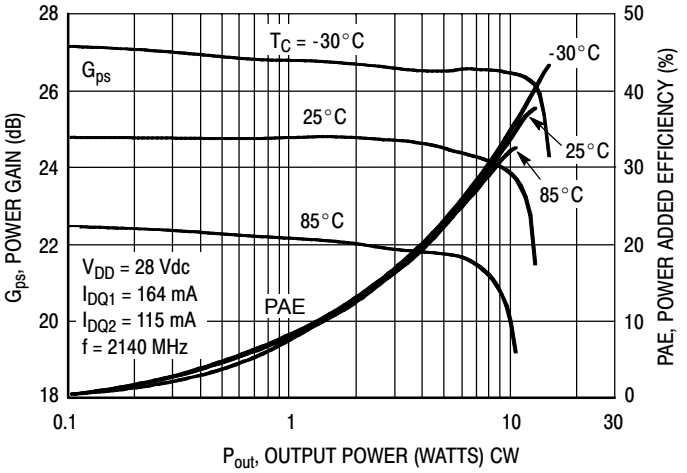


Figure 6. Power Gain and Power Added Efficiency versus Output Power

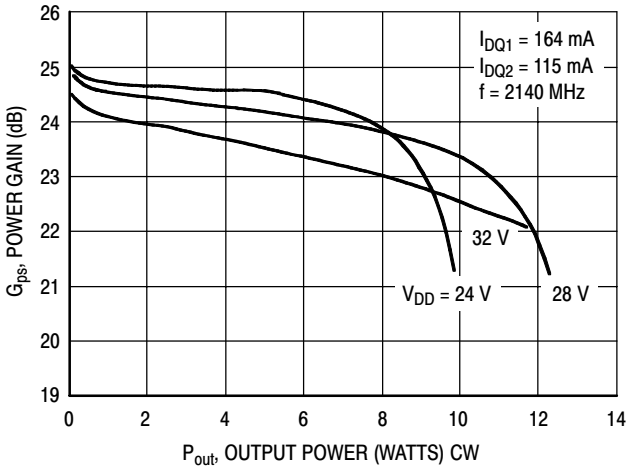


Figure 7. Power Gain versus Output Power

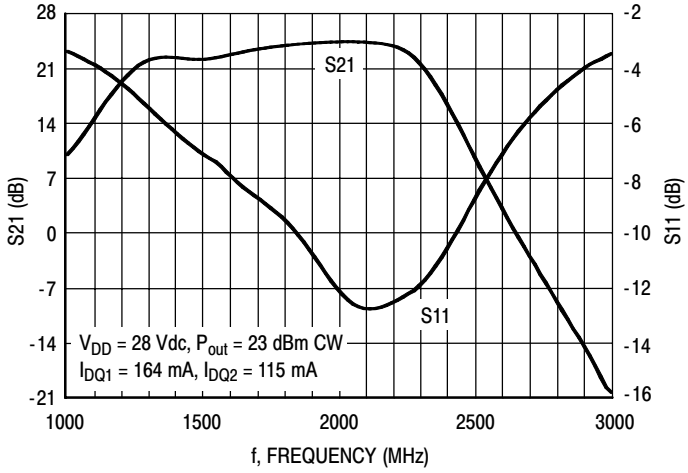


Figure 8. Broadband Frequency Response

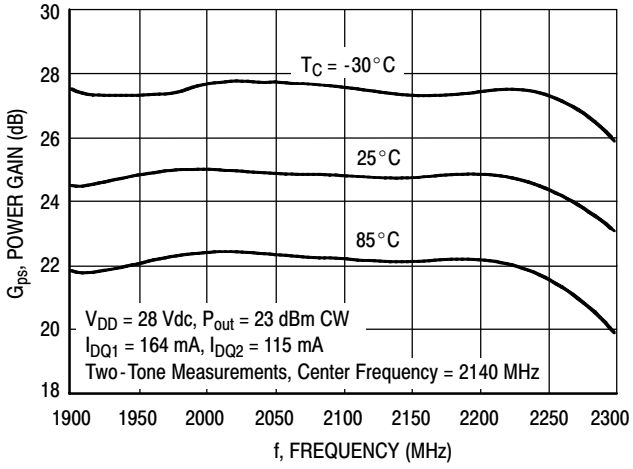
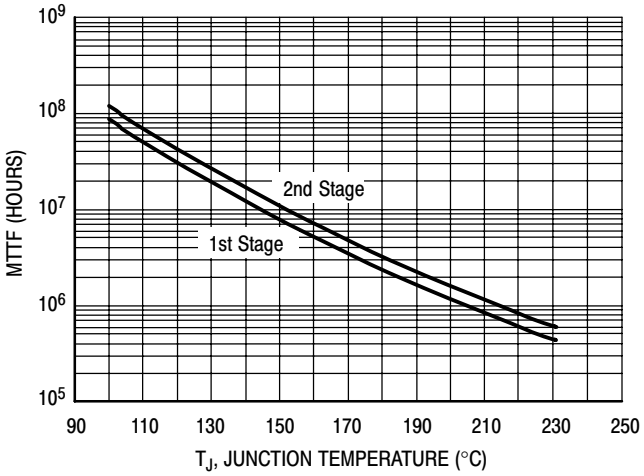


Figure 9. Power Gain versus Frequency

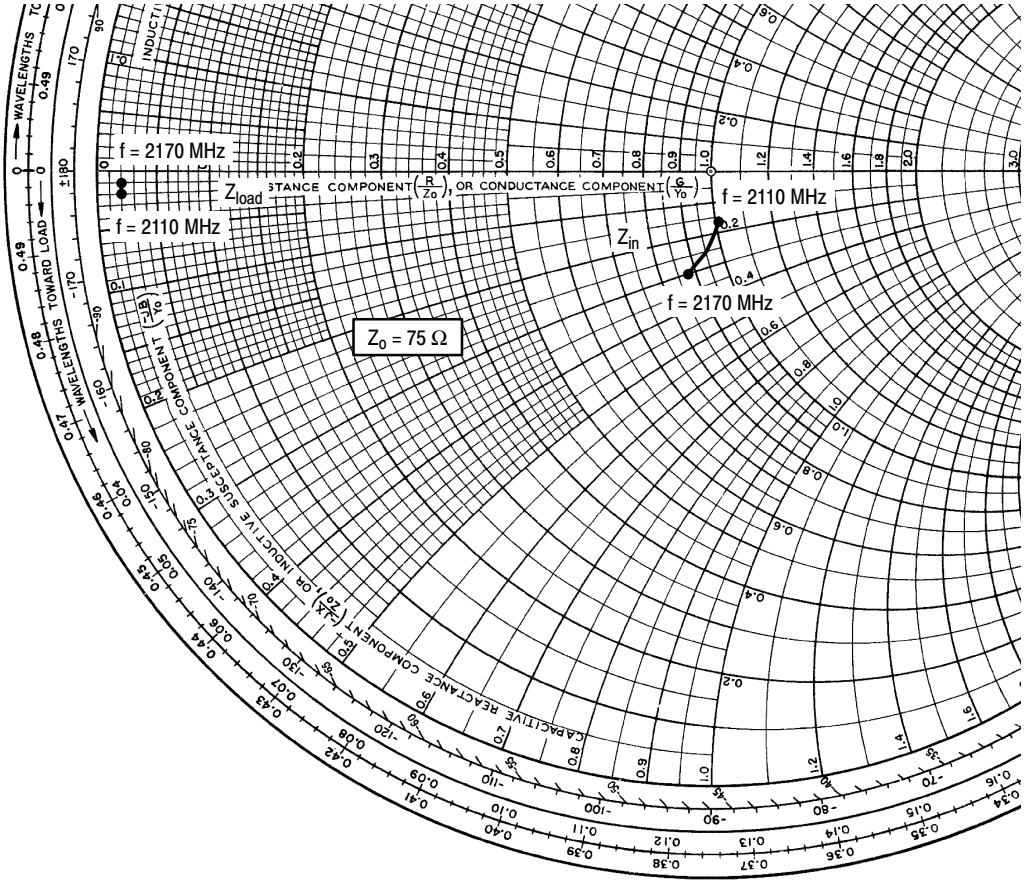
TYPICAL CHARACTERISTICS



This above graph displays calculated MTTF in hours when the device is operated at V_{DD} = 28 Vdc and P_{out} = 23 dBm.

MTTF calculator available at http:/www.freescale.com/rf. Select Tools/Software/Application Software/Calculators to access the MTTF calculators by product.

Figure 10. MTTF versus Junction Temperature



V_{DD} = 28 Vdc, I_{DQ1} = 164 mA, I_{DQ2} = 115 mA, P_{out} = 23 dBm

f MHz	Z_{in} Ω	Z_{load} Ω
2110	75.39 - j12.39	1.03 - j0.87
2140	71.11 - j18.83	0.99 - j0.61
2170	66.07 - j22.68	0.94 - j0.35

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

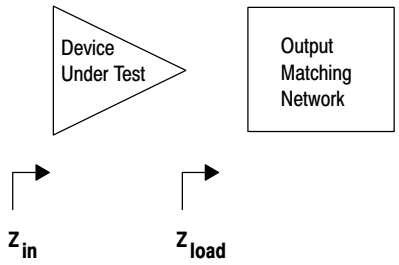
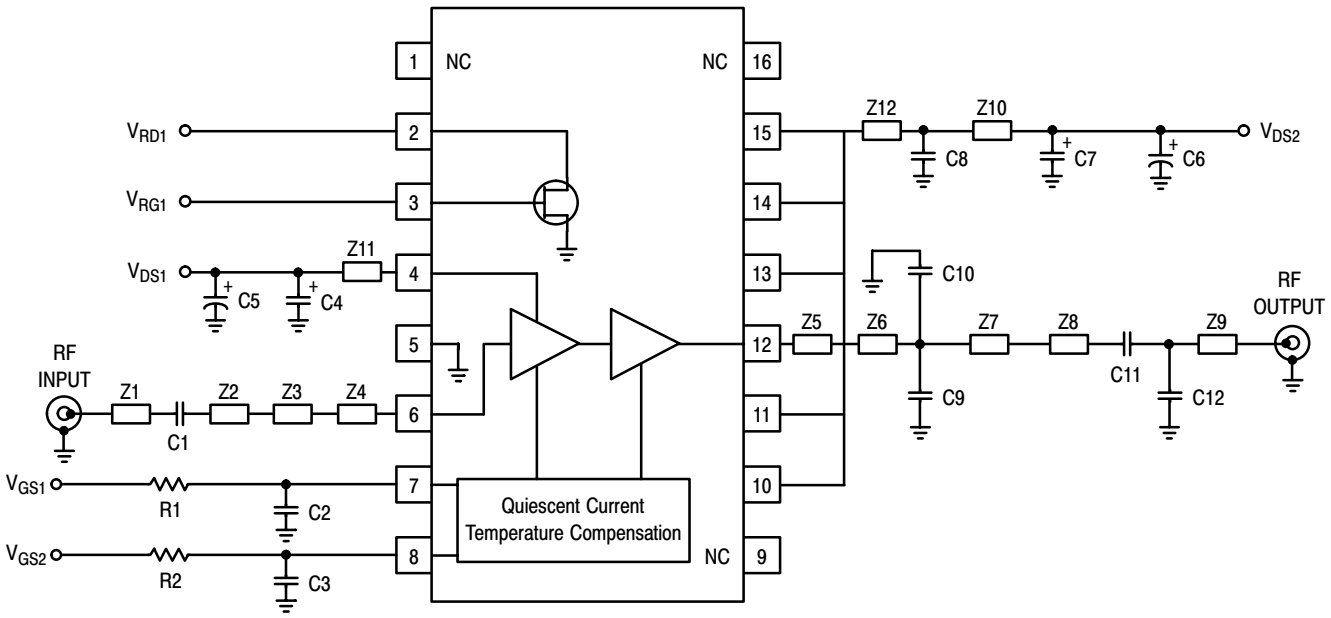


Figure 11. Series Equivalent Input and Load Impedance, 2140 MHz

N-CDMA DRIVER APPLICATION



Z1	0.045″ x 0.1289″ Microstrip	Z8	0.0559″ x 0.1145″ Microstrip
Z2	0.0443″ x 0.0161″ Microstrip	Z9	0.0450″ x 0.2671″ Microstrip
Z3	0.0308″ x 0.0416″ x 0.03″ Taper	Z10	0.3319″ x 0.0349″ Microstrip
Z4	0.0161″ x 0.0685″ Microstrip	Z11	0.0027″ x 2.0413″ Microstrip
Z5	0.0838″ x 0.1759″ Microstrip	Z12	0.9151″ x 0.0349″ Microstrip
Z6	0.1425″ x 1.7590″ Microstrip	PCB	Rogers 4350, 0.020″, ε_r = 3.5
Z7	0.0105″ x 0.1200″ Microstrip		

Figure 12. MHV5IC2215NR2 Test Circuit Schematic

Table 7. MHV5IC2215NR2 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	22 pF, 25 V Chip Capacitor	06033J220GBS	AVX
C2, C3	6.8 pF, 50 V Chip Capacitors	06035J6R8BBS	AVX
C4, C7	1 μF, 35 V Tantalum Chip Capacitors	TAJA105K035R	AVX
C5, C6	330 μF, 50 V Electrolytic Chip Capacitors	MCR35V337M10X16	Multicomp
C8	0.01 μF, 50 V Chip Capacitor	0805C103K5RACTR	Kemet
C9, C10	2.4 pF, 50 V Chip Capacitors	06035J2R4BBS	AVX
C11	15 pF, 25 V Chip Capacitor	06033J150GBS	AVX
C12	1.5 pF, 50 V Chip Capacitor	06035J1R5BBS	AVX
R1, R2	1 kΩ, 1/8 W Chip Resistors	CRCW08051000FKTA	Vishay

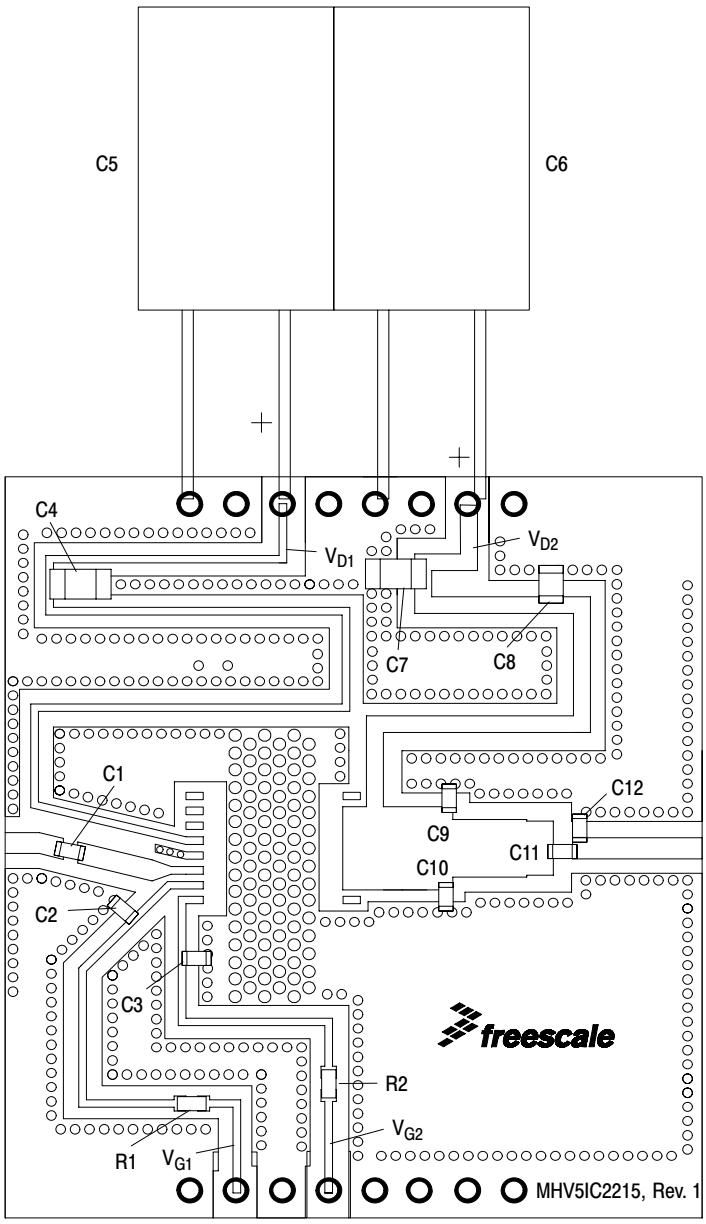


Figure 13. MHV5IC2215NR2 Test Circuit Component Layout

TYPICAL N-CDMA DRIVER APPLICATION CHARACTERISTICS

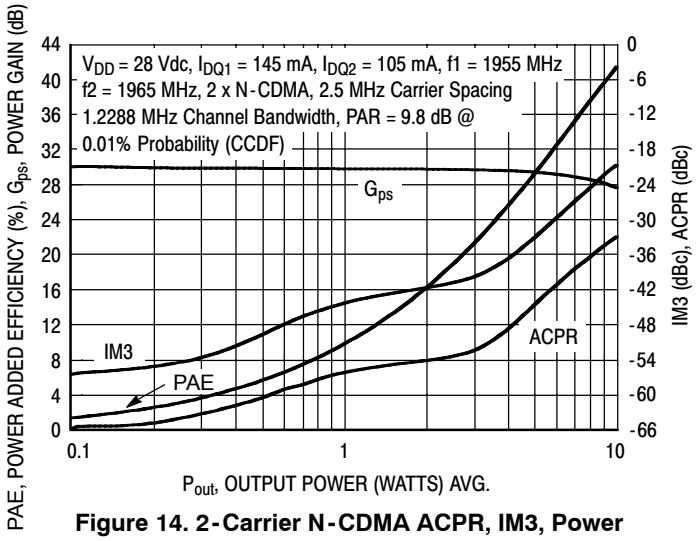


Figure 14. 2-Carrier N-CDMA ACPR, IM3, Power Gain and Power Added Efficiency versus Output Power

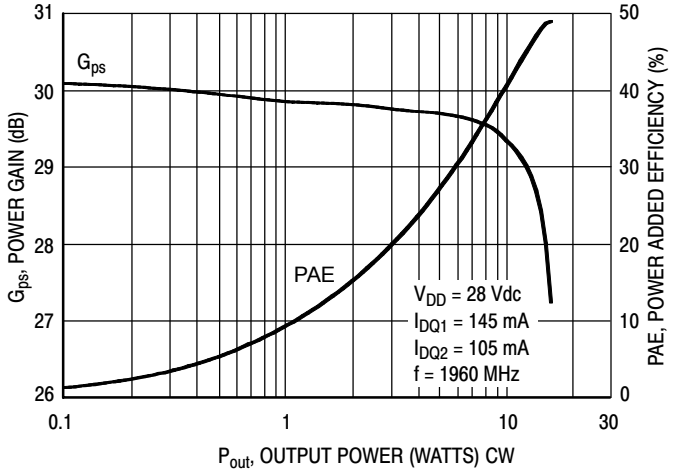


Figure 15. Power Gain and Power Added Efficiency versus Output Power

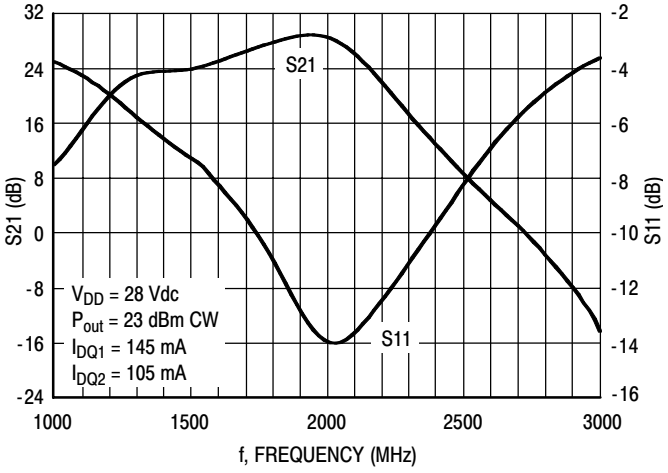
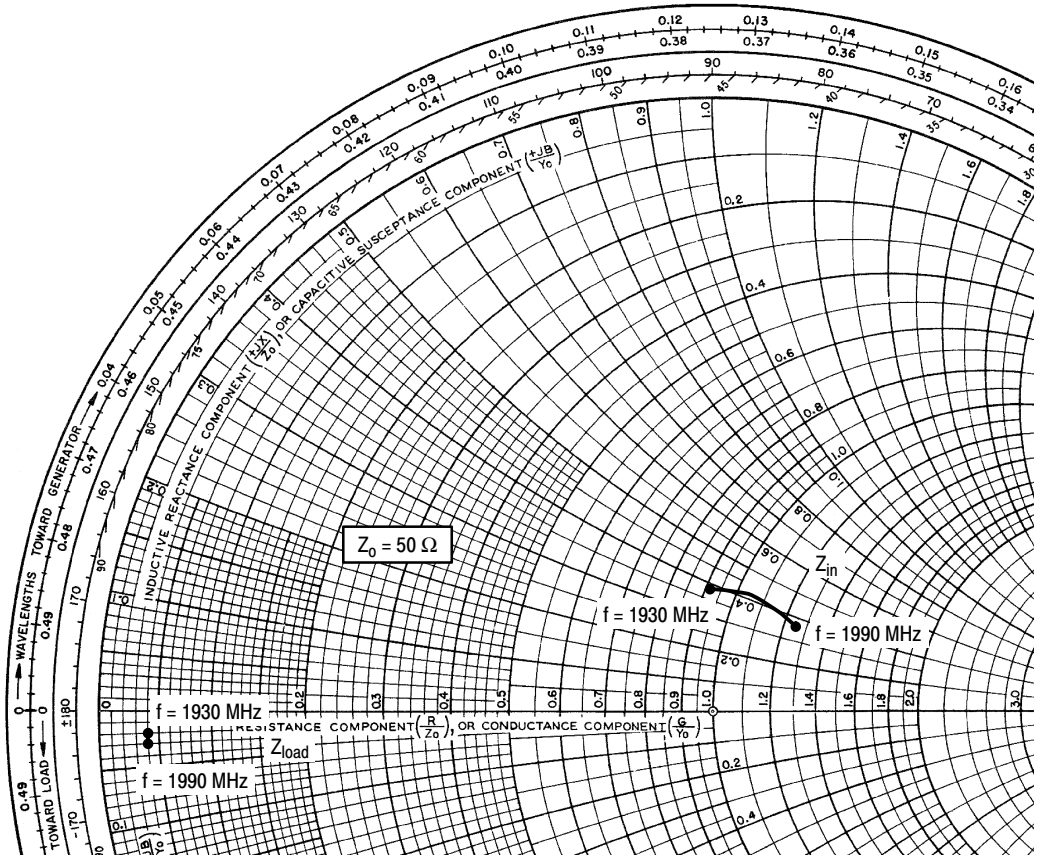


Figure 16. Broadband Frequency Response



V_{DD} = 28 Vdc, I_{DQ1} = 164 mA, I_{DQ2} = 115 mA, P_{out} = 23 dBm

f MHz	Z_{in} Ω	Z_{load} Ω
1930	45.98 + j19.10	2.18 - j0.88
1960	53.88 + j20.43	2.15 - j1.18
1990	62.55 + j18.70	2.12 - j1.49

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

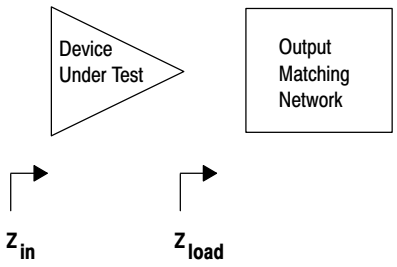


Figure 17. Series Equivalent Input and Load Impedance, 1960 MHz

Table 8. Common Source Scattering Parameters (V_{DC} = 28 V, T_C = 25°C, 50 ohm system)

I_{DQ1} = 164 mA, I_{DQ2} = 115 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ
1000	0.68244	21.958	3.27363	-46.706	0.00073	9.794	0.98732	153.093
1200	0.60173	-30.075	10.23125	-119.333	0.00072	13.436	1.00029	126.919
1400	0.47213	-92.332	13.7957	123.921	0.0007	-2.999	0.94139	106.192
1600	0.39882	175.345	13.86577	44.495	0.00088	-45.669	0.93605	87.096
1800	0.35107	59.2	16.61251	-38.246	0.00141	-13.097	0.91624	65.161
2000	0.23689	-70.587	17.30592	-133.04	0.0018	-35.967	0.88891	37.263
2200	0.21492	162.587	17.05916	121.911	0.00324	-62.618	0.56059	-24.504
2400	0.30222	113.328	6.44934	-14.639	0.00275	-134.469	0.69074	84.748
2600	0.46271	74.437	1.40717	-89.824	0.00149	-169.397	0.92384	34.554
2800	0.60247	39.529	0.39763	-141.044	0.00109	167.909	0.958	6.133
3000	0.69273	8.867	0.10191	-174.046	0.00129	122.208	0.9351	-18.125

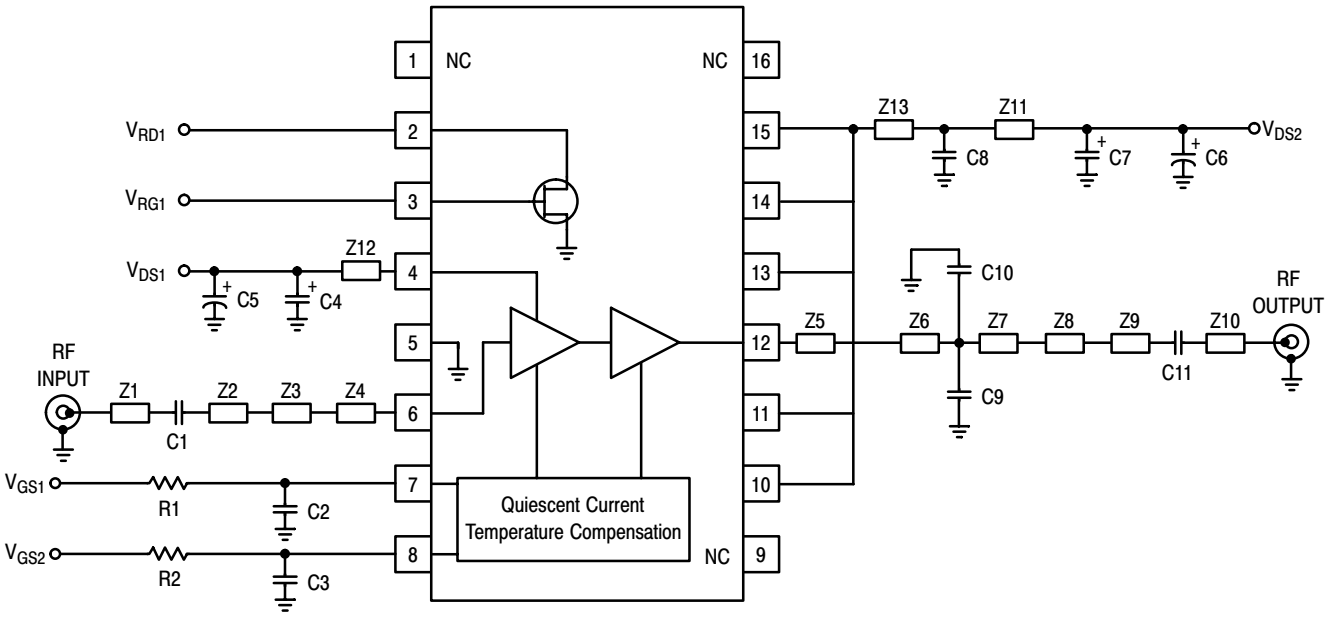
I_{DQ1} = 164 mA, I_{DQ2} = 345 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ
1000	0.67537	21.709	5.31667	-50.942	0.0008	6.129	0.99279	152.416
1200	0.59017	-29.975	15.91709	-129.84	0.00067	-0.12	0.99768	124.892
1400	0.46708	-92.31	19.32081	119.077	0.00075	-10.343	0.91612	105.353
1600	0.39635	174.623	20.10313	41.013	0.00083	-45.427	0.91179	87.084
1800	0.32171	55.947	23.76068	-42.642	0.00135	-6.07	0.89001	65.729
2000	0.2053	-76.58	24.4731	-136.766	0.0017	-34.308	0.86052	38.165
2200	0.20173	154.548	23.13058	117.16	0.00282	-62.743	0.47971	-18.382
2400	0.29085	112.112	8.78893	-12.308	0.00276	-133.95	0.65353	80.165
2600	0.46015	74.095	2.0309	-88.099	0.00145	-172.129	0.91226	34.199
2800	0.60229	39.22	0.58259	-140.332	0.00109	165.352	0.95453	6.049
3000	0.69238	8.662	0.15083	-173.655	0.00114	127.091	0.93394	-18.148

I_{DQ1} = 164 mA, I_{DQ2} = 500 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ
1000	0.6711	21.546	5.75013	-53.329	0.0007	24.45	0.99347	152.201
1200	0.58525	-30.018	16.76169	-134.625	0.00077	-1.375	0.9925	124.548
1400	0.46378	-92.504	19.69001	116.925	0.00076	5.296	0.91107	105.394
1600	0.39336	174.232	20.76629	39.298	0.0009	-40.621	0.90699	87.053
1800	0.31114	55.471	24.51619	-44.522	0.00124	-10.794	0.88668	65.947
2000	0.19301	-78.069	25.16732	-138.656	0.00189	-36.619	0.85513	38.413
2200	0.19638	152.604	23.41998	115.327	0.00305	-62.675	0.46723	-15.877
2400	0.28869	111.542	9.01024	-12.58	0.00259	-134.95	0.64185	79.222
2600	0.45971	73.791	2.10623	-88.735	0.00142	-166.566	0.90861	34.114
2800	0.60251	39.001	0.60593	-141.146	0.00107	168.738	0.95346	6.03
3000	0.69282	8.463	0.15674	-174.755	0.00121	124.35	0.93359	-18.226

TD-SCDMA CHARACTERIZATION



Z1	0.045″ x 0.1289″ Microstrip	Z8	0.0105″ x 0.1200″ Microstrip
Z2	0.0443″ x 0.0161″ Microstrip	Z9	0.0559″ x 0.1145″ Microstrip
Z3	0.0308″ x 0.0416″ x 0.03″ Taper	Z10	0.045″ x 0.2671″ Microstrip
Z4	0.0161″ x 0.0685″ Microstrip	Z11	0.7775″ x 0.0349″ Microstrip
Z5	0.0838″ x 0.1759″ Microstrip	Z12	2.0413″ x 0.0027″ Microstrip
Z6	0.089″ x 0.1759″ Microstrip	Z13	0.4697″ x 0.0349″ Microstrip
Z7	0.054″ x 0.1759″ Microstrip	PCB	Rogers 4350, 0.020″, ε_r = 3.5

Figure 18. MHV5IC2215NR2 Test Circuit Schematic — TD-SCDMA

Table 9. MHV5IC2215NR2 Test Circuit Component Designations and Values — TD-SCDMA

Part	Description	Part Number	Manufacturer
C1	22 pF, 50 V Chip Capacitor	06033J220GBS	AVX
C2, C3	6.8 pF, 50 V Chip Capacitors	06035J6R8BBS	AVX
C4, C7	1 μF, 35 V Tantalum Chip Capacitors	TAJA105K035R	AVX
C5, C6	330 μF, 50 V Electrolytic Chip Capacitors	MCR35V337M10X16	Multicomp
C8	0.01 μF, 50 V Chip Capacitor	0805C103K5RACTR	Kemet
C9, C10	2.7 pF, 50 V Chip Capacitors	06035J2R7BBS	AVX
C11	15 pF, 25 V Chip Capacitor	06033J150GBS	AVX
R1, R2	1 kΩ, 1/8 W Chip Resistors	CRCW08051000FKTA	Vishay

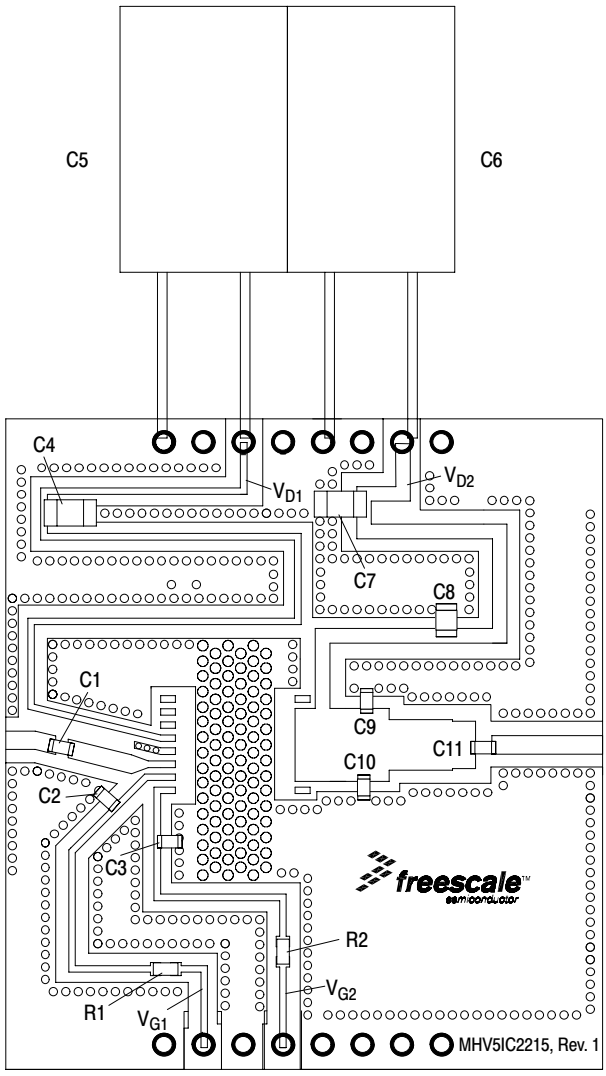


Figure 19. MHV5IC2215NR2 Test Circuit Component Layout — TD-SCDMA

TYPICAL CHARACTERISTICS

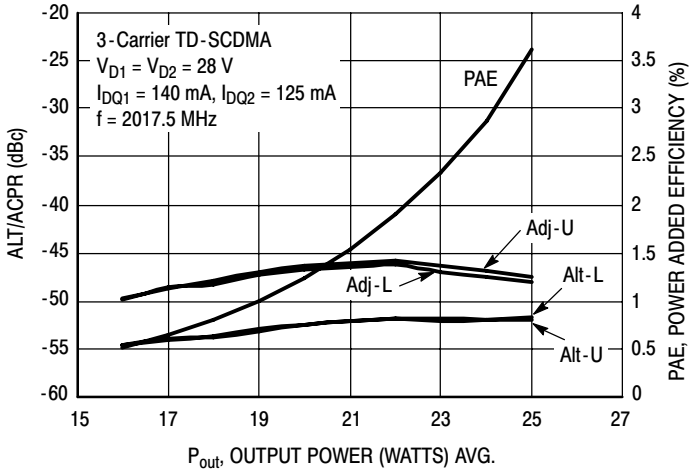


Figure 20. 3-Carrier TD-SCDMA ACPR, ALT and Power Added Efficiency versus Output Power

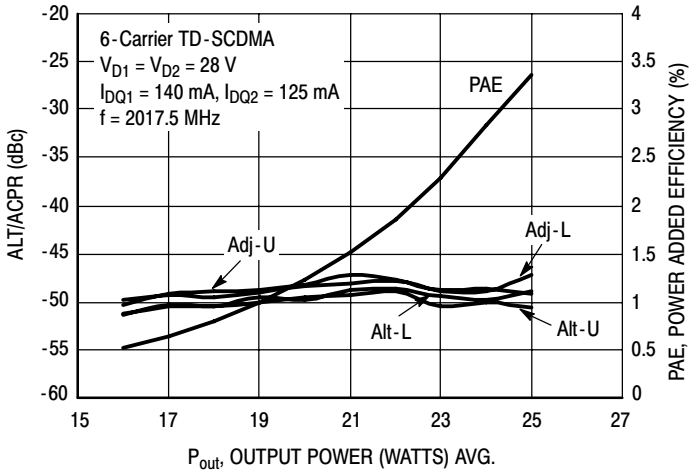


Figure 21. 6-Carrier TD-SCDMA ACPR, ALT and Power Added Efficiency versus Output Power

TD-SCDMA TEST SIGNAL

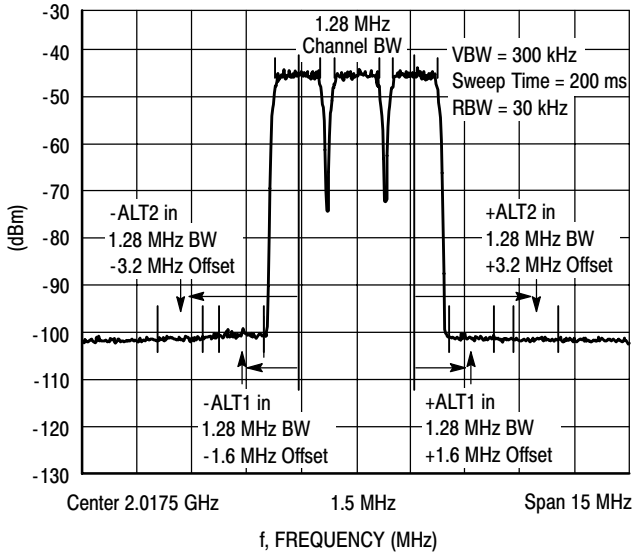


Figure 22. 3-Carrier TD-SCDMA Spectrum

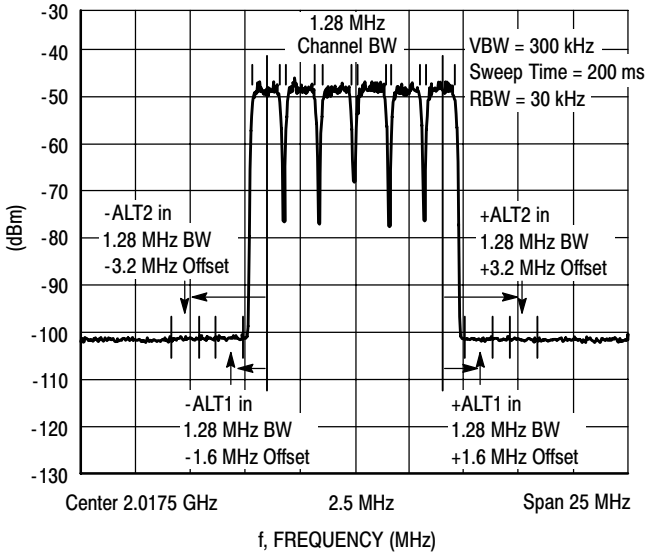
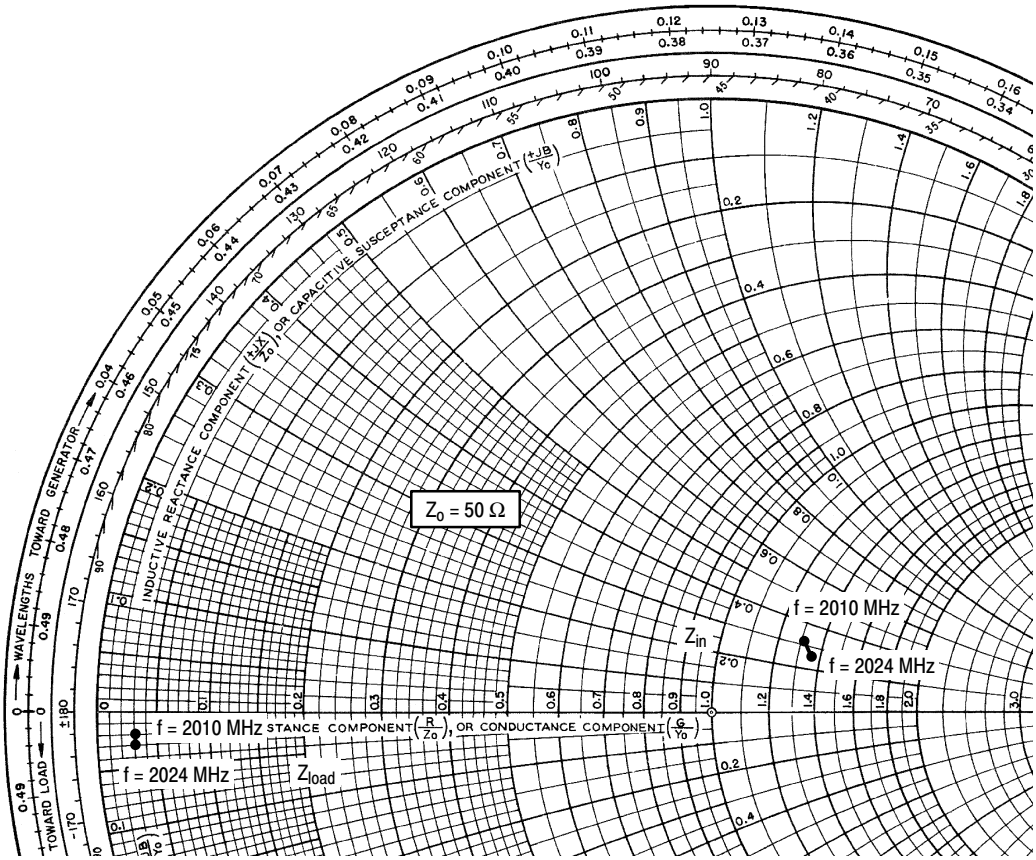


Figure 23. 6-Carrier TD-SCDMA Spectrum



V_{DD} = 28 Vdc, I_{DQ1} = 140 mA, I_{DQ2} = 125 mA

f MHz	Z_{in} Ω	Z_{load} Ω
2010	65.31 + j15.57	1.34 - j1.00
2017	67.01 + j14.27	1.36 - j1.17
2024	68.60 + j12.82	1.39 - j1.30

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

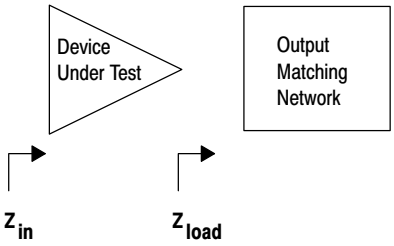
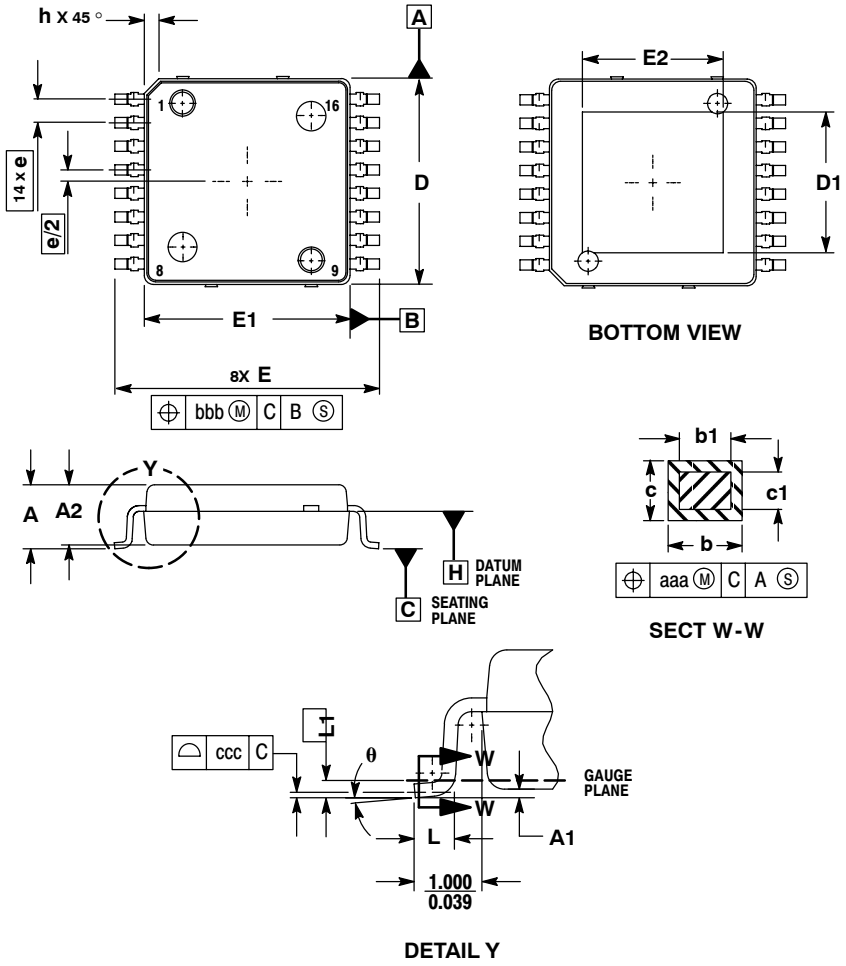


Figure 24. Series Equivalent Input and Load Impedance — TD-SCDMA

PACKAGE DIMENSIONS



NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.127 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.

	MILLIMETERS	
DIM	MIN	MAX
A	2.000	2.300
A1	0.025	0.100
A2	1.950	2.100
D	6.950	7.100
D1	4.372	5.180
E	8.850	9.150
E1	6.950	7.100
E2	4.372	5.180
L	0.466	0.720
L1	0.250 BSC	
b	0.300	0.432
b1	0.300	0.375
c	0.180	0.279
c1	0.180	0.230
e	0.800 BSC	
h	---	0.600
θ	0 °	7 °
aaa	0.200	
bbb	0.200	
ccc	0.100	

CASE 978-03
ISSUE C
PFP-16

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1949: Mounting Method for the MHVIC910HR2 (PFP-16) and Similar Surface Mount Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
3	Jan. 2007	• Added “including TD-SCDMA” to data sheet description paragraph, p. 1 • Updated verbiage in Typical N-CDMA Tests table, p. 2 • Corrected ordering of Z11 and Z13 numbers in Z list, Fig. 3, Test Circuit Schematic and updated Part Numbers in Table 6, Component Designations and Values (for W-CDMA), to RoHS compliant part numbers, p. 3 • Adjusted scale for Fig. 6, Power Gain and Power Added Efficiency versus Output Power, to better match the device’s capabilities, p. 5 • Removed lower voltage tests from Fig. 7, Power Gain versus Output Power, due to fixed tuned fixture limitations, p. 5 • Replaced Fig. 10, MTTF versus Junction Temperature with updated graph. Removed $Amps^2$ and listed operating characteristics and location of MTTF calculator for device, p. 6 • Corrected ordering of Z10 and Z11 numbers in Z list, Fig. 12, Test Circuit Schematic and updated Part Numbers in Table 7, Component Designations and Values (for N-CDMA), to RoHS compliant part numbers, p. 8 • Adjusted scale for Fig. 15, Power Gain and Power Added Efficiency versus Output Power, to better match the device’s capabilities, p. 10 • Updated Z_{in} values and chart in Fig. 11, W-CDMA Series Impedance, p. 7, and in Fig. 17, N-CDMA Series Impedance, p. 11 • Added TD-SCDMA test circuit schematic, component designations and values, component layout, typical characteristic curves, test signal and series impedance, p. 13-16 • Added Product Documentation and Revision History, p. 18

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