FN6283.0

MMIC Silicon Bipolar Broadband Amplifier

The ISL55013 is a high performance gain block featuring a Darlington configuration using high f_T transistors and excellent thermal performance. They are an ideal choice for DVB-S LNB cable receiver applications.

Other members of the family include:

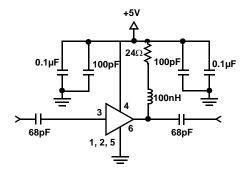
ISL55012 and ISL55015 match a 75 Ω source to a 50 Ω load. ISL55013 and ISL55014 match a 50 Ω source to a 50 Ω load.

Ordering Information

PART NUMBER (Note)	PART MARKING	TAPE & REEL	PACKAGE (Pb-Free)	PKG. DWG.#
ISL55013IEZ-T7	ССН	7" (3k pcs)	6 Ld SC-70	P6.049

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Typical Application Circuit



Features

Input impedance of 50Ω

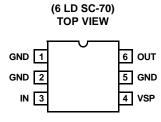
February 13, 2007

- Output impedance of 50Ω
- Gain of 11.8dB @1GHz
- Noise figure of 5.0dB
- · OIP3 of 31dBm
- · Low input and output return losses
- · Pb-free available (RoHS compliant)

Applications

- LNB and LNB-T (HDTV) amplifiers
- · IF gain blocks for satellite and terrestrial STBs
- · PA driver amplifier
- · Wireless data, satellite
- · Bluetooth/WiFi
- Satellite locator and signal strength meters

Pinout



ISL55013

Absolute Maximum Ratings $(T_A = +25^{\circ}C)$

Thermal Information

Supply Voltage from VSP to GND 6V
Input Voltage
Ambient Operating Temperature
Storage Temperature65°C to +125°C
Operating Junction Temperature
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) 6000V
Machine Model (Per FIAJ FD-4701 Method C-111)

Thermal Resistance (Typical)	θ _{JA} (°C/W
6 Ld SC-70	200

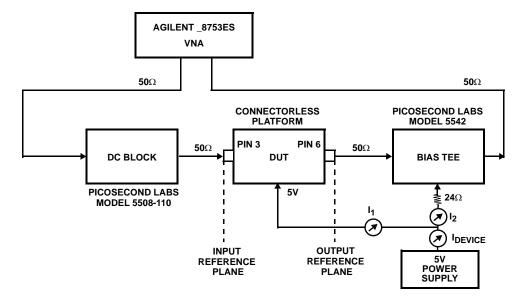
CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only.

$\textbf{Electrical Specifications} \hspace{0.5cm} V_{SP} = +5V, \hspace{0.1cm} Z_{RSC} = Z_{LOAD} = 50\Omega, \hspace{0.1cm} T_{A} = +25^{\circ}C, \hspace{0.1cm} 24\Omega \hspace{0.1cm} V_{SP} \hspace{0.1cm} \text{to OUT, unless otherwise specified.} \\$

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V _{SP}	Supply Voltage	To operate below 5V, the 24Ω resistor to supply should be reduced	3.0		5.5	V
Gt	Small Signal Gain	1.0GHz	10.6	11.8	13.1	dB
		1.5GHz	10	11.2	12.5	dB
		2.0GHz	9.8	11.2	12.3	dB
P1dB	Output Power at 1dB Compression	1.0GHz	15.9	17.4	18.9	dBm
		2.0GHz	15.5	17	18.5	dBm
OIP3	Output Third Order Intercept Point	1.0GHz		31.5		dBm
		2.0GHz		28.3		dBm
OIP2	Output Second Order Intercept Point	Input tones at 1.0GHz and 1.1GHz, at Input Power = -15dBm, Output tone 2.1GHz		49.1		dBm
BW	3dB Bandwidth	3dB below Gain @ 500MHz		2.8		GHz
IRL	Input Return Loss	1.0GHz		15.8		dB
ORL	Output Return Loss	1.0GHz		15.9		dB
RISOL	Reverse Isolation	2.0GHz		17.8		dB
NF	Noise Figure	2.0GHz		5.0		dB
ID	Device Operating Current		54	62.3	69	mA

Device Test Setup



Typical Performance Curves 50Ω environment

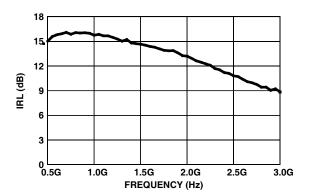


FIGURE 1. INPUT RETURN LOSS vs FREQUENCY

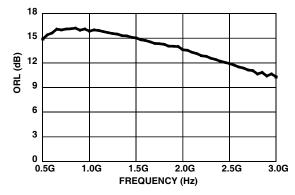
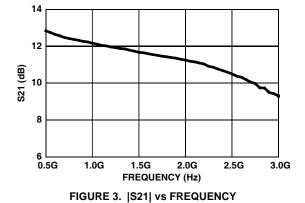


FIGURE 2. OUTPUT RETURN LOSS vs FREQUENCY



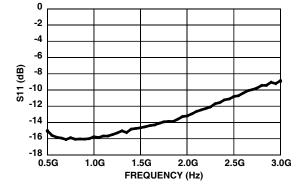


FIGURE 4. |S11| vs FREQUENCY

Typical Performance Curves 50Ω environment (Continued)

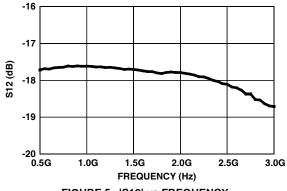


FIGURE 5. |S12| vs FREQUENCY

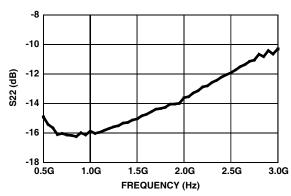


FIGURE 6. |S22| vs FREQUENCY

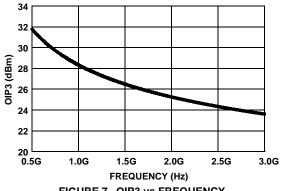


FIGURE 7. OIP3 vs FREQUENCY

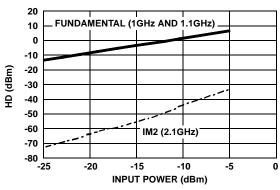


FIGURE 8. IM2 vs INPUT POWER

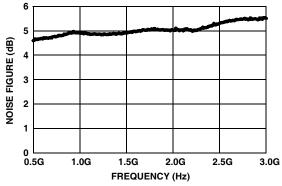


FIGURE 9. NOISE FIGURE vs FREQUENCY

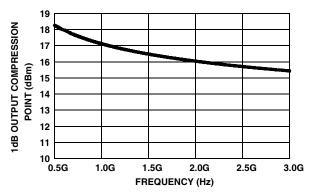


FIGURE 10. P1dB vs FREQUENCY

Typical Performance Curves 50Ω environment (Continued)

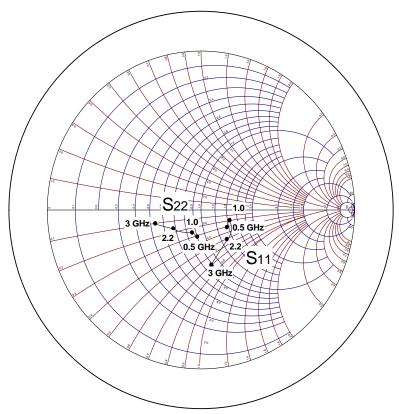
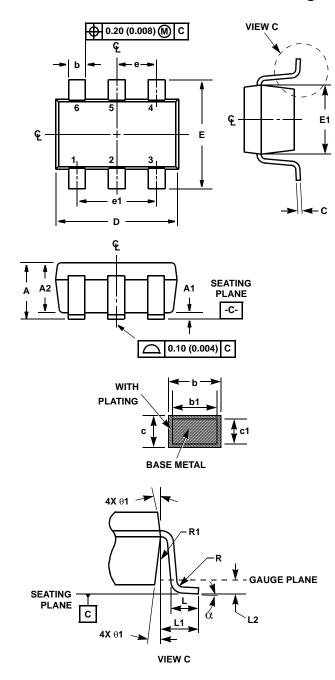


FIGURE 11. S11 AND S22 vs FREQUENCY

Pb-free reflow profile see link below http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Small Outline Transistor Plastic Packages (SC70-6)



P6.049A
6 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

	INCHES		MILLIN		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
Α	0.031	0.039	0.80	1.00	-
A1	0.001	0.004	0.025	0.10	-
A2	0.034	0.036	0.85	0.90	-
b	0.006	0.012	0.15	0.30	-
b1	0.006	0.010	0.15	0.25	-
С	0.004	0.008	0.10	0.20	6
c1	0.004	0.006	0.10	0.15	6
D	0.073	0.085	1.85	2.15	3
Е	0.084 BSC		2.1 BSC		-
E1	0.045	0.053	1.15	1.35	3
е	0.0256 Ref		0.65 Ref		-
e1	0.0512 Ref		1.30 Ref		-
L	0.010	0.018	0.26	0.46	4
L1	0.016 Ref.		0.400 Ref.		-
L2	0.006 BSC		0.15 BSC		-
N	6		6		5
R	0.004	-	0.10	-	-
α	0°	8 ⁰	0°	8 ⁰	-

Rev. 0 7/05

NOTES:

- 1. Dimensioning and tolerance per ASME Y14.5M-1994.
- 2. Package conforms to EIAJ SC70 and JEDEC MO203AB.
- Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
- 4. Footlength L measured at reference to gauge plane.
- 5. "N" is the number of terminal positions.
- 6. These Dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
- Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems. Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com

intersil